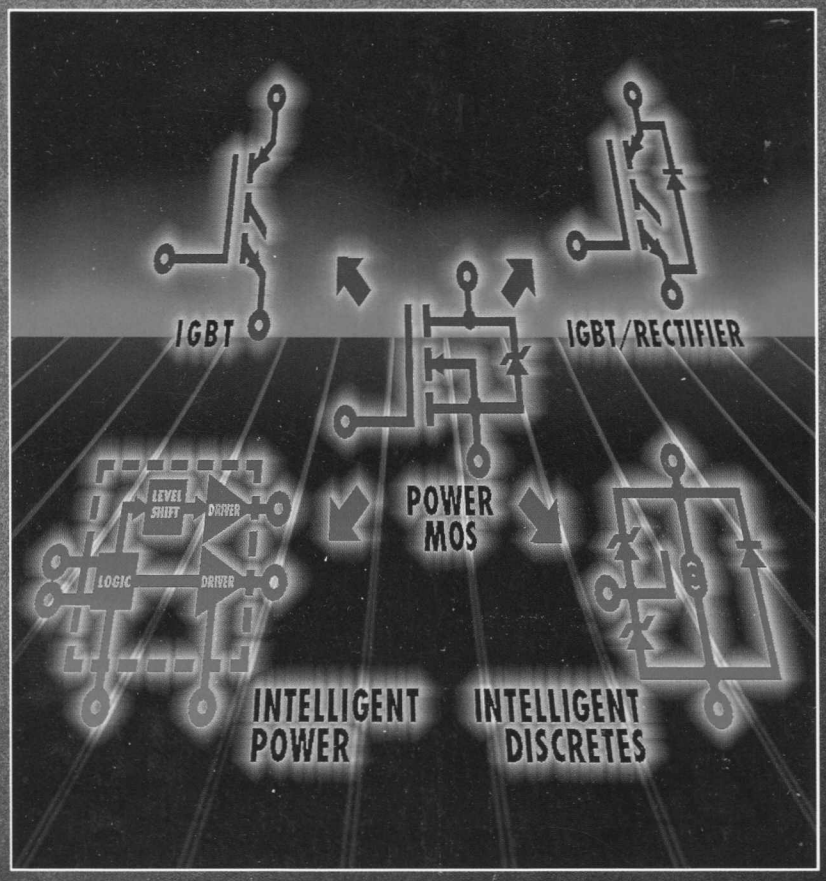


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This MOSFET databook offers an extensive line of power MOSFET products for use in a wide range of consumer, industrial and high-reliability applications. This databook contains detailed technical information on the broad line of more than 1000 power MOSFETs, including standard power MOSFETs (the popular RF-series types, the IRF-series of industry replacement types, and JEDEC types), MegaFETs, logic-level power MOSFETs (L^2FETs), ruggedized power MOSFETs, enhancement-mode insulated gate bipolar transistors (IGBTs), advanced discrete, high-reliability and radiation-hardened power MOSFETs.

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Separate data sections provide definitive ratings and characteristics for each major category of devices. Data pages for individual devices are organized in numeric-alphanumerical sequence for each section. Because some devices are grouped together to show similarity of function or data, some individual types numbers may be out of sequence. If you have difficulty finding a type number check the Index of Devices, Section 1.

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POWER MOSFETs

FOR COMMERCIAL AND HIGH RELIABILITY APPLICATIONS

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Industry Replacement Guide

Power MOSFETs

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2N6660	RFL2N06
2N6661	RFL1N10
2N6755	2N6755
2N6756	2N6756
2N6757	2N6757
2N6758	2N6758
2N6759	2N6759
2N6760	2N6760
2N6751	2N6761
2N6762	2N6762
2N6763	2N6763
2N6764	2N6764
2N6765	2N6765
2N6766	2N6766
2N6767	2N6767
2N6768	2N6768
2N6769	2N6769
2N6770	2N6770
2N6782	2N6782
2N6784	2N6784
2N6786	2N6782
2N6788	2N6788
2N6790	2N6790
2N6792	2N6792
2N6794	2N6794
2N6796	2N6796
2N6798	2N6798
2N6800	2N6800
2N6802	2N6802
2SJ101	RFP12P08
2SJ102	RFP12P08
2SJ112	2N6898
2SJ113	RFH25P10
2SJ127	RFP10P12
2SK294	IRF522
2SK295	IRF522
2SK296	IRF723
2SK308	RFM10N12
2SK310	IRF732
2SK311	RFM3N45
2SK312	IRF453
2SK313	IRF453
2SK319	IRF730
2SK345	IRF521
2SK346	IRF521
2SK349	RFH10N45
2SK382	RFP3N50
2SK383	RFP15N12
2SK398	RFM12N10
2SK401	IRF351
2SK408	RFP2N18
2SK409	RFP2N18
2SK412	RFH12N35
2SK428	RFP15N06
2SK440	IRF630
2SK512	IRF450
2SK549	RFP15N06
2SK550	RFP25N06
2SK551	RFP15N12
2SK552	RFP6N45
2SK553	RFP6N45
2SK556	RFH10N45
2SK557	RFH10N50
2SK558	RFHI0N50
2SK561	RFM25N06
BSR80	RFP4N05
BSR81	IRF513
BSR82	RFP2N08
BSS93	IRFF212

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
BST90	RFL1N08
BUP60	RFM7N35
BUP61	IRF331
BUP62	RFM7N40
BUP63	IRF330
BUP64	RFM6N45
BUP65	IRF431
BUP66	RFM6N50
BUP67	IRF430
BUP68	RFM7N35
BUP69	RFM7N40
BUP70	RFM6N45
BUP71	RFM6N50
BUZ10	RFP25N05
BUZ10B	IRF533
BUZ11A	RFP25N05
BUZ14	RFK45N05
BUZ14A	IRF153
BUZ14C	IRF131
BUZ14D	IRF133
BUZ15	RFK45N05
BUZ17	RFK45N05
BUZ20	RFP12N10
BUZ20A	IRF532
BUZ20B	IRF520
BUZ21	RFP18N10
BUZ23	RFM12N10
BUZ23A	IRF130
BUZ23B	IRF152
BUZ24	RFK35N10
BUZ25	RFM18N10
BUZ30	IRF632
BUZ32	IRF630
BUZ32A	IRF631
BUZ32B	IRF632
BUZ32C	IRF633
BUZ33	IRF220
BUZ33A	IRF232
BUZ33B	IRF233
BUZ34	IRF240
BUZ35	IRF230
BUZ35A	IRF231
BUZ36	IRF240
BUZ40	IRF822
BUZ41A	IRF830
BUZ41B	IRF431
BUZ42	IRF832
BUZ42A	IRF833
BUZ42B	IRF820
BUZ42C	IRF821
BUZ42D	IRF822
BUZ43	IRF422
BUZ44A	IRF430
BUZ44B	IRF831
BUZ45	RFM10N50
BUZ45A	RFM10N50
BUZ45B	IRF452
BUZ46	IRF432
BUZ46A	IRF433
BUZ46B	IRF821
BUZ60	IRF730
BUZ60A	IRF731
BUZ60B	IRF732
BUZ60C	IRF733
BUZ60D	IRF720
BUZ63	IRF330
BUZ63A	IRF331
BUZ63B	IRF332
BUZ63C	IRF333
BUZ63D	IRF730

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
BUZ64	IRF352
BUZ67	IRF352
BUZ71	RFP25N05
BUZ71A	RFP25N05
BUZ72	RFP12N10
BUZ72A	IRF532
BUZ73	IRF630
BUZ73A	IRF632
BUZ74	IRF820
BUZ74A	IRF822
BUZ76	IRF720
BUZ76A	IRF732
BUZ201	IRF352
BUZ210	RFM10N50
BUZ211	RFM10N50
BUZ351	RFH12N40
BUZ353	RFH10N50
BUZ354	RFH10N50
D82AK2	IRFD1Z1
D82AL2	IRFD1Z0
D82AM2	IRFD2Z1
D82AN2	IRFD2Z0
D84BK1	IRF511
D84BK2	IRF511
D84BL1	IRF510
D84BL2	IRF510
D84BM1	IRF611
D84BM2	IRF611
D84BN1	IRF610
D84BN2	IRF610
D84BQ1	IRF723
D84BQ2	IRF722
D84CK1	IRF521
D84CK2	IRF521
D84CL1	IRF520
D84CL2	IRF520
D84CM1	IRF621
D84CM2	IRF621
D84CN1	IRF620
D84CN2	IRF620
D84CQ1	IRF721
D84CQ2	IRF720
D84CR1	IRF821
D84CR2	IRF820
D84DK1	IRF531
D84DK2	IRF531
D84DL1	IRF530
D84DL2	IRF530
D84DM1	IRF631
D84DM2	IRF631
D84DN1	IRF630
D84DN2	IRF630
D84DQ1	IRF731
D84DQ2	IRF730
D84DR1	IRF831
D84DR2	IRF830
D84EM1	IRF641
D84EM2	IRF641
D86DK1	IRF131
D86DK2	IRF131
D86DL1	IRF130
D86DL2	IRF130
D86DM1	RFM10N12
D86DM2	IRF631
D86DN1	IRF230
D86DN2	IRF230
D86DQ1	IRF331
D86DQ2	IRF330
D86DR1	IRF431
D86DR2	IRF430

Power MOSFETs

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
D86EM1	IRF241
D86EM2	IRF241
D86EN1	IRF240
D86EN2	IRF240
D86FK1	RFK45N05
D86FK2	RFK45N06
D86FL1	RFK35N08
D86FL2	IRF150
D86FM1	IRF251
D86FM2	IRF251
D86FN1	IRF250
D86FN2	IRF250
D86FQ1	IRF351
D86FQ2	IRF350
D86FR1	IRF451
D86FR2	IRF450
D88FK1	IRFP151
D88FK2	IRFP151
D88FL1	IRFP150
D88FL2	IRFP150
D88FM1	IRFP251
D88FM2	IRFP251
D88FN1	IRFP250
D88FN2	IRFP250
D88FQ1	IRFP351
D88FQ2	IRFP350
D88FR1	IRFP451
D88FR2	IRFP450
GF2A10	IRFD110R
GF2A13	IRFD120R
GF2B06	IRFD210R
GF2B08	IRFD220R
GF2D04	IRFD310R
GF2D05	IRFD320R
GF4A4	IRF510R
GF4A8	IRF520R
GF4A14	IRF530R
GF4A27	IRF540R
GF4B2	IRF610R
GF4B5	IRF620R
GF4B9	IRF630R
GF4B18	IRF640R
GF4D1	IRF710R
GF4D3	IRF720R
GF4D5	IRF730R
GF4D10	IRF740R
GF4E2	IRF820R
GF4E4	IRF830R
GF4E8	IRF840R
GF6A14	IRF130R
GF6A27	IRF140R
GF6A40	IRF150R
GF6B9	IRF230R
GF6B18	IRF240R
GF6B30	IRF250R
GF6D5	IRF330R
GF6D10	IRF340R
GF6D15	IRF350R
GF6E4	IRF430R
GF6E8	IRF440R
GF6E13	IRF450R
GF8A40	IRFP150R
GF8B30	IRFP250R
GF8D15	IRFP350R
GF8E13	IRFP450R
GF14A35	IRFF110R
GF14A60	IRFF120R
GF14A80	IRFF130R
GF14B22	IRFF210R
GF14B35	IRFF220R

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
GF14B55	IRFF230R
GF14D14	IRFF310R
GF14D25	IRFF320R
GF14D35	IRFF330R
GF14E16	IRFF420R
GF14E28	IRFF430R
IRF120	IRF120
IRF121	IRF121
IRF122	IRF122
IRF123	IRF123
IRF130	IRF130
IRF131	IRF131
IRF132	IRF132
IRF133	IRF133
IRF150	IRF150
IRF151	IRF151
IRF152	IRF152
IRF153	IRF153
IRF220	IRF220
IRF221	IRF221
IRF222	IRF222
IRF223	IRF223
IRF230	IRF230
IRF231	IRF231
IRF232	IRF232
IRF233	IRF233
IRF240	IRF240
IRF241	IRF241
IRF243	IRF243
IRF250	IRF250
IRF251	IRF251
IRF252	IRF252
IRF253	IRF253
IRF320	IRF320
IRF321	IRF321
IRF322	IRF322
IRF323	IRF323
IRF330	IRF330
IRF331	IRF331
IRF332	IRF332
IRF333	IRF333
IRF350	IRF350
IRF351	IRF351
IRF352	IRF352
IRF353	IRF353
IRF420	IRF420
IRF421	IRF421
IRF422	IRF422
IRF423	IRF423
IRF430	IRF430
IRF431	IRF431
IRF432	IRF432
IRF433	IRF433
IRF450	IRF450
IRF451	IRF451
IRF452	IRF452
IRF453	IRF453
IRF510	IRF510
IRF511	IRF511
IRF512	IRF512
IRF513	IRF513
IRF520	IRF520
IRF521	IRF521
IRF522	IRF522
IRF523	IRF523
IRF530	IRF530
IRF531	IRF531
IRF532	IRF532
IRF533	IRF533
IRF610	IRF610

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
IRF611	IRF611
IRF612	IRF612
IRF613	IRF613
IRF620	IRF620
IRF621	IRF621
IRF622	IRF622
IRF623	IRF623
IRF630	IRF630
IRF631	IRF631
IRF632	IRF632
IRF633	IRF633
IRF641	IRF641
IRF643	IRF643
IRF710	IRF722
IRF711	IRF723
IRF712	IRF722
IRF713	IRF722
IRF720	IRF720
IRF721	IRF721
IRF722	IRF722
IRF723	IRF723
IRF730	IRF730
IRF731	IRF731
IRF732	IRF732
IRF733	IRF733
IRF820	IRF820
IRF821	IRF821
IRF822	IRF822
IRF823	IRF823
IRF830	IRF830
IRF831	IRF831
IRF832	IRF832
IRF833	IRF833
IRF9130	RFM12P10
IRF9131	RFM12P08
IRF9132	RFM8P10
IRF9133	RFM8P08
IRF9140	RFK25P10
IRF9141	RFK25P08
IRF9142	RFM12P10
IRF9143	RFM12P08
IRF9231	RFM10P15
IRF9233	RFM5P15
IRF9241	RFM10P15
IRF9242	RFM10P15
IRF9510	RFP5P12
IRF9511	RFP5P12
IRF9512	RFP5P12
IRF9513	RFD5P12
IRF9520	RFP6P10
IRF9521	RFP6P08
IRF9522	RFP6P10
IRF9523	RFP6P08
IRF9530	RFP12P10
IRF9531	RFP12P08
IRF9532	RFP8P10
IRF9533	RFP8P08
IRF9542	RFP12P10
IRF9543	RFP12P08
IRF9611	RFP5P15
IRF9613	RFP5P15
IRF9621	RFP6P08
IRF9623	RFP6P08
IRF9631	RFP12P08
IRF9633	RFP12P08
IRF9641	RFP10P15
IRF9643	RFP10P15
IRFD1Z0	IRFD1Z0
IRFD1Z1	IRFD1Z1
IRFD1Z2	IRFD1Z2

Power MOSFETs

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
IRFD1Z3	IRFD1Z3
IRFF110	IRFF110
IRFF111	IRFF111
IRFF112	IRFF112
IRFF113	IRFF113
IRFF120	IRFF120
IRFF121	IRFF121
IRFF122	IRFF122
IRFF123	IRFF123
IRFF130	IRFF130
IRFF131	IRFF131
IRFF132	IRFF132
IRFF133	IRFF133
IRFF210	IRFF210
IRFF211	IRFF211
IRFF212	IRFF212
IRFF213	IRFF213
IRFF220	IRFF220
IRFF221	IRFF221
IRFF222	IRFF222
IRFF223	IRFF223
IRFF230	IRFF230
IRFF231	IRFF231
IRFF232	IRFF232
IRFF233	IRFF233
IRFF320	IRFF320
IRFF321	IRFF321
IRFF322	IRFF322
IRFF323	IRFF323
IRFF330	IRFF330
IRFF331	IRFF331
IRFF332	IRFF332
IRFF333	IRFF333
IRFF420	IRFF420
IRFF421	IRFF421
IRFF422	IRFF422
IRFF423	IRFF423
IRFF430	IRFF430
IRFF431	IRFF431
IRFF432	IRFF432
IRFF433	IRFF433
IRFZ20	RFP25N05
IRFZ22	RFP25N05
IRFZ32	RFP25N05
IVN5000TND	RFL2N05
IVN5000TNE	RFL2N06
IVN5000TNF	RFL1N08
IVN5000TNH	RFL1N10
IVN5000SND	RFL2N05
IVN5000SNE	RFL2N06
IVN5000SNF	RFL1N08
IVN5000SNH	RFL1N10
IVN5001TND	RFL2N05
IVN5001TNE	RFL2N06
IVN5001TNF	RFL1N08
IVN5001TNH	RFL1N10
IVN5001SND	RFL2N05
IVN5001SNE	RFL2N06
IVN5001SNF	RFL1N08
IVN5001SNH	RFL1N10
IVN5200HND	IRF523
IVN5200HNE	IRF523
IVN5200HNF	IRF522
IVN5200HNH	IRF522
IVN5200KND	IRF123
IVN5200KNE	IRF123
IVN5200KNF	IRF122
IVN5200KNH	IRF122
IVN5200TND	IRFF123
IVN5200TNE	IRFF123

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
IVN5200TNF	IRFF122
IVN5200TNH	IRFF122
IVN5201CND	IRF523
IVN5201CNE	IRF523
IVN5201CNF	IRF522
IVN5201CNH	IRF522
IVN5201KND	IRF123
IVN5201KNE	IRF123
IVN5201KNF	IRF122
IVN5201KNH	IRF122
IVN5201TND	IRFF123
IVN5201TNE	IRFF123
IVN5201TNF	IRFF122
IVN5201TNH	IRFF122
IVN6000CNE	IRF523
IVN6000CNF	IRF522
IVN6000CNH	IRF522
IVN6000CNR	IRF722
IVN6000CNS	IRF722
IVN6000CNT	IRF821
IVN6000CNU	IRF822
IVN6000KNE	IRF123
IVN6000KNF	IRF122
IVN6000KNH	IRF122
IVN6000KNR	IRF322
IVN6000KNS	IRF322
IVN6000KNT	IRF421
IVN6000KNU	IRF422
IVN6000TNE	IRFF113
IVN6000TNF	IRFF112
IVN6000TNH	IRFF112
IVN6000TNR	IRFF322
IVN6000TNS	IRFF322
IVN6000TNT	IRFF423
IVN6000TNU	IRFF422
IVN6001CNE	IRF523
IVN6001CNF	IRF522
IVN6001CNH	IRF522
IVN6001KNE	IRF123
IVN6001KNF	IRF122
IVN6001KNH	IRF122
IVN6001TNE	IRFF113
IVN6001TNF	IRFF112
IVN6001TNH	IRFF112
IVN6002CND	IRF523
IVN6002KND	IRF123
IVN6002TND	IRFF113
IVN6100TNS	IRFF312
IVN6100TNT	IRFF423
IVN6100TNU	IRFF423
IVN6200ANE	IRF531
IVN6200ANF	RFP12N08
IVN6200ANH	RFP12N10
IVN6200ANM	RFP8N20
IVN6200ANP	RFP8N20
IVN6200ANS	IRF732
IVN6200ANT	IRF831
INV6200ANU	IRF830
IVN6200CND	IRF521
IVN6200CNE	IRF533
IVN6200CNF	IRF532
IVN6200CNH	IRF532
IVN6200CNM	RFP8N20
IVN6200CNP	RFP8N20
IVN6200CNR	RFP4N40
IVN6200CNS	IRF730
IVN6200CNT	IRF831
IVN6200CNU	IRF831
IVN6200KNE	IRF133
IVN6200KNF	IRF132

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
IVN6200KNH	IRF132
IVN6200KNM	RFM8N20
IVN6200KNP	IRF353
IVN6200KNR	RFM4N40
IVN6200KNS	IRF332
IVN6200KNT	IRF431
IVN6200KNU	IRF432
IVN6300SNE	RFL2N06
IVN6300SNF	RFL1N08
IVN6300SNH	RFL1N10
IVN6300SNM	RFL1N20
IVN6300SNP	IRFF313
IVN6300SNS	IRFF312
IVN6300SNT	IRFF423
IVN6300SNU	IRFF422
IVN6660	RFL1N08
IVN6661	RFL1N08
MTH7N45	RFH10N45
MTH7N50	RFH10N50
MTH8N35	RFH12N35
MTH8N40	RFH12N40
MTH15N12	IRF251
MTH15N15	IRF251
MTH15N18	RFH25N18
MTH15N20	RFH25N20
MTH25N08	RFK35N08
MTH25N10	RFH35N10
MTM2N45	RFM3N45
MTM2N50	RFM3N50
MTM3N35	RFM4N35
MTM3N40	RFM4N40
MTM4N45	2N6762
MTM4N50	2N6762
MTM5N18	RFM8N18
MTM5N20	RFM8N20
MTM5N35	IRF330
MTM5N40	IRF330
MTM7N12	RFM8N18
MTM7N15	RFM8N18
MTM7N18	IRF232
MTM7N20	RFM8N20
MTM7N45	RFM10N45
MTM7N50	RFM10N50
MTM8N08	2N6757
MTM8N10	2N6758
MTM8N12	2N6757
MTM8N15	2N6757
MTM8N18	RFM8N18
MTM8N20	RFM8N20
MTM10N05	RFM15N05
MTM10N06	RFM15N06
MTM10N08	RFM12N08
MTM10N10	RFM12N10
MTM10N12	RFM10N12
MTM10N15	RFM10N15
MTM12N05	RFM15N05
MTM12N06	RFM15N06
MTM12N08	RFM12N08
MTM12N10	RFM12N10
MTM12N12	IRF230
MTM12N15	IRF230
MTM12N18	RFM12N18
MTM12N20	RFM12N20
MTM15N05	RFM15N05
MTM15N06	RFM15N06
MTM15N12	RFM15N12
MTM15N15	RFM15N15
MTM15N18	RFK25N18
MTM15N20	RFK25N20
MTM15N35	RFM12N35

Power MOSFETs

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
MTM15N40	RFM12N40
MTM15N45	IRF450
MTM15N50	IRF451
MTM20N08	RFM18N08
MTM20N10	RFM18N10
MTM20N12	RFK30N12
MTM20N15	RFK30N15
MTM25N05	RFM25N05
MTM25N06	RFM25N06
MTM25N08	RFK35N08
MTM25N10	RFK35N10
MTM35N05	RFK45N05
MTM35N06	RFK45N06
MTM40N18	IRF250
MTM40N20	IRF250
MTM45N12	RFK30N12
MTM45N15	RFK30N15
MTM8P08	RFM8P08
MTM8P10	RFM8P10
MTP1N45	RFP3N45
MTP1N50	RFP3N50
MTP2N18	RFP2N18
MTP2N20	RFP2N20
MTP2N25	IRF721
MTP2N35	RFP4N35
MTP2N40	RFP4N40
MTP2N45	RFP3N45
MTP2N50	RFP3N50
MTP3N12	IRF623
MTP3N15	IRF623
MTP3N35	RFP3N45
MTP3N40	RFP3N50
MTP4N08	IRF510
MTP4N10	IRF510
MTP4N45	RFP6N45
MTP4N50	RFP6N50
MTP5N05	RFP6P08
MTP5N06	RFP6P08
MTP5N18	RFP8N18
MTP5N20	RFP8N20
MTP5N35	RFP7N35
MTP5N40	RFP7N40
MTP7N12	RFP8N18
MTP7N15	RFP8N18
MTP7N18	RFP8N18
MTP7N20	RFP8N20
MTP8N08	RFP8N18
MTP8N10	RFP8N18
MTP8N12	RFP10N12
MTP8N15	RFP10N15
MTP8N18	RFP8N18
MTP8N20	RFP8N20
MTP10N05	RFP15N05
MTP10N06	RFP15N06
MTP10N08	RFP12N08
MTP10N10	RFP12N10
MTP10N12	RFP10N12
MTP10N15	RFP10N15
MTP12N05	RFP15N05
MTP12N06	RFP15N06
MTP12N08	RFP12N08
MTP12N10	RFP12N10
MTP12N18	RFP12N18
MTP12N20	RFP12N20
MTP15N05	RFP15N05
MTP15N06	RFP15N06
MTP15N12	RFP15N12
MTP15N15	RFP15N15
MTP20N08	RFP18N08
MTP25N05	RFP25N05

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
MTP25N06	RFP25N06
MTP8P08	RFP8P08
MTP8P10	RFP8P10
NOS100B	RFL1N15
NOS101B	RFL1N12
NOS102B	RFL1N08
PA40N200LM	IRF131
PA40N200LT	IRF531
PA40N200SM	IRF131
PA40N200ST	IRF531
PA40N280LM	IRF132
PA40N280LT	IRF532
PA40N280SM	IRF132
PA40N280ST	IRF532
PA40N300LM	IRF121
PA40N300LT	IRF521
PA40N300SM	IRF121
PA40N300ST	IRF521
PA75N150LM	RFM15N06
PA75N150LT	RFP15N06
PA75N150SM	RFM15N06
PA75N150ST	RFP15N06
PA125N40LM	RFK45N06
PA125N40LP	RFK45N06
PA125N40SM	RFK45N06
PA125N60LM	RFH45N06
PA125N60LP	RFH45N06
PA125N60SM	RFK45N06
PA125N60SP	RFH45N06
PB40N400LM	IRF122
PB40N400LT	IRF522
PB40N400SM	IRF122
PB40N400ST	IRF522
PB75N180LM	IRF130
PB75N180LT	IRF530
PB75N180SM	IRF130
PB75N180ST	IRF530
PB125N60LM	IRF150
PB125N60LP	RFH35N10
PB125N60SM	IRF150
PB125N60SP	RFH35N10
PB125N80LM	IRF152
PB125N80LP	RFH35N10
PB125N80SM	IRF152
PB125N80SP	RFH35N10
PC40N500LM	IRF231
PC40N500LT	IRF631
PC40N500SM	IRF231
PC40N500ST	IRF631
PC40N800LM	IRF221
PC40N800LT	IRF621
PC40N800SM	IRF221
PC40N800ST	IRF621
PC75N250LM	IRF243
PC75N250LT	IRF643
PC75N250SM	IRF243
PC75N250ST	IRF643
PC75N400LM	IRF231
PC75N400LT	IRF631
PC75N400SM	IRF231
PC75N400ST	IRF631
PC125N130LM	IRF253
PC125N130LP	RFH30N15
PC125N130SM	IRF253
PC125N130SP	RFH30N15
PC125N180LM	IRF241
PC125N180LP	RFH30N15
PC125N180LT	IRF641
PC125N180SM	IRF241
PC125N180SP	RFH30N15

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
PM509P	IRF523
PM510P	IRF521
PM512M	IRF131
PM512P	IRF531
PM604P	IRF511
PM605P	IRF523
PM608M	IRF121
PM608P	IRF521
PM609P	IRF521
PM610P	IRF521
PM612M	IRF131
PM612P	IRF531
PM614M	IRF131
PM614P	IRF531
PM804P	IRF510
PM805P	IRF522
PM808M	RFM12N08
PM808P	RFP12N08
PM814M	IRF131
PM814P	IRF531
PM1003P	IRF512
PM1004P	IRF510
PM1006M	IRF122
PM1006P	IRF522
PM1010M	RFM12N10
PM1010P	RFP12N10
PM1203P	IRF621
PM1204P	IRF631
PM1206M	RFM10N12
PM1206P	RFP10N12
PM1210M	RFM15N12
PM1210P	RFP15N12
PM1503P	IRF623
PM1504P	IRF623
PM1506M	IRF631
PM1506P	IRF231
PM1510M	RFM10N15
PM1510P	RFP10N15
SEF120	IRF120
SEF121	IRF121
SEF122	IRF122
SEF123	IRF123
SEF130	IRF130
SEF131	IRF131
SEF132	IRF132
SEF133	IRF133
SEF150	IRF150
SEF151	IRF151
SEF152	IRF152
SEF153	IRF153
SEF220	IRF220
SEF221	IRF221
SEF222	IRF222
SEF223	IRF223
SEF230	IRF230
SEF231	IRF231
SEF232	IRF232
SEF233	IRF233
SEF240	IRF240
SEF241	IRF241
SEF243	IRF243
SEF320	IRF320
SEF321	IRF321
SEF322	IRF322
SEF323	IRF323
SEF330	IRF330
SEF331	IRF331
SEF332	IRF332
SEF333	IRF333
SEF420	IRF420

Power MOSFETs

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
SEF421	IRF421
SEF422	IRF422
SEF423	IRF423
SEF430	IRF430
SEF431	IRF431
SEF432	IRF432
SEF433	IRF433
SEF510	IRF510
SEF511	IRF511
SEF512	IRF512
SEF513	IRF513
SEF520	IRF520
SEF521	IRF521
SEF522	IRF522
SEF523	IRF523
SEF530	IRF530
SEF531	IRF531
SEF532	IRF532
SEF533	IRF533
SEF620	IRF620
SEF621	IRF621
SEF622	IRF620
SEF623	IRF623
SEF630	IRF620
SEF631	IRF631
SEF632	IRF632
SEF633	IRF633
SEF710	IRF722
SEF711	IRF723
SEF712	IRF722
SEF713	IRF722
SEF720	IRF720
SEF721	IRF721
SEF722	IRF722
SEF723	IRF723
SEF730	IRF730
SEF731	IRF731
SEF732	IRF732
SEF733	IRF733
SEF820	IRF820
SEF821	IRF821
SEF822	IRF822
SEF823	IRF823
SEF830	IRF830
SEF831	IRF831
SEF832	IRF832
SEF833	IRF833
SEFF120	IRFF120
SEFF121	IRFF121
SEFF122	IRFF122
SEFF123	IRFF123
SEFH7N45	RFH10N45
SEFH7N50	RFH10N50
SEFH8N35	RFH12N35
SEFH8N40	RFH12N40
SEFH15N18	RFH25N18
SEFH15N20	RFH25N20
SEFH25N08	RFH35N08
SEFH25N10	RFH35N10
SEFH35N05	RFH45N05
SEFH35N06	RFH45N06
SEFM2N45	IRF423
SEFM3N35	IRF323
SEFM3N40	IRF322
SEFM4N45	IRF431
SEFM4N50	IRF430
SEFM5N18	RFM8N18
SEFM5N20	RFM8N20
SEFM5N35	RFM7N35
SEFM5N40	RFM7N40

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
SEFM7N45	RFK10N45
SEFM7N50	RFK10N50
SEFM8N18	IRF230
SEFM8N20	IRF230
SEFM10N05	IRF133
SEFM10N06	IRF133
SEFM10N08	IRF120
SEFM10N10	IRF120
SEFM12N05	IRF131
SEFM12N06	IRF131
SEFM12N08	RFM12N08
SEFM12N10	RFM12N10
SEFM15N05	RFM15N05
SEFM15N06	RFM15N06
SEFM15N18	RFK25N18
SEFM15N20	RFK25N20
SEFM25N05	RFM25N05
SEFM25N06	RFM25N06
SEFM25N08	RFK35N08
SEFM25N10	RFK35N10
SEFM35N05	FRK45N05
SEFM35N06	RFK45N06
SEFP2N45	IRF823
SEFP3N35	IRF323
SEFP3N40	IRF322
SEFP4N45	IRF831
SEFP4N50	IRF830
SEFP5N05	IRF123
SEFP5N06	IRF123
SEFP5N18	RFP8N18
SEFP5N20	RFP8N20
SEFP5N35	IRF331
SEFP5N40	IRF330
SEFP8N18	RFP12N18
SEFP8N20	RFP12N10
SEFP10N05	IRF133
SEFP10N06	IRF133
SEFP10N08	RFP12N08
SEFP10N10	RFP12N10
SEFP12N05	RFP15N05
SEFP12N06	RFP15N06
SEFP12N08	RFP12N08
SEFP12N10	RFP12N10
SEFP15N05	RFP15N05
SEFP15N06	RFP15N06
SEFP25N05	RFP25N05
SEFP25N06	RFP25N06
SGSP101	IRFF110
SGSP102	RFL1N08
SGSP111	IRFF120
SGSP112	IRFF120
SGSP116	IRFF230
SGSP117	IRFF330
SGSP119	IRFF430
SGSP121	IRFF131
SGSP122	IRFF131
SGSP130	IRFF421
SGSP131	IRFF322
SGSP132	IRFF323
SGSP139	IRFF420
SGSP151	IRFF122
SGSP152	IRFF122
SGSP154	IRFF423
SGSP157	IRFF121
SGSP158	IRFF121
SGSP301	RFP2N10
SGSP302	RFP2N10
SGSP311	IRF520
SGSP312	IRF520
SGSP316	IRF723

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
SGSP317	IRF632
SGSP319	IRF820
SGSP321	RFP15N06
SGSP322	RFP15N05
SGSP330	IRF821
SGSP331	IRF722
SGSP332	IRF723
SGSP351	IRF522
SGSP352	IRF522
SGSP354	IRF823
SGSP357	IRF521
SGSP358	IRF521
SGSP361	RFP15N05
SGSP362	RFP18N08
SGSP364	IRF831
SGSP365	IRF730
SGSP366	IRF731
SGSP367	RFP12N20
SGSP369	IRF830
SGSP381	RFP25N06
SGSP382	RFP25N05
SGSP422	RFH45N08
SGSP461	RFH35N10
SGS462	RFH35N08
SGSP463	RFH12N35
SGSP464	RFH10N45
SGSP465	RFH12N40
SGSP466	RFH12N35
SGSP467	RFH12N35
SGSP469	RFH10N50
SGSP471	RFH35N10
SGSP472	RFH35N08
SGSP474	RFH10N45
SGSP475	RFH12N40
SGSP476	RFH12N35
SGSP477	RFH25N20
SGSP479	RFH10N50
SGSP481	RFH35N08
SGSP482	RFH35N08
SGSP491	RFH45N06
SGSP492	RFH45N05
SGSP511	IRF120
SGSP512	IRF120
SGSP516	IRF331
SGSP517	IRF232
SGSP519	IRF420
SGSP530	IRF421
SGSP531	IRF322
SGSP532	IRF323
SGSP561	RFM18N10
SGSP562	RFM18N08
SGSP563	IRF353
SGSP564	IRF431
SGSP565	IRF330
SGSP566	IRF331
SGSP567	RFM12N20
SGSP569	IRF430
SGSP571	RFK35N10
SGSP572	RFK35N08
SGSP573	IRF351
SGSP574	RFM10N45
SGSP577	RFH25N20
SGSP579	RFM10N50
SGSP581	RFK45N06
SGSP582	RFK45N05
SGSP591	RFK45N06
SGSP592	RFK45N05
TN0106N2	RFL1N08
TN0110N2	RFL1N10
TN0520N2	RFL1N20

Power MOSFETs

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
UNF120	IRF120
UNF121	IRF121
UNF122	IRF122
UNF123	IRF123
UNF130	IRF130
UNF131	IRF131
UNF132	IRF132
UNF133	IRF133
UNF150	IRF150
UNF151	IRF151
UNF152	IRF152
UNF153	IRF153
UNF220	IRF220
UNF221	IRF221
UNF222	IRF222
UNF223	IRF223
UFN230	IRF230
UFN231	IRF231
UNF232	IRF232
UFN233	IRF233
UFN240	IRF240
UFN241	IRF241
UFN243	IRF243
UFN250	IRF250
UFN251	IRF251
UFN252	IRF252
UFN253	IRF253
UFN320	IRF320
UFN321	IRF321
UFN322	IRF322
UFN323	IRF323
UFN330	IRF330
UFN331	IRF331
UFN332	IRF332
UFN333	IRF333
UFN350	IRF350
UFN351	IRF351
UFN352	IRF352
UFN353	IRF353
UFN420	IRF420
UFN421	IRF421
UFN422	IRF422
UFN423	IRF423
UFN430	IRF430
UFN431	IRF431
UFN432	IRF432
UFN433	IRF433
UFN450	IRF450
UFN451	IRF451
UFN452	IRF452
UFN453	IRF453
UFN510	IRF510
UFN511	IRF511
UFN512	IRF512
UFN513	IRF513
UFN520	IRF520
UFN521	IRF521
UFN522	IRF522
UFN523	IRF523
UFN530	IRF530
UFN531	IRF531
UFN532	IRF532
UFN533	IRF533
UFN610	IRF610
UFN611	IRF611
UFN612	IRF612
UFN613	IRF613
UFN620	IRF620
UFN621	IRF621
UFN622	IRF622

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
UFN623	IRF623
UFN630	IRF630
UFN631	IRF631
UFN632	IRF632
UFN633	IRF633
UFN641	IRF641
UFN643	IRF643
UFN710	IRF722
UFN711	IRF723
UFN712	IRF722
UFN713	IRF723
UFN720	IRF720
UFN721	IRF721
UFN722	IRF722
UNF723	IRF723
UFN730	IRF730
UFN731	IRF731
UFN732	IRF732
UFN733	IRF733
UFN820	IRF820
UFN821	IRF821
UFN822	IRF822
UFN823	IRF823
UFN830	IRF830
UFN831	IRF831
UFN832	IRF832
UFN833	IRF833
UFNF432	IRFF432
UFNF433	IRFF433
UFNF110	IRFF110
UFNF111	IRFF111
UFNF112	IRFF112
UFNF113	IRFF113
UFNF120	IRFF120
UFNF121	IRFF121
UFNF122	IRFF122
UFNF123	IRFF123
UFNF130	IRFF130
UFNF131	IRFF131
UFNF132	IRFF132
UFNF133	IRFF133
UFNF210	IRFF210
UFNF211	IRFF211
UFNF212	IRFF212
UFNF213	IRFF213
UFNF220	IRFF220
UFNF221	IRFF221
UFNF222	IRFF222
UFNF223	IRFF223
UFNF230	IRFF230
UFNF231	IRFF231
UFNF232	IRFF232
UFNF233	IRFF233
UFNF320	IRFF320
UFNF321	IRFF321
UFNF322	IRFF322
UFNF323	IRFF323
UFNF330	IRFF330
UFNF331	IRFF331
UFNF332	IRFF332
UFNF333	IRFF333
UFNF420	IRFF420
UFNF421	IRFF421
UFNF422	IRFF422
UFNF423	IRFF423
UFNF430	IRFF430
UFNF431	IRFF431
UFNF432	IRFF432
UFNF433	IRFF433
VM1210N1	RFM12N10

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
VN10KE	IRFF113
VN30AB	RFL2N05
VN35AA	IRF513
VN35AB	RFL2N05
VN35AK	RFL2N05
VN40AD	IRF513
VN46AD	IRF513
VN64GA	IRF133
VN66AD	IRF513
VN66AK	RFL2N06
VN67AA	IRF513
VN67AB	RFL2N06
VN67AD	IRF513
VN67AK	RFL2N06
VN88AD	IRF510
VN89AB	RFL1N08
VN89AD	IRF512
VN90AA	IRF512
VN90AB	RFL1N10
VN98AK	RFL1N10
VN99AA	IRF512
VN99AK	RFL1N10
VN0104N2	RFL1N08
VN0104N5	IRF513
VN0106N2	RFL1N08
VN0106N5	IRF513
VN0109N2	RFL1N10
VN0109N4	IRFF112
VN0109N5	RFP2N10
VN0110N2	IRFF112
VN0110N5	IRF512
VN0114N2	IRFF223
VN0114N5	IRF611
VN0116N2	RFL1N18
VN0116N5	RFP2N18
VN0120N2	RFL1N20
VN0120N5	RFP2N20
VN0204N2	RFL2N05
VN0204N5	IRF513
VN0206N2	RFL2N06
VN0206N5	IRF513
VN0210N2	RFL1N10
VN0210N5	IRF512
VN0215N2	IRFF231
VN0215N5	IRF633
VN0216N2	RFL1N18
VN0216N5	RFP2N18
VN0220N2	RFL1N20
VN0220N5	RFP2N20
VN0300B	RFL2N05
VN0300D	RFP4N05
VN0330N1	IRF353
VN0330N2	IRFF331
VN0335N1	IRF323
VN0335N2	IRFF323
VN0335N5	IRF723
VN0340N1	IRF320
VN0340N2	IRFF322
VN0340N5	IRF322
VN0345N1	IRF421
VN0345N2	IRFF423
VN0345N5	IRF823
VN0350N1	IRF420
VN0350N2	IRFF422
VN0350N5	IRF822
VN0400A	RFM15N05
VN0400D	RFP15N05
VN0401A	RFM15N05
VN0401D	RFP15N05
VN0430N1	IRF351

Industry Replacement Guide

Power MOSFETs

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
VN0435N1	IRF351
VN0440N1	IRF350
VN0445N1	IRF451
VN0450N1	IRF450
VN0545N2	IRFF423
VN0600A	RFM25N06
VN0600D	RFP25N06
VN0601A	RFM15N06
VN0601D	RFP15N06
VN0800A	RFM18N08
VN0800D	RFP18N08
VN0801A	RFM12N08
VN0801D	RFP12N08
VN1000A	IRF130
VN1000D	IRF530
VN1001A	IRF132
VN1001D	IRF532
VN1106N1	IRF121
VN1106N2	IRFF111
VN1106N5	IRF511
VN1110N1	IRF122
VN1110N2	IRFF130
VN1110N5	IRF522
VN1116N1	IRF222
VN1116N2	IRFF222
VN1116N5	IRF613
VN1120N1	IRF222
VN1120N2	IRFF212
VN1120N5	IRF612
VN1156N1	IRF231
VN1156N2	IRFF231
VN1156N5	IRF631
VN1200A	RFM15N12
VN1200D	RPF15N12
VN1201A	RFM15N12
VN1201D	RFP15N12
VN1204N1	IRF121
VN1204N2	IRFF121
VN1204N5	IRF521
VN1206B	RFL1N12
VN1206D	RFP2N12
VN1206N1	IRF121
VN1206N2	IRFF121
VN1206N3	IRF521
VN1210N2	IRFF120
VN1210N5	IRF520
VN1215N1	IRF241
VN1215N2	IRFF231
VN1215N5	IRF641

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
VN1216N1	IRF220
VN1216N2	IRFF220
VN1216N5	IRF620
VN1220N1	IRF220
VN1220N2	IRFF220
VN1220N5	IRF620
VN1304N2	RFL1N08
VN1306N2	RFL1N08
VN1310N2	RFL1N10
VN1315N2	IRFF213
VN1320N2	IRFF212
VN1706B	RFL1N18
VN1706D	RFP2N18
VN2345N1	RFM6N45
VN2345N5	RFP6N45
VN2350N1	RFM6N50
VN2350N5	RFP6N50
VN2406B	IRF723
VN3500A	RFM7N35
VN3500D	RFP7N35
VN3501A	IRF331
VN3501D	IRF731
VN4000A	RFM7N40
VN4000D	RFP7N40
VN4001A	IRF330
VN4001D	IRF730
VN4501A	RFM6N45
VN4501D	RFP6N45
VN4502A	IRF431
VN4502D	IRF831
VN5001A	RFM6N50
VN5001D	IRF430
VN5002	RFP6N50
VN5002A	IRF430
VN5002D	IRF830
VP0104N2	RFL1P08
VP0104N5	RFP2P08
VP0106N2	RFL1P08
VPO106N5	RFP2P08
VPO109N5	RFP2P08
VPO204N2	RFL1P08
VP0204N5	RFP2P08
VPO206N2	RFL1P08
VPO206N5	RFP2P08
VP0210N2	RFL1P10
VP1106N1	RFM6P08
VP1106N5	RFP6P08
VP1110N1	RFM6P10
VP1110N5	RFP6P10

INDUSTRY TYPE	HARRIS REPLACEMENT TYPE
ZVN0102B	IRFF113
ZVN0102L	IRF513
ZVN0106B	RFL1N08
ZVN0106L	RFP2N08
ZVN0108B	RFL1N08
ZVN0108L	RFP2N08
ZVN2104B	IRFF113
ZVN2104L	IRF513
ZVN2106B	IRFF113
ZVN2106L	IRF513
ZVN2110B	RFL1N10
ZVN2110L	RFP2N10
ZVN2202B	IRFF123
ZVN2202L	IRF523
ZVN2202M	IRF123
ZVN2204B	IRFF123
ZVN2204L	IRF523
ZVN2204M	IRF123
ZVN2206B	IRFF123
ZVN2206L	IRF523
ZVN2206M	IRF123
ZVN2208B	IRFF112
ZVN2208L	IRF512
ZVN2208M	IRF122
ZVN2210B	IRFF112
ZVN2210L	IRF512
ZVN2210M	IRF122
ZVN2215B	IRFF213
ZVN2215L	IRF613
ZVN2215M	IRF223
ZVN2220B	IRFF212
ZVN2220L	IRF612
ZVN2220M	IRF222
ZVP0102B	RFL1P08
ZVP0102L	RFP2P08
ZVP2104B	RFL1P08
ZVP2104L	RFP2P08
ZVP2106B	RFL1P08
ZVP2106L	RFP2P08
ZVP2202L	RFP6P08
ZVP2202M	RFM6P08
ZVP2204L	RFP6P08
ZVP2204M	RFM6P08
ZVP2206L	RFP6P08
ZVP2206M	RFM6P08
ZVP2208M	RFM6P08
ZVP2210M	RFM6P10
ZVP2215L	RFP5P15
ZVP2215M	RFM5P15

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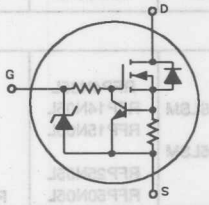
Advanced Power MOS

Current Limiting MOSFETs

Features:

- Current Limits to a Pre-Set Level in a Shorted Load Condition
- Monolithic Device Incorporates a Bipolar Transistor, 2 Resistors, a Zener Diodes and a Power MOSFET
- ESD Protected to 2kV
- "Logic-Level" Gate Input Allows Fully on Condition at 5V

Terminal Diagram



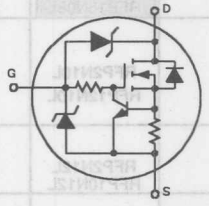
Maximum Ratings				Package
BV_{DSS} (V)	$I_{DS(LIM)}$ (A)	$r_{DS(ON)}$ (Ω)	ESD (kV)	TO-220
80	1	0.75	2	RLP1N08LE
80	5.5	0.12	2	RLP5N08LE

Voltage Clamping, Current Limiting MOSFETs

Features:

- Current Limits to a Pre-Set Level in a Shorted Load Condition
- Monolithic Device Incorporates a Bipolar Transistor, 2 Resistors, 2 Zener Diodes and a Power MOSFET
- Excessive Drain-Source Voltage Clamped by Active Region Turn-On

Terminal Diagram



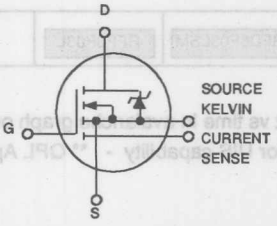
Maximum Ratings				Package
BV_{DSS} (V)	$I_{DS(LIM)}$ (A)	$r_{DS(ON)}$ (Ω)	ESD (kV)	TO-220
60	1	0.75	2	RLP1N06CLE

Current Sensing MOSFETs

Features:

- Built-In Current Sensing Function to be Used as a Feed-Back Signal for Control and/or Protection
- Low $R_{DS(ON)}$ = 0.1Ω
- Current Sensing Ratio = 1560 ± 2.5%
- Avalanche Energy Rated for Ruggedness

Terminal Diagram



Maximum Ratings				Package
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ (Ω)	ESD (kV)	TS-001
100	18A	0.10	-	RFB18N10CS

MOSFETs

Logic Level Product Series

Maximum Ratings BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204AA	TO-251	TO-252	TO-220AB	TO-247	4 PIN DIP
N-Channel										
50	2	0.750	N.R.	RFL2N05L						
	4	0.600	N.R.					RFP4N05L		
	14	0.100	100			RFD14N05L	RFD14N05LSM	RFP14N05L		
	15	0.140	N.R.		RFM15N05L			RFP15N05L		
	16	0.047	200			RFD16N05L	RFD16N05LSM			
	25	0.047	200					RFP25N05L		
	50	0.022	*					RFP50N05L	RFG50N05L	
60	2	0.750	N.R.	RFL2N06L						
	2	0.160	*							RFW2N06RLE
	4	0.600	N.R.			RFD4N06L	RFD4N06LSM	RFP4N06L		
	12	0.135	*			RFD12N06RLE	RFD12N06LESM	RFP12N06RLE		
	12	0.160	*			RFD3055RLE	RFD3055RLESM	RFP3055RLE		
	15	0.140	N.R.		RFM15N06L			RFP15N06L		
	17	0.100	N.R.					RFP17N06L		
	25	0.070	N.R.		RFM25N06L					
80	1	1.200	N.R.	RFL1N08L						
	2	1.050	N.R.					RFP2N08L		
	3	0.800	N.R.			RFD3N08L	RFD3N08LSM			
	12	0.200	N.R.		RFM12N08L			RFP12N08L		
	15	0.140	N.R.					RFP15N08L		
100	1	1.200	N.R.	RFL1N10L						
	1.5	1.400	N.R.	2N6901**						
	2	1.050	N.R.					RFP2N10L		
	12	0.200	N.R.		RFM12N10L			RFP12N10L		
	12	0.200	N.R.		2N6902**					
120	1	1.900	N.R.	RFL1N12L						
	2	1.750	N.R.					RFP2N12L		
	10	0.300	N.R.		RFM10N12L			RFP10N12L		
150	1	1.900	N.R.	RFL1N15L						
	2	1.750	N.R.					RFP2N15L		
	10	0.300	N.R.		RFM10N15L			RFP10N15L		
180	1	3.650	N.R.	RFL1N18L						
	2	3.500	N.R.					RFP2N18L		
	8	0.500	N.R.		RFM8N18L			RFP8N18L		
200	1	3.650	N.R.	RFL1N20L						
	1.5	3.650	N.R.	2N6903**						
	2	3.500	N.R.					RFP2N20L		
	8	0.650	N.R.		RFM8N20L			RFP8N20L		
	8	0.500	N.R.		2N6904**					
P-Channel										
30	8	0.300	*			RFD8P03L	RFD8P03LSM	RFP8P03L		

*More complete ruggedness capability now specified; UIS current vs time in avalanche graph on data sheet

SHADING indicates Developmental Products - N.R. Not Rated for UIS capability - ** QPL Approved Types

Power MOSFETs

Rugged and Standard IRF-Series Power MOSFETs

The Rugged Series of Power MOSFETs are designed, tested and guaranteed to withstand a specified level of circuit induced electrical stress in the breakdown avalanche mode of operation. These are n-channel enhancement mode polysilicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor and relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power.

Using state-of-the-art integrated circuit processing techniques these Rugged MOSFETs provide superior performance in inductive switching applications. The design is optimized to suppress the parasitic bipolar transistor and improve system reliability. These types can be driven directly from integrated circuits.

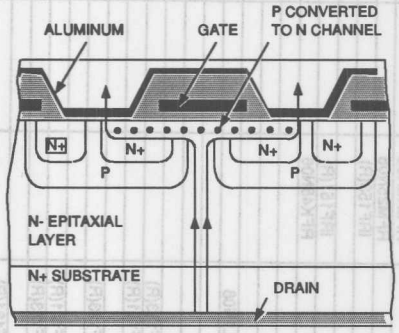
Rugged Series devices are identified by the suffix letter R following the type number.

Features:

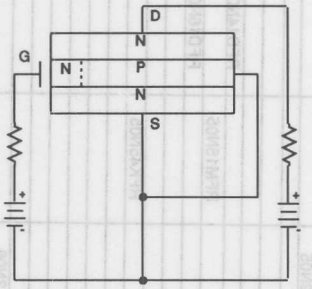
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Allows Reduced Protection Circuitry
- Reduced Drive Requirements
- Increased System Reliability

N-Channel Power MOSFET

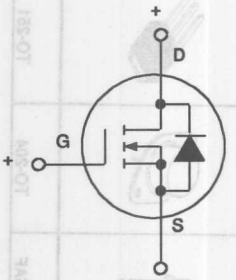
Cross Section of Chip Structure

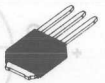
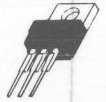
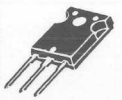
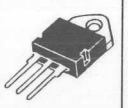


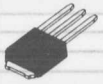
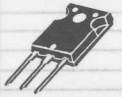
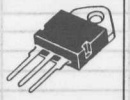
Junction Diagram Showing Biasing Arrangements



Schematic Symbol



Maximum Ratings												
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	TO-218	MO-093	4 PIN DIP
N-Channel												
50V	2.0	0.80	NR	RFL2N05								
	4.0	0.95	NR					RFP4N05				
	13.0	0.120	NR					BUZ71A				
	14.0	0.100	NR					BUZ71				
	14.0	0.100	100			RFD14N05	RFD14N05SM	RFP14N05				
	15.0	0.140	NR		RFM15N05			RFP15N05				
	16.0	0.047	200			RFD16N05	RFD16N05SM					
	25.0	0.047	200					RFP25N05				
	30.0	0.040	NR					BUZ11				
	45.0	0.040	NR		RFK45N05					RFH45N05		
	50.0	0.022	400					RFP50N05	RFG50N05			
	75.0	0.010	800							RFH75N05E		
	100.0	0.010	800								RFA100N05E	
60V	0.40	3.2	NR									IRFD1Z3
	0.05	2.4	NR									IRFD1Z1
	0.80	2.0	NR					RFP4N06				
	0.95	4.0	NR	RFL2N06								
	8.00	0.36	NR		IRF123							
	9.20	0.27	NR		IRF121							
	15.00	0.14	NR		RFM15N06			RFP15N06				
	25.00	0.07	NR		RFM25N06							
	33.00	0.08	150		IRF153(R)							
	34.0	0.085	150						IRFP153(R)			
	40.0	0.055	150		IRF151(R)				IRFP151(R)			
	45.0	0.04	NR		RFK45N06					RFH45N06		
	70.0	0.014	*					RFP70N06	RFG70N06			
80V	0.80	0.8	19									IRFD113(R)
	1.0	0.6	19									IRFD111(R)
	1.0	1.2	NR	RFL1N08								
	1.1	0.4	36									IRFD123(R)
	1.3	0.3	36									IRFD121(R)
	2.0	1.05	NR					RFP2N08				
	3.0	0.8	19	IRFF113(R)								
	3.5	0.6	19	IRFF111(R)								
	4.9	0.74	19					IRF513(R)				
	5.0	0.4	36	IRFF123(R)								
	5.6	0.54	19					IRF511(R)				
	6.0	0.3	36	IRFF121(R)								
	7.0	0.25	69	IRFF133(R)								
	8.0	0.36	36					IRF523(R)				
	8.0	0.18	69	IRFF131(R)								

Maximum Ratings				Package								
												
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mJ)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	TO-218	MO-093	4 PIN DIP
N-Channel												
80V	8.4	0.27	36			IRFU121	IRFR121					
(cont)	9.2	0.27	36					IRF521(R)				
	12.0	0.20	NR		RFM12N08			RFP12N08				
	12.0	0.23	50		IRF133(R)							
	12.0	0.23	69					IRF533(R)				
	14.0	0.16	50		IRF131(R)							
	14.0	0.16	69					IRF531(R)				
	18.0	0.10	NR		RFM18N08			RFP18N08				
	25.0	0.10	100		IRF143(R)							
	25.0	0.10	230					IRF543(R)				
	27.0	0.099	100						IRFP143R			
	28.0	0.077	100		IRF141(R)							
	28.0	0.077	230					IRF541(R)				
	31.0	0.077	100						IRFP141R			
	35.0	0.055	NR		RFK35N08					RFH35N08		
100V	0.4	3.2	NR									IRFD1Z2
	0.5	2.4	NR									IRFD1Z0
	0.8	0.8	19									IRFD112(R)
	1.0	0.6	19									IRFD110(R)
	1.0	1.2	NR	RFL1N10								
	1.1	0.4	36									IRFD122(R)
	1.3	0.3	36									IRFD120(R)
	2.0	1.05	NR					RFP2N10				
	3.0	0.8	19	IRFF112(R)								
	3.5	0.6	19	IRFF110(R)								
	4.9	0.74	19					IRF512(R)				
	5.0	0.4	36	IRFF122(R)								
	5.6	0.54	19					IRF510(R)				
	6.0	0.3	36	IRFF120(R)								
	7.0	0.25	69	IRFF132(R)								
	8.0	0.36	36					IRF522(R)				
	8.0	0.18	69	IRFF130(R)								
	8.0	0.36	NR		IRF122							
	8.4	0.27	36			IRFU120	IRFR120					
	9.0	0.25	NR					BUZ72A				
	9.2	0.27	36					IRF520(R)				
	9.2	0.27	NR		IRF120							
	12.0	0.2	NR		RFM12N10			RFP12N10				
	12.0	0.2	NR					BUZ20				
	12.0	0.23	50		IRF132(R)							
	12.0	0.23	69					IRF532(R)				

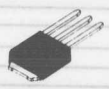
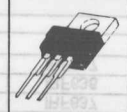
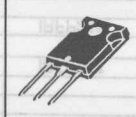
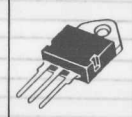
MOSFETs

N-Channel (Continued)

Maximum Ratings / Package												
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mJ)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	TO-218	MO-093	4 PIN DIP
N-Channel												
100V	14.0	0.16	50		IRF130(R)							
(cont)	14.0	0.16	69					IRF530(R)				
	4.7	0.54	19			IRFU110	IRFR110					
	18.0	0.1	NR		RFM18N10			RFP18N10				
	19.0	0.1	NR					BUZ21				
	22.0	0.080	*					RFP22N10				
	25.0	0.10	100		IRF142(R)							
	25.0	0.10	230					IRF542(R)				
	27.0	0.099	100						IRFP142R			
	28.0	0.077	100		IRF140(R)							
	28.0	0.077	230					IRF540(R)				
	31.0	0.077	100						IRFP140R			
	33.0	0.08	150		IRF152(R)							
	34.0	0.085	150						IRFP152(R)			
	35.0	0.055	NR		RFK35N10					RFH35N10		
	40.0	0.055	150		IRF150(R)				IRFP150(R)			
	40.0	0.040	*					RFP40N10	RFG40N10			
120V	1.0	1.9	NR	RFL1N12								
	2.0	1.75	NR					RFP2N12				
	4.0	0.4	NR	RFL4N12								
	10.0	0.3	NR		RFM10N12			RFP10N12				
	15.0	0.15	NR		RFM15N12			RFP15N12				
	30.0	0.075	NR		RFK30N12					RFH30N12		
150V	0.30	6.5	NR									IRFD2Z3
	0.32	5.0	NR									IRFD2Z1
	0.45	2.4	30									IRFD213(R)
	0.60	1.5	30									IRFD211(R)
	0.70	1.2	85									IRFD223(R)
	0.80	0.8	85									IRFD221(R)
	1.0	1.9	NR	RFL1N15								
	1.8	2.4	30	IRFF213(R)								
	2.0	1.75	NR					RFP2N15				
	2.2	1.5	30	IRFF211(R)								
	2.6	2.4	46					IRF613(R)				
	3.0	1.2	85	IRFF223(R)								
	3.3	1.5	46					IRF611(R)				
	3.5	0.8	85	IRFF221(R)								
	4.0	0.4	NR	RFL4N15								
	4.0	1.2	NR		IRF223							
	4.0	1.2	85					IRF623(R)				
	4.5	0.6	85	IRFF233(R)								

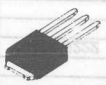
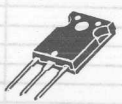
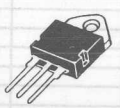
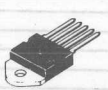
MOSFETs

N-Channel (Continued)

Maximum Ratings												
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	TO-218	MO-093	4 PIN DIP
N-Channel												
150V	4.6	0.8	85			IRFU221	IRFR221					
(cont)	5.0	0.8	NR		IRF221							
	5.0	0.8	85					IRF621(R)				
	5.5	0.4	85	IRFF231(R)								
	8.0	0.6	150		IRF233(R)			IRF633(R)				
	9.0	0.4	150		IRF231(R)			IRF631(R)				
	10.0	0.3	NR		RFM10N15			RFP10N15				
	15.0	0.15	NR		RFM15N15			RFP15N15				
	16.0	0.22	510						IRFP243R			
	16.0	0.22	580		IRF243(R)			IRF643(R)				
	18.0	0.18	510						IRFP241(R)			
	18.0	0.18	580		IRF241(R)			IRF641(R)				
	25.0	0.12	910		IRF253(R)							
	27.0	0.12	810						IRFP253(R)			
	30.0	0.075	NR		RFK30N15					RFH30N15		
	30.0	0.085	910		IRF251(R)							
	33.0	0.085	810						IRFP251(R)			
180V	1.0	3.65	NR	RFL1N18								
	2.0	3.5	NR					RFP2N18				
	8.0	0.5	NR		RFM8N18			RFP8N18				
	12.0	0.25	NR		RFM12N18			RFP12N18				
	25.0	0.15	NR		RFK25N18					RFH25N18		
200V	0.30	6.5	NR									IRFD2Z2
	0.32	5.0	NR									IRFD2Z0
	0.45	2.4	30									IRFD212(R)
	0.60	1.5	30									IRFD210(R)
	0.70	1.2	85									IRFD222(R)
	0.80	0.8	85									IRFD220(R)
	1.0	3.65	NR	RFL1N20								
	1.8	2.4	30	IRFF212(R)								
	2.0	3.5	NR					RFP2N20				
	2.2	1.5	30	IRFF210(R)								
	2.6	2.4	46					IRF612(R)				
	3.0	1.2	85	IRFF222(R)								
	3.3	1.5	46					IRF610(R)				
	3.5	0.8	85	IRFF220(R)								
	3.8	1.2	85			IRFU222	IRFR222					
	4.0	1.2	NR		IRF222							
	4.0	1.2	85					IRF622(R)				
	4.5	0.6	85	IRFF232(R)								
	4.6	0.8	85			IRFU220	IRFR220					

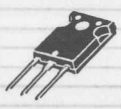
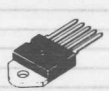
MOSFETs

N-Channel (Continued)

Maximum Ratings				Package								
												
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	TO-218	MO-093	4 PIN DIP
N-Channel												
200V	5.0	0.8	NR		IRF220							
(cont)	5.0	0.8	NR					IRF620(R)				
	5.5	0.4	85	IRFF230(R)								
	5.8	0.6	NR									
	8.0	0.5	NR					BUZ73A				
	8.0	0.6	150		IRF232(R)			RFP8N20				
	9.0	0.4	150		IRF230(R)			IRF632(R)				
	9.5	0.4	NR		RFM8N20			IRF630(R)				
	12.0	0.25	NR		RFM12N20			BUZ32				
	12.5	0.2	NR					RFP12N20				
	16.0	0.22	510					BUZ31				
	16.0	0.22	580		IRF242(R)				IRFP242R			
	18.0	0.18	510					IRF642(R)				
	18.0	0.18	580		IRF240(R)				IRFP240R			
	25.0	0.12	910		IRF252(R)			IRF640(R)				
	25.0	0.15	NR		RFK25N20							
	27.0	0.12	810							RFH25N20		
	30.0	0.085	910		IRF250(R)				IRFP252(R)			
	33.0	0.085	810									
250V	3.3	1.5	120						IRFP250(R)			
	3.8	1.1	120					IRF625				
	6.5	0.68	180		IRF235			IRF624				
	8.1	0.45	180		IRF234			IRF635				
	13.0	0.34	550		IRF245			IRF634				
	14.0	0.28	550		IRF244			IRF645	IRFP245			
	15.0	0.28	550					IRF644				
	20.0	0.17	1000		IRF255				IRFP244			
	21.0	0.17	1000									
	22.0	0.14	1000		IRF254				IRFP255			
	23.0	0.14	1000									
275V	3.3	1.5	120						IRFP254			
	3.8	1.1	120					IRF627				
	6.5	0.68	180		IRF237			IRF626				
	8.1	0.45	180		IRF236			IRF637				
	13.0	0.34	550		IRF247			IRF636				
	14.0	0.28	550		IRF246			IRF647	IRFP247			
	15.0	0.28	550					IRF646				
	20.0	0.17	1000		IRF257				IRFP246			
	21.0	0.17	1000									
	22.0	0.14	1000		IRF256				IRFP257			
	23.0	0.14	1000						IRFP256			

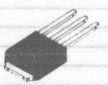
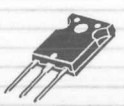
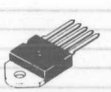
MOSFETs

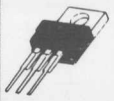
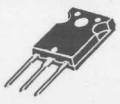
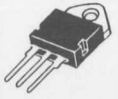
N-Channel (Continued)

Maximum Ratings				Package								
												
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	TO-218	MO-093	4 PIN DIP
N-Channel												
350V	0.3	5.0	45									IRFD313(R)
	0.4	3.6	45									IRFD311(R)
	0.4	2.5	100									IRFD323(R)
	0.5	1.8	100									IRFD321(R)
	1.15	5.0	150	IRFF313(R)								
	1.35	3.6	150	IRFF311(R)								
	1.7	5.0	120					IRF713(R)				
	2.0	3.6	120					IRF711(R)				
	2.0	2.5	100	IRFF323(R)								
	2.5	1.8	100	IRFF321(R)								
	2.8	2.5	190					IRF723(R)				
	2.8	2.5	NR		IRF323							
	3.0	1.5	300	IRFF333(R)								
	3.1	1.8	190			IRFU321	IRFR321					
	3.3	1.8	190					IRF721(R)				
	3.3	1.8	NR		IRF321							
	3.5	1.0	300	IRFF331(R)								
	4.0	2.0	NR		RFM4N35			RFP4N35				
	4.5	1.5	300		IRF333(R)			IRF733(R)				
	5.5	1.0	300		IRF331(R)			IRF731(R)				
	7.0	0.75	NR		RFM7N35			RFP7N35				
	8.0	0.8	520					IRF743(R)				
	8.3	0.8	520		IRF343(R)							
	8.7	0.8	480						IRFP343R			
	10.0	0.55	520		IRF341(R)			IRF741(R)				
	11.0	0.55	480						IRFP341R			
	12.0	0.5	NR		RFM12N35					RFH12N35		
	13.0	0.4	700		IRF353(R)							
	14.0	0.4	700						IRFP353(R)			
	15.0	0.3	700		IRF351(R)				IRFP351(R)			
	16.0	0.3	700									
400V	0.3	5.0	45									IRFD312(R)
	0.4	3.6	45									IRFD310(R)
	0.4	2.5	100									IRFD322(R)
	0.5	1.8	100									IRFD320(R)
	1.15	5.0	150	IRFF312(R)								
	1.35	3.6	150	IRFF310(R)								
	1.7	5.0	120					IRF712(R)				
	2.0	3.6	120					IRF710(R)				
	2.0	2.5	100	IRFF322(R)								
	2.5	1.8	100	IRFF320(R)								

MOSFETs

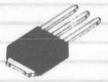
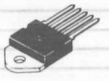
N-Channel (Continued)

Maximum Ratings				Package								
												
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	TO-218	MO-093	4 PIN DIP
							N-Channel					
400V (cont)	2.6	2.5	190			IRFU322	IRFR322					
	2.6	2.5	NR					BUZ76A				
	2.8	2.5	190					IRF722(R)				
	2.8	2.5	NR		IRF322							
	3.0	1.8	NR					BUZ76				
	3.0	1.5	300	IRFF332(R)								
	3.1	1.8	190			IRFU320	IRFR320					
	3.3	1.8	190					IRF720(R)				
	3.3	1.8	NR		IRF320							
	3.5	1.0	300	IRFF330(R)								
	4.0	2.0	NR		RFM4N40			RFP4N40				
	4.5	1.5	300		IRF332(R)			IRF732(R)				
	4.5	1.5	NR					BUZ60B				
	5.5	1.0	300		IRF330(R)			IRF730(R)				
	5.5	1.0	NR					BUZ60				
	7.0	0.75	NR		RFM7N40			RFP7N40				
	8.0	0.8	520					IRF742(R)				
	8.3	0.8	520		IRF342(R)				IRFP342R			
	8.7	0.8	480									
	10.0	0.55	520		IRF340(R)			IRF740(R)				
	11.0	0.55	480						IRFP340R			
	11.5	0.4	NR							BUZ351		
	12.0	0.5	NR		RFM12N40					RFH12N40		
	13.0	0.4	700		IRF352(R)							
	14.0	0.4	700						IRFP352(R)			
	15.0	0.3	700		IRF350(R)							
	16.0	0.3	700						IRFP350(R)			
	20.0	0.25	1200						IRFP362			
	22.0	0.25	980		IRF362							
	23.0	0.2	1200						IRFP360			
	25.0	0.2	980		IRF360							
450V	1.4	4.0	210	IRFF423(R)								
	1.6	3.0	210	IRFF421(R)								
	2.2	4.0	210					IRF823(R)				
	2.2	4.0	NR		IRF423							
	2.25	2.0	300	IRFF433(R)								
	2.5	3.0	210			IRFU421	IRFR421	IRF821(R)				
	2.5	3.0	NR		IRF421							
	2.75	1.5	300	IRFF431(R)								
	3.0	3.0	NR		RFM3N45			RFP3N45				
	4.0	2.0	300		IRF433(R)			IRF833(R)				

Maximum Ratings				Package								
												
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	TO-218	MO-093	4 PIN DIP
N-Channel												
450V (cont)	4.5	1.5	300		IRF431(R)			IRF831(R)				
	6.0	1.25	NR		RFM6N45			RFP6N45				
	7.0	1.1	510		IRF443(R)			IRF843(R)				
	7.0	1.1	480						IRFP443R			
	8.0	0.85	510		IRF441(R)			IRF841(R)				
	8.0	0.85	480						IRFP441R			
	10.0	0.6	NR		RFM10N45					RFH10N45		
	11.0	0.5	860		IRF453(R)							
	12.0	0.5	860						IRFP453(R)			
	13.0	0.4	860		IRF451(R)							
	14.0	0.4	860						IRFP451(R)			
500V	1.4	4.0	210	IRFF422(R)								
	1.6	3.0	210	IRFF420(R)								
	2.2	4.0	210			IRFU422	IRFR422	IRF822(R)				
	2.2	4.0	NR		IRF422							
	2.25	2.0	300	IRFF432(R)								
	2.5	3.0	210			IRFU420	IRFR420	IRF820(R)				
	2.5	3.0	NR		IRF420							
	2.75	1.5	300	IRFF430(R)								
	3.0	3.0	NR		RFM3N50			RFP3N50				
	4.0	2.0	300		IRF432(R)			IRF832(R)				
	4.0	2.0	NR					BUZ42				
	4.5	1.5	300		IRF430(R)			IRF830(R)				
	4.5	1.5	NR					BUZ41A				
	6.0	1.25	NR		RFM6N50			RFP6N50				
	7.0	1.1	510		IRF442(R)			IRF842(R)				
	7.0	1.1	480						IRFP442(R)			
	8.0	0.85	510		IRF440(R)			IRF840(R)				
	8.0	0.85	480						IRFP440(R)			
	8.3	0.8	NR		BUZ45A							
	9.6	0.6	NR		BUZ45							
	10.0	0.6	NR		RFM10N50					RFH10N50		
	10.0	0.5	NR		BUZ45B							
	11.0	0.5	860		IRF452(R)							
	12.0	0.5	860						IRFP452(R)			
	13.0	0.4	860		IRF450(R)							
	14.0	0.4	860						IRFP450(R)			
	17.0	0.35	960						IRFP462			
	19.0	0.35	1220		IRF462							
	20.0	0.27	960						IRFP460			
	21.0	0.27	1200		IRF460							

MOSFETs

N-Channel (Continued)

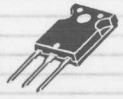
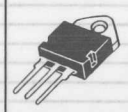
Maximum Ratings				Package								
												
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	TO-218	MO-093	4 PIN DIP
N-Channel												
600V	5.4	1.6	570		IRFAC42R			IRFBC42R				
	5.9	1.6	410						IRFPC42R			
	6.2	1.2	570		IRFAC40R			IRFBC40R				
	6.8	1.2	410						IRFPC40R			
1000V	3.9	4.2	490						IRFPG42			
	4.3	3.5	490						IRFPG40			
	4.3	3.5	NR					RFP4N100				

* More complete ruggedness capability now specified; UIS current vs time in avalanche graph data sheet

SHADING indicates Developmental Products - N.R. Not Rated for UIS capability - **QPL Approved Types

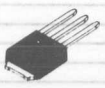
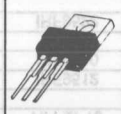
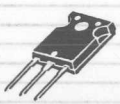
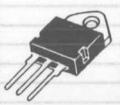
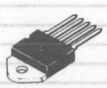
MOSFETs

P-Channel

Maximum Ratings				Package								
												
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	TO-218	MO-093	4 PIN DIP
							P-Channel					
50V	8.0	0.3	NR			RFD8P05	RFD8P05SM	RFP8P05				
	15.0	0.15	NR			RFD15P05	RFD15P05SM	RFP15P05				
	30.0	0.065	NR					RFP30P05	RFG30P05			
	60.0	0.026	NR						RFG60P05E			
60V	0.6	1.6	190									IRFD9113
	0.8	0.8	370									IRFD9123
	2.5	1.9	190					IRF9513				
	3.0	1.2	190					IRF9511				
	3.5	0.8	370	IRFF9123								
	4.0	0.6	370	IRFF9121								
	5.0	0.8	370					IRF9523				
	5.5	0.4	500	IRFF9133								
	6.0	0.6	370					IRF9521				
	6.5	0.3	500	IRFF9131								
	10.0	0.4	500		IRF9133			IRF9533				
	12.0	0.3	500		IRF9131			IRF9531				
	15.0	0.3	960		IRF9143			IRF9543				
	16.0	0.3	960						IRFP9143			
	19.0	0.2	960		IRF9141			IRF9541	IRFP9141			
	25.0	0.15	1300		IRF9151				IRFP9151			
	30.0	0.075	NR					RFP30P06	RFG30P06			
	60.0	0.030	NR						RFG60P06E			
80V	1.0	3.65	NR	RFL1P08								
	2.0	3.5	NR					RFP2P08				
	6.0	0.6	NR		RFM6P08			RFP6P08				
	8.0	0.4	NR		RFM8P08			RFP8P08				
	12.0	0.3	NR		RFM12P08			RFP12P08				
	25.0	0.15	NR		RFK25P08					RFH25P08		
100V	0.7	1.2	190									IRFD9110
	1.0	0.6	370									IRFD9120
	1.0	3.65	NR	RFL1P10								
	2.0	3.5	NR					RFP2P10				
	2.5	1.6	190									
	3.0	1.2	190					IRF9512				
	3.5	0.8	370	IRFF9122				IRF9510				
	4.0	0.6	370	IRFF9120								
	5.0	0.8	370					IRF9522				
	5.5	0.4	500	IRFF9132								
	6.0	0.6	370					IRF9520				

MOSFETs

P-Channel (Continued)

Maximum Ratings				Package								
												
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	TO-218	MO-093	4 PIN DIP
P-Channel												
100V	6.0	0.6	NR		RFM6P10			RFP6P10				
(cont)	8.0	0.3	500	IRFF9130								
	8.0	0.4	NR		RFM8P10			RFP8P10				
	10.0	0.4	500		IRF9132			IRF9532				
	12.0	0.3	500		IRF9130			IRF9530				
	12.0	0.3	NR		RFM12P10			RFP12P10				
	15.0	0.3	960		IRF9142			IRF9542				
	16.0	0.3	960						IRFP9142			
	19.0	0.2	960		IRF9140			IRF9540	IRFP9140			
	25.0	0.15	1300		IRF9150				IRFP9150			
	25.0	0.15	NR		RFK25P10					RFH25P10		
120V	5.0	1.0	NR		RFM5P12			RFP5P12				
	10.0	0.5	NR		RFM10P12			RFP10P12				
150V	0.45	2.4	290									IRFD9223
	2.0	2.4	290	IRFF9223								
	2.5	1.5	290	IRFF9221								
	3.0	2.4	290					IRF9623				
	3.5	1.5	290					IRF9621				
	3.5	1.2	500	IRFF9233								
	4.0	0.8	500	IRFF9231								
	5.0	1.0	NR		RFM5P15			RFP5P15				
	5.5	1.2	500		IRF9233			IRF9633				
	6.5	0.8	500		IRF9231			IRF9631				
	9.0	0.7	790		IRF9243			IRF9643				
	10.0	0.5	NR		RFM10P15			RFP10P15				
	10.0	0.7	790						IRFP9243			
	11.0	0.5	790		IRF9241			IRF9641				
	12.0	0.5	790						IRFP9241			
200V	0.6	1.5	290									IRFD9220
	2.0	2.4	290	IRFF9222								
	2.5	1.5	290	IRFF9220								
	3.0	2.4	290					IRF9622				
	3.5	1.5	290					IRF9620				
	3.5	1.2	500	IRFF9232								
	4.0	0.8	500	IRFF9230								
	5.5	1.2	500		IRF9232			IRF9632				
	6.5	0.8	500		IRF9230			IRF9630				
	9.0	0.7	790		IRF9242			IRF9642				
	10.0	0.7	790						IRFP9242			
	11.0	0.5	790		IRF9240			IRF9640				
	12.0	0.5	790						IRFP9240			

MOSFETs

JEDEC N-Channel

Maximum Ratings			Package	
				
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	TO-205AF	TO-204
60	12.0	0.25		2N6755
	31.0	0.08		2N6763
100	3.5	0.6	2N6782*	
	6.0	0.3	2N6788*	
	8.0	0.18	2N6796*	
	14.0	0.18		2N6756*
	38.0	0.055		2N6764*
150	8.0	0.6		2N6757
	25.0	0.12		2N6765
200	2.25	1.5	2N6784*	
	3.5	0.8	2N6790*	
	5.5	0.4	2N6798*	
	9.0	0.4		2N6758*
	30.0	0.085		2N6766*
350	4.5	1.5		2N6759
	12.0	0.4		2N6767
400	1.25	3.6	2N6786*	
	2.0	1.8	2N6792*	
	3.0	1.0	2N6800*	
	5.5	1.0		2N6760*
	14.0	0.3		2N6768*
450	4.0	2.0		2N6761
	11.0	0.5		2N6769
500	1.5	3.0	2N6794*	
	3.5	1.5	2N6802*	
	4.5	1.5		2N6762*
	12.0	0.4		2N6770*

* QPL Approved Types

JEDEC P-Channel

Maximum Ratings			Package	
				
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	TO-205AF	TO-204
100	1.16	3.65	2N6895	
	6.0	0.6		2N6896
	6.5	0.3	2N6849	
	11.0	0.3		2N6804
	12.0	0.3		2N6897
	25.0	0.2		2N6898
200	4.0	0.8	2N6851	

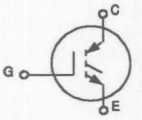
IGBTs

Combines the characteristics of a power MOSFET, a bipolar transistor.

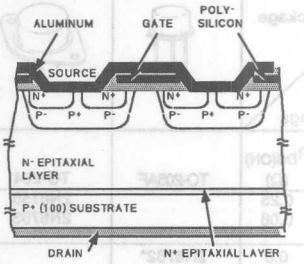
Features:

• Voltage Gated	Requires small gate power. Similar to standard power MOSFET
• Turn Off	Turns off when gate drive is removed
• On-State Voltage Drop	Nonlinear. Temperature independent. Unlike the typical 2X variation of a power MOSFET
• Turn-On Speed	Fast! Comparable to a standard power MOSFET
• Turn-Off Speed	Comparable to a bipolar transistor.

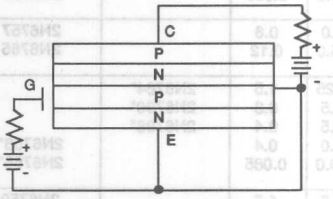
Schematic Symbol



Cross Section Of Chip Structure

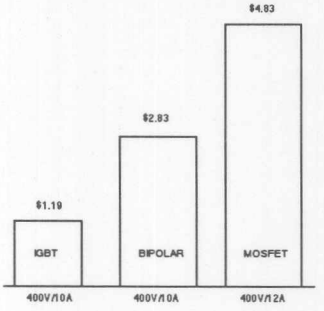


Junction Diagram Showing Biasing Arrangements

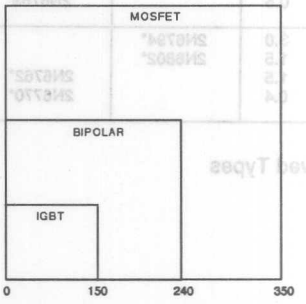


Comparisons

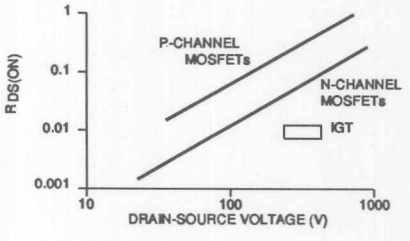
Cost Comparison - 1K Price Less Than Half the MOSFET Price!



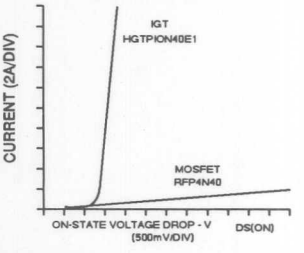
Size Comparison - 500V, 15A Capability



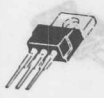
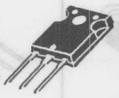
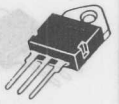
$R_{DS(ON)}$ Performance Comparison



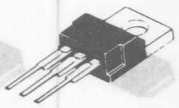
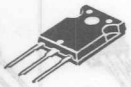
Performance; I/V Characteristic-N-Channel MOSFET vs. IGT (Same Size Dies)



IGBTs

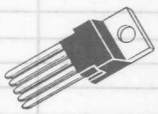
Maximum Ratings / Package										
BV_{CES} (V)	I_{C90} (A)	I_{CM} (A)	t_f (μS)	TO-204AA	TO-220AB	TO-247	TO-218AC	TO-251	TO-252	MO-093
400	5	10	1.0	2N6975						
			0.5	2N6977						
	6	7.5	1.0					HGTD6N40E1	HGTD6N40E1S	
	10	12	1.2					HGTD10N40F1	HGTD10N40F1S	
	10	17.5	1.0		HGTP10N40E1					
			0.5		HGTP10N40C1					
	12	17.5	1.0	HGTM12N40E1			HGTH12N40E1			
			0.5	HGTM12N40C1			HGTH12N40C1			
	15	35	1.0		HGTP15N40E1					
			0.5		HGTP15N40C1					
	20	35	1.0	HGTM20N40E1			HGTH20N40E1			
			0.5	HGTM20N40C1			HGTH20N40C1			
500	5	10	1.0	2N6976						
			0.5	2N6978						
	6	7.5	1.0					HGTD6N50E1	HGTD6N50E1S	
	10	12	1.2					HGTD10N50F1	HGTD10N50F1S	
	10	17.5	1.0		HGTP10N50E1					
			0.5		HGTP10N50C1					
	12	17.5	1.0	HGTM12N50E1			HGTH12N50E1			
			0.5	HGTM12N50C1			HGTH12N50C1			
	15	35	1.0		HGTP15N50E1					
			0.5		HGTP15N50C1					
	20	35	1.0	HGTM20N50E1			HGTH20N50E1			
			0.5	HGTM20N50C1			HGTH20N50C1			
600	12	48	0.6	HGTM12N60D1	HGTP12N60D1					
	24	96	0.6	HGTM24N60D1		HGTG24N60D1				
	32	200	0.8	HGTM32N60E2		HGTG32N60E2				
1000	20	100	0.68	HGTM20N100D2		HGTG20N100D2				HGTA32N60E2
	34	200	0.87	HGTM34N100E2		HGTG34N100E2				
1200	20	100				HGTG20N120D2				
	30	200	0.75			HGTG30N120E2				

IGBTs w/ Integral Reverse Diode

Maximum Ratings / Package						
BV_{CES} (V)	I_{C90} (A)	I_{CM} (A)	t_f (µS)	TO-220AB	TO-218AC	TO-247
400	6	7.5	1.0	HGTP6N40E1D		
	10	12	1.2	HGTP10N40F1D		
	10	17.5	1.0	HGTP10N40E1D		
			0.5	HGTP10N40C1D		
	12	17.5	1.0		HGTH12N40E1D	
			0.5		HGTH12N40C1D	
	20	35	1.0		HGTH20N40E1D	
			0.5		HGTH20N40C1D	
500	6	7.5	1.0	HGTP6N50E1D		
	10	12	1.2	HGTP10N50F1D		
	10	17.5	1.0	HGTP10N50E1D		
			0.5	HGTP10N50C1D		
	12	17.5	1.0		HGTH12N50E1D	
			0.5		HGTH12N50C1D	
	20	35	1.0		HGTH20N50E1D	
			0.5		HGTH20N50C1D	HGTG20N50C1D
600	12	48	0.6			HGTG12N60D1D
	24	96	0.6			HGTG24N60D1D

NOTES:
1. I_{C90} =maximum continuous current rating at T_C = 90°C
2. I_{CM} = maximum pulsed current rating
3. t_f measured at T_C = 150°C

IGBTs w/ Current Sensing

Maximum Ratings / Package				
BV_{CES} (V)	I_{C90} (A)	I_{CM} (A)	t_f (µS)	TS-001
600	12	40	1.0	HGTB12N60D1C
	24	80	1.6	

NOTES:
1. I_{C90} =maximum continuous current rating at T_C = 90°C
2. I_{CM} = maximum pulsed current rating
3. t_f measured at T_C = 150°C

POWER MOSFETs 4

N-CHANNEL POWER MOSFETs

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RFM6N45, RFM6N50, RFP6N45, RFP6N50	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-610
RFM7N35, RFM7N40, RFP7N35, RFP7N40	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-614
RFM8N18, RFM8N20, RFP8N18, RFP8N20	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-618
RFM10N12, RFM10N15, RFP10N12, RFP10N15	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-622
RFH10N45, RFH10N50	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-626
RFM10N45, RFM10N50	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-630
RFM12N08, RFM12N10, RFP12N08, RFP12N10	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-634
RFM12N18, RFM12N20, RFP12N18, RFP12N20	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-638
RFH12N35, RFH12N40	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-642
RFM12N35, RFM12N40	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-646
RFD14N05, RFD14N05SM, RFP14N05	N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)	4-650
RFM15N05, RFM15N06, RFP15N05, RFP15N06	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-655
RFM15N12, RFM15N15, RFP15N12, RFP15N15	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-661
RFD16N05, RFD16N05SM	N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)	4-665
RFM18N08, RFM18N10, RFP18N08, RFP18N10	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-669
RFP22N10	N-Channel Enhancement-Mode Power Field-Effect Transistor (MegaFET)	4-673
RFP25N05	N-Channel Enhancement-Mode Power Field-Effect Transistor (MegaFET)	4-677
RFM25N06, RFP25N06	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-682
RFH25N18, RFH25N20	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-686
RFK25N18, RFK25N20	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-690
RFH30N12, RFH30N15	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-694
RFK30N12, RFK30N15	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-698
RFH35N08, RFH35N10	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-702
RFK35N08, RFK35N10	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-706
RFG40N10, RFP40N10	N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)	4-710
RFH45N05, RFH45N06	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-715
RFK45N05, RFK45N06	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-719
RFP50N05, RFG50N05	N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)	4-723
RFG75N05E, RFH75N05E	N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)	4-728
RFA100N05E	N-Channel Enhancement-Mode Power Field-Effect Transistor (MegaFET)	4-733

HARRIS

2N6755
2N6756

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 12A and 14A, 60V - 100V
- $r_{DS(on)}$ = 0.18Ω and 0.25Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

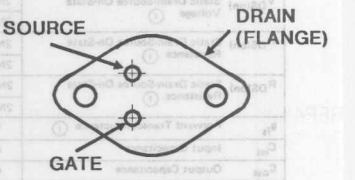
Description

The 2N6755 and 2N6756 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

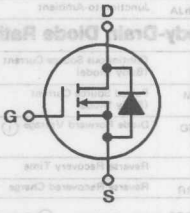
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6755	2N6756	UNITS
Drain-Source Voltage	V_{DS}	60*	100*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	60*	100*	V
Continuous Drain Current				
T_C = +25°C	I_D	12*	14*	A
T_C = +100°C	I_D	8.0*	9.0*	A
Pulsed Drain Current	I_{DM}	25	30	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C (See Fig. 11)	P_D	75*	75*	W
T_C = +100°C (See Fig. 11)	P_D	30*	30*	W
Linear Derating Factor (See Fig. 11)		0.6*	0.6*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	25	30	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1586.1

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6755	60	–	–	V	V_{GS} = 0
		2N6756	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, $T_C = 125^oC$
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6755	–	–	3.0*	V	V_{GS} = 10V, I_D = 12A
		2N6756	–	–	2.52*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6755	–	0.20	0.25*	Ω	V_{GS} = 10V, I_D = 8A
		2N6756	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 9A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6755	–	–	0.45*	Ω	V_{GS} = 10V, I_D = 8A, $T_C = 125^oC$
		2N6756	–	–	0.33*	Ω	V_{GS} = 10V, I_D = 9A, $T_C = 125^oC$
g_{fs}	Forward Transconductance (1)	ALL	4.0*	5.5	12.0*	S (℧)	V_{DS} = 15V, I_D = 9A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	150*	300	500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 36V$, I_D = 9A, $Z_o = 15\Omega$ (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	75*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	40*	ns	
t_f	Fall Time	ALL	–	–	45*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6755	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6756	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6755	–	–	25	A	
		2N6756	–	–	30		
V_{SD}	Diode Forward Voltage (1)	2N6755	0.85*	–	1.7*	V	$T_C = 25^oC$, I_S = 12A, V_{GS} = 0
		2N6756	0.90*	–	1.8*	V	$T_C = 25^oC$, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

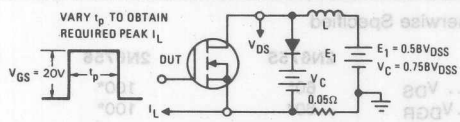


Fig. 1 – Clamped Inductive Test Circuit

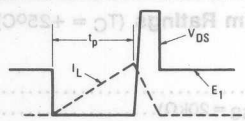


Fig. 2 – Clamped Inductive Waveforms

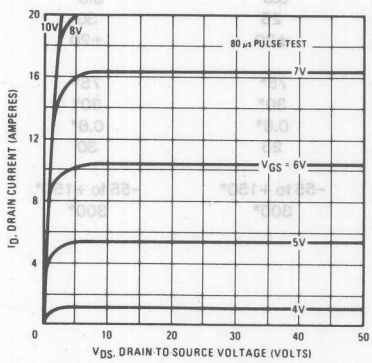


Fig. 3 – Typical Output Characteristics

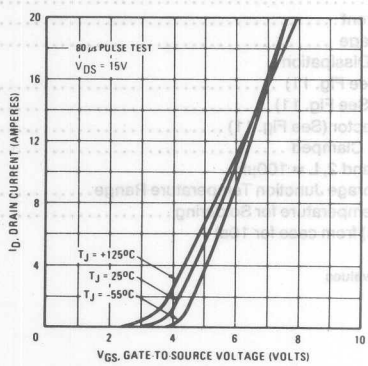


Fig. 4 – Typical Transfer Characteristics

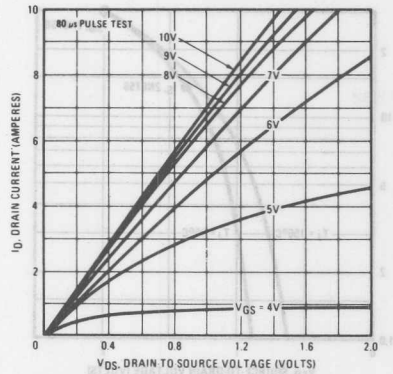


Fig. 5– Typical Saturation Characteristics (2N6755)

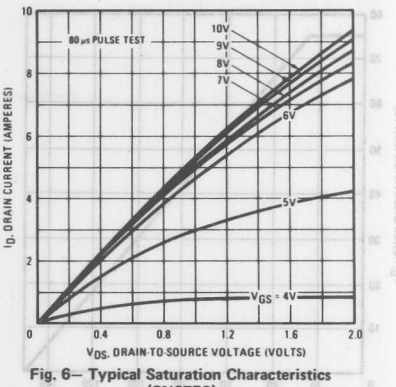


Fig. 6– Typical Saturation Characteristics (2N6756)

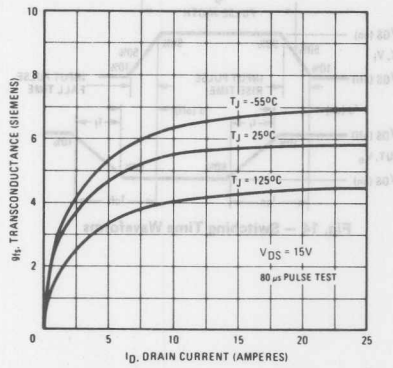


Fig. 7 – Typical Transconductance Vs. Drain Current

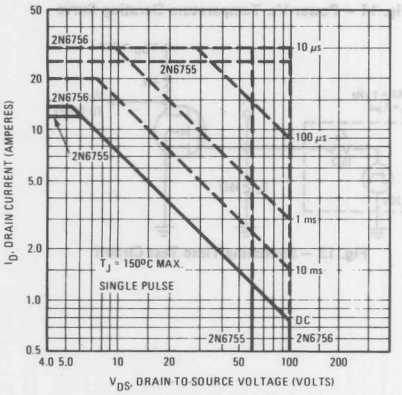


Fig. 8 – Maximum Safe Operating Area

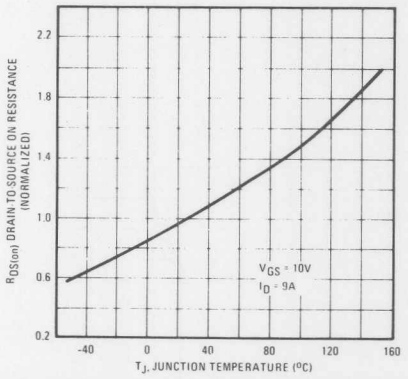


Fig. 9 – Normalized Typical On-Resistance Vs. Temperature

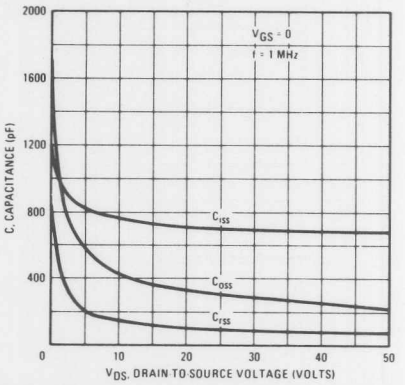


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

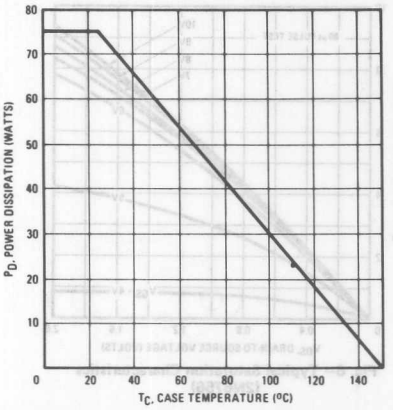


Fig. 11 — Power Vs. Temperature Derating Curve

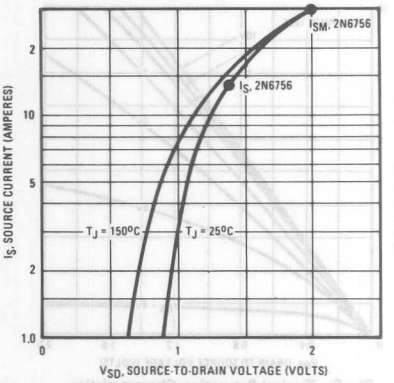


Fig. 12 — Typical Body-Drain Diode Forward Voltage

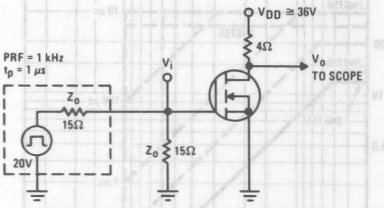


Fig. 13 — Switching Time Test Circuit

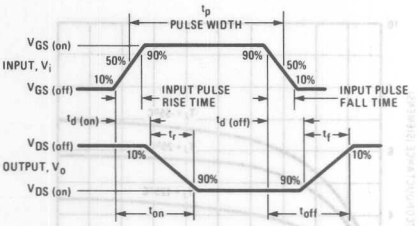


Fig. 14 — Switching Time Waveforms

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2N6757
2N6758

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 8A and 9A, 150V - 200V
- $r_{DS(on)}$ = 0.4Ω and 0.6Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

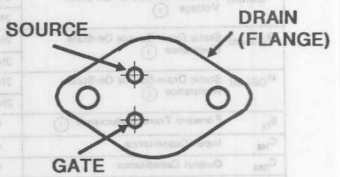
Description

The 2N6757 and 2N6758 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

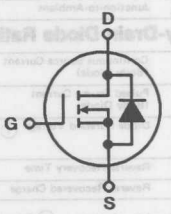
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4
N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6757	2N6758	UNITS
Drain-Source Voltage	V_{DS}	150*	200*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	150*	200*	V
Continuous Drain Current				
T_C = +25°C	I_D	8.0*	9.0*	A
T_C = +100°C	I_D	5.0*	6.0*	A
Pulsed Drain Current	I_{DM}	12	15	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C (See Figure 11)	P_D	75*	75*	W
T_C = +100°C (See Figure 11)	P_D	30*	30*	W
Linear Derating Factor (See Figure 11)		0.6*	0.6*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	12	15	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1587.1

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6757	150	–	–	V	$V_{GS} = 0$
		2N6758	200	–	–	V	$I_D = 1.0$ mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	$V_{GS} = 20V$
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_C = 125^oC$
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6757	–	–	4.8*	V	$V_{GS} = 10V$, $I_D = 8A$
		2N6758	–	–	3.6*	V	$V_{GS} = 10V$, $I_D = 9A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6757	–	0.4	0.6*	Ω	$V_{GS} = 10V$, $I_D = 5A$
		2N6758	–	0.25	0.4*	Ω	$V_{GS} = 10V$, $I_D = 6A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6757	–	–	1.13*	Ω	$V_{GS} = 10V$, $I_D = 5A$, $T_C = 125^oC$
		2N6758	–	–	0.75*	Ω	$V_{GS} = 10V$, $I_D = 6A$, $T_C = 125^oC$
g_{fs}	Forward Transconductance ①	ALL	3.0*	5.0	9.0*	S (℧)	$V_{DS} = 15V$, $I_D = 6A$
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	100*	250	450*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	40*	80	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 90V$, $I_D = 6A$, $Z_o = 15\Omega$ (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50*	ns	
t_f	Fall Time	ALL	–	–	40*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6757	–	–	8.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6758	–	–	9.0*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6757	–	–	12	A	
		2N6758	–	–	15		
V_{SD}	Diode Forward Voltage ①	2N6757	0.75*	–	1.50*	V	$T_C = 25^oC$, $I_S = 8A$, $V_{GS} = 0$
		2N6758	0.80*	–	1.60*	V	$T_C = 25^oC$, $I_S = 9A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

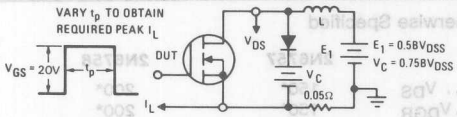


Fig. 1 – Clamped Inductive Test Circuit

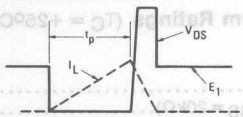


Fig. 2 – Clamped Inductive Waveforms

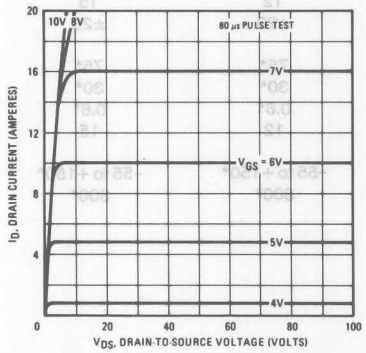


Fig. 3 – Typical Output Characteristics

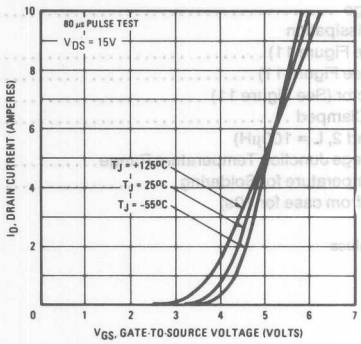


Fig. 4 – Typical Transfer Characteristics

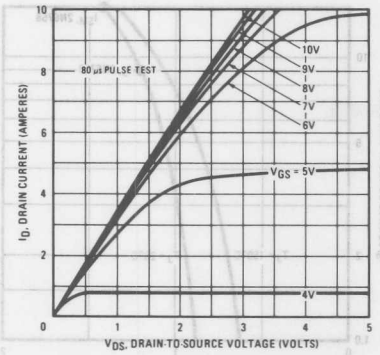


Fig. 5– Typical Saturation Characteristics (2N6757)

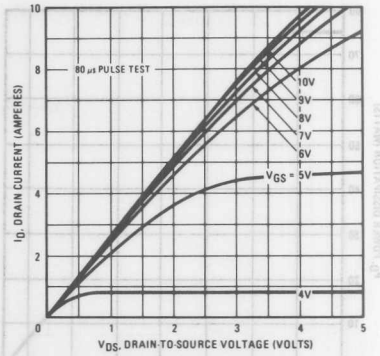


Fig. 6– Typical Saturation Characteristics (2N6758)

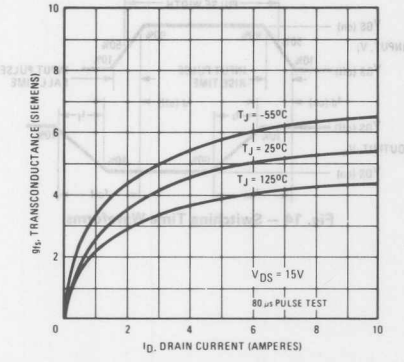


Fig. 7 – Typical Transconductance Vs. Drain Current

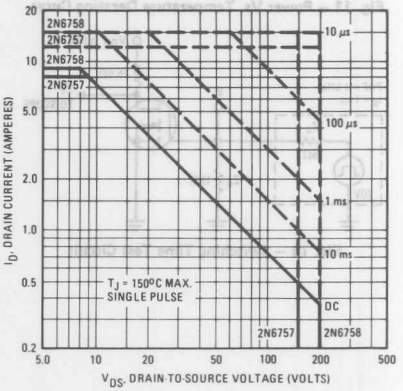


Fig. 8 – Maximum Safe Operating Area

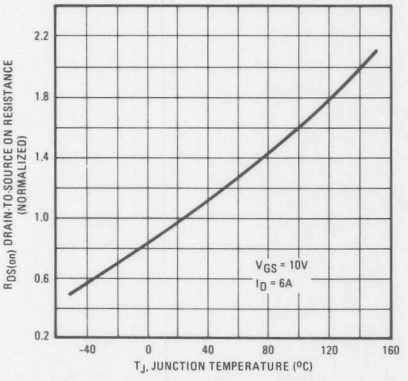


Fig. 9 – Normalized Typical On-Resistance Vs. Temperature

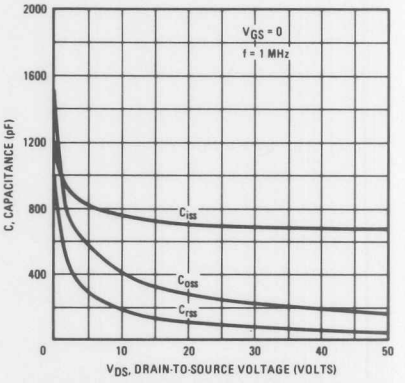


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

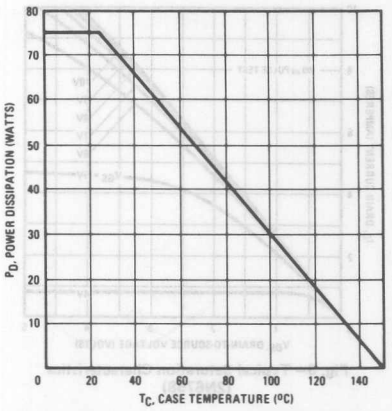


Fig. 11 — Power Vs. Temperature Derating Curve

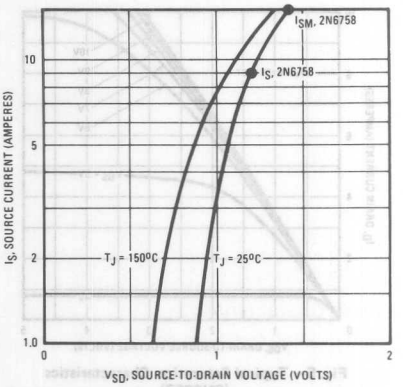


Fig. 12 — Typical Body-Drain Diode Forward Voltage

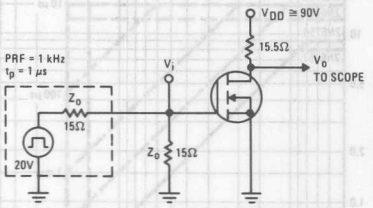


Fig. 13 — Switching Time Test Circuit

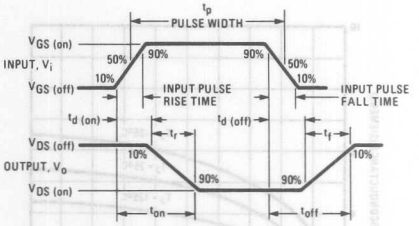


Fig. 14 — Switching Time Waveforms

HARRIS

2N6759
2N6760

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 4.5A and 5.5A, 350V - 400V
- $r_{DS(on)}$ = 1.0Ω and 1.5Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

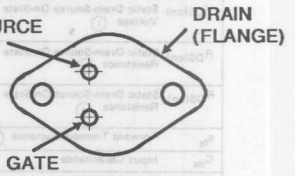
Description

The 2N6759 and 2N6760 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

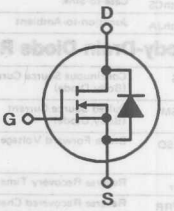
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		2N6759	2N6760	UNITS
Drain-Source Voltage	V_{DS}	350*	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	350*	400*	V
Continuous Drain Current				
T_C = +25°C	I_D	4.5*	5.5*	A
T_C = +100°C	I_D	3.0*	3.5*	A
Pulsed Drain Current	I_{DM}	7.0	8.0	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C (See Figure 11)	P_D	75*	75*	W
T_C = +100°C (See Figure 11)	P_D	30*	30*	W
Linear Derating Factor (See Figure 11)		0.6*	0.6*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	7.0	8.0	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1588.1

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6759	350	–	–	V	V_{GS} = 0
		2N6760	400	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, $T_C = 125^oC$
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6759	–	–	7.0*	V	V_{GS} = 10V, I_D = 4.5A
		2N6760	–	–	6.7*	V	V_{GS} = 10V, I_D = 5.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6759	–	1.0	1.5*	Ω	V_{GS} = 10V, I_D = 3A
		2N6760	–	0.8	1.0*	Ω	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6759	–	–	3.3*	Ω	V_{GS} = 10V, I_D = 3A, $T_C = 125^oC$
		2N6760	–	–	2.2*	Ω	V_{GS} = 10V, I_D = 3.5A, $T_C = 125^oC$
g_{fs}	Forward Transconductance (1)	ALL	3.0*	4.5	9.0*	S (℧)	V_{DS} = 15V, I_D = 3.5A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	50*	150	300*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	20*	40	80*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 175V$, I_D = 3.5A, $Z_o = 15\Omega$
t_r	Rise Time	ALL	–	–	35*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	35*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6759	–	–	4.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6760	–	–	5.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6759	–	–	7.0	A	
		2N6760	–	–	8.0		
V_{SD}	Diode Forward Voltage (1)	2N6759	0.70*	–	1.4*	V	$T_C = 25^oC$, I_S = 4.5A, V_{GS} = 0
		2N6760	0.75*	–	1.5*	V	$T_C = 25^oC$, I_S = 5.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	550	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	8.0	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

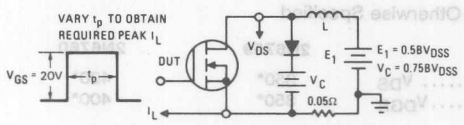


Fig. 1 – Clamped Inductive Test Circuit

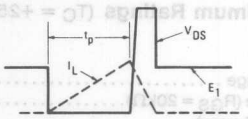


Fig. 2 – Clamped Inductive Waveforms

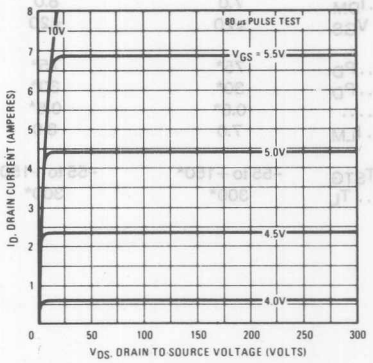


Fig. 3 – Typical Output Characteristics

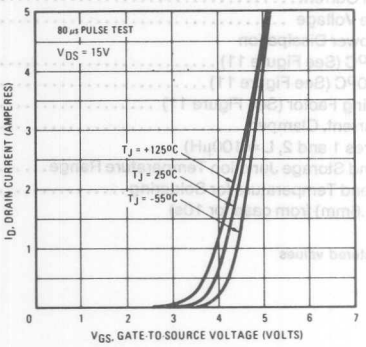


Fig. 4 – Typical Transfer Characteristics

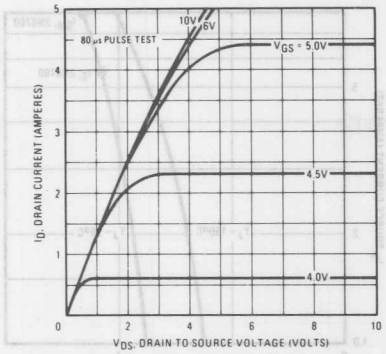


Fig. 5— Typical Saturation Characteristics (2N6759)

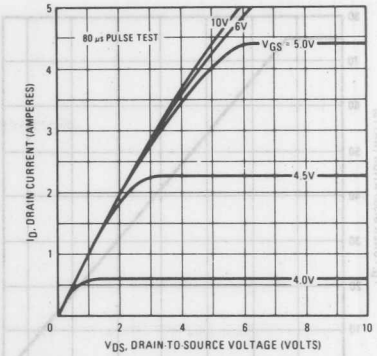


Fig. 6— Typical Saturation Characteristics (2N6760)

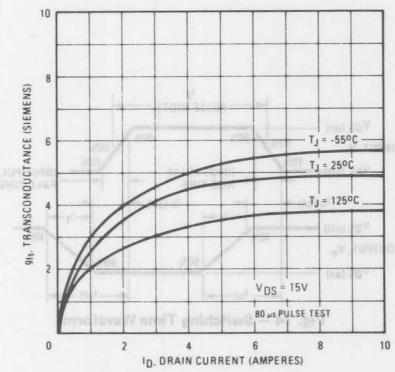


Fig. 7 — Typical Transconductance Vs. Drain Current

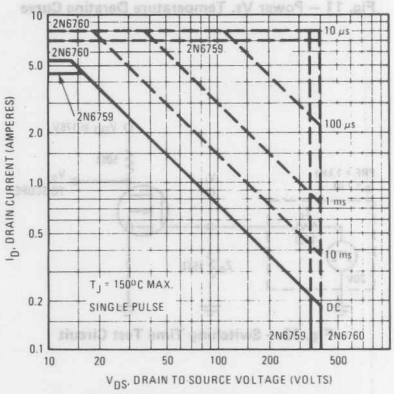


Fig. 8 — Maximum Safe Operating Area

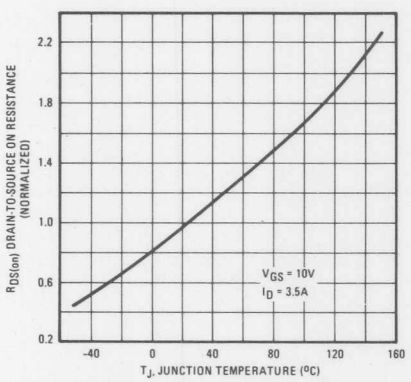


Fig. 9—Normalized Typical On-Resistance Vs. Temperature

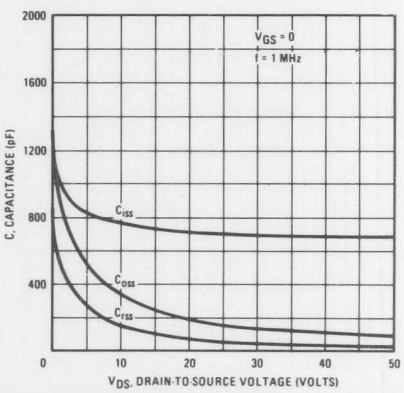


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

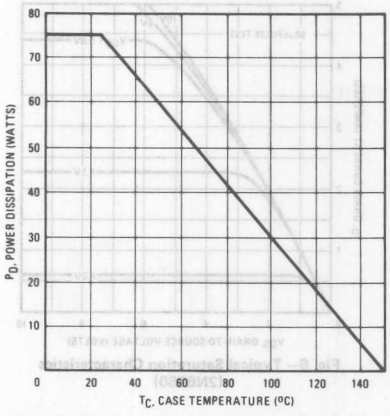


Fig. 11 – Power Vs. Temperature Derating Curve

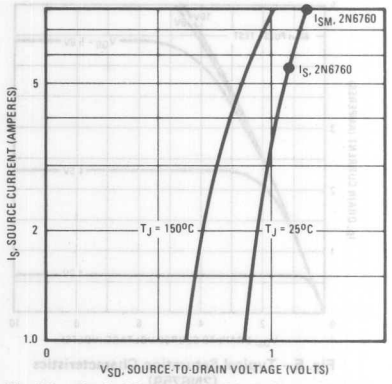


Fig. 12 – Typical Body-Drain Diode Forward Voltage

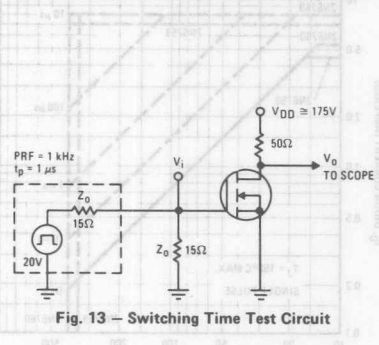


Fig. 13 – Switching Time Test Circuit

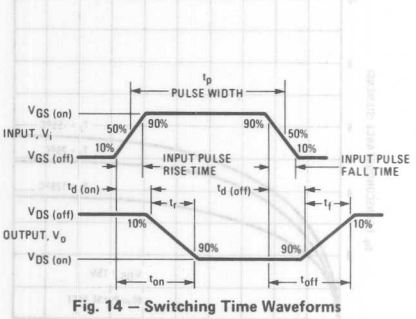


Fig. 14 – Switching Time Waveforms

HARRIS

2N6761
2N6762

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 4.0A and 4.5A, 450V - 500V
- $r_{DS(on)}$ = 1.5Ω and 2.0Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

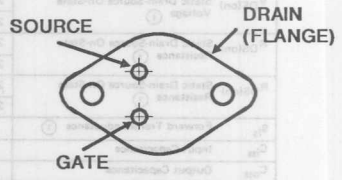
Description

The 2N6761 and 2N6762 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

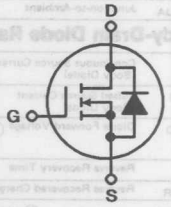
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6761	2N6762	UNITS
Drain-Source Voltage	V_{DS}	450*	500*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	450*	500*	V
Continuous Drain Current				
T_C = +25°C	I_D	4.0*	5.5*	A
T_C = +100°C	I_D	2.5*	3.0*	A
Pulsed Drain Current	I_{DM}	6.0	7.0	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C (See Figure 11)	P_D	75*	75*	W
T_C = +100°C (See Figure 11)	P_D	30*	30*	W
Linear Derating Factor (See Figure 11)		0.6*	0.6*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	6.0	7.0	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1589.1

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6761	450	–	–	V	V_{GS} = 0
		2N6762	500	–	–	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, $T_C = 25^oC$ to 125^oC
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6761	–	–	8.0*	V	V_{GS} = 10V, I_D = 4A
		2N6762	–	–	7.7*	V	V_{GS} = 10V, I_D = 4.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6761	–	1.5	2.0*	Ω	V_{GS} = 10V, I_D = 2.5A
		2N6762	–	1.3	1.5*	Ω	V_{GS} = 10V, I_D = 3.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6761	–	–	4.4*	Ω	V_{GS} = 10V, I_D = 2.5A, $T_C = 125^oC$
		2N6762	–	–	3.3*	Ω	V_{GS} = 10V, I_D = 3.0A, $T_C = 125^oC$
g_{fs}	Forward Transconductance ①	ALL	2.5*	3.5	7.5*	S (℧)	V_{DS} = 16V, I_D = 3A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	25*	100	200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	15*	30	60*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 225V$, I_D = 3A, $Z_o = 15\Omega$
t_r	Rise Time	ALL	–	–	30*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	30*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6761	–	–	4.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6762	–	–	4.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6761	–	–	6.0	A	
		2N6762	–	–	7.0		
V_{SD}	Diode Forward Voltage ①	2N6761	0.65*	–	1.3*	V	$T_C = 25^oC$, I_S = 4A, V_{GS} = 0
		2N6762	0.7*	–	1.4*	V	$T_C = 25^oC$, I_S = 4.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.0	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

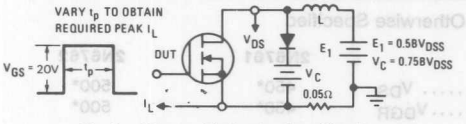


Fig. 1 – Clamped Inductive Test Circuit

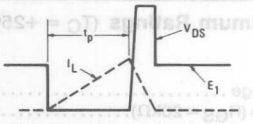


Fig. 2 – Clamped Inductive Waveforms

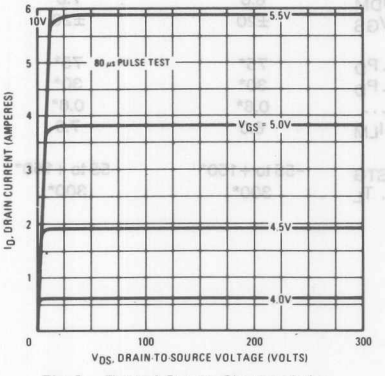


Fig. 3 – Typical Output Characteristics

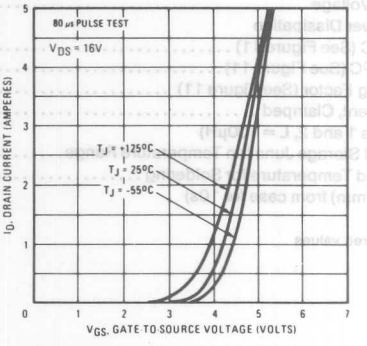


Fig. 4 – Typical Transfer Characteristics

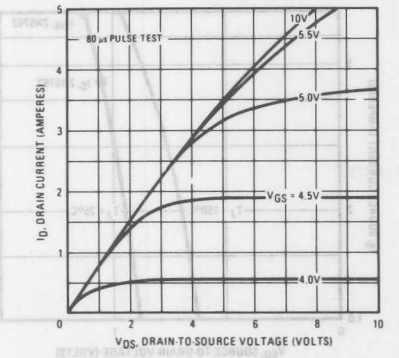


Fig. 5— Typical Saturation Characteristics (2N6761)

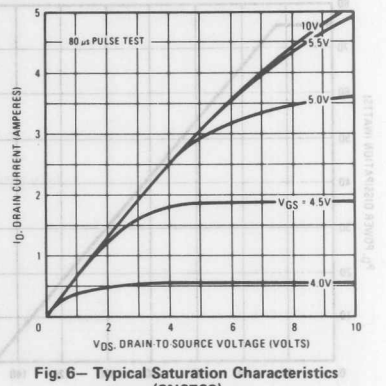


Fig. 6— Typical Saturation Characteristics (2N6762)

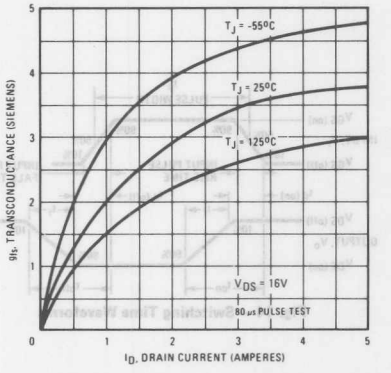


Fig. 7 — Typical Transconductance Vs. Drain Current

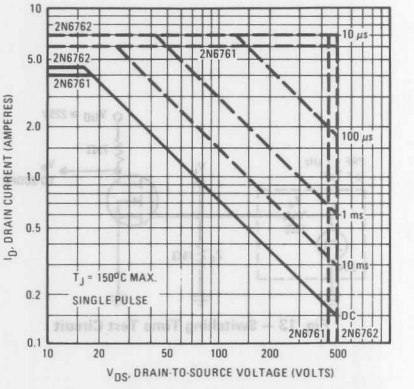


Fig. 8 — Maximum Safe Operating Area

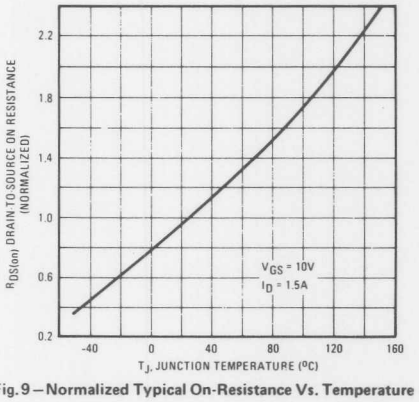


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

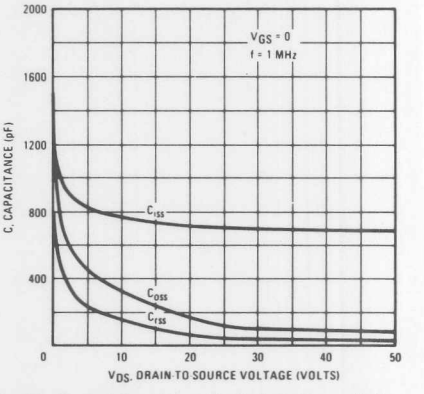


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

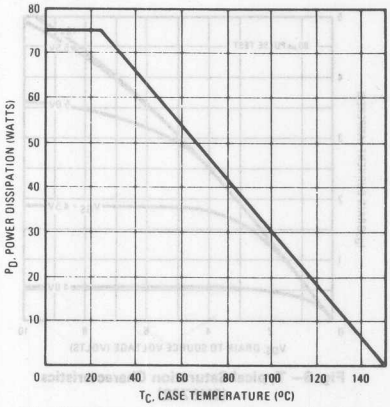


Fig. 11 – Power Vs. Temperature Derating Curve

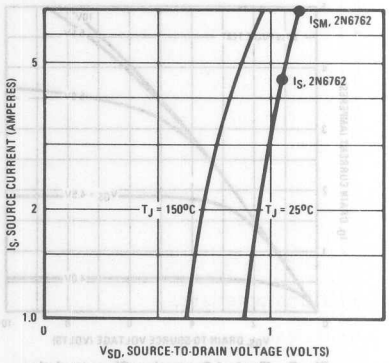


Fig. 12 – Typical Body-Drain Diode Forward Voltage

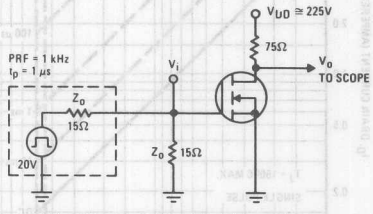


Fig. 13 – Switching Time Test Circuit

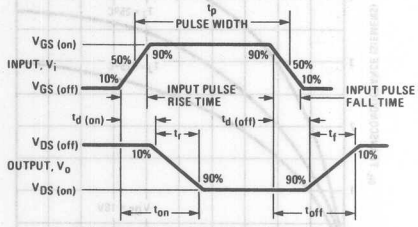


Fig. 14 – Switching Time Waveforms

HARRIS

2N6763
2N6764

N-Channel Enhancement-Mode Power MOS Field-Effect Transistors

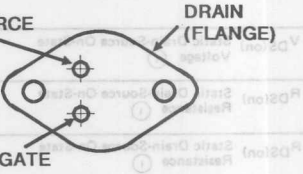
August 1991

Features

- 31A and 38A, 60V - 100V
- $r_{DS(on)}$ = 0.08Ω and 0.055Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AE
BOTTOM VIEW



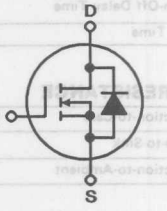
Description

The 2N6763 and 2N6764 are n-channel enhancement-mode silicon-gate power MOS field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AE steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	2N6763	2N6764	UNITS
Drain-Source Voltage ..... V_{DS}	60*	100*	V
Drain-Gate Voltage (R_{GS} = 20kΩ) ..... V_{DGR}	60*	100*	V
Continuous Drain Current			
T_C = +25°C ..... I_D	31	38	A
T_C = +100°C ..... I_D	20	24	A
Pulsed Drain Current ..... I_{DM}	60	70	A
Gate-Source Voltage ..... V_{GS}	±20*	±20*	V
Maximum Power Dissipation			
T_C = +25°C (See Figure 11) ..... P_D	150*	150*	W
T_C = +100°C (See Figure 11) ..... P_D	60*	60*	W
Linear Derating Factor (See Figure 11)	1.2	1.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figures 1 and 2, L = 100μH)	60	70	A
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1590.1

ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6763	60	–	–	V	V_{GS} = 0
		2N6764	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6763	–	–	2.48*	V	V_{GS} = 10V I_D = 31A
		2N6764	–	–	2.09*	V	V_{GS} = 10V, I_D = 38A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6763	–	0.06	0.08*	Ω	V_{GS} = 10V, I_D = 20A
		2N6764	–	0.045	0.055*	Ω	V_{GS} = 10V, I_D = 24A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6763	–	–	0.136*	Ω	V_{GS} = 10V, I_D = 20A, T_C = 125°C
		2N6764	–	–	0.094*	Ω	V_{GS} = 10V, I_D = 24A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	9.0*	12.5	27*	S (℧)	V_{DS} = 15V, I_D = 24A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	500*	1000	1500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	150*	350	500*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong$ 24V, I_D = 24A, Z_o = 4.7Ω (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100*	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	
t_f	Fall Time	ALL	–	–	100*	ns	

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	2N6763	–	–	31*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6764	–	–	38*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6763	–	–	60	A	
		2N6764	–	–	70		
V_{SD}	Diode Forward Voltage ①	2N6763	0.90*	–	1.8*	V	T_C = 25°C, I_S = 31A, V_{GS} = 0
		2N6764	0.95*	–	1.9*	V	T_C = 25°C, I_S = 38A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

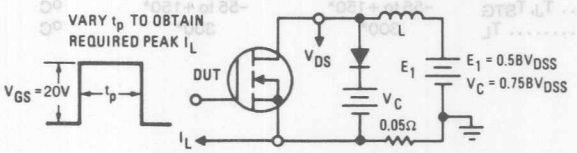


Fig. 1 - Clamped inductive test circuit.

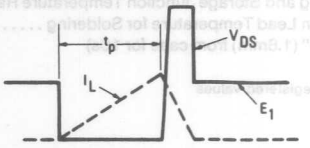


Fig. 2 - Clamped inductive waveforms.

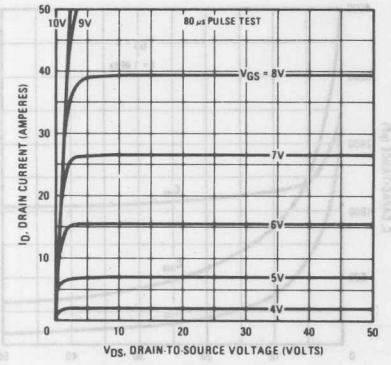


Fig. 3 - Typical output characteristics.

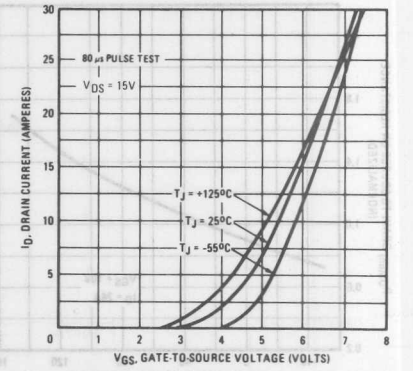


Fig. 4 - Typical transfer characteristics.

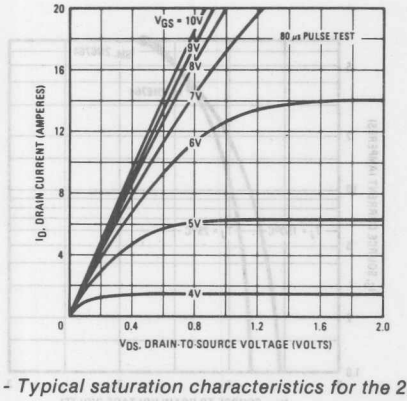


Fig. 5 - Typical saturation characteristics for the 2N6763.

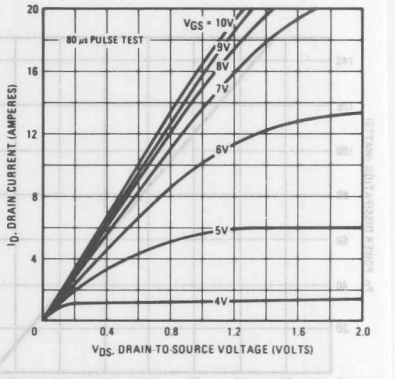


Fig. 6 - Typical saturation characteristics for the 2N6764.

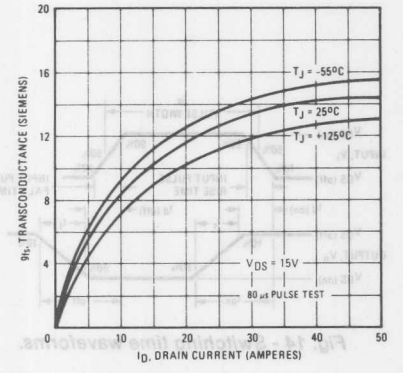


Fig. 7 - Typical transconductance vs. drain current.

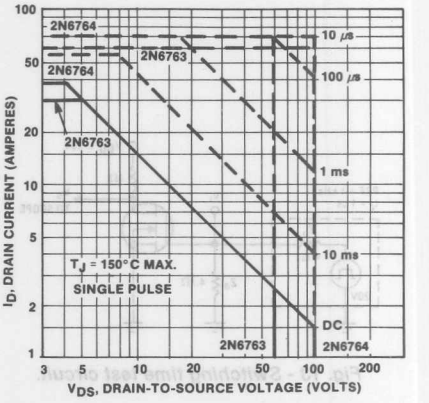


Fig. 8 - Maximum safe operating areas.

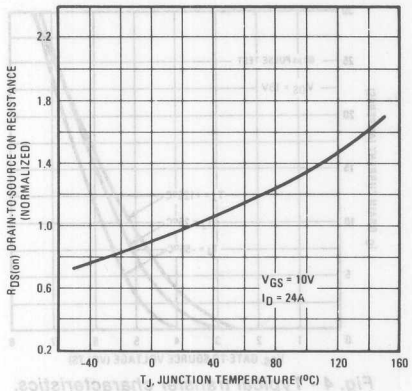


Fig. 9 - Typical normalized on-resistance vs. temperature.

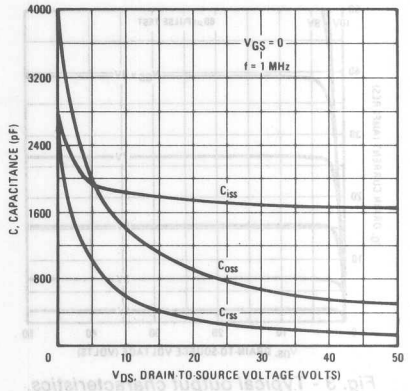


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

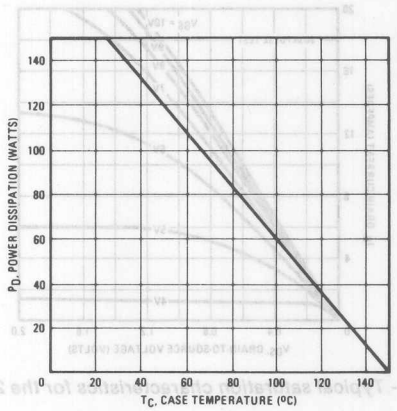


Fig. 11 - Power vs. temperature derating curve.

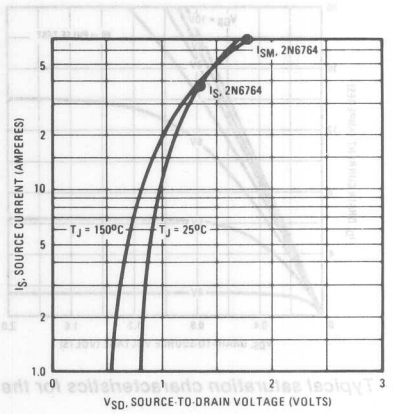


Fig. 12 - Typical body-drain diode forward voltage.

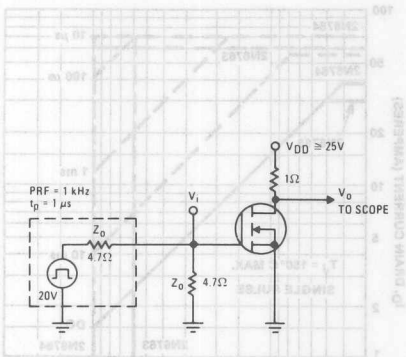


Fig. 13 - Switching time test circuit.

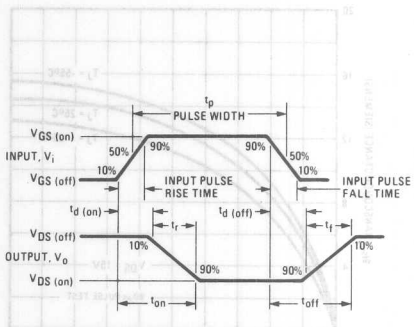


Fig. 14 - Switching time waveforms.

HARRIS

2N6765
2N6766

N-Channel Enhancement-Mode Power Field-Effect Transistors

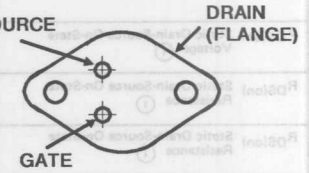
August 1991

Features

- 25A and 30A, 150V - 200V
- $r_{DS(on)}$ = 0.085Ω and 0.12Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AE
BOTTOM VIEW



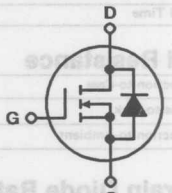
Description

The 2N6765 and 2N6766 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AE steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	2N6765	2N6766	UNITS
Drain-Source Voltage ..... V_{DS}	150*	200*	V
Drain-Gate Voltage (R_{GS} = 20kΩ) ..... V_{DGR}	150*	200*	V
Continuous Drain Current			
T_C = +25°C ..... I_D	25*	30*	A
T_C = +100°C ..... I_D	16*	19*	A
Pulsed Drain Current ..... I_{DM}	50	60	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = +25°C (See Figure 11) ..... P_D	150*	150*	W
T_C = +100°C (See Figure 11) ..... P_D	60*	60*	W
Linear Derating Factor (See Figure 11)	1.2*	1.2*	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figures 1 and 2, L = 100μH)	50	60	A
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1591.1

Electrical Characteristics @ T_C = 25° C (Unless Otherside Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6765	150	–	–	V	V_{GS} = 0
		2N6766	200	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6765	–	–	3.0*	V	V_{GS} = 10V, I_D = 25A
		2N6766	–	–	2.7*	V	V_{GS} = 10V, I_D = 30A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6765	–	0.09	0.12*	Ω	V_{GS} = 10V, I_D = 16A
		2N6766	–	0.07	0.085*	Ω	V_{GS} = 10V, I_D = 19A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6765	–	–	0.216*	Ω	V_{GS} = 10V, I_D = 16A, T_C = 125°C
		2N6766	–	–	0.153*	Ω	V_{GS} = 10V, I_D = 19A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	9.0*	15.5	27*	S (℧)	V_{DS} = 15V, I_D = 19A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	450*	800	1200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	150*	300	500*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong 95V$, I_D = 19A, Z_o = 4.7Ω (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100*	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	
t_f	Fall Time	ALL	–	–	100*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Typical socket mount

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6765	–	–	25*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6766	–	–	30*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6765	–	–	50	A	
		2N6766	–	–	60		
V_{SD}	Diode Forward Voltage ①	2N6765	0.85*	–	1.7*	V	T_C = 25°C, I_S = 25A, V_{GS} = 0
		2N6766	0.9*	–	1.8*	V	T_C = 25°C, I_S = 30A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

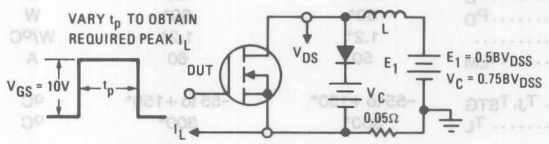


Fig. 1 – Clamped Inductive Test Circuit



Fig. 2 – Clamped Inductive Waveforms

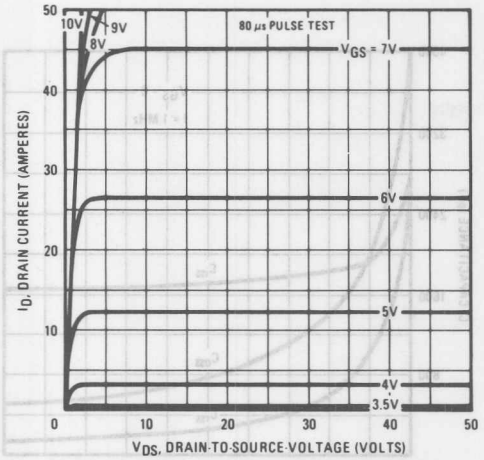


Fig. 3 — Typical Output Characteristics

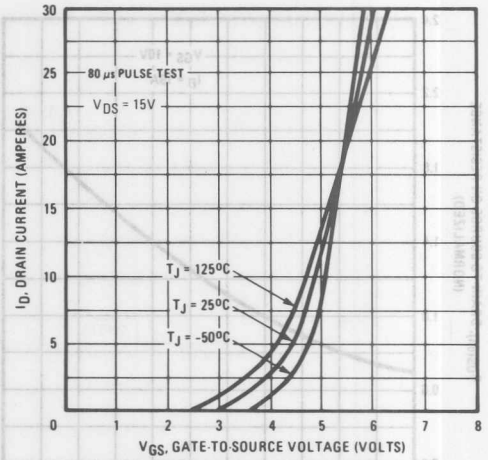


Fig. 4 — Typical Transfer Characteristics

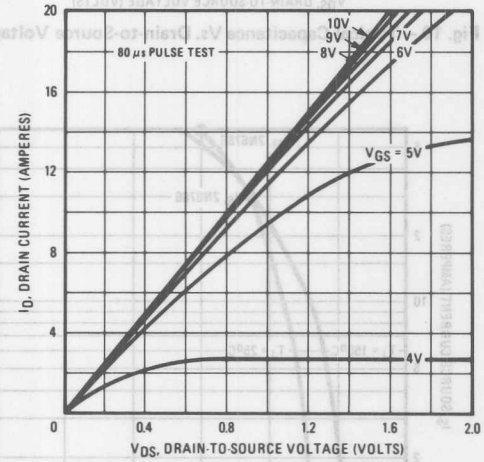


Fig. 5— Typical Saturation Characteristics (2N6765)

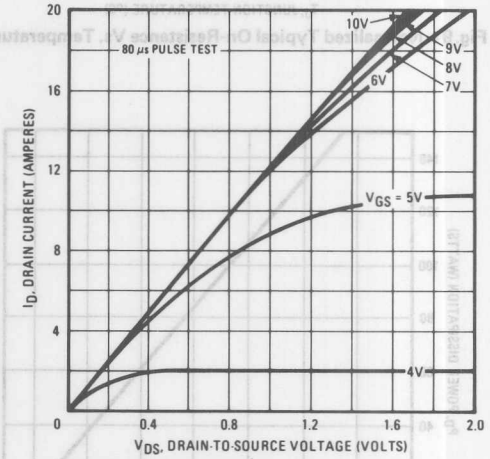


Fig. 6— Typical Saturation Characteristics (2N6766)

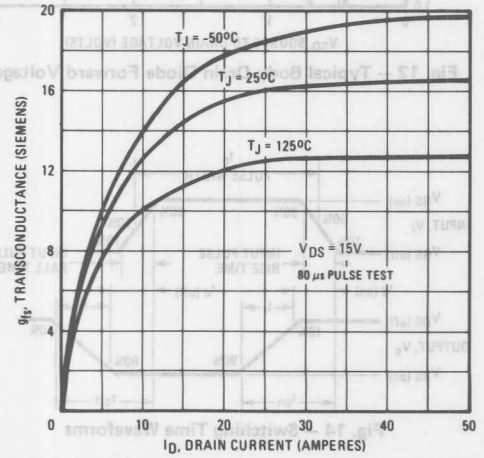


Fig. 7 — Typical Transconductance Vs. Drain Current

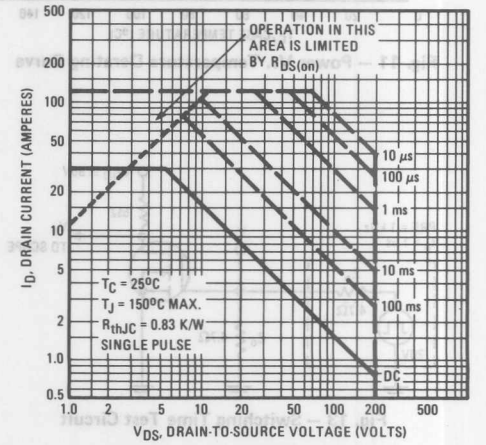


Fig. 8 — Maximum Safe Operating Area

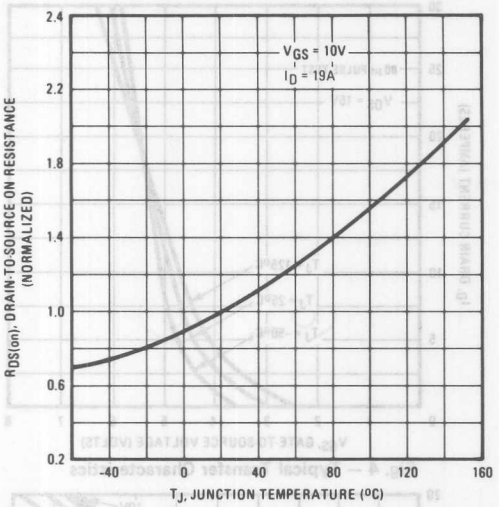


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

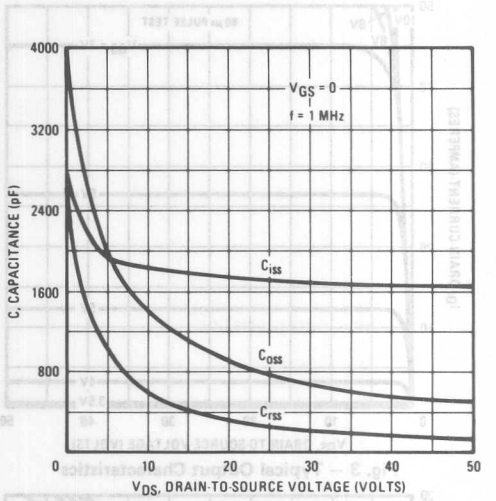


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

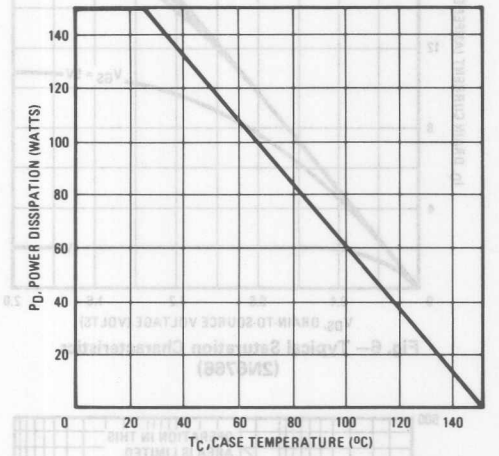


Fig. 11 — Power Vs. Temperature Derating Curve

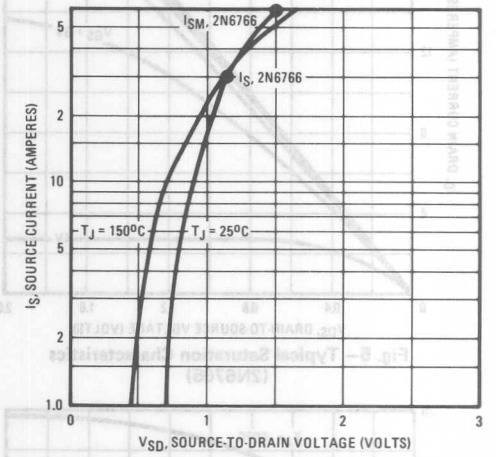


Fig. 12 — Typical Body-Drain Diode Forward Voltage

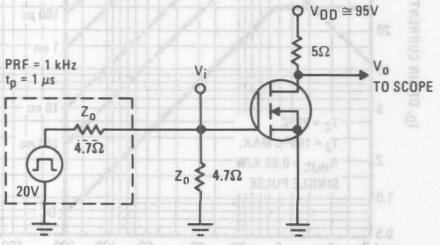


Fig. 13 — Switching Time Test Circuit

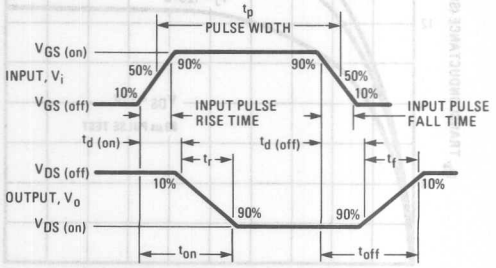


Fig. 14 — Switching Time Waveforms

HARRIS

2N6767
2N6768

N-Channel Enhancement-Mode Power MOS Field-Effect Transistors

August 1991

Features

- 12A and 14A, 350V - 400V
- $r_{DS(on)}$ = 0.4Ω and 0.3Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

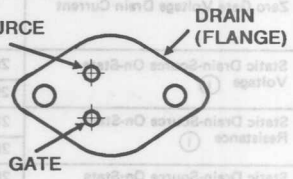
Description

The 2N6767 and 2N6768 are n-channel enhancement-mode silicon-gate power MOS field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

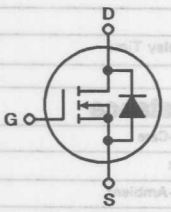
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6767	2N6768	UNITS
Drain-Source Voltage	V_{DS}	350*	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	350*	400*	V
Continuous Drain Current				
T_C = +25°C	I_D	12*	14*	A
T_C = +100°C	I_D	7.75*	9*	A
Pulsed Drain Current	I_{DM}	20	25	A
Gate-Source Voltage	V_{GS}	±20*	±20*	V
Maximum Power Dissipation				
T_C = +25°C (See Figure 11)	P_D	150*	150*	W
Above T_C = +25°C, Derate Linearly		1.2*	1.2*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	20	25	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1898.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6767	350	–	–	V	V_{GS} = 0
		2N6768	400	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6767	–	–	5.4*	V	V_{GS} = 10V, I_D = 12A
		2N6768	–	–	5.6*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6767	–	0.3	0.4*	Ω	V_{GS} = 10V, I_D = 7.75A
		2N6768	–	0.25	0.3*	Ω	V_{GS} = 10V, I_D = 9.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6767	–	–	0.88*	Ω	V_{GS} = 10V, I_D = 7.75A, T_C = 125°C
		2N6768	–	–	0.66*	Ω	V_{GS} = 10V, I_D = 9.0A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	8.0*	11.0	24*	S (℧)	V_{DS} = 15V, I_D = 9.0A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	200*	400	600*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong$ 180V, I_D = 9.0A, Z_o = 4.7Ω (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	65*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	150*	ns	
t_f	Fall Time	ALL	–	–	75*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6767	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6768	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6767	–	–	20	A	
		2N6768	–	–	25		
V_{SD}	Diode Forward Voltage ①	2N6767	0.8*	–	1.6*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6768	0.85*	–	1.7*	V	T_C = 25°C, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	1000	–	ns	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	25	–	μC	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

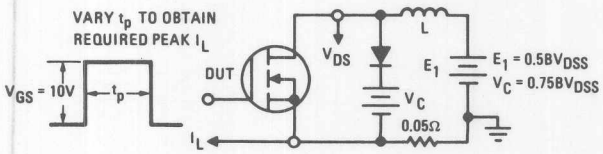


Fig. 1 - Clamped inductive test circuit.

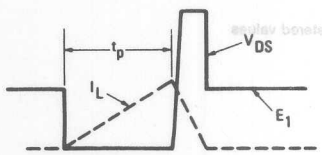


Fig. 2 - Clamped inductive waveforms.

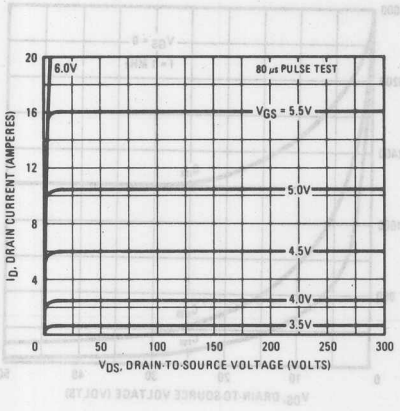


Fig. 3 - Typical output characteristics for both types.

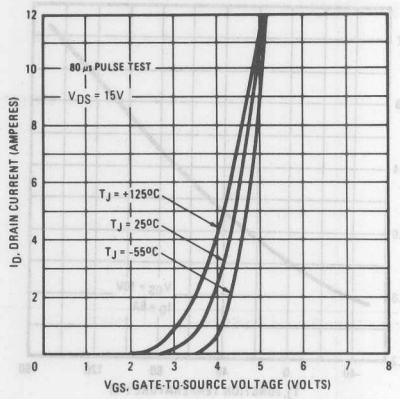


Fig. 4 - Typical transfer characteristics for both types.

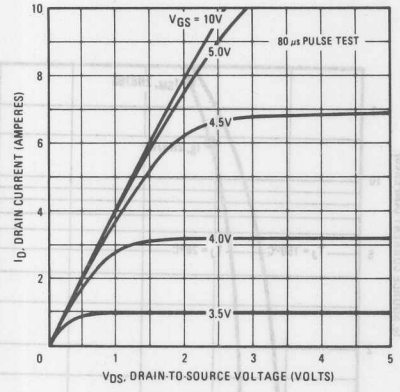


Fig. 5 - Typical saturation characteristics for the 2N6767.

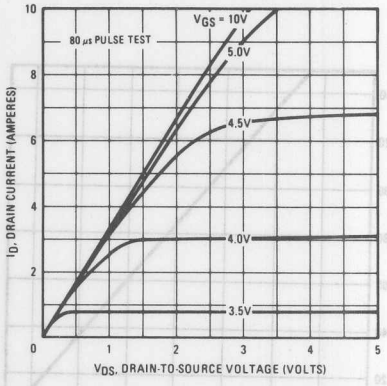


Fig. 6. - Typical saturation characteristics for the 2N6768.

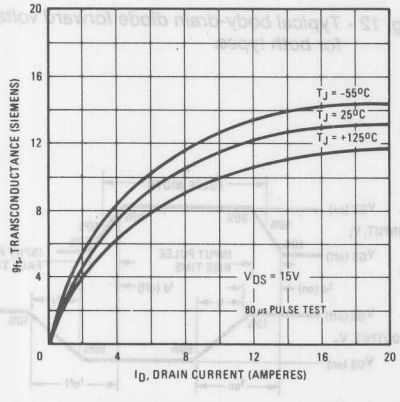


Fig. 7 - Typical transconductance versus drain current for both types.

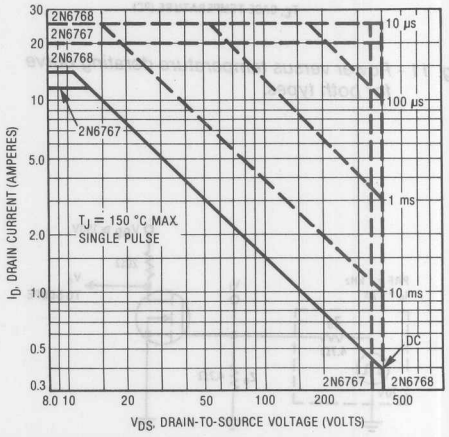


Fig. 8 - Maximum safe operating area for both types.

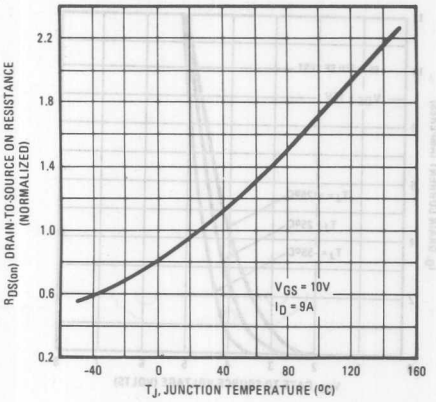


Fig. 9 - Typical normalized on-resistance versus temperature for both types.

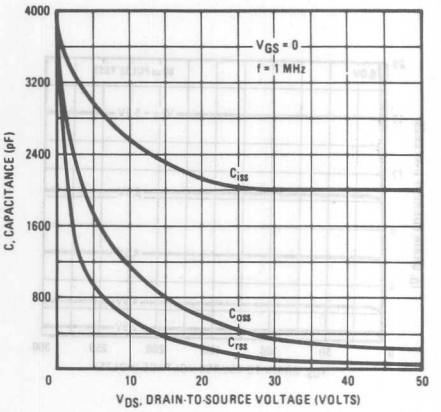


Fig. 10 - Typical capacitance versus drain-to-source voltage for both types.

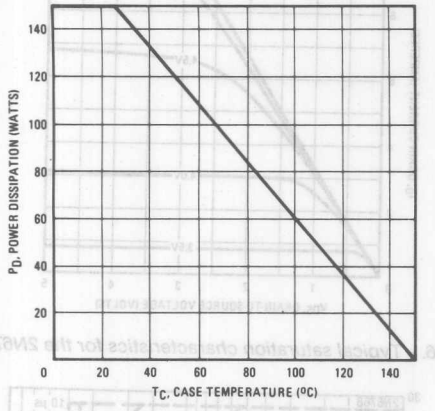


Fig. 11 - Power versus temperature derating curve for both types.

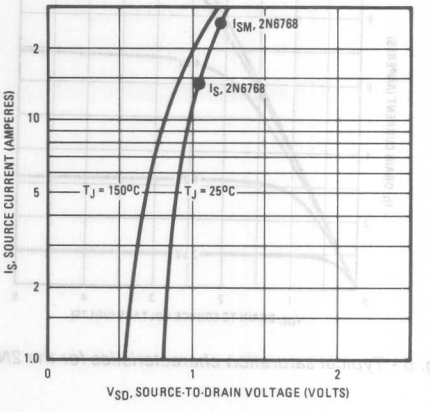


Fig. 12 - Typical body-drain diode forward voltage for both types.

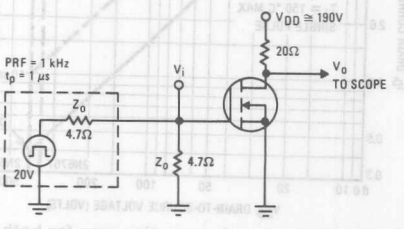


Fig. 13 - Switching time test circuit.

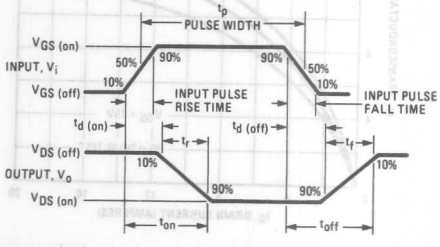


Fig. 14 - Switching time waveforms

2N6769
2N6770

N-Channel Enhancement-Mode Power MOS Field-Effect Transistors

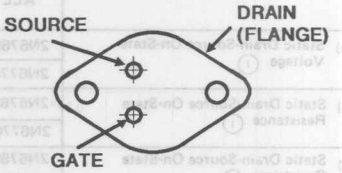
August 1991

Features

- 11A and 12A, 450V - 500V
- $r_{DS(on)}$ = 0.5Ω and 0.4Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AA
BOTTOM VIEW



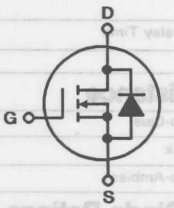
Description

The 2N6769 and 2N6770 are n-channel enhancement-mode silicon-gate power MOS field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		2N6769	2N6770	UNITS
Drain-Source Voltage	V_{DS}	450*	500*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	450*	500*	V
Continuous Drain Current				
T_C = +25°C	I_D	11	12	A
T_C = +100°C	I_D	7	7.75	A
Pulsed Drain Current	I_{DM}	20	25	A
Gate-Source Voltage	V_{GS}	±20*	±20*	V
Maximum Power Dissipation				
T_C = +25°C (See Figure 11)	P_D	150*	150*	W
Above T_C = +25°C, Derate Linearly (See Figure 11)		1.2*	1.2*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	20	25	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6769	450	–	–	V	V_{GS} = 0
		2N6770	500	–	–	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 25°C to 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6769	–	–	6.0*	V	V_{GS} = 10V, I_D = 11A
		2N6770	–	–	6.0*	V	V_{GS} = 10V, I_D = 12A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6769	–	0.4	0.5*	Ω	V_{GS} = 10V, I_D = 7A
		2N6770	–	0.3	0.4*	Ω	V_{GS} = 10V, I_D = 7.75A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6769	–	–	1.1*	Ω	V_{GS} = 10V, I_D = 7.0A, T_C = 125°C
		2N6770	–	–	0.88*	Ω	V_{GS} = 10V, I_D = 7.75A, T_C = 125°C
g_{fs}	Forward Transconductance (1)	ALL	8.0*	12.0	24*	S (℧)	V_{GS} = 10V I_D = 7.75A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	200*	400	600*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong$ 210V, I_D = 7.75A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	50*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	150*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	70*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6769	–	–	11*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6770	–	–	12*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6769	–	–	20	A	
		2N6770	–	–	25		
V_{SD}	Diode Forward Voltage (1)	2N6769	0.75*	–	1.5*	V	T_C = 25°C, I_S = 11A, V_{GS} = 0
		2N6770	0.80*	–	1.6*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	1300	–	ns	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.4	–	μC	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

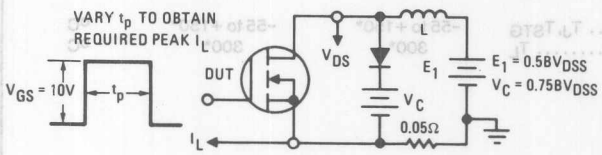


Fig. 1 - Clamped inductive test circuit.

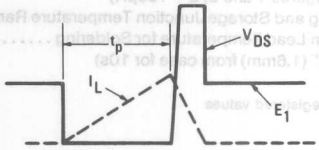


Fig. 2 - Clamped inductive waveforms.

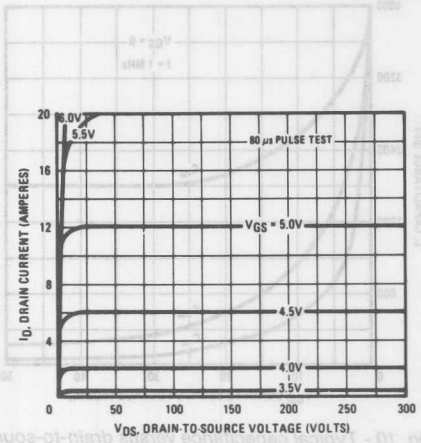


Fig. 3 - Typical output characteristics for both types.

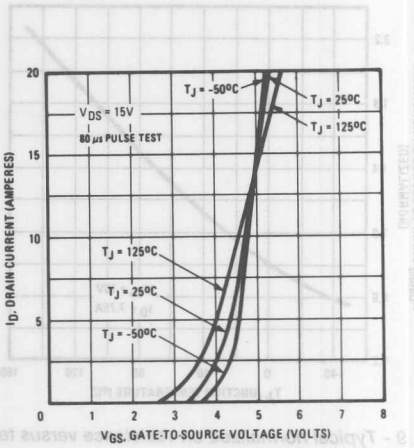


Fig. 4 - Typical transfer characteristics for both types.

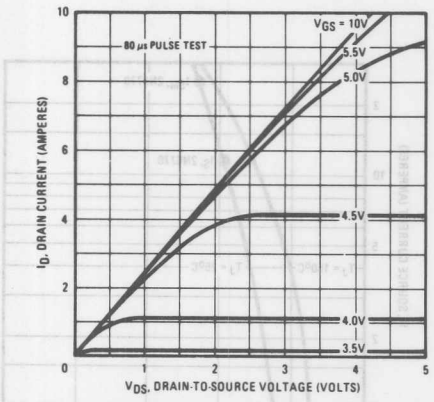


Fig. 5 - Typical saturation characteristics for the 2N6769.

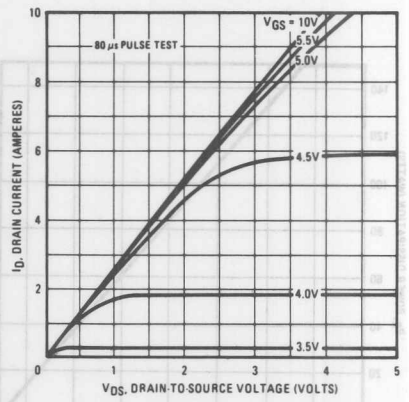


Fig. 6. - Typical saturation characteristics for the 2N6770.

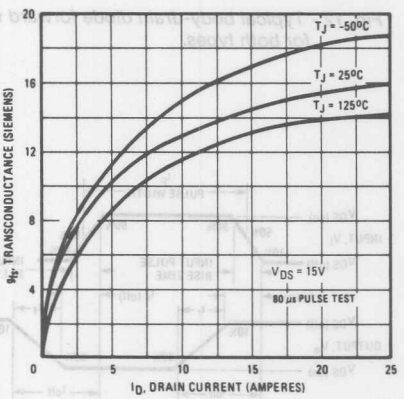


Fig. 7 - Typical transconductance versus drain current for both types.

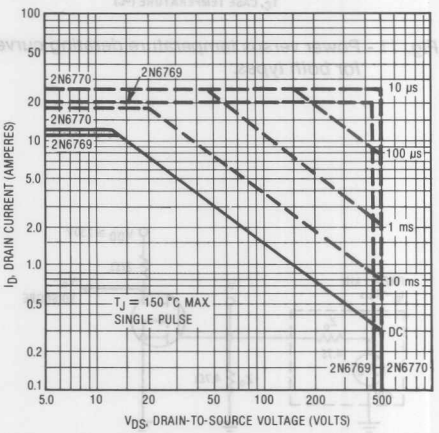


Fig. 8 - Maximum safe operating area for both types.

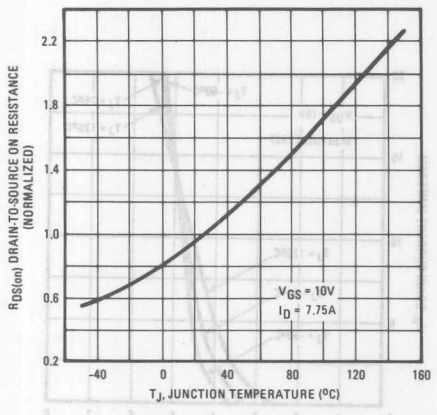


Fig. 9 - Typical normalized on-resistance versus temperature for both types.

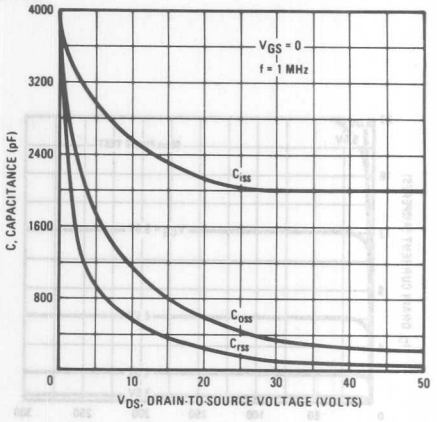


Fig. 10 - Typical capacitance versus drain-to-source voltage for both types.

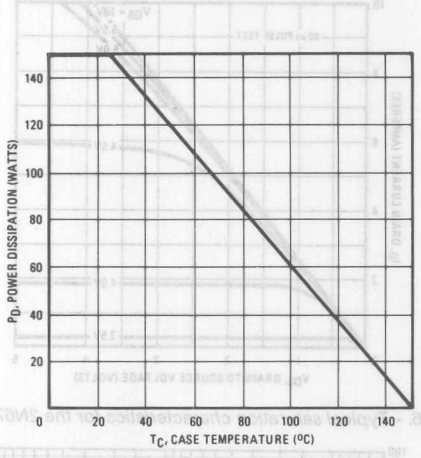


Fig. 11 - Power versus temperature derating curve for both types.

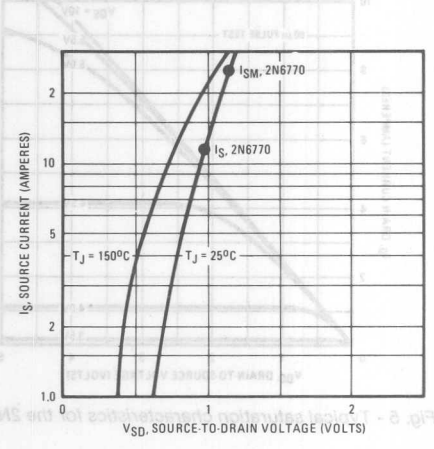


Fig. 12 - Typical body-drain diode forward voltage for both types.

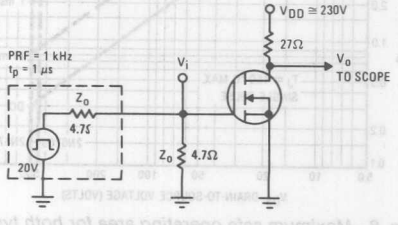


Fig. 13 - Switching time test circuit.

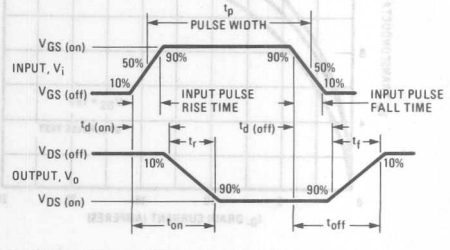


Fig. 14 - Switching time waveforms

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2N6782

N-Channel Enhancement-Mode Power Field-Effect Transistor

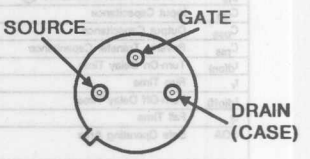
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Features

- 3.5A, 100V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-205AF
BOTTOM VIEW



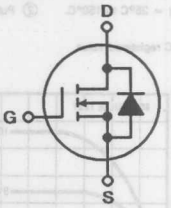
Description

The 2N6782 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6782 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		2N6782	UNITS
Drain-Source Voltage (Note 1)	V_{DS}	100*	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100*	V
Continuous Drain Current			
T_C = +25°C	I_D	3.5*	A
T_C = +100°C	I_D	2.25*	A
Pulsed Drain Current (Note 2)	I_{DM}	14*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current (Body Diode)	I_S	3.50*	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}	14*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	15*	W
Linear Derating Factor (See Figure 14)		0.12*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	14	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

NOTES:

1. T_J = +25°C to +150°C
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	–	–	2.1*	V	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	–	0.5	0.6*	Ω	V_{GS} = 10V, I_D = 2.25A, T_C = 25°C
		–	–	1.08*	Ω	V_{GS} = 10V, I_D = 2.25A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.75*	–	1.5*	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	1.0*	1.5	3.0*	S(℧)	V_{DS} = 5V, I_D = 2.25A
C_{iss}	Input Capacitance	60*	135	200*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	40*	80	100*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	10*	20	25*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	15*	ns	V_{DD} ≅ 34V, I_D = 2.25A, Z_o = 50Ω
t_r	Rise Time	–	–	25*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	25*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	–	–	20*	ns	
SOA	Safe Operating Area	15	–	–	W	V_{DS} = 80V, I_D = 188 mA, See Fig. 16.
		15	–	–	W	V_{DS} = 4.28V, I_D = 3.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	8.33*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	200	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.0	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

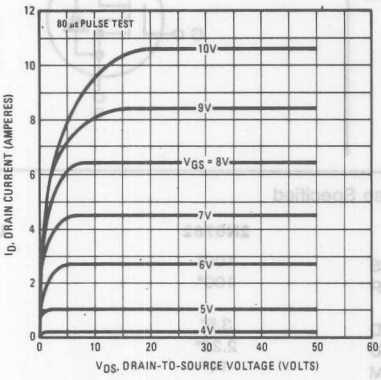


Fig. 1 – Typical Output Characteristics

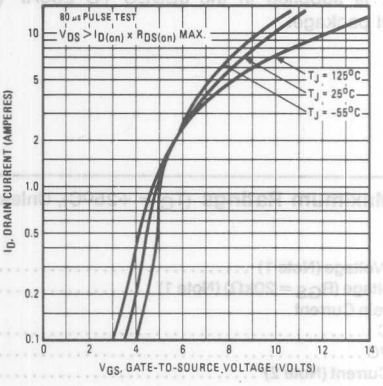


Fig. 2 – Typical Transfer Characteristics

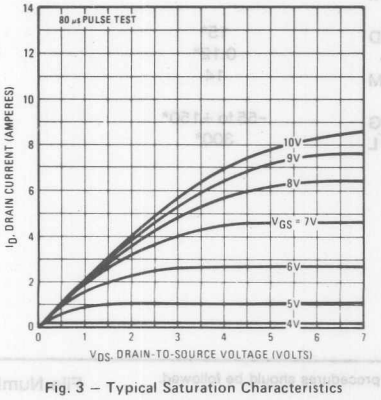


Fig. 3 – Typical Saturation Characteristics

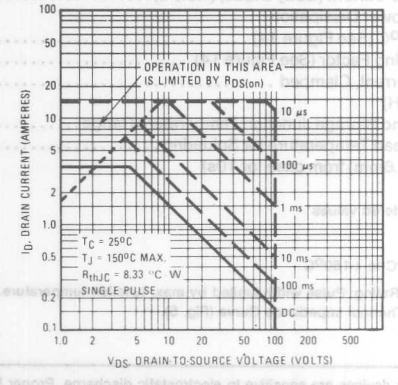


Fig. 4 – Maximum Safe Operating Area

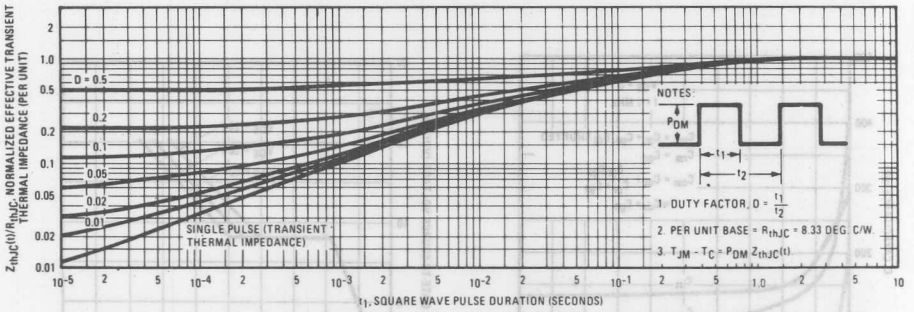


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

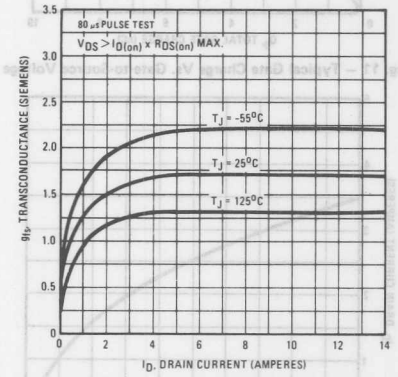


Fig. 6 – Typical Transconductance Vs. Drain Current

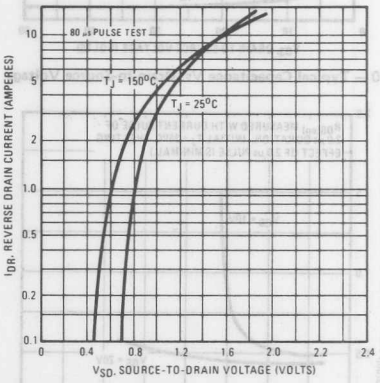


Fig. 7 – Typical Source-Drain Diode Forward Voltage

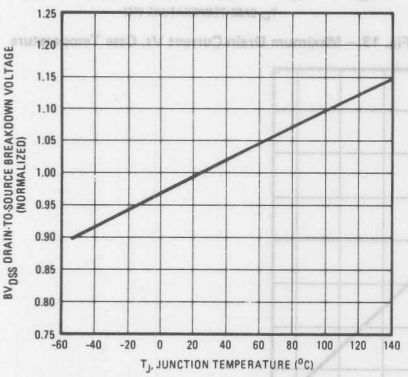


Fig. 8 – Breakdown Voltage Vs. Temperature

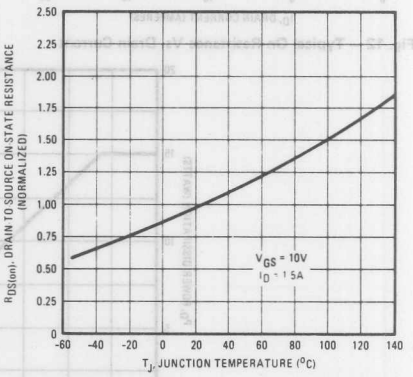


Fig. 9 – Normalized On-Resistance Vs. Temperature

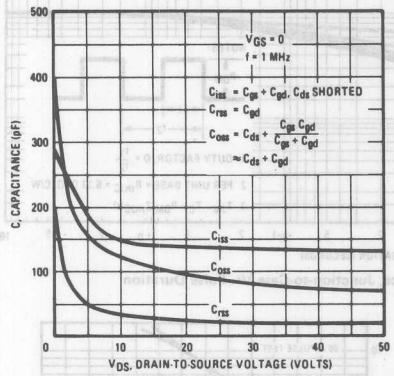


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

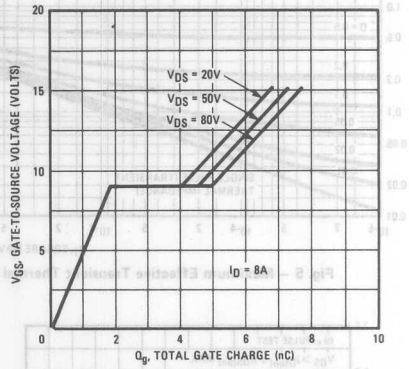


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

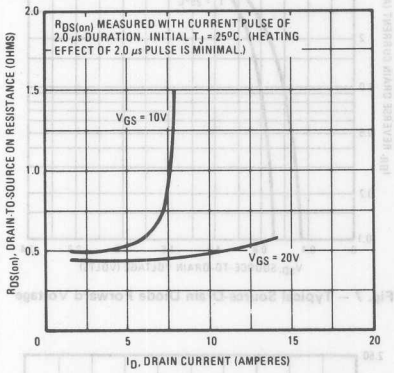


Fig. 12 — Typical On-Resistance Vs. Drain Current

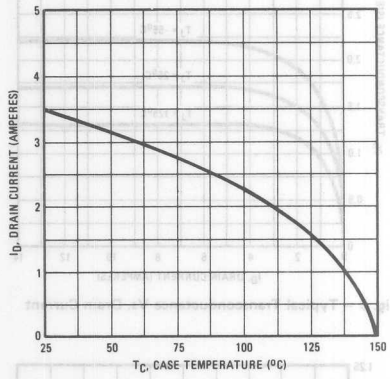


Fig. 13 — Maximum Drain Current Vs. Case Temperature

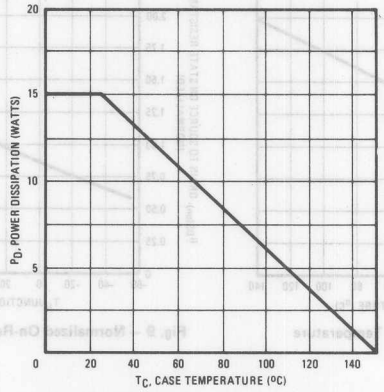
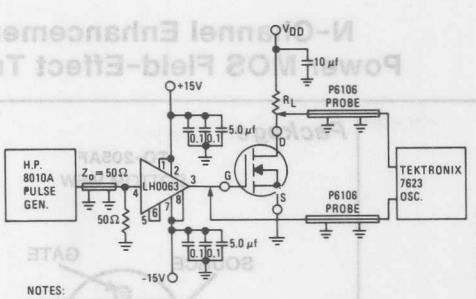
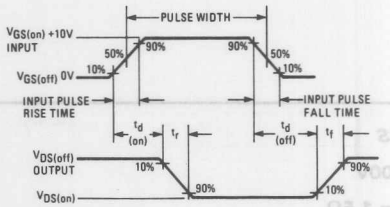


Fig. 14 — Power Vs. Temperature Derating Curve

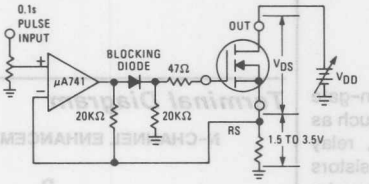


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 — Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D * R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 — Safe Operating Area Test Circuit

HARRIS

2N6784

August 1991

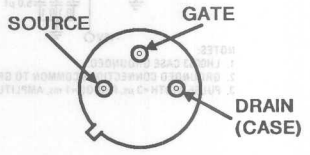
N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

Features

- 2.25A, 200V
- $r_{DS(on)} = 1.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-205AF
BOTTOM VIEW



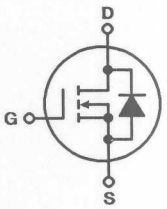
Description

The 2N6784 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6784 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6784	UNITS
Drain-Source Voltage	V_{DS}	200*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	200*	V
Continuous Drain Current			
T_C = +25°C	I_D	2.25*	A
T_C = +100°C	I_D	1.5*	A
Pulsed Drain Current (Note 2)	I_{DM}	9*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current (Body Diode)	I_S	2.25*	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}	9*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	15*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.12*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	9	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1906.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	200*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 200V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 160V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	3.37*	V	V_{GS} = 10V, I_D = 2.25A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	1.0	1.5*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 25°C
		–	–	2.81*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.7*	–	1.5*	V	T_C = 25°C, I_S = 2.25A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	0.9*	1.3	2.7*	S(℧)	V_{DS} = 5V, I_D = 1.5A
C_{iss}	Input Capacitance	60*	135	200*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	20*	60	80*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	5.0*	16	25*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	15*	ns	$V_{DD} \cong$ 75V, I_D = 1.5A, Z_o = 50Ω
t_r	Rise Time	–	–	20*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	30*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	20*	ns	of operating temperature.)
SOA	Safe Operating Area	15	–	–	W	V_{DS} = 160V, I_D = 94 mA, See Fig. 16.
		15	–	–	W	V_{DS} = 6.67V, I_D = 2.25A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	8.33*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	290	ns	T_J = 150°C, I_F = 2.25A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	2.0	μC	T_J = 150°C, I_F = 2.25A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

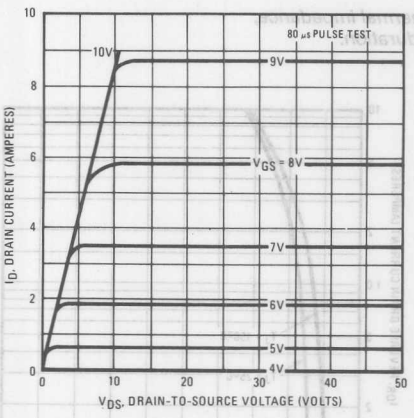


Fig. 1 - Typical output characteristics.

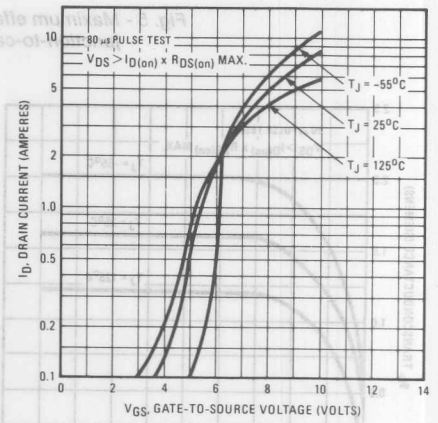


Fig. 2 - Typical transfer characteristics.

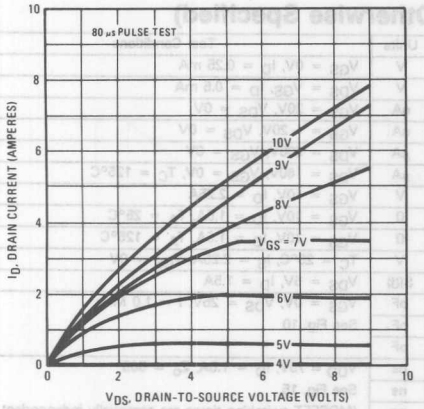


Fig. 3 - Typical saturation characteristics.

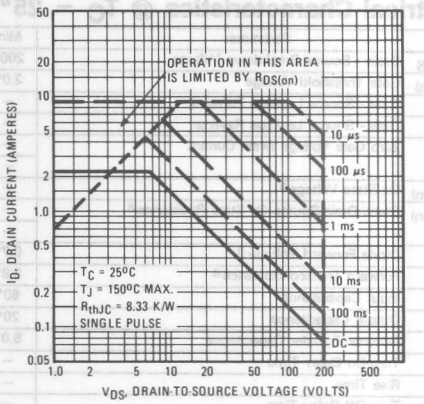


Fig. 4 - Maximum safe operating area.

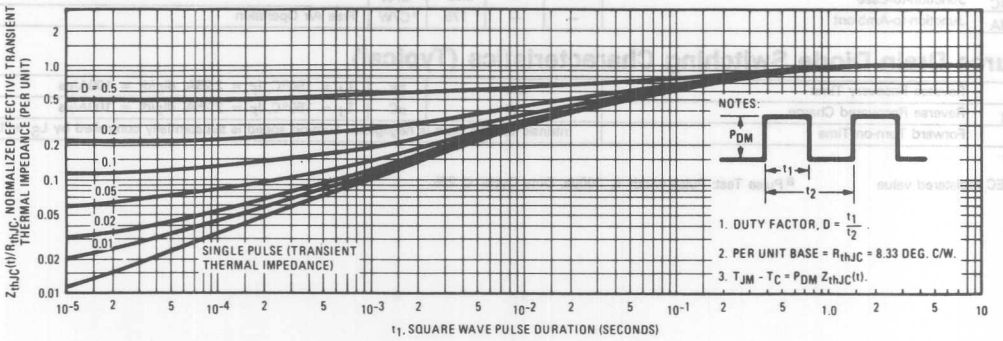


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

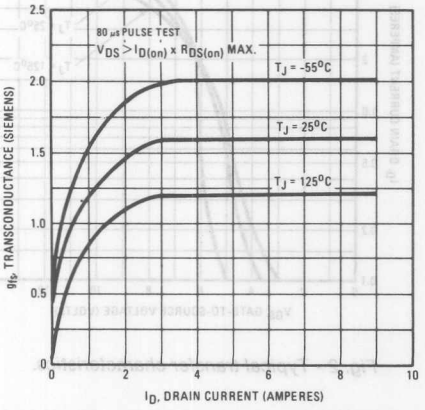


Fig. 6 - Typical transconductance versus drain current.

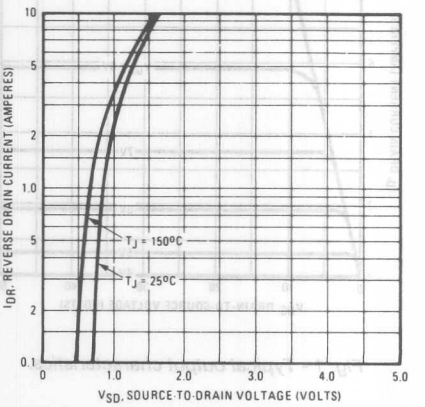


Fig. 7 - Typical source-drain diode forward voltage.

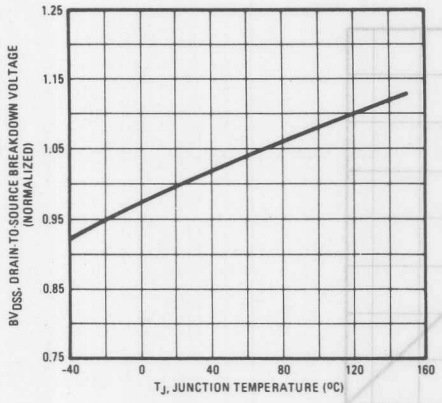


Fig. 8 - Breakdown voltage versus temperature.

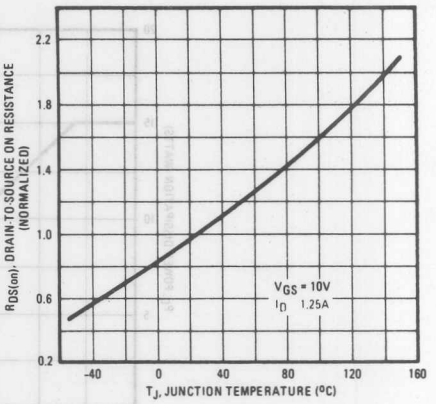


Fig. 9 - Typical normalized on-resistance versus temperature.

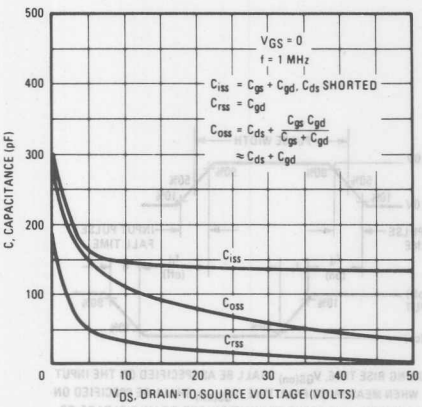


Fig. 10 - Typical capacitance versus drain-to-source voltage.

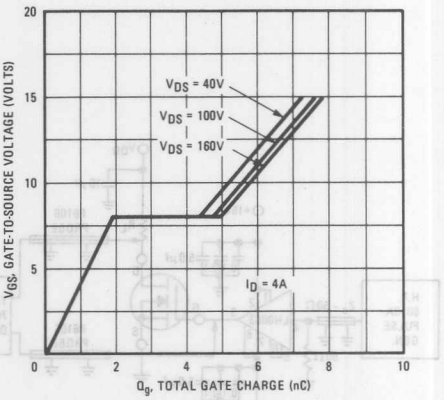


Fig. 11 - Typical gate charge versus gate-to-source voltage.

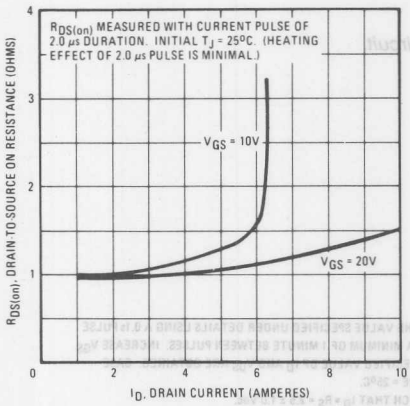


Fig. 12 - Typical on-resistance versus drain current.

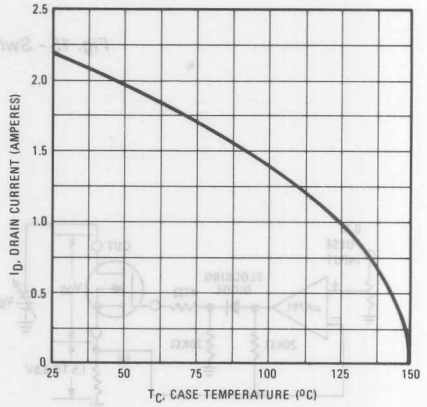


Fig. 13 - Maximum drain current versus case temperature.

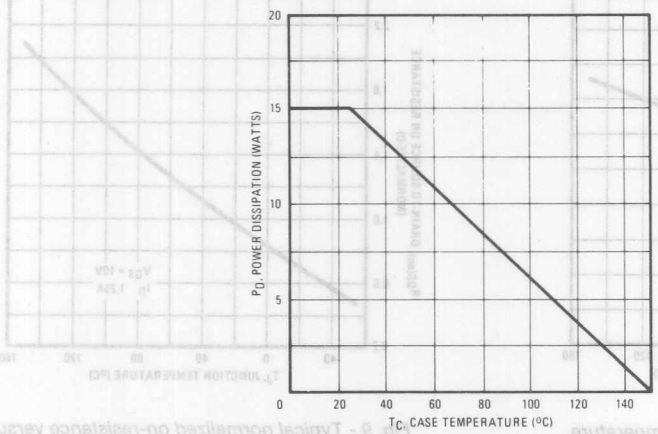
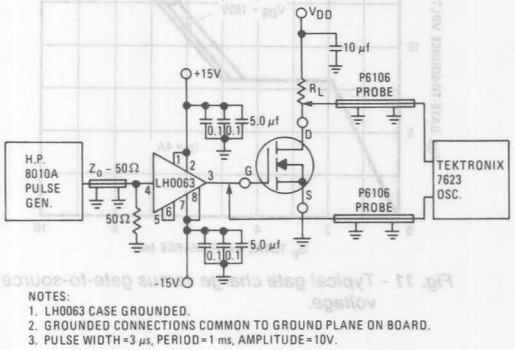
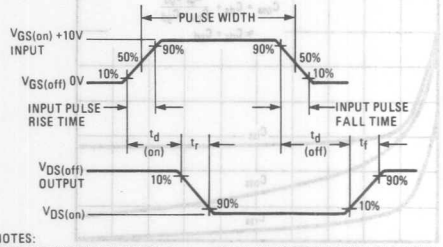


Fig. 14 - Power versus temperature derating curve.

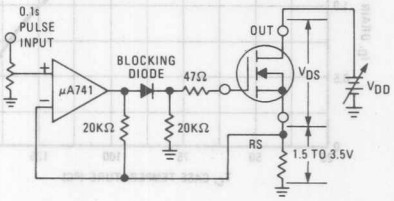


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

HARRIS

2N6786

August 1991

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

Features

- 1.25A, 400V
- $r_{DS(on)} = 3.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

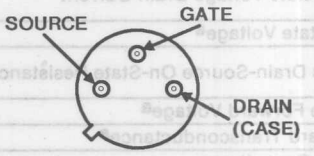
Description

The 2N6786 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6786 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

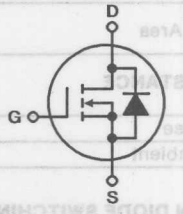
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6786	UNITS
Drain-Source Voltage	V_{DS}	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400*	V
Continuous Drain Current			
T_C = +25°C	I_D	1.25*	A
T_C = +100°C	I_D	0.8*	A
Pulsed Drain Current	I_{DM}	5.5*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	1.25*	A
Pulse Source Current	I_{SM}	5.5*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	15*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.12*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	5.5	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2207.1

ELECTRICAL CHARACTERISTICS at T_C = 25°C (Unless Otherwise Specified)

CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	400*	—	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.5 mA	2.0*	—	4.0*	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	—	100*	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	—	—	100*	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V	—	—	250*	μA
		V_{DS} = 320 V, V_{GS} = 0 V, T_C = 125°C	—	—	1000*	μA
On-State Voltage[a]	$V_{DS}(on)$	V_{GS} = 10 V, I_D = 1.25 A	—	—	4.5*	V
Static Drain-Source On-State Resistance[a]	$r_{DS}(on)$	V_{GS} = 10 V, I_D = 0.8 A, T_A = 25°C	—	3.3	3.6*	Ω
		V_{GS} = 10 V, I_D = 0.8 A, T_A = 125°C	—	—	7.92*	Ω
Diode Forward Voltage[a]	V_{SD}	T_C = 25°C, I_S = 1.25 A, V_{GS} = 0 V	0.6*	—	1.4*	V
Forward Transconductance[a]	g_{fs}	V_{DS} = 5 V, I_D = 0.8 A	0.7*	1.2	2.1*	S(℧)
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz See Fig. 10	60*	135	200*	pF
Output Capacitance	C_{oss}		15*	35	50*	pF
Reverse Transfer Capacitance	C_{rss}		2*	8	15*	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} ≅ 170 V, I_D = 0.8 A, Z_O = 50 Ω See Fig. 15. (MOSFET switching times are essentially independent of operating temperature.)	—	—	15*	ns
Rise Time	t_r		—	—	20*	ns
Turn-Of Delay Time	$t_d(off)$		—	—	35*	ns
Fall Time	t_f		—	—	30*	ns
Safe Operating Area	SOA	V_{DS} = 200 V, I_D = 75 mA, See Fig. 16.	15	—	—	W
		V_{DS} = 12 V, I_D = 1.25 A, See Fig. 16.	15	—	—	W

THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$		—	—	8.33*	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	—	—	175	°C/W

SOURCE-DRAIN DIODE SWITCHING CHARACTERISTICS (TYPICAL)

Reverse Recovery Time	t_{rr}	T_J=150°C, I_F=1.25 A, di_F/dt=100 A/μs	380	ns
Reverse Recovered Charge	Q_{RR}	T_J=150°C, I_F=1.25 A, di_F/dt=100 A/μs	2.7	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value.

[a]Pulse Test: Pulse width ≤ 300 μs, duty cycle ≤ 2%.

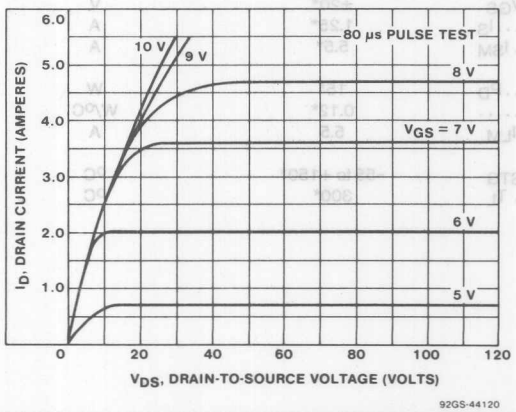


Fig. 1 - Typical output characteristics.

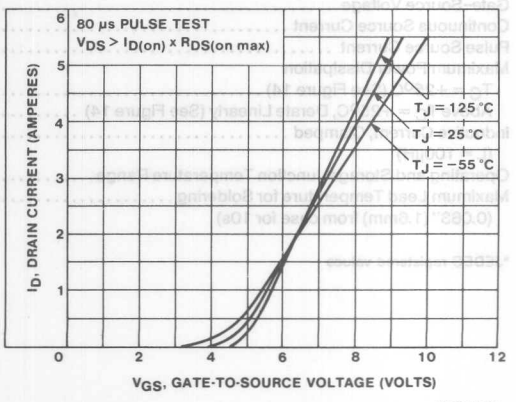


Fig. 2 - Typical transfer characteristics.

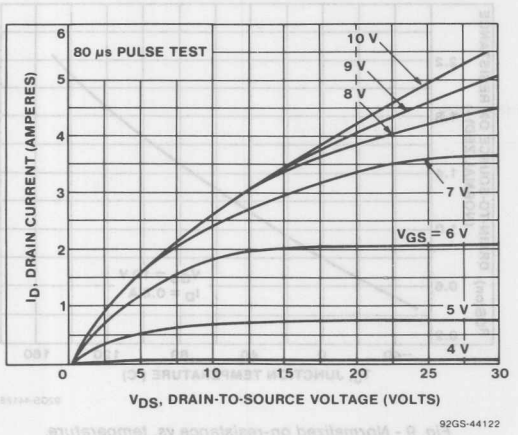


Fig. 3 - Typical saturation characteristics.

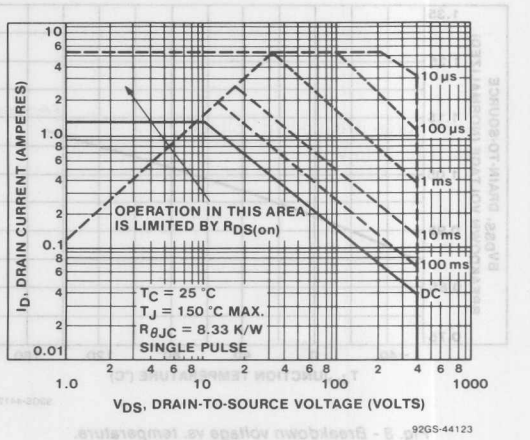


Fig. 4 - Maximum safe operating area.

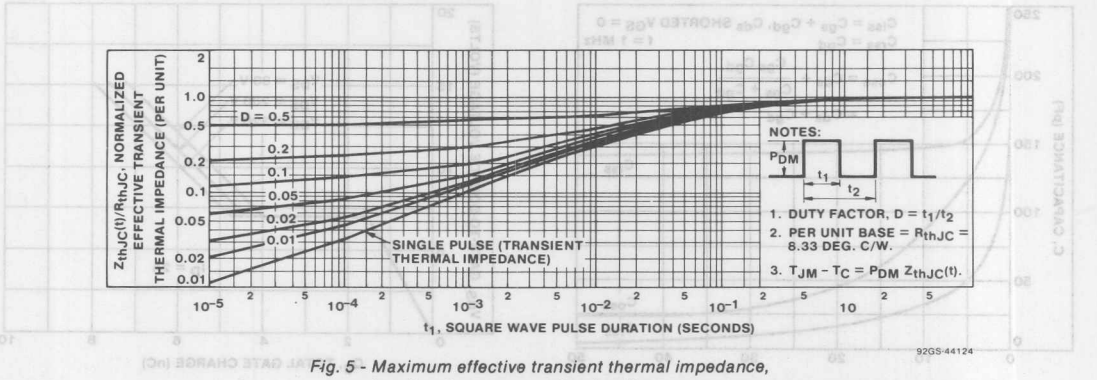


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

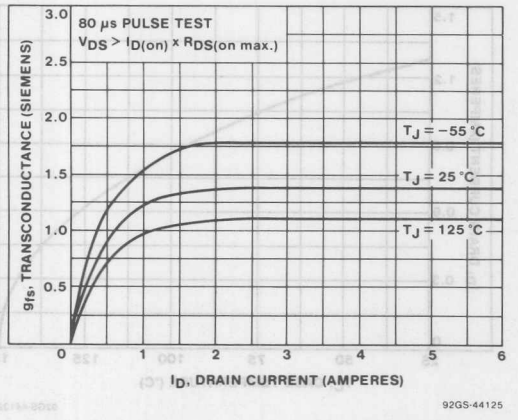


Fig. 6 - Typical transconductance vs. drain current.

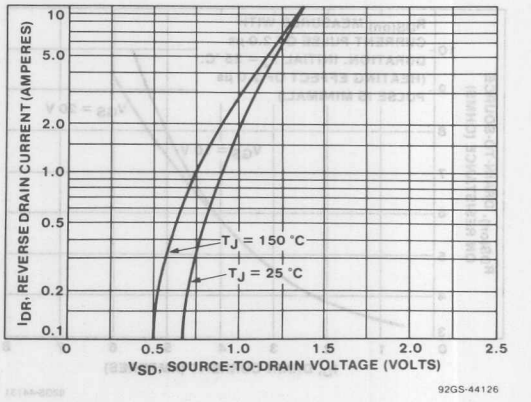


Fig. 7 - Typical source-drain diode forward voltage.

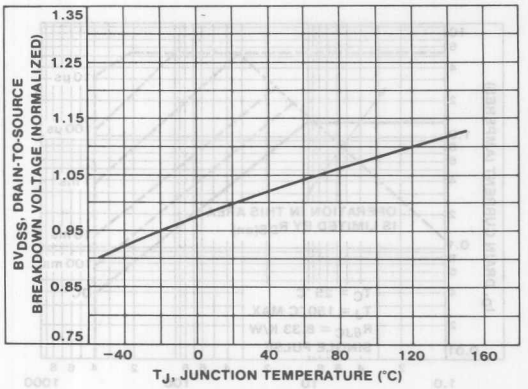


Fig. 8 - Breakdown voltage vs. temperature.

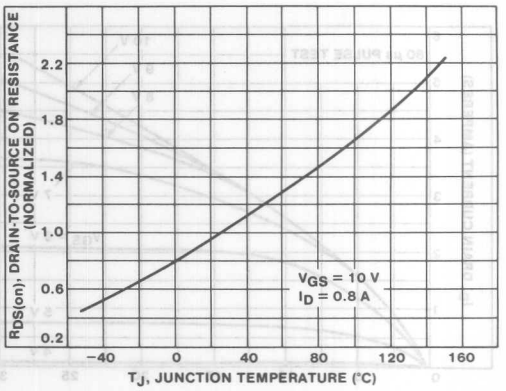


Fig. 9 - Normalized on-resistance vs. temperature.

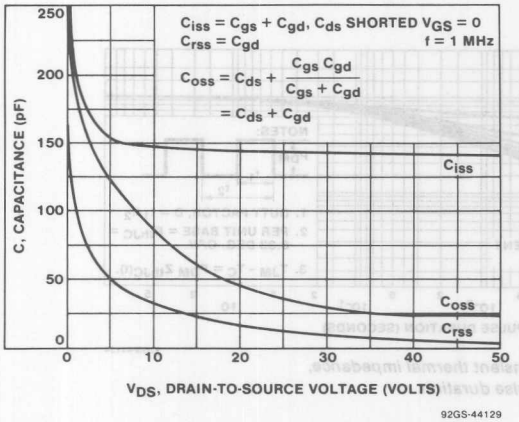


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

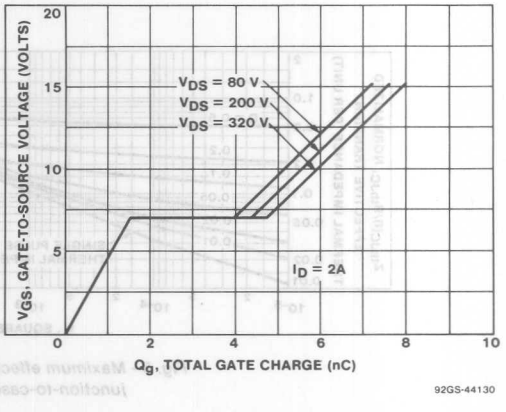


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

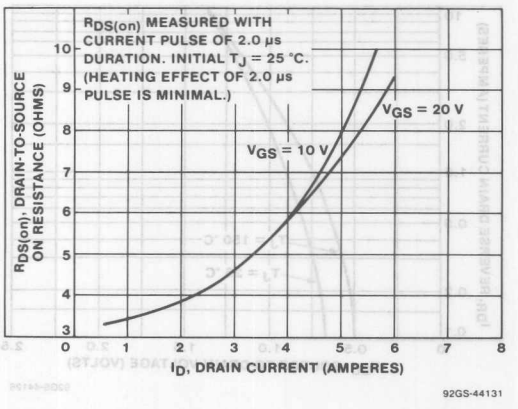


Fig. 12 - Typical on-resistance vs. drain current.

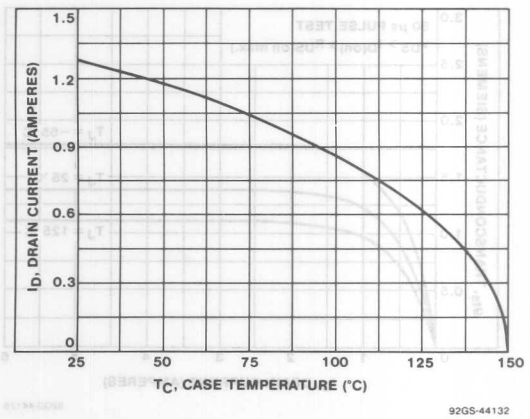


Fig. 13 - Maximum drain current vs. case temperature.

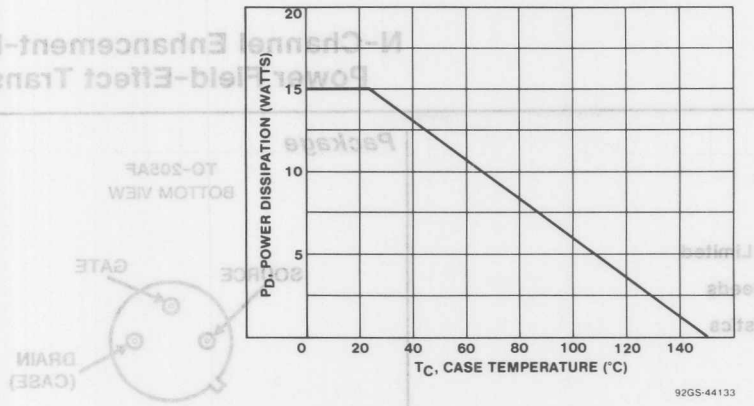


Fig. 14 - Power vs. temperature derating curve.

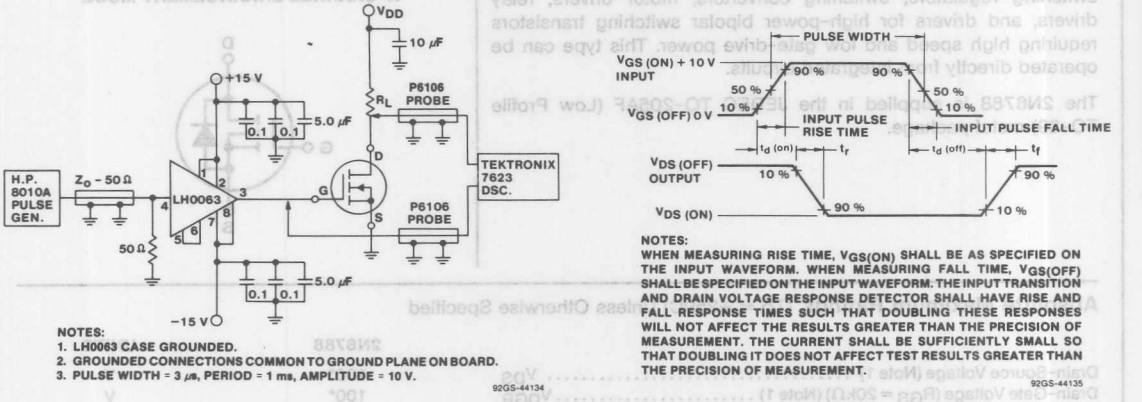


Fig. 15 - Switching time test circuit.

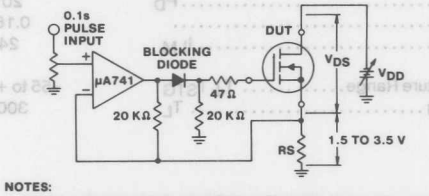


Fig. 16 - Safe operating test circuit.

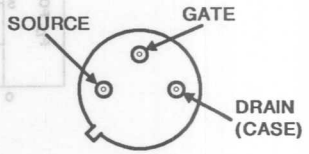
N-Channel Enhancement-Mode Power Field-Effect Transistor

Features

- 6.0A, 100V
- $r_{DS(on)} = 0.30\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-205AF
BOTTOM VIEW



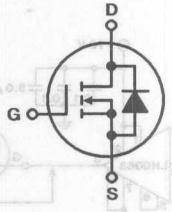
Description

The 2N6788 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6788 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6788	UNITS
Drain-Source Voltage (Note 1)	V_{DS}	100*	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100*	V
Continuous Drain Current			
T_C = +25°C	I_D	6.0*	A
T_C = +100°C	I_D	3.5*	A
Pulsed Drain Current (Note 2)	I_{DM}	24*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current (Body Diode)	I_S	6.0*	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}	24*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	20*	W
Linear Derating Factor (See Figure 14)		0.16*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	24	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

NOTES:

1. T_J = +25°C to +150°C
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1593.1**

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	–	–	2.10*	V	V_{GS} = 10V, I_D = 6.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	–	0.25	0.30*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 25°C
		–	–	0.54*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.8*	–	1.8*	V	T_C = 25°C, I_S = 6.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	1.5*	2.9	4.5*	S(℧)	V_{DS} = 5V, I_D = 3.5A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100*	200	400*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	20*	50	100*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	40*	ns	V_{DD} ≅ 35V, I_D = 3.5A, Z_o = 50Ω
t_r	Rise Time	–	–	70*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	40*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	70*	ns	of operating temperature.)
SOA	Safe Operating Area	20	–	–	W	V_{DS} = 80V, I_D = 250 mA, See Fig. 16.
		20	–	–	W	V_{DS} = 3.3V, I_D = 60A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	230	ns	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.2	μC	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

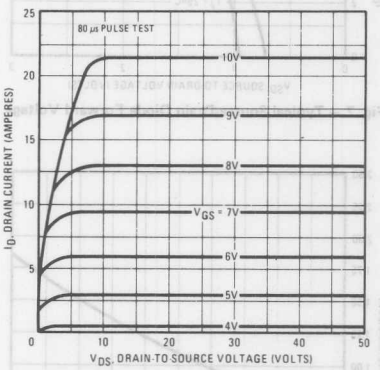


Fig. 1 – Typical Output Characteristics

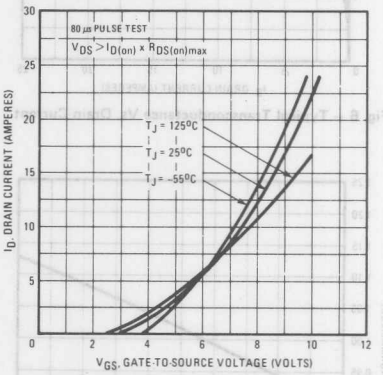


Fig. 2 – Typical Transfer Characteristics

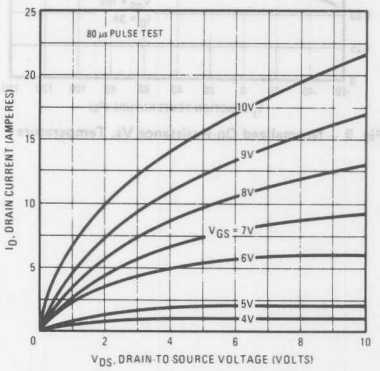


Fig. 3 – Typical Saturation Characteristics

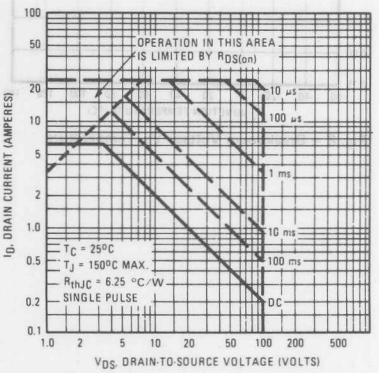


Fig. 4 – Maximum Safe Operating Area

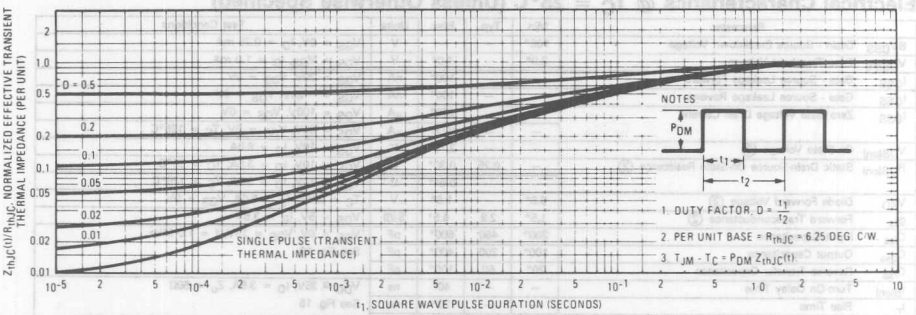


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

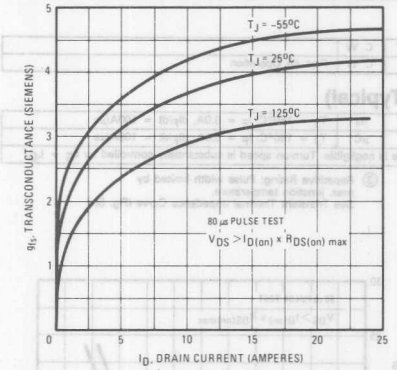


Fig. 6 – Typical Transconductance Vs. Drain Current

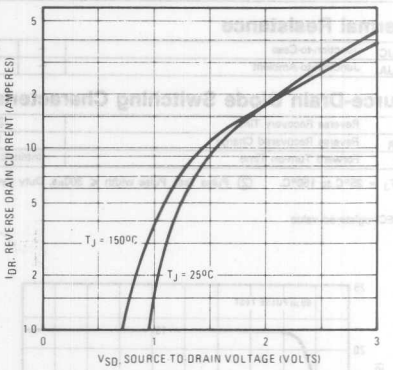


Fig. 7 – Typical Source-Drain Diode Forward Voltage

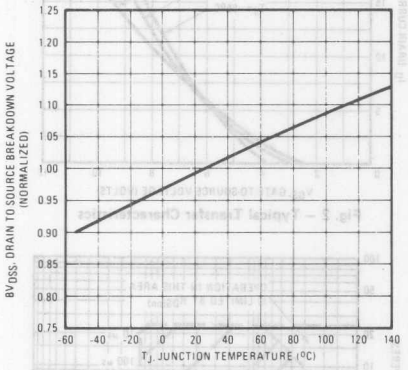


Fig. 8 – Breakdown Voltage Vs. Temperature

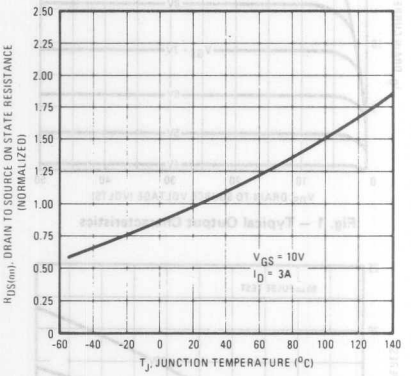


Fig. 9 – Normalized On-Resistance Vs. Temperature

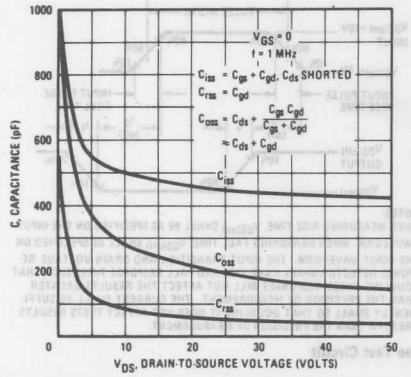


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

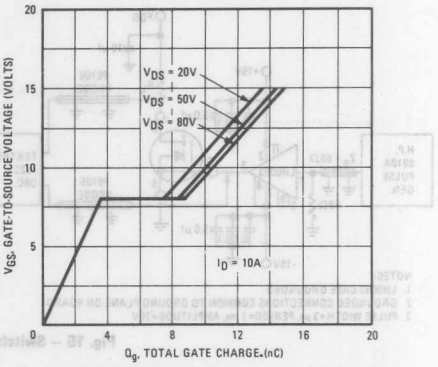


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

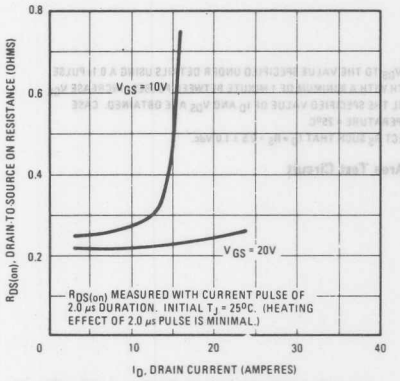


Fig. 12 – Typical On-Resistance Vs. Drain Current

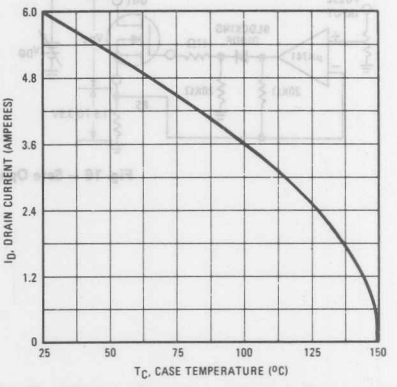


Fig. 13 – Maximum Drain Current Vs. Case Temperature

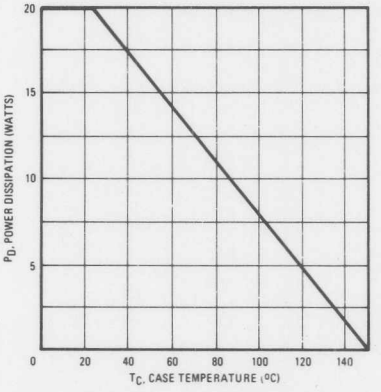
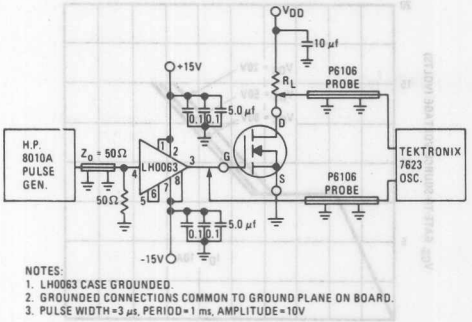
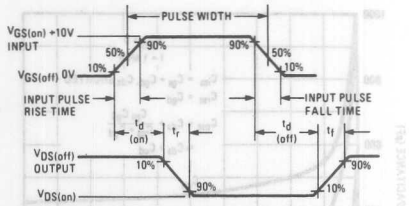


Fig. 14 – Power Vs. Temperature Derating Curve

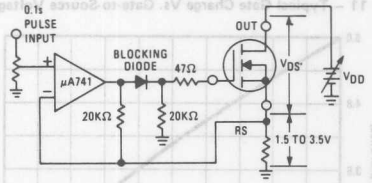


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 — Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \bullet R_S$ = 2.5 ± 1.0 Vdc.

Fig. 16 — Safe Operating Area Test Circuit

HARRIS

2N6790

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

August 1991

Features

- 3.5A, 200V
- $r_{DS(on)} = 0.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

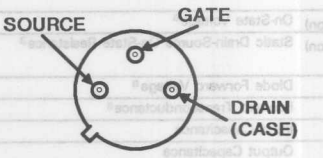
Description

The 2N6790 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6790 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

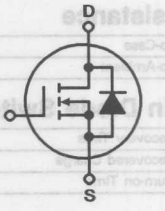
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	2N6790	UNITS
Drain-Source Voltage ..... V_{DS}	200*	V
Drain-Gate Voltage (R_{GS} = 20kΩ) ..... V_{DGR}	200*	V
Continuous Drain Current		
T_C = +25°C ..... I_D	3.5*	A
T_C = +100°C ..... I_D	2.25*	A
Pulsed Drain Current ..... I_{DM}	14*	A
Gate-Source Voltage ..... V_{GS}	±20*	V
Continuous Source Current (Body Diode) ..... I_S	3.5*	A
Pulse Source Current (Body Diode) (Note 2) ..... I_{SM}	14*	A
Maximum Power Dissipation		
T_C = +25°C (See Figure 14) ..... P_D	20*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)	0.16*	W/°C
Inductive Current, Clamped ..... I_{LM} (L = 100μH)	14	A
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1900.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	200*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 200V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 160V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	2.8*	V	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	0.50	0.80*	Ω	V_{GS} = 10V, I_D = 2.25A, T_A = 25°C
		–	–	1.50*	Ω	V_{GS} = 10V, I_D = 2.25A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.7*	–	1.5*	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	1.5*	2.25	4.5*	S(℧)	V_{DS} = 5V, I_D = 2.25A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	60*	150	300*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	15*	40	80*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	40*	ns	V_{DD} ≅ 74V, I_D = 2.25A, Z_o = 50Ω
t_r	Rise Time	–	–	50*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	50*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	50*	ns	of operating temperature.)
SOA	Safe Operating Area	20	–	–	W	V_{DS} = 160V, I_D = 125 mA, See Fig. 16.
		20	–	–	W	V_{DS} = 5.7V, I_D = 3.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	350	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	2.3	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

a Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

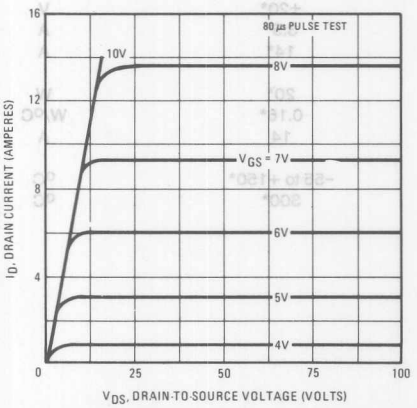


Fig. 1 - Typical output characteristics.

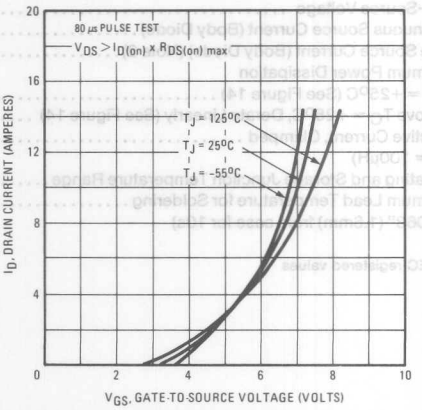


Fig. 2 - Typical transfer characteristics.

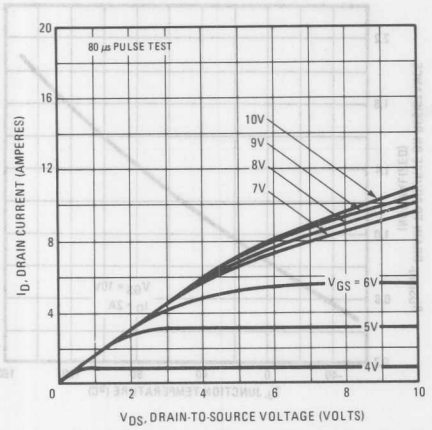


Fig. 3 - Typical saturation characteristics.

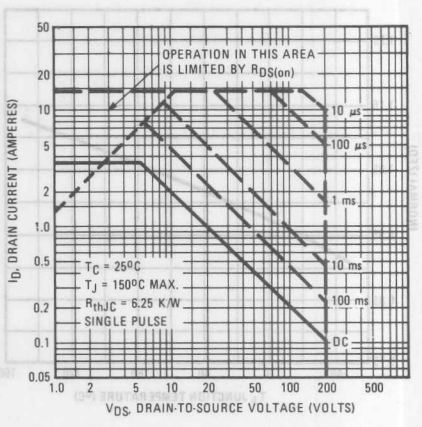


Fig. 4 - Maximum safe operating area.

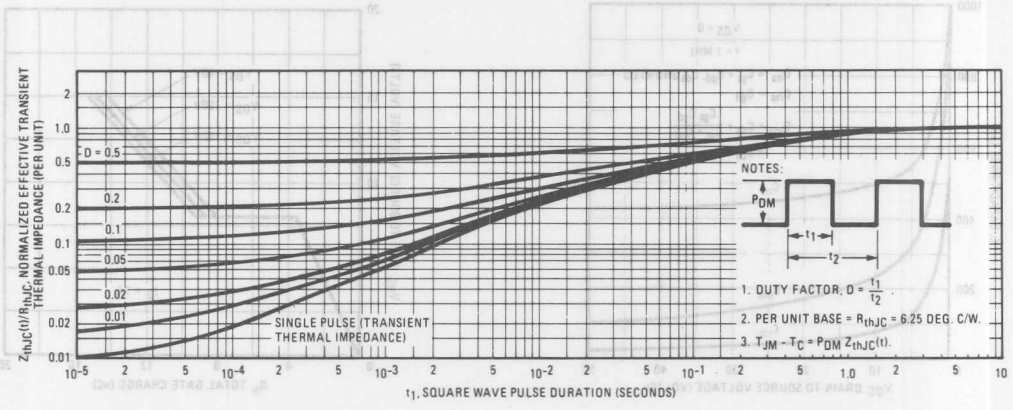


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

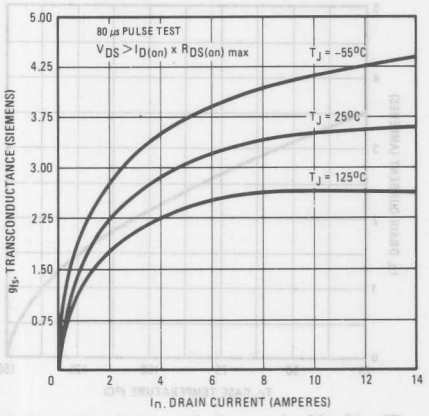


Fig. 6 - Typical transconductance versus drain current.

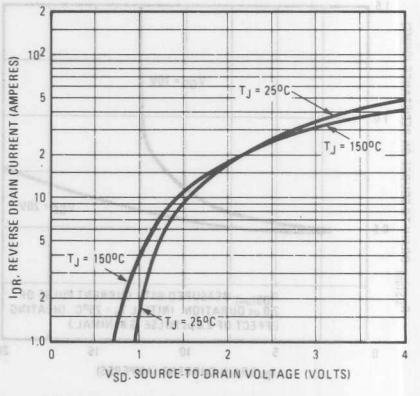


Fig. 7 - Typical source-drain diode forward voltage.

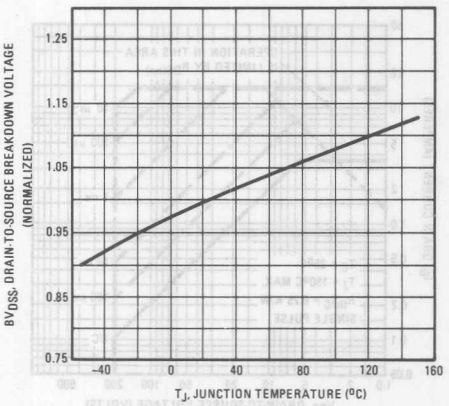


Fig. 8 - Breakdown voltage versus temperature.

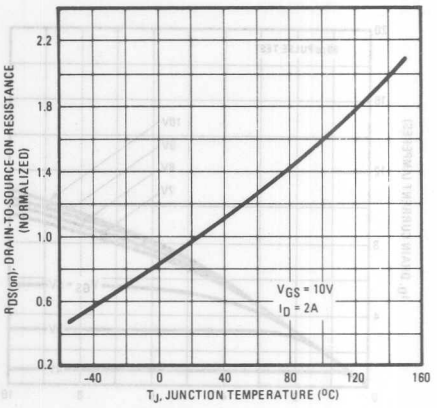


Fig. 9 - Typical normalized on-resistance versus temperature.

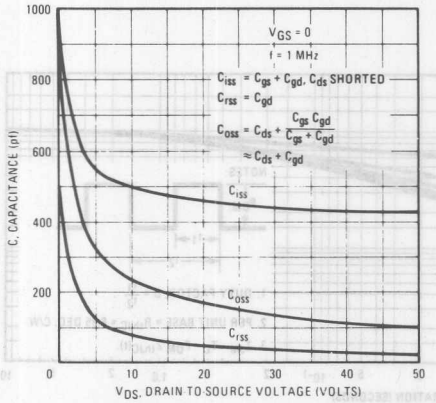


Fig. 10 - Typical capacitance versus drain-to-source voltage.

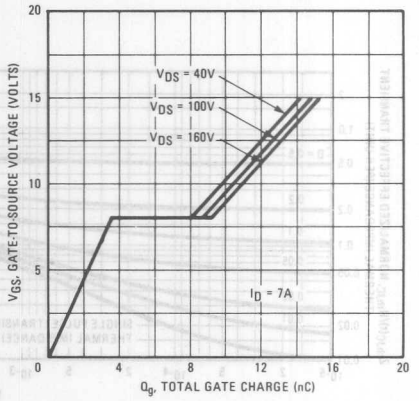


Fig. 11 - Typical gate charge versus gate-to-source voltage.

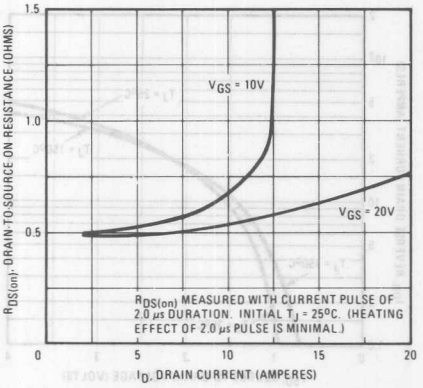


Fig. 12 - Typical on-resistance versus drain current.

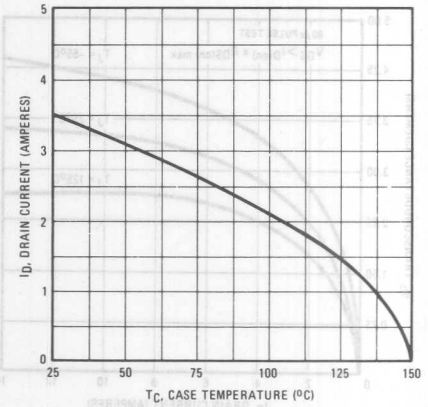


Fig. 13 - Maximum drain current versus case temperature.

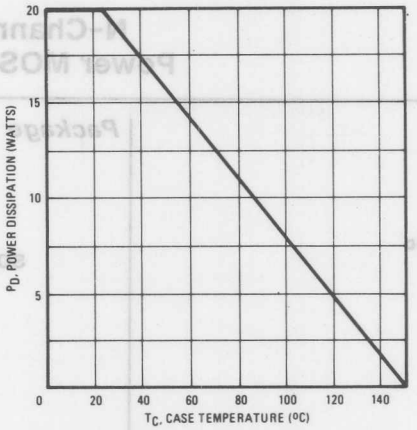
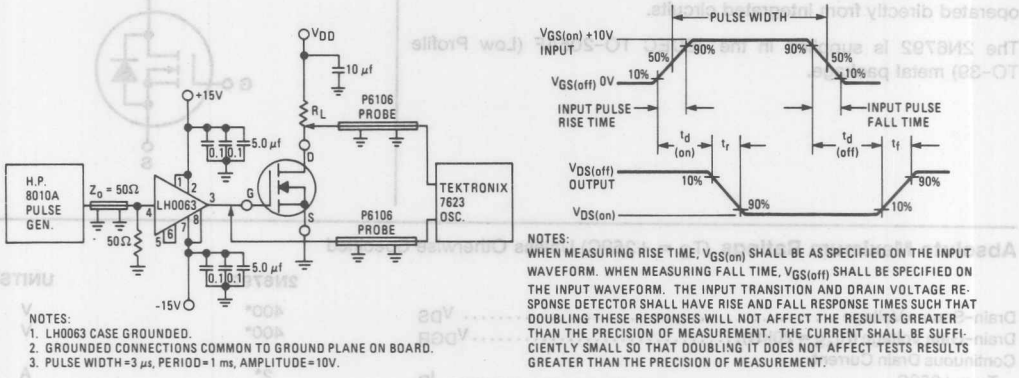


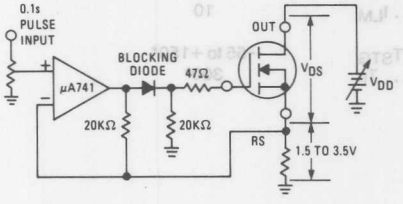
Fig. 14 - Power versus temperature derating curve.



NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.

NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating area test circuit.

HARRIS

2N6792

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

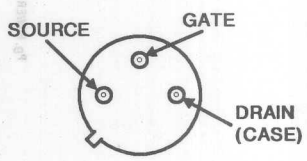
August 1991

Features

- 2A, 400V
- $r_{DS(on)} = 1.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-205AF
BOTTOM VIEW



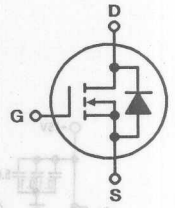
Description

The 2N6792 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6792 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6792	UNITS
Drain-Source Voltage	V_{DS}	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400*	V
Continuous Drain Current			
T_C = +25°C	I_D	2*	A
T_C = +100°C	I_D	1.25*	A
Pulsed Drain Current	I_{DM}	10*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	2*	A
Pulse Source Current	I_{SM}	10*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	20*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.16*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	10	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1901.1**

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	400*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 400V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 320V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage [a]	–	–	3.6*	V	V_{GS} = 10V, I_D = 2.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance [a]	–	1.50	1.80*	Ω	V_{GS} = 10V, I_D = 1.25A, T_A = 25°C
		–	–	4.00*	Ω	V_{GS} = 10V, I_D = 1.25A, T_A = 125°C
V_{SD}	Diode Forward Voltage [a]	0.6*	–	1.4*	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance [a]	1.0*	2.0	3.0*	S(℧)	V_{DS} = 5V, I_D = 1.25A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	40*	100	200*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	5.0*	20	40*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	40*	ns	V_{DD} ≅ 175V, I_D = 1.25A, Z_o = 50Ω
t_r	Rise Time	–	–	35*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	60*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	35*	ns	of operating temperature.)
SOA	Safe Operating Area	20	–	–	W	V_{DS} = 200V, I_D = 100 mA, See Fig. 16.
		20	–	–	W	V_{DS} = 10V, I_D = 2.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	450	ns	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	3.1	μC	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

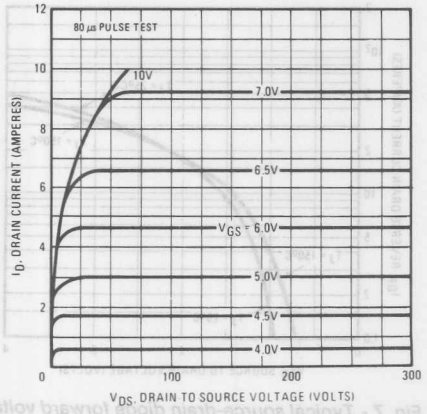


Fig. 1 - Typical output characteristics.

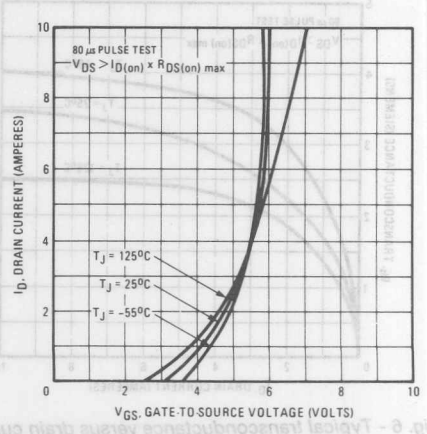


Fig. 2 - Typical transfer characteristics.

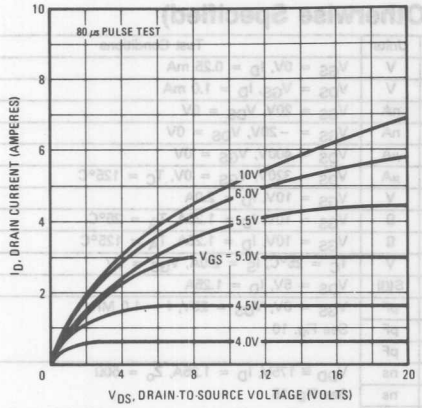


Fig. 3 - Typical saturation characteristics.

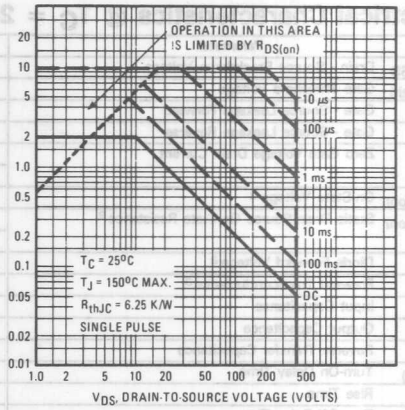


Fig. 4 - Maximum safe operating area.

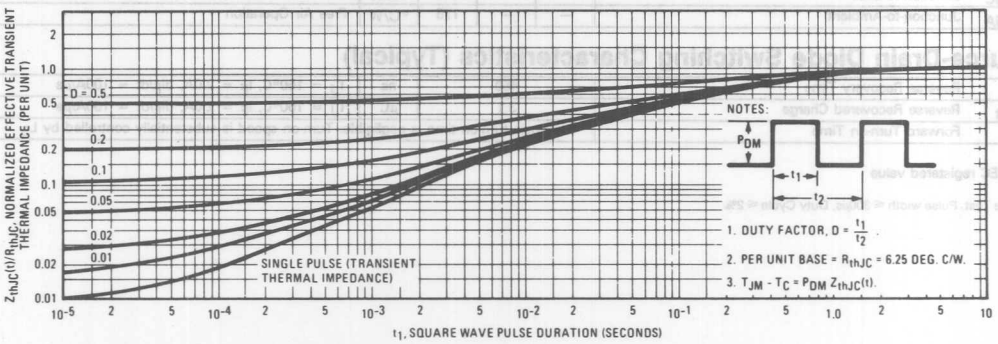


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

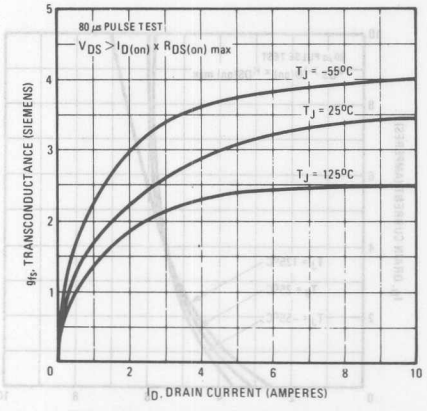


Fig. 6 - Typical transconductance versus drain current.

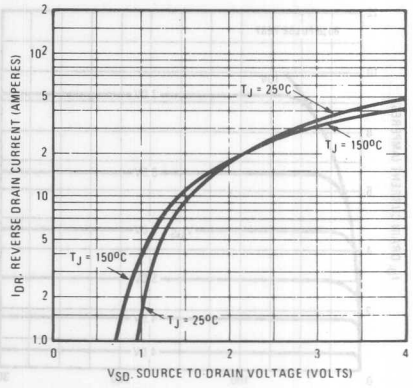


Fig. 7 - Typical source-drain diode forward voltage.

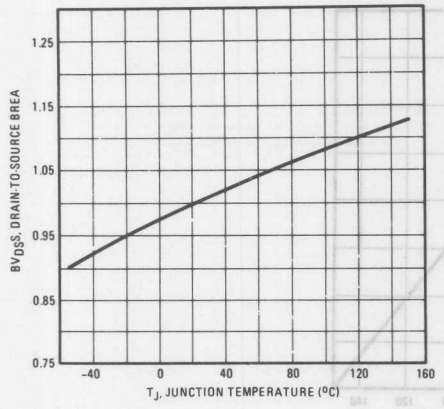


Fig. 8 - Breakdown voltage versus temperature.

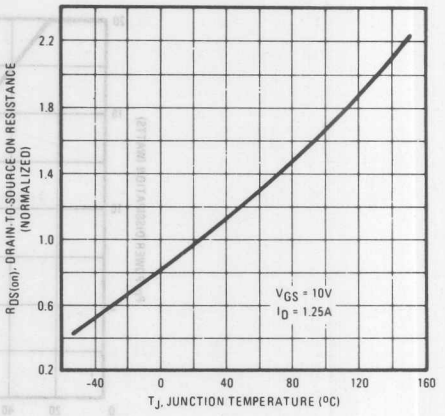


Fig. 9 - Typical normalized on-resistance versus. temperature.

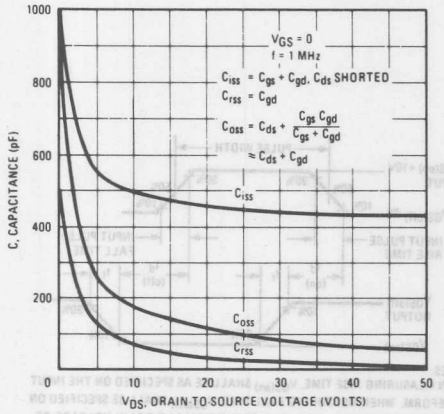


Fig. 10 - Typical capacitance versus drain-to-source. voltage.

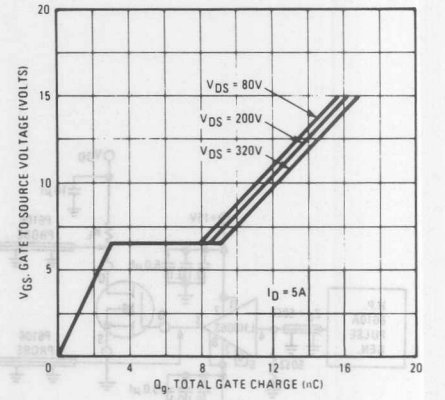


Fig. 11 - Typical gate charge versus gate-to-source. voltage.

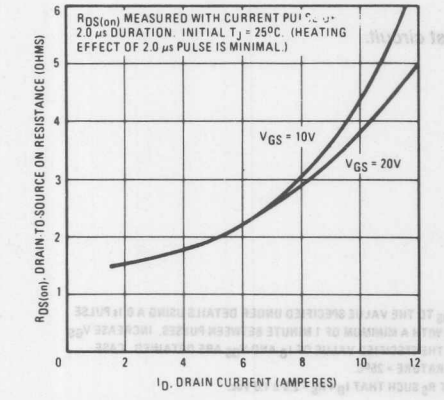


Fig. 12 - Typical on-resistance versus drain current.

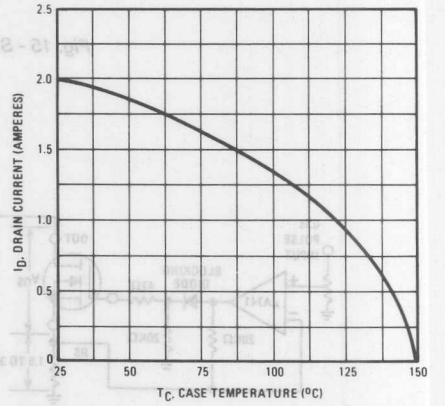


Fig. 13 - Maximum drain current versus case. temperature.

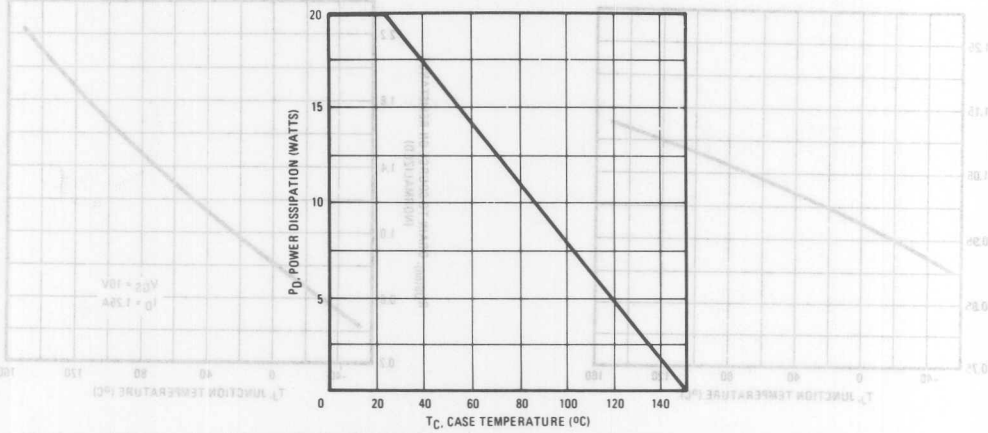
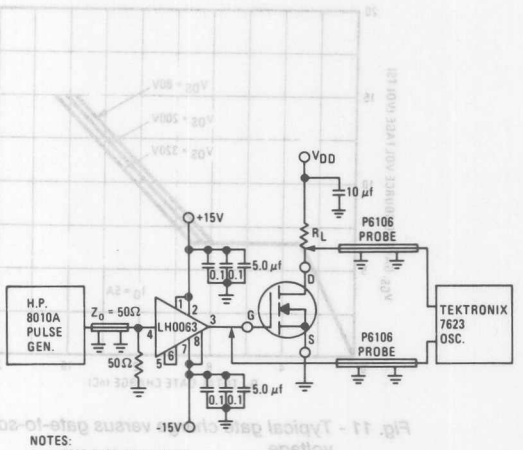
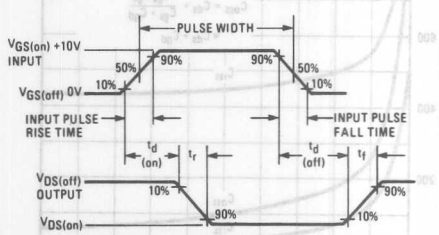


Fig. 14 - Power versus temperature derating curve.

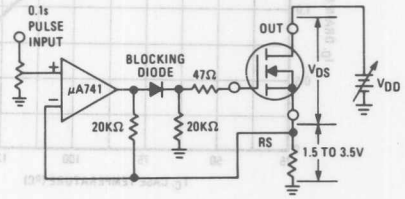


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D * R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating area test circuit.

2N6794

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

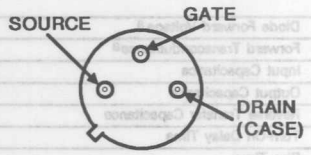
August 1991

Features

- 1.5A, 500V
- $r_{DS(on)} = 3\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-205AF
BOTTOM VIEW



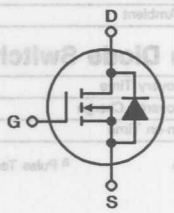
Description

The 2N6794 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6794 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6794	UNITS
Drain-Source Voltage	V_{DS}	500*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500*	V
Continuous Drain Current			
T_C = +25°C	I_D	1.5*	A
T_C = +100°C	I_D	1*	A
Pulsed Drain Current	I_{DM}	6.5*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	1.5*	A
Pulse Source Current	I_{SM}	6.5*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	20*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.16*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	6.5	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	500*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 500V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 400V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	4.5*	V	V_{GS} = 10V, I_D = 1.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	2.5	3.0*	Ω	V_{GS} = 10V, I_D = 1.0A, T_A = 25°C
		–	–	6.6*	Ω	V_{GS} = 10V, I_D = 1.0A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.6*	–	1.2*	V	T_C = 25°C, I_S = 1.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	1.0*	1.75	3.0*	S(℧)	V_{DS} = 5V, I_D = 1.00A
C_{iss}	Input Capacitance	200*	300	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	30*	75	150*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	5.0*	20	40*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	40*	ns	V_{DD} ≅ 225V, I_D = 1.0A, Z_o = 50Ω
t_r	Rise Time	–	–	30*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	60*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	30*	ns	of operating temperature.)
SOA	Safe Operating Area	20	–	–	W	V_{DS} = 200V, I_D = 100 mA, See Fig. 16.
		20	–	–	W	V_{DS} = 13.3V, I_D = 1.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	600	ns	T_J = 150°C, I_F = 1.50A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	3.5	μC	T_J = 150°C, I_F = 1.50A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

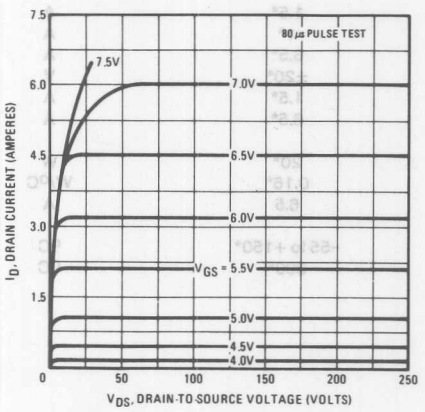


Fig. 1 - Typical output characteristics.

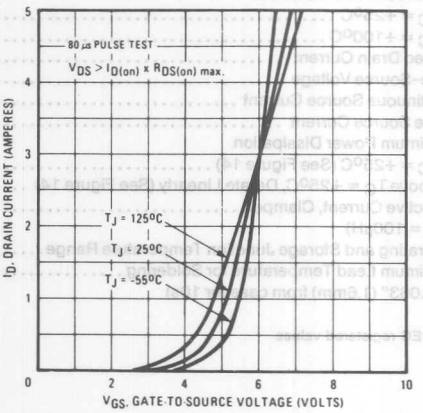


Fig. 2 - Typical transfer characteristics.

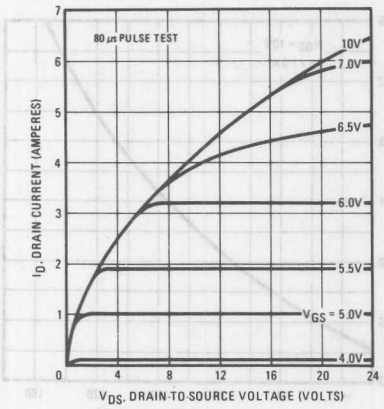


Fig. 3 - Typical saturation characteristics.

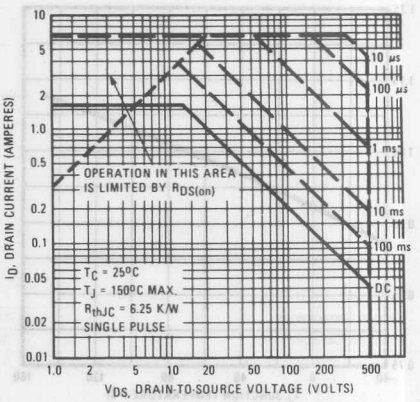


Fig. 4 - Maximum safe operating area.

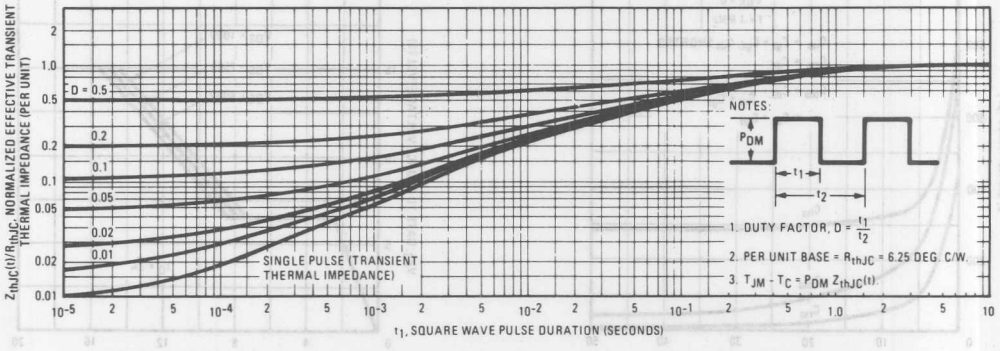


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

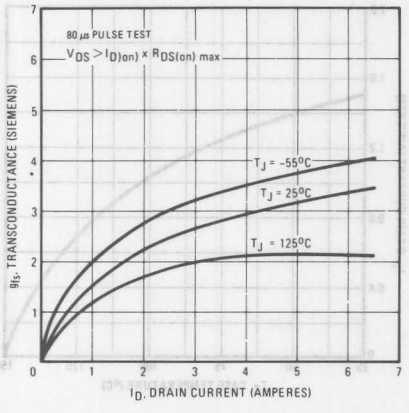


Fig. 6 - Typical transconductance versus drain current.

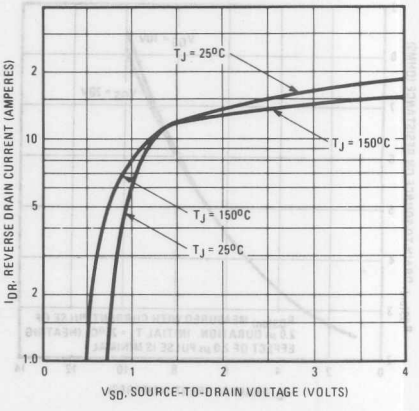


Fig. 7 - Typical source-drain diode forward voltage.

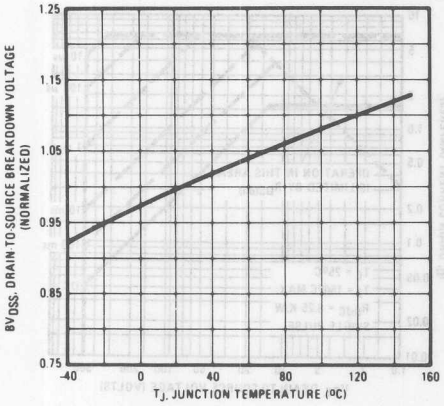


Fig. 8 - Breakdown voltage versus temperature.

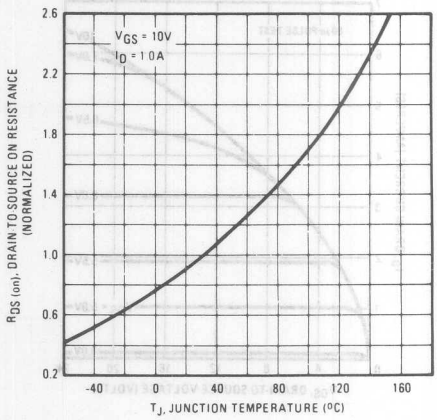


Fig. 9 - Typical normalized on-resistance versus temperature.

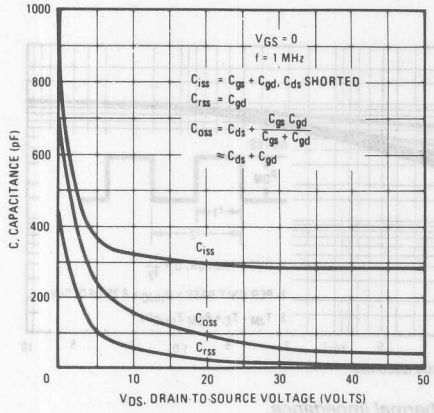


Fig. 10 - Typical capacitance versus drain-to-source voltage.

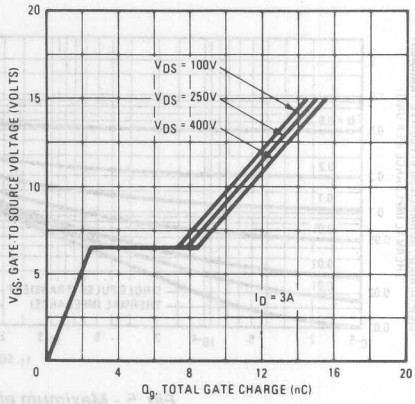


Fig. 11 - Typical gate charge versus gate-to-source voltage.

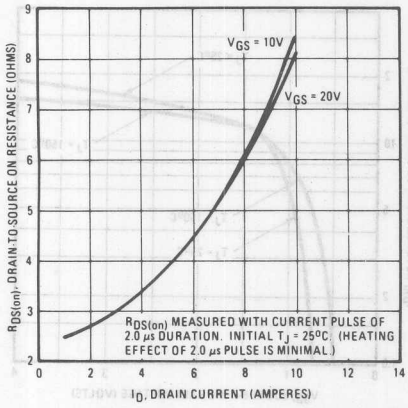


Fig. 12 - Typical on-resistance versus drain current.

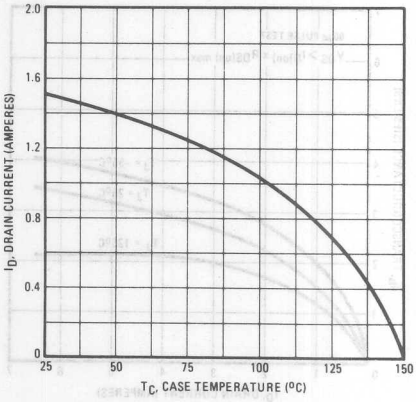


Fig. 13 - Maximum drain current versus case temperature.

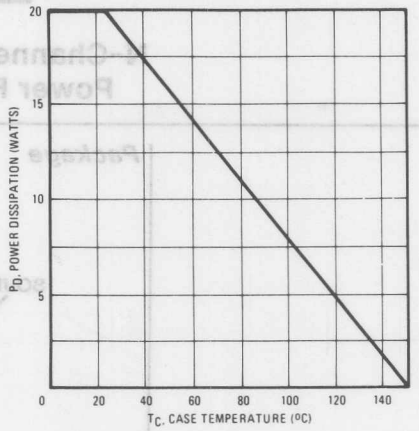
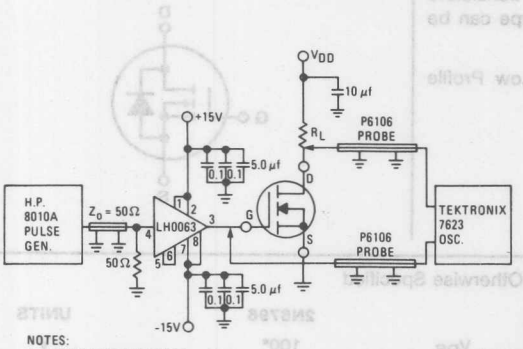
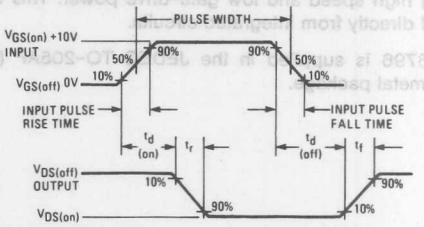


Fig. 14 - Power versus temperature derating curve.

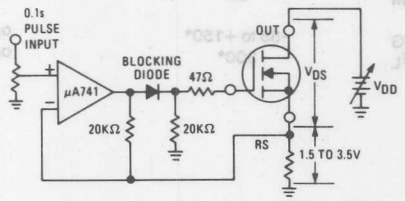


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

HARRIS

2N6796

N-Channel Enhancement-Mode Power Field-Effect Transistor

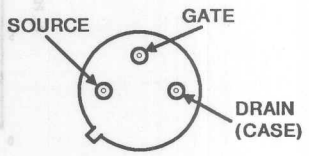
August 1991

Features

- 8.0A, 100V
- $r_{DS(on)} = 0.18\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-205AF
BOTTOM VIEW



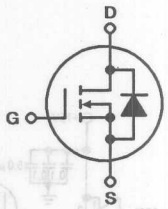
Description

The 2N6796 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6796 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6796	UNITS
Drain-Source Voltage (Note 1)	V_{DS}	100*	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100*	V
Continuous Drain Current			
T_C = +25°C	I_D	8.0*	A
T_C = +100°C	I_D	5.0*	A
Pulsed Drain Current (Note 2)	I_{DM}	32*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current (Body Diode)	I_S	8.0*	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}	32*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	25*	W
Linear Derating Factor (See Figure 14)		0.20*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	32	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

NOTES:

1. T_J = +25°C to +150°C
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1594.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	–	–	1.56*	V	V_{GS} = 10V, I_D = 8.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 5.0A, T_C = 25°C
		–	–	0.35*	Ω	V_{GS} = 10V, I_D = 5.0A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.75*	–	1.5*	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	3.0*	5.5	9.0*	S(℧)	V_{DS} = 5V, I_D = 5.0A
C_{iss}	Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	150*	300	500*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	50*	100	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	30*	ns	V_{DD} ≅ 30V, I_D = 5.0A, Z_o = 50Ω
t_r	Rise Time	–	–	75*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	40*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	45*	ns	of operating temperature.)
SOA	Safe Operating Area	25	–	–	W	V_{DS} = 80V, I_D = 310 mA, See Fig. 16.
		25	–	–	W	V_{DS} = 3.12V, I_D = 8.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	300	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.5	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

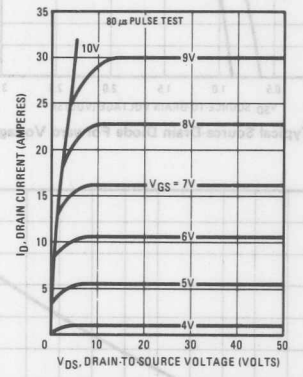


Fig. 1 – Typical Output Characteristics

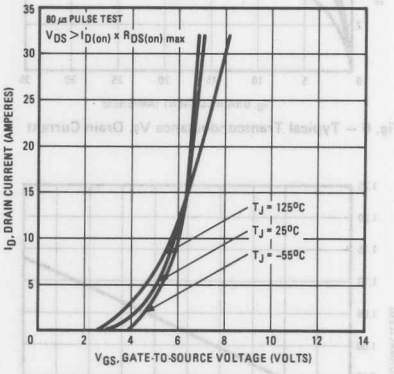


Fig. 2 – Typical Transfer Characteristics

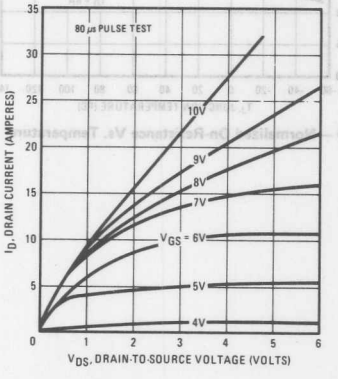


Fig. 3 – Typical Saturation Characteristics

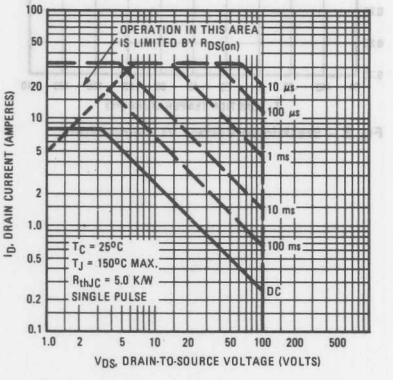


Fig. 4 – Maximum Safe Operating Area

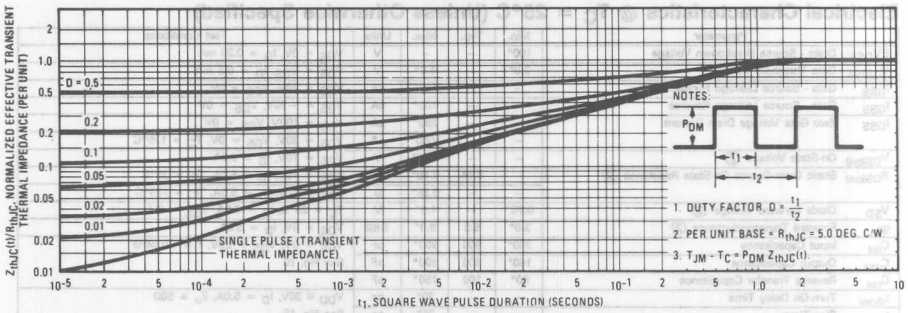


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

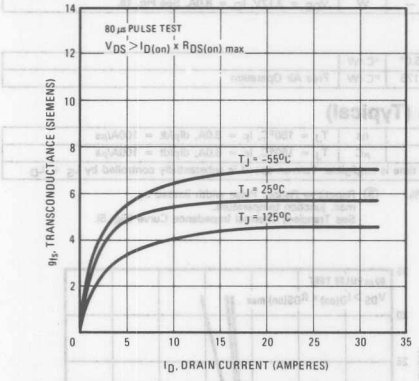


Fig. 6 — Typical Transconductance Vs. Drain Current

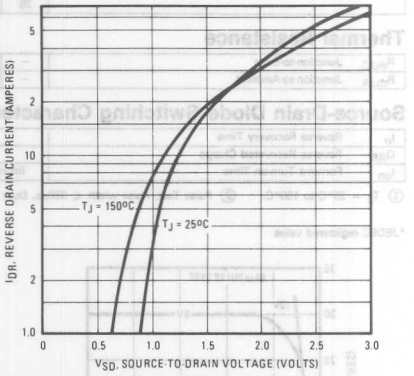


Fig. 7 — Typical Source-Drain Diode Forward Voltage

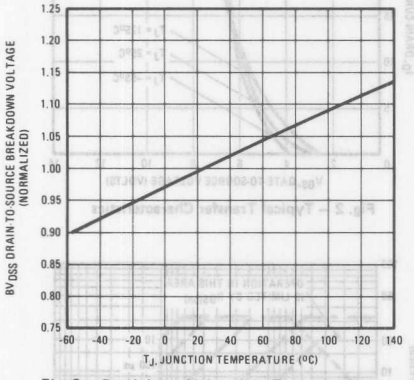


Fig. 8 — Breakdown Voltage Vs. Temperature

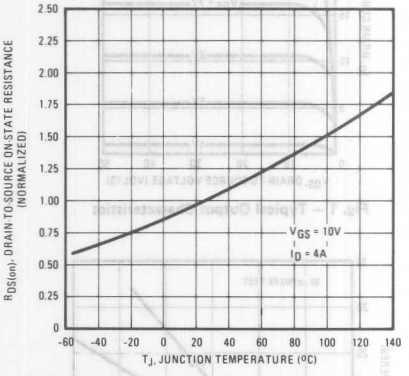


Fig. 9 — Normalized On-Resistance Vs. Temperature

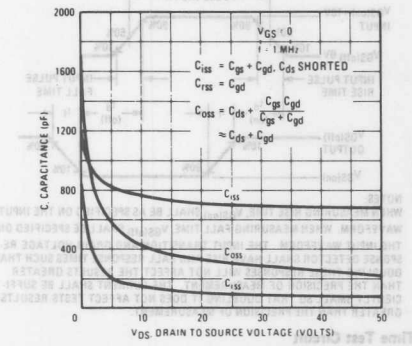


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

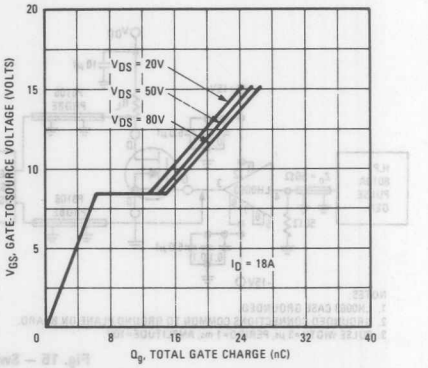


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

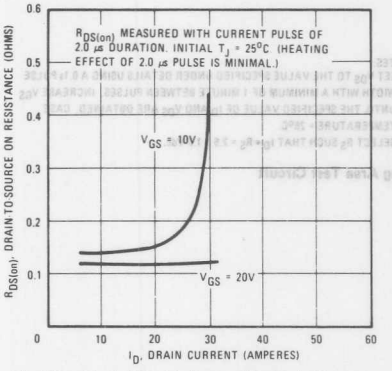


Fig. 12 – Typical On-Resistance Vs. Drain Current

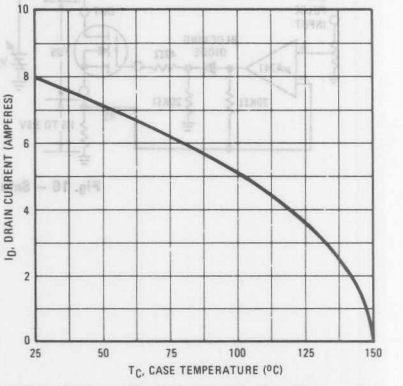


Fig. 13 – Maximum Drain Current Vs. Case Temperature

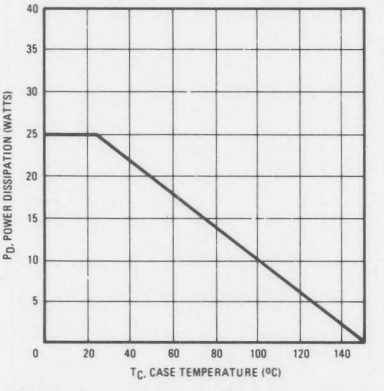
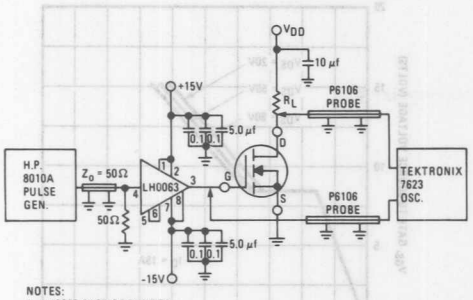
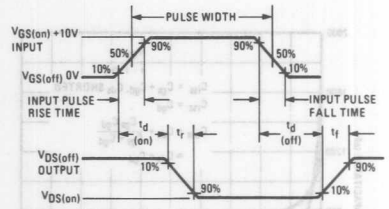


Fig. 14 – Power Vs. Temperature Derating Curve

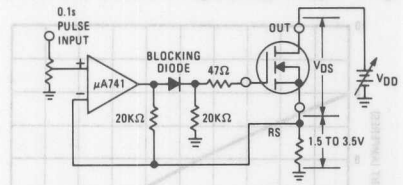


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 — Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 — Safe Operating Area Test Circuit

HARRIS

2N6798

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

August 1991

Features

- 5.5A, 200V
- $r_{DS(on)} = 0.4\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

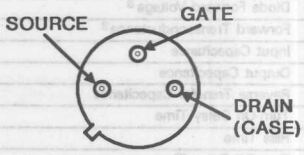
Description

The 2N6798 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6798 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

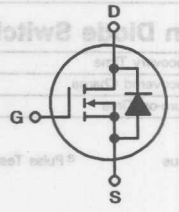
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6798	UNITS
Drain-Source Voltage	V_{DS}	200*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	200*	V
Continuous Drain Current			
T_C = +25°C	I_D	5.5*	A
T_C = +100°C	I_D	3.5*	A
Pulsed Drain Current	I_{DM}	22*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	5.5*	A
Pulse Source Current	I_{SM}	22*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	25*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.20*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	22	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1903.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	200*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 200V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 160V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	2.20*	V	V_{GS} = 10V, I_D = 5.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	0.25	0.4*	Ω	V_{GS} = 10V, I_D = 3.5A, T_A = 25°C
		–	–	0.75*	Ω	V_{GS} = 10V, I_D = 3.5A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.70*	–	1.4*	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	2.5*	4.5	7.5*	S(℧)	V_{DS} = 5V, I_D = 3.5A
C_{iss}	Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100*	250	450*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	40*	80	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	30*	ns	V_{DD} ≅ 77V, I_D = 3.5A, Z_o = 50Ω
t_r	Rise Time	–	–	50*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	50*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	40*	ns	of operating temperature.)
SOA	Safe Operating Area	25	–	–	W	V_{DS} = 160V, I_D = 155 mA, See Fig. 16.
		25	–	–	W	V_{DS} = 4.5V, I_D = 5.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	450	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	3.0	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ⩽ 300μs, Duty Cycle ⩽ 2%.

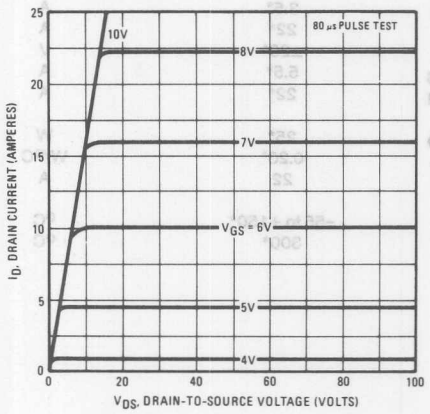


Fig. 1 - Typical output characteristics.

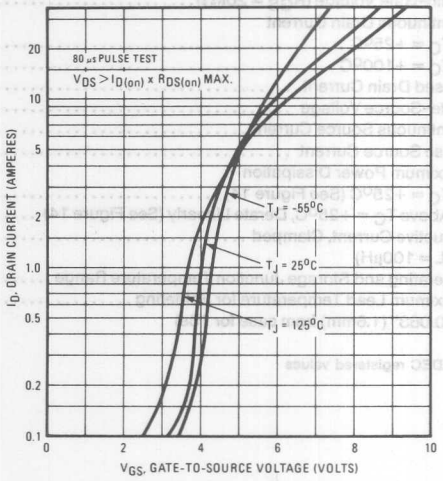


Fig. 2 - Typical transfer characteristics.

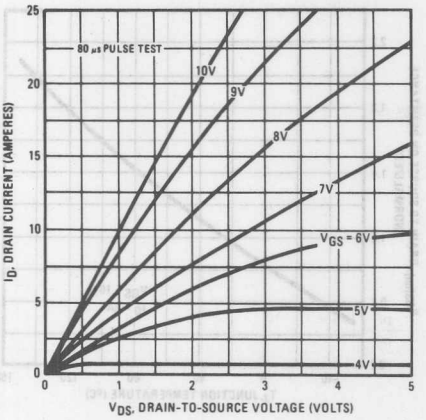


Fig. 3 - Typical saturation characteristics.

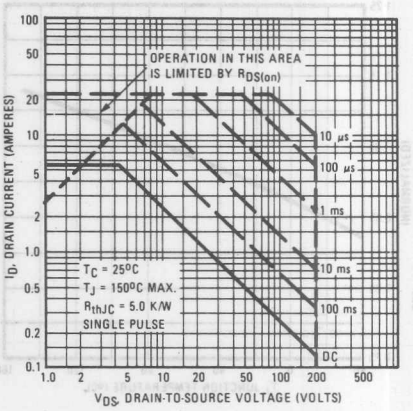


Fig. 4 - Maximum safe operating area.

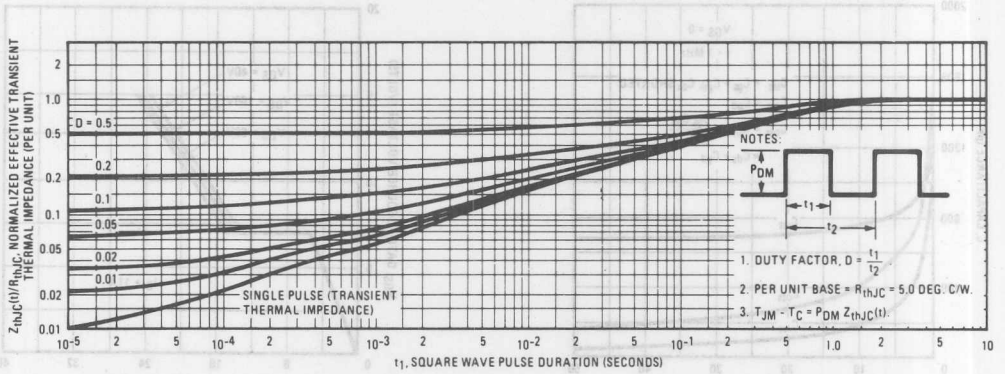


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

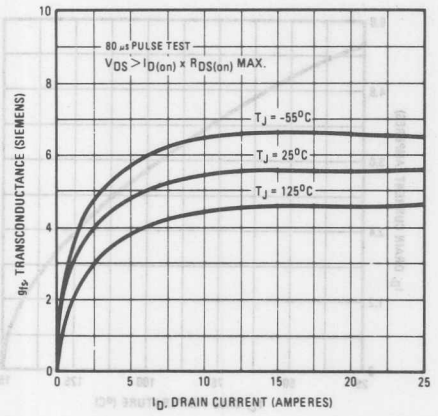


Fig. 6 - Typical transconductance versus drain current.

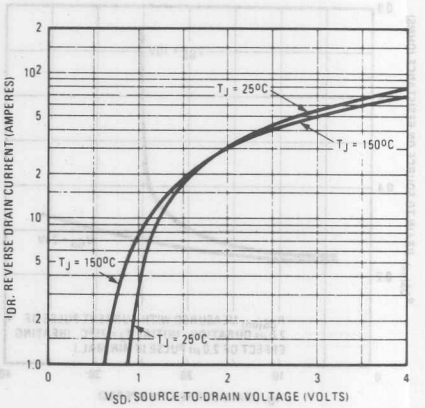


Fig. 7 - Typical source-drain diode forward voltage.

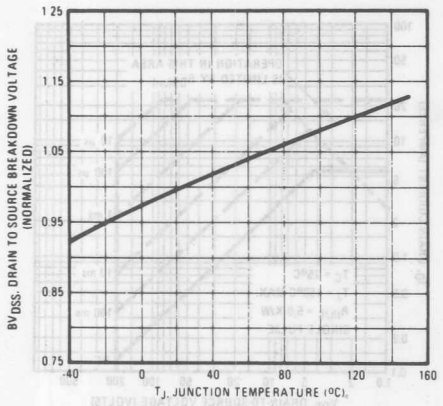


Fig. 8 - Breakdown voltage versus temperature.

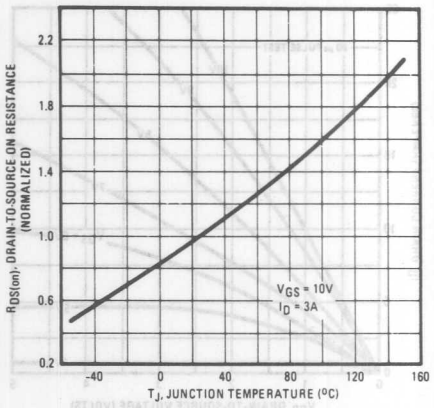


Fig. 9 - Typical normalized on-resistance versus temperature.

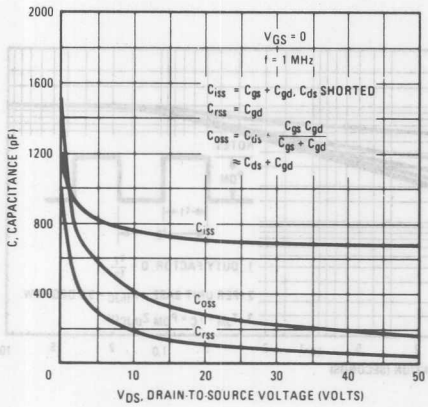


Fig. 10 - Typical capacitance versus drain-to-source voltage.

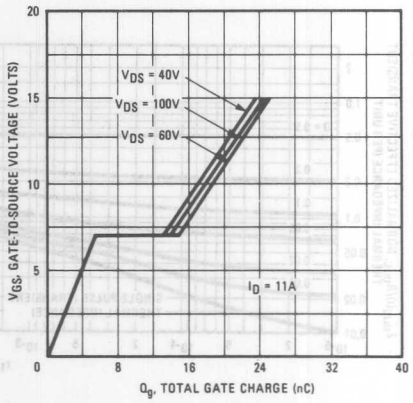


Fig. 11 - Typical gate charge versus gate-to-source voltage.

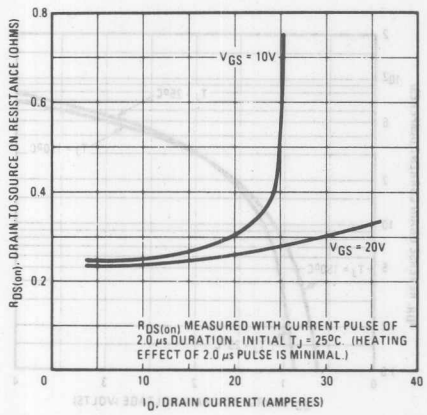


Fig. 12 - Typical on-resistance versus drain current.

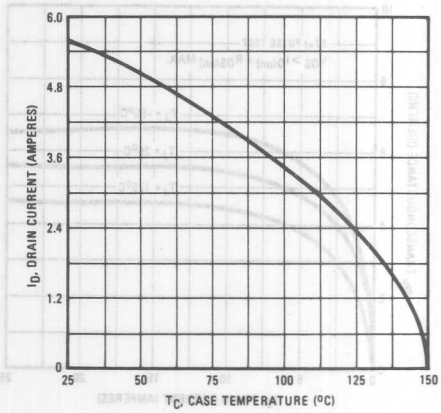


Fig. 13 - Maximum drain current versus case temperature.

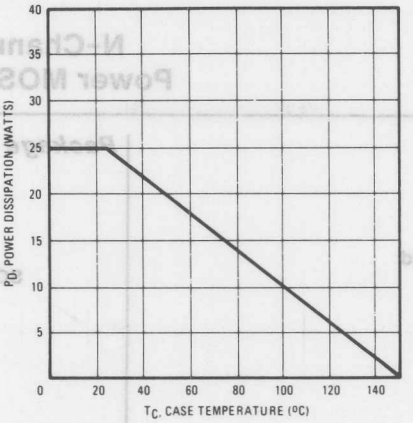
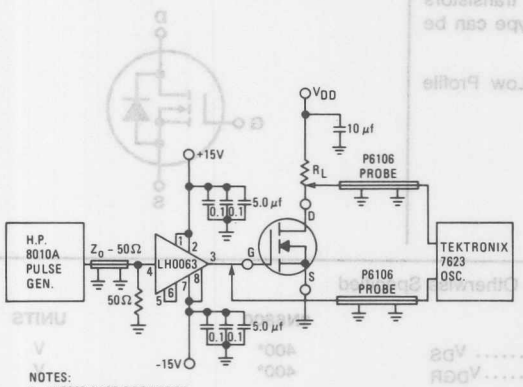
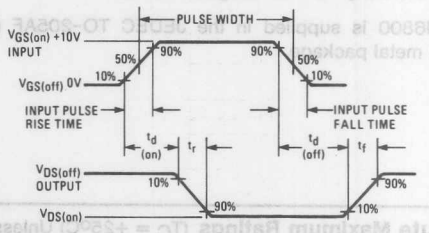


Fig. 14 - Power versus temperature derating curve.

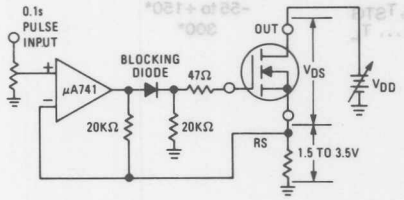


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D * R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

HARRIS

2N6800

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

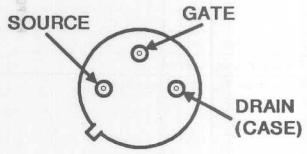
August 1991

Features

- 3A, 400V
- $r_{DS(on)} = 1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-205AF
BOTTOM VIEW



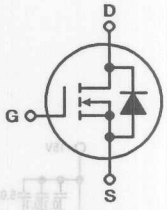
Description

The 2N6800 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6800 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6800	UNITS
Drain-Source Voltage	V_{DS}	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400*	V
Continuous Drain Current			
T_C = +25°C	I_D	3*	A
T_C = +100°C	I_D	2*	A
Pulsed Drain Current	I_{DM}	14*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	3*	A
Pulse Source Current	I_{SM}	14*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	25*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.20*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	14	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1904.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	400*	—	—	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	—	—	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	—	—	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250*	μA	V_{DS} = 400V, V_{GS} = 0V
		—	—	1000*	μA	V_{DS} = 320V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	—	—	3.0*	V	V_{GS} = 10V, I_D = 3.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	—	0.8	1.0*	Ω	V_{GS} = 10V, I_D = 2.0A, T_A = 25°C
		—	—	2.4*	Ω	V_{GS} = 10V, I_D = 2.0A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.70*	—	1.4*	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	2.0*	3.5	6.0*	S(℧)	V_{DS} = 5V, I_D = 2.0A
C_{iss}	Input Capacitance	350*	700	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	50*	150	300*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	20*	40	80*	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	30*	ns	$V_{DD} \cong$ 176V, I_D = 2.0A, Z_o = 50Ω
t_r	Rise Time	—	—	35*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	—	—	55*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	—	35*	ns	
SOA	Safe Operating Area	25	—	—	W	V_{DS} = 200V, I_D = 125 mA, See Fig. 16.
		25	—	—	W	V_{DS} = 8.3V, I_D = 3.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	600	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	4.0	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

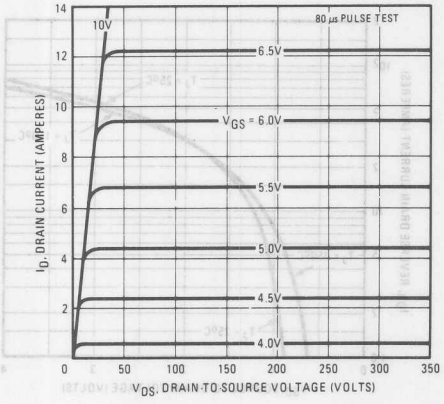


Fig. 1 - Typical output characteristics.

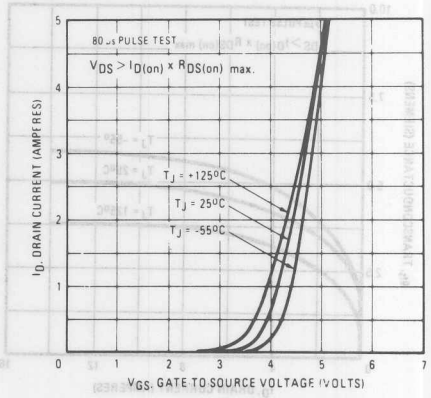


Fig. 2 - Typical transfer characteristics.

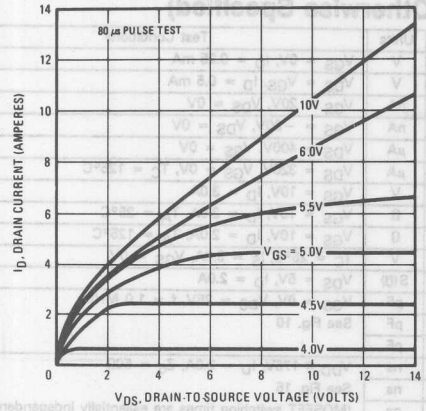


Fig. 3 - Typical saturation characteristics.

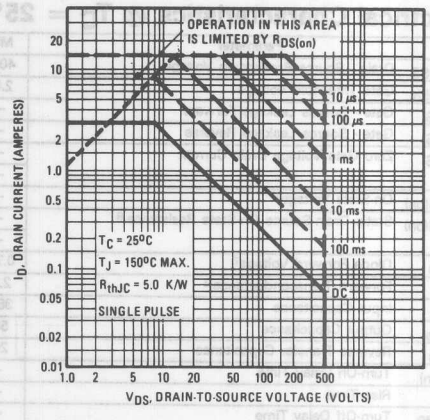


Fig. 4 - Maximum safe operating area.

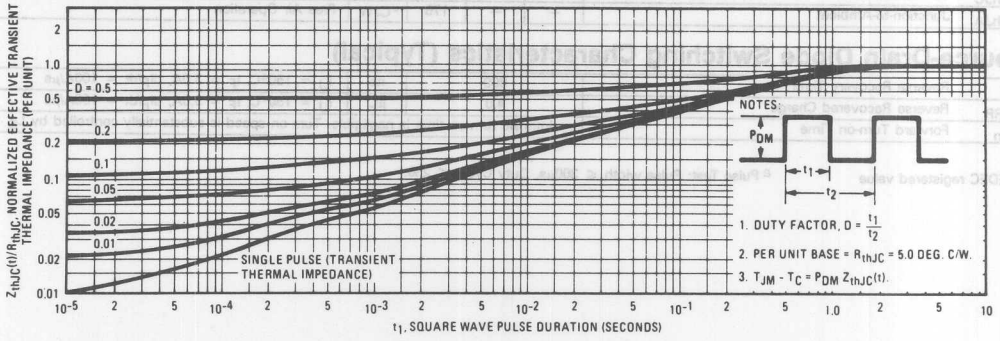


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

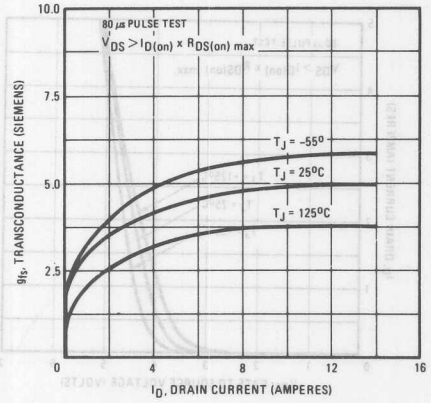


Fig. 6 - Typical transconductance versus drain current.

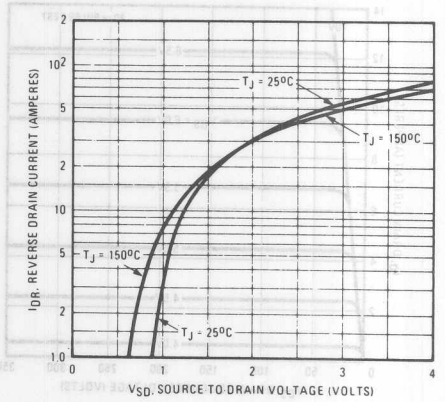


Fig. 7 - Typical source-drain diode forward voltage.

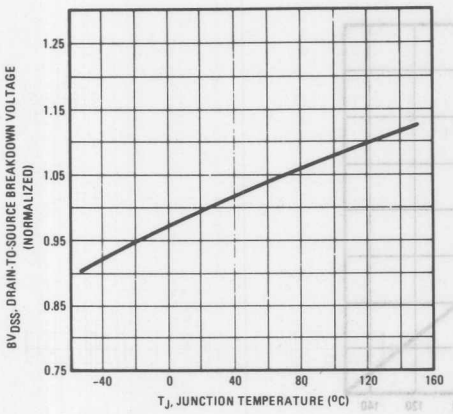


Fig. 8 - Breakdown voltage versus temperature.

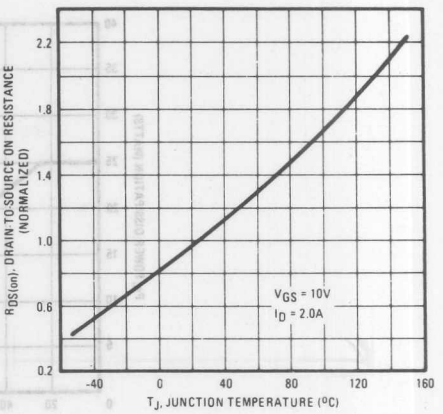


Fig. 9 - Typical normalized on-resistance versus temperature.

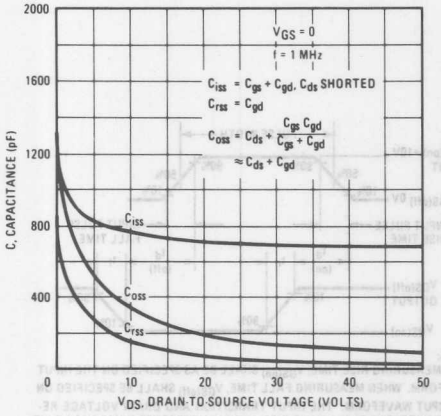


Fig. 10 - Typical capacitance versus drain-to-source voltage.

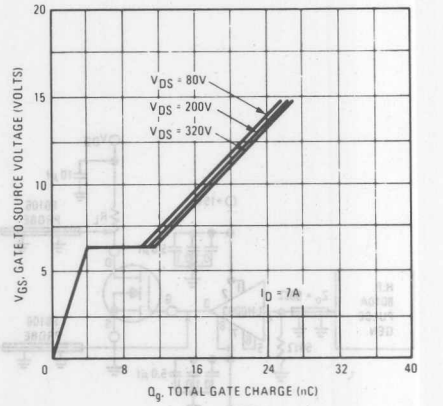


Fig. 11 - Typical gate charge versus gate-to-source voltage.

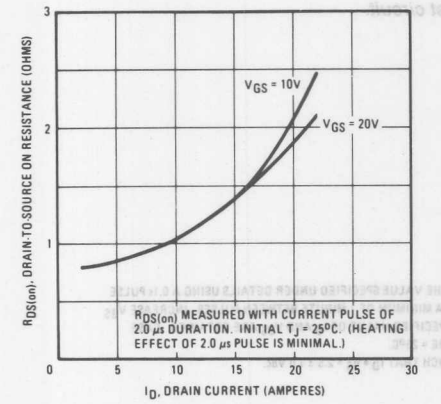


Fig. 12 - Typical on-resistance versus drain current.

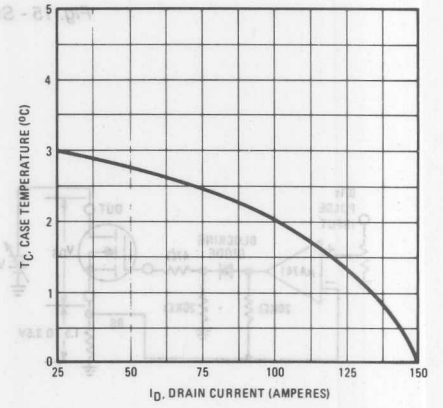


Fig. 13 - Maximum drain current versus case temperature.

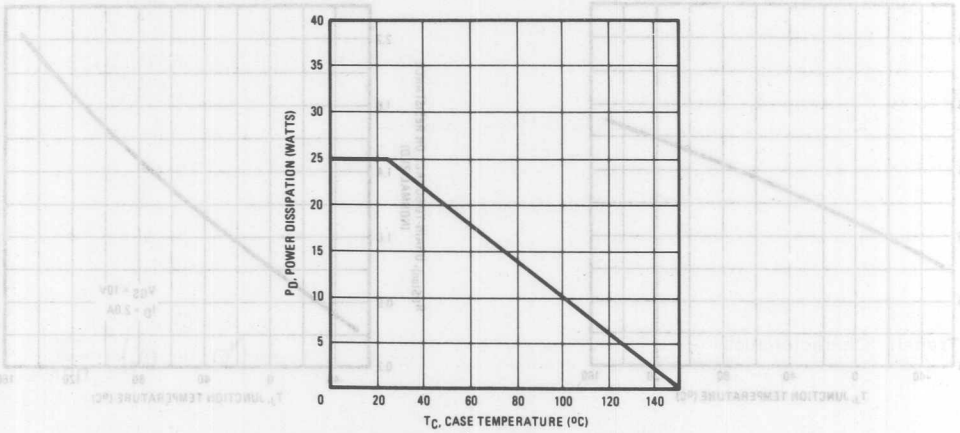
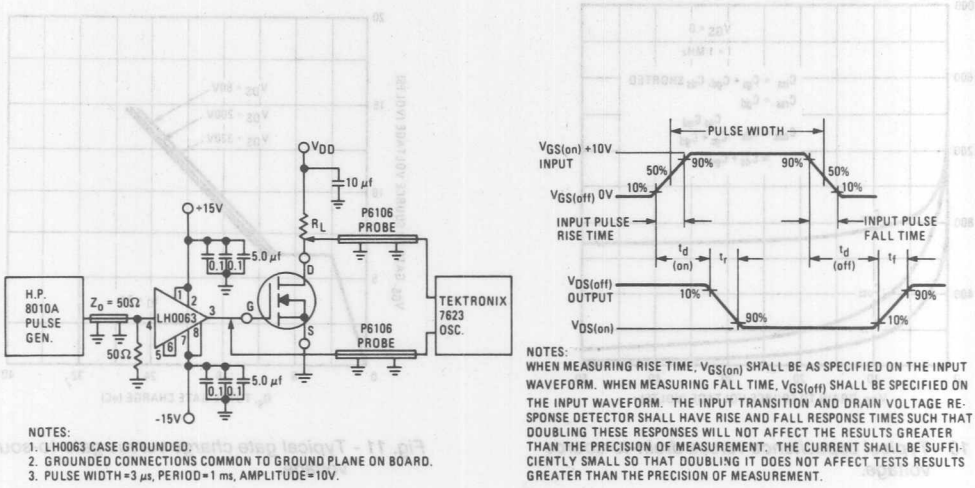


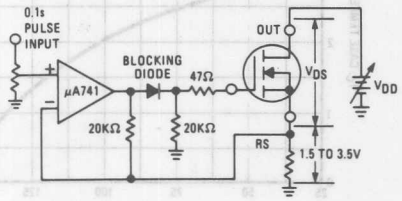
Fig. 14 - Power versus temperature derating curve.



NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.

NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D * R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

HARRIS

2N6802

August 1991

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

Features

- 3.5A, 500V
- $r_{DS(on)} = 1.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

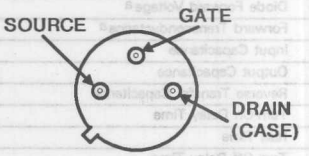
Description

The 2N6802 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6802 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

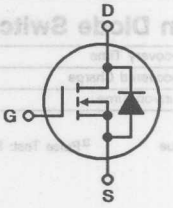
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6802	UNITS
Drain-Source Voltage	V_{DS}	500*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500*	V
Continuous Drain Current			
T_C = +25°C	I_D	3.5*	A
T_C = +100°C	I_D	1.5*	A
Pulsed Drain Current	I_{DM}	11*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	2.5*	A
Pulse Source Current	I_{SM}	11*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	25*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.20*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	11	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1905.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	500*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 500V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 400V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	3.75*	V	V_{GS} = 10V, I_D = 2.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	1.3	1.5*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 25°C
		–	–	3.5*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.70*	–	1.4*	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	1.5*	2.5	4.5*	S(℧)	V_{DS} = 5V, I_D = 1.5A
C_{iss}	Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	25*	100	200*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	15*	30	60*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	30*	ns	V_{DD} ≅ 225V, I_D = 1.5A, Z_o = 50Ω
t_r	Rise Time	–	–	30*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	55*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	30*	ns	of operating temperature.)
SOA	Safe Operating Area	25	–	–	W	V_{DS} = 200V, I_D = 125 mA, See Fig. 16.
		25	–	–	W	V_{DS} = 10V, I_D = 2.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	800	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	4.6	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

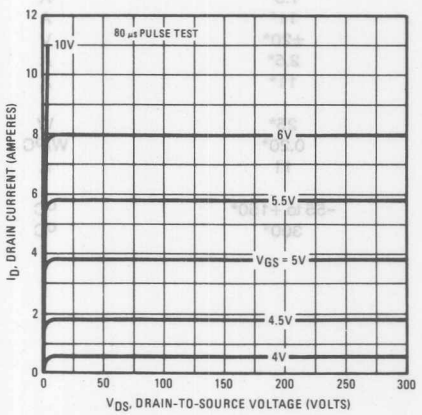


Fig. 1 - Typical output characteristics.

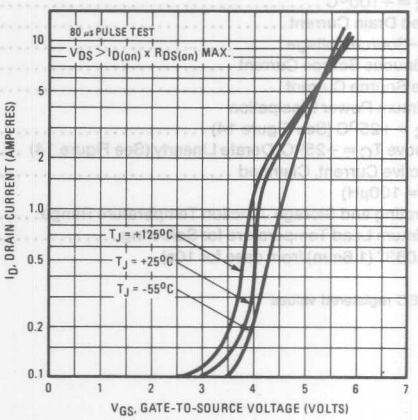


Fig. 2 - Typical transfer characteristics.

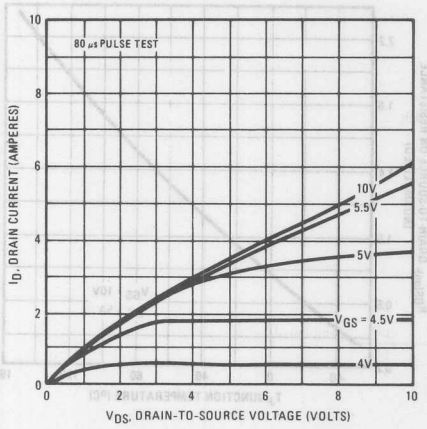


Fig. 3 - Typical saturation characteristics.

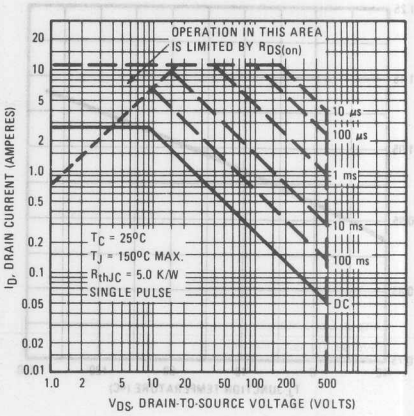


Fig. 4 - Maximum safe operating area.

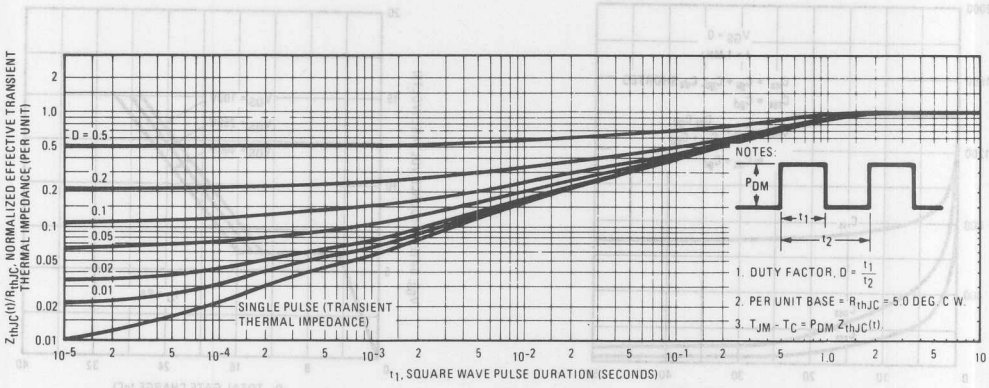


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

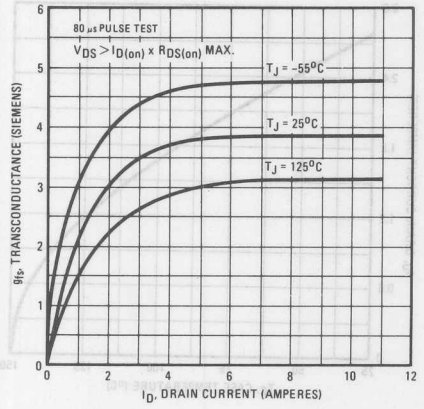


Fig. 6 - Typical transconductance versus drain current.

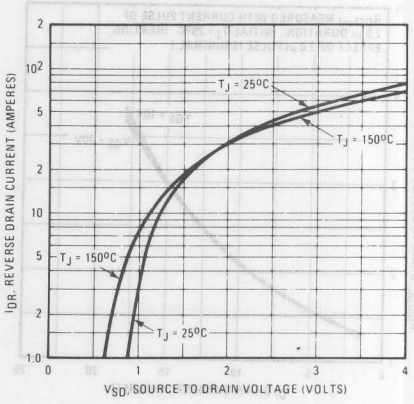


Fig. 7 - Typical source-drain diode forward voltage.

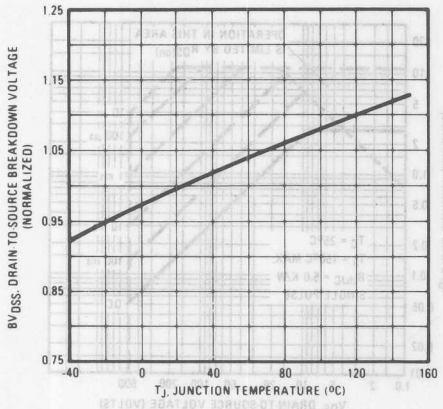


Fig. 8 - Breakdown voltage versus temperature.

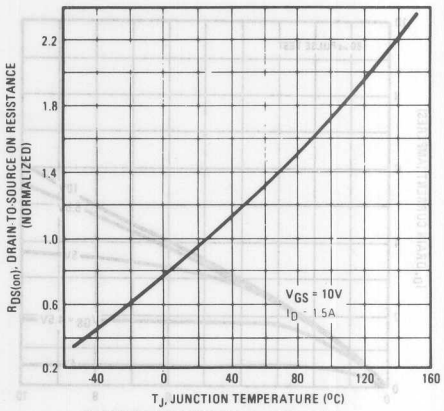


Fig. 9 - Typical normalized on-resistance versus temperature.

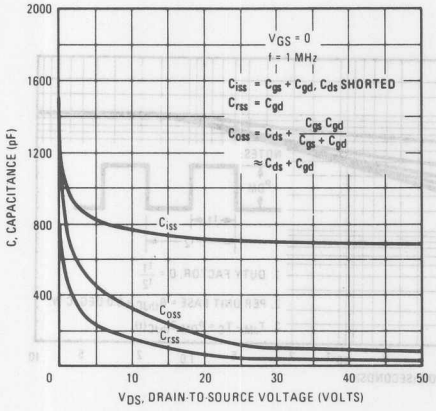


Fig. 10 - Typical capacitance versus drain-to-source voltage.

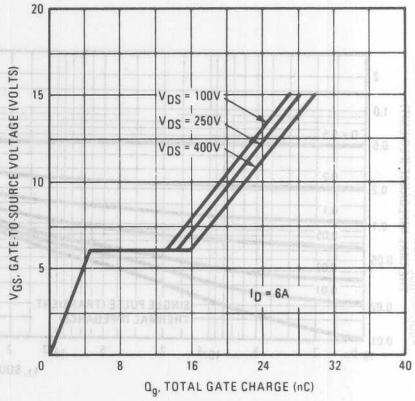


Fig. 11 - Typical gate charge versus gate-to-source voltage.

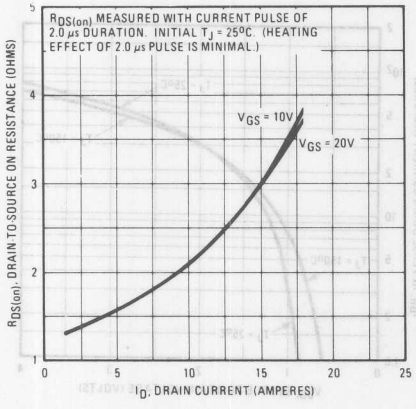


Fig. 12 - Typical on-resistance versus drain current.

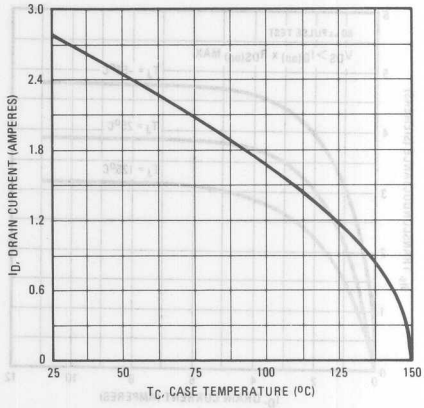


Fig. 13 - Maximum drain current versus case temperatu

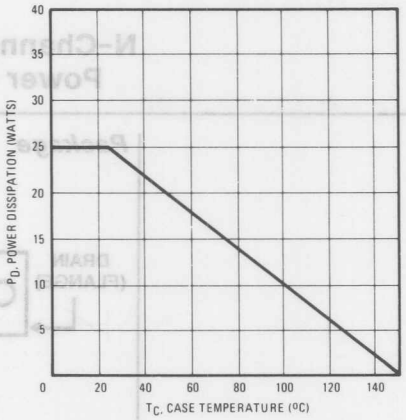
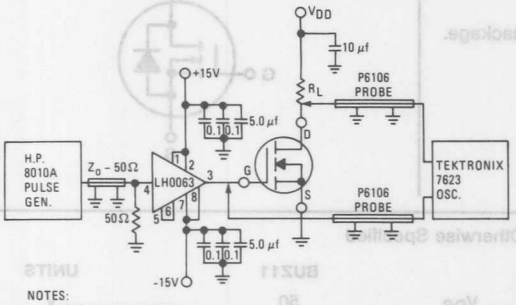
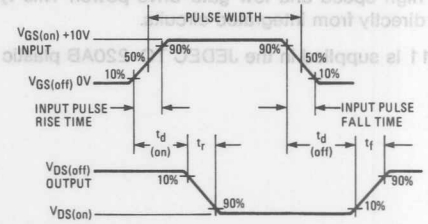


Fig. 14 - Power versus temperature derating curve.

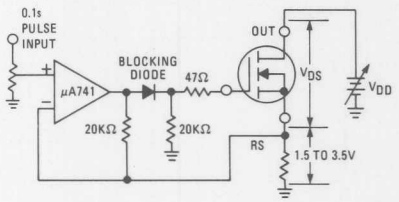


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

HARRIS

BUZ11

N-Channel Enhancement-Mode Power Field-Effect Transistor

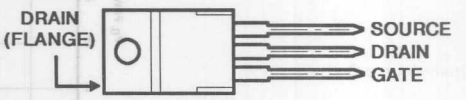
August 1991

Features

- 30A, 50V
- $r_{DS(on)} = 0.04\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-220AB
TOP VIEW



Description

The BUZ11 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ11 is supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ11	UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	50	V
Continuous Drain Current			
T_C = +30°C	I_D	30	A
Pulsed Drain Current			
T_C = +25°C	I_{DM}	120	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2253

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	50	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C, V_{DS} = 50 V, V_{GS} = 0 V	—	20	250	μA
		T_j = 125 °C, V_{DS} = 50 V, V_{GS} = 0 V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A	—	0.03	0.04	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 15 A	4.0	8.0	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	—	1500	2000	pF
Output Capacitance	C_{oss}		—	750	1100	pF
Reverse Transfer Capacitance	C_{rss}		—	250	400	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	V_{CC} = 30 V, I_D = 3 A, V_{GS} = 10 V, R_{GS} = 50 Ω	—	30	45	ns
	t_r		—	70	110	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$		—	180	230	ns
	t_r		—	130	170	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 1.67		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 75		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	30	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	120	A
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR}, V_{GS} = 0 V, T_j = 25 °C	—	1.7	2.6	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DR}, dI_F/dt = 100 A/μs, V_R = 30 V	—	200	—	ns
Reverse Recovered Charge	Q_{RR}		—	0.25	—	μC

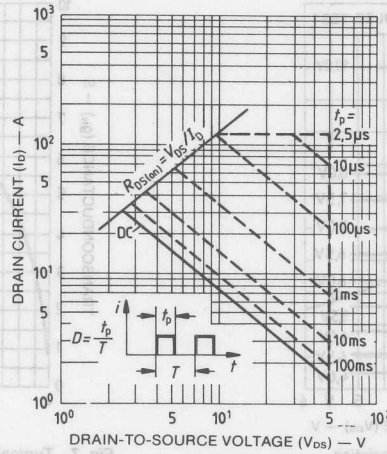


Fig. 1 - Maximum safe operating areas for all types.

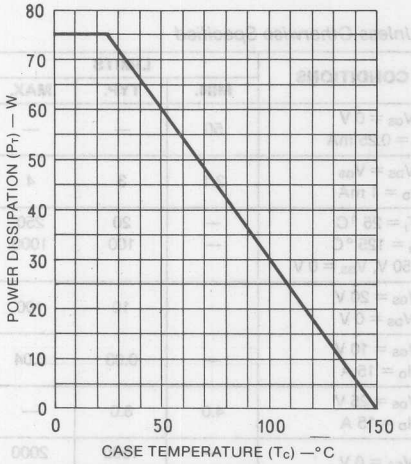


Fig. 2 - Power vs. temperature derating curve for all types.

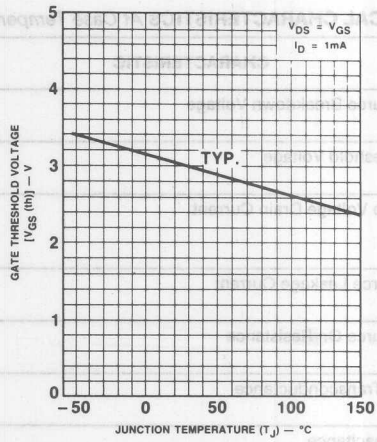


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

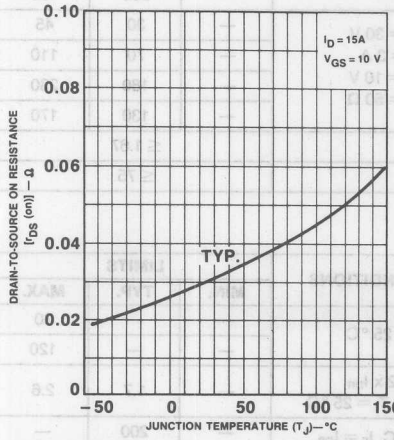


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

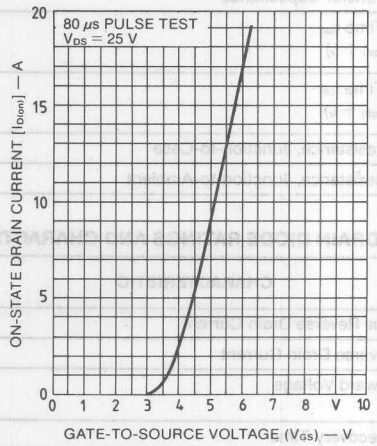


Fig. 5 - Typical transfer characteristics for all types.

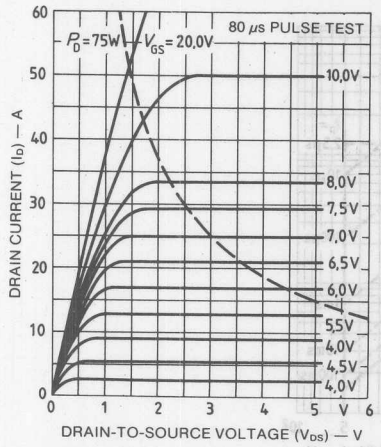


Fig. 6 - Typical output characteristics.

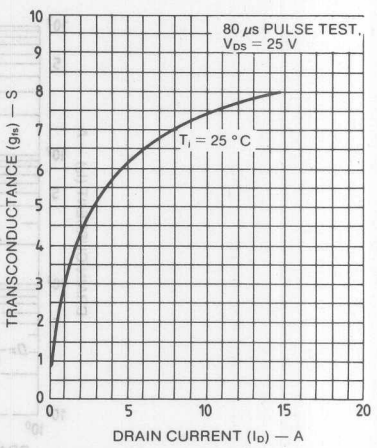


Fig. 7 - Typical transconductance vs. drain current.

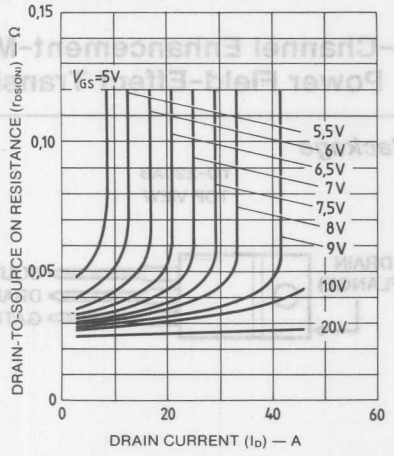


Fig. 8 - Typical on-resistance vs. drain current.

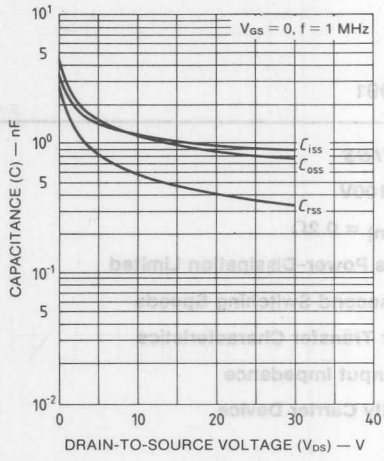


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

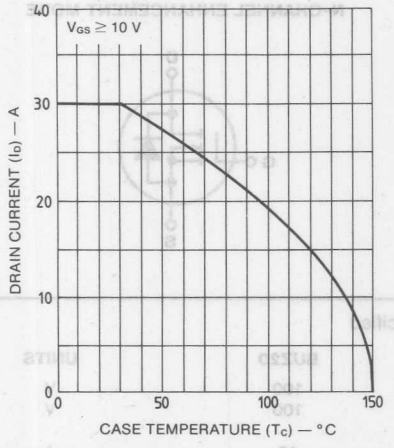


Fig. 10 - Maximum drain current vs. case temperature.

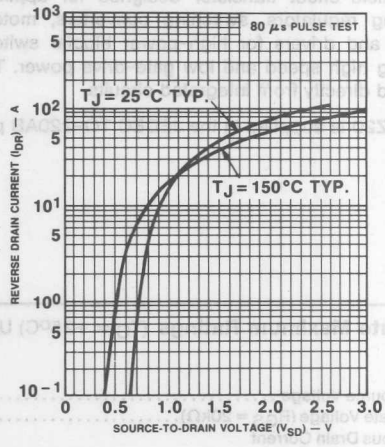


Fig. 11 - Typical source-drain diode forward voltage.

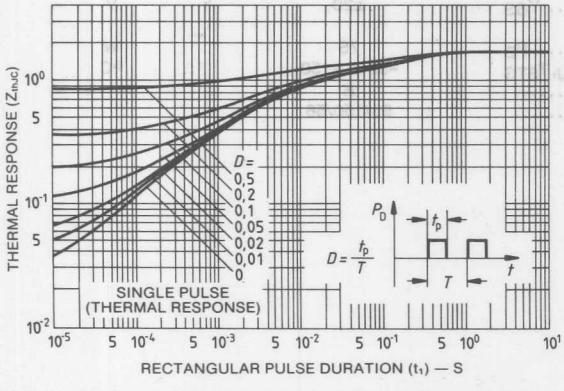


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

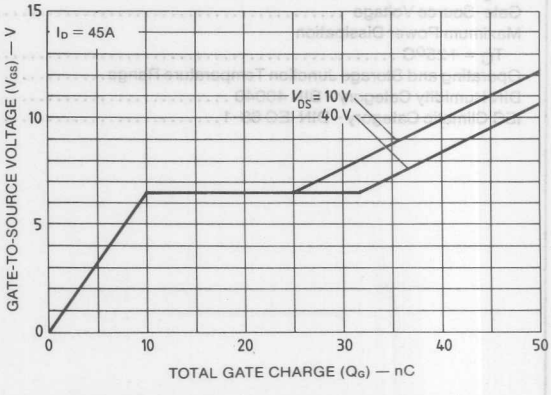


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ20

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 12A, 100V
- $r_{DS(on)} = 0.2\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

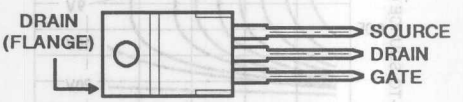
Description

The BUZ20 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ20 is supplied in the JEDEC TO-220AB plastic package.

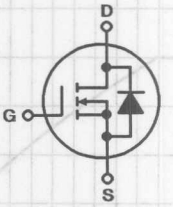
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		BUZ20	UNITS
Drain-Source Voltage	V_{DS}	100	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	100	V
Continuous Drain Current T_C = +30°C	I_D	12	A
Pulsed Drain Current T_C = +25°C	I_{DM}	48	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2254

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	100	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C, V_{DS} = 100 V, V_{GS} = 0 V	—	20	250	μA
		T_j = 125 °C, V_{DS} = 100 V, V_{GS} = 0 V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 6 A	—	0.15	0.2	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 6 A	2.7	4.0	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	—	1500	2000	pF
Output Capacitance	C_{oss}		—	300	500	pF
Reverse Transfer Capacitance	C_{rss}		—	80	140	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	V_{CC} = 30 V, I_D = 2.9 A, V_{GS} = 10 V, R_{GS} = 50 Ω	—	30	45	ns
	t_r		—	50	75	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$		—	110	140	ns
	t_r		—	60	80	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 1.67		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 75		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	12	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	48	A
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR}, V_{GS} = 0 V, T_j = 25 °C	—	1.4	1.8	V
Reverse Recovery Time	t_{rr}	T_j = 25° C, I_F = I_{DR}, dI_F/dt = 100 A/μs, V_R = 30 V	—	200	—	ns
Reverse Recovered Charge	Q_{RR}		—	1.6	—	μC

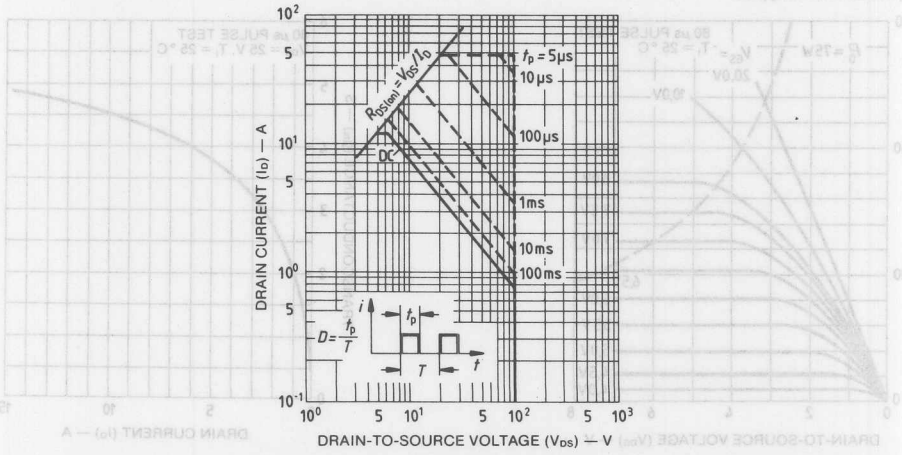


Fig. 1 - Maximum safe operating areas for all types.

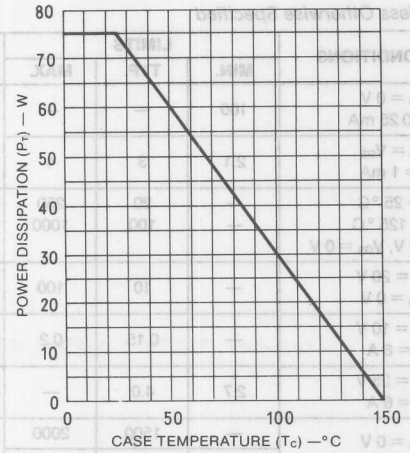


Fig. 2 - Power vs. temperature derating curve for all types.

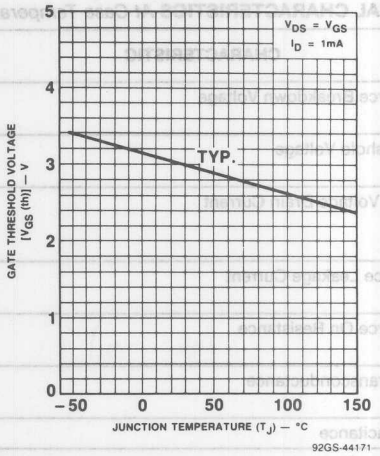


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

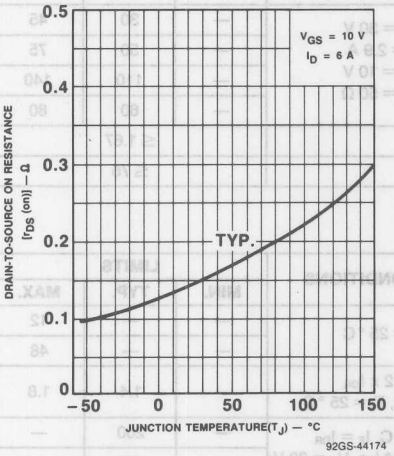


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

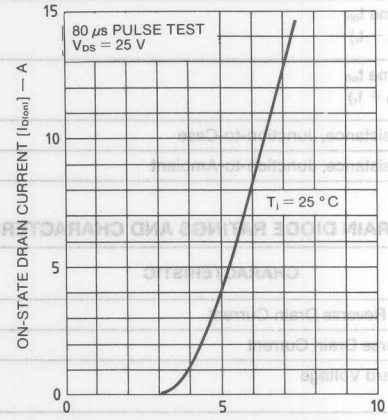


Fig. 5 - Typical transfer characteristics for all types.

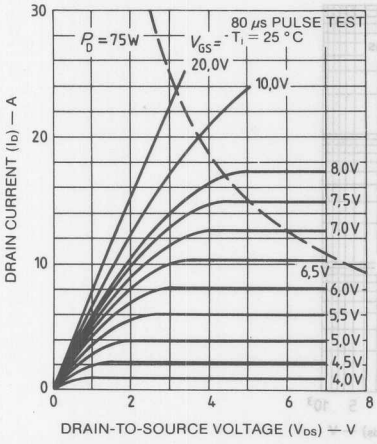


Fig. 6 - Typical output characteristics.

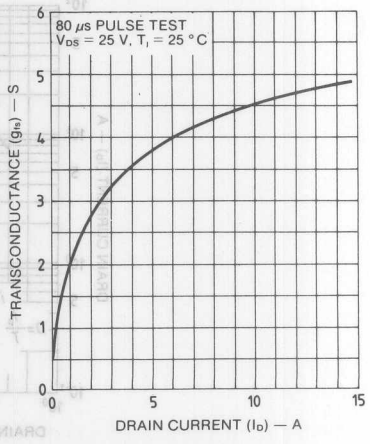


Fig. 7 - Typical transconductance vs. drain current.

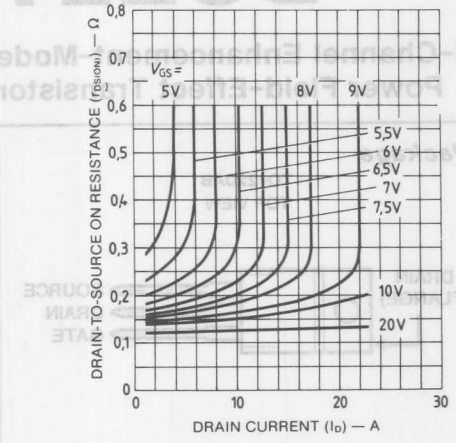


Fig. 8 - Typical on-resistance vs. drain current.

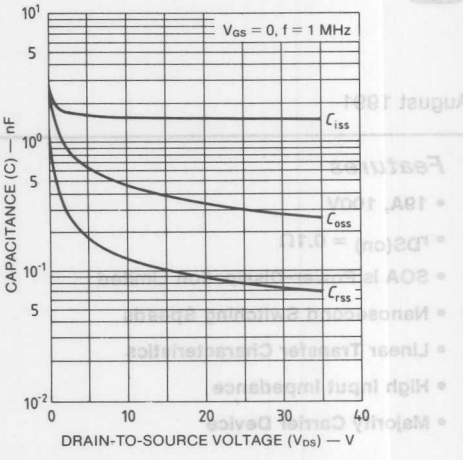


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

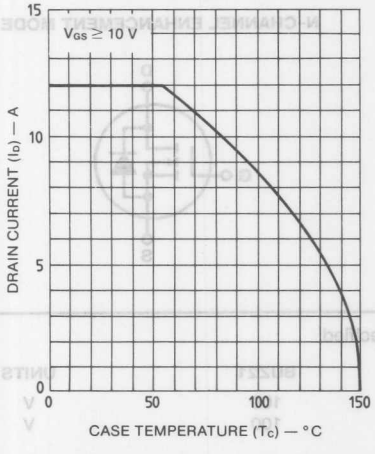


Fig. 10 - Maximum drain current vs. case temperature.

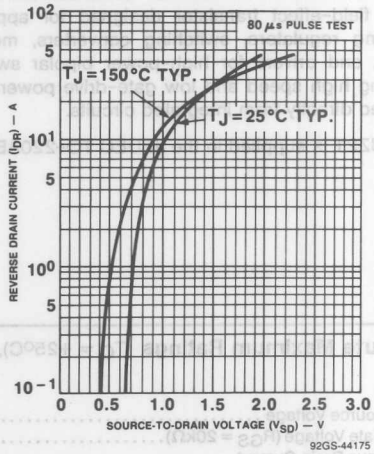


Fig. 11 - Typical source-drain diode forward voltage.

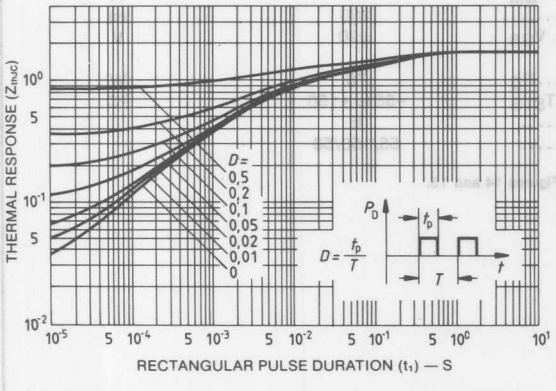


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

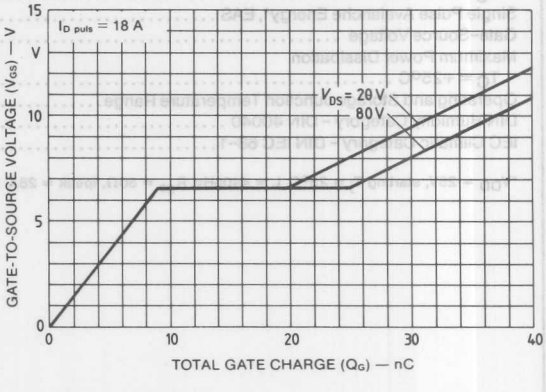


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ21

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 19A, 100V
- $r_{DS(on)} = 0.1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

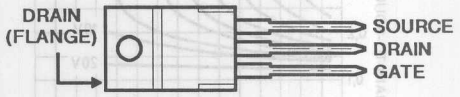
Description

The BUZ21 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ21 is supplied in the JEDEC TO-220AB plastic package.

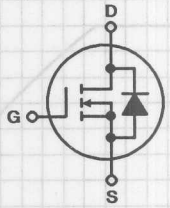
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ21	UNITS
Drain-Source Voltage	V_{DS}	100	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	100	V
Continuous Drain Current T_C = +55°C	I_D	19	A
Pulsed Drain Current T_C = +25°C	I_{DM}	75	A
Single Pulse Avalanche Energy*, EAS		230	mj
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

*V_{DD} = 25V, starting T_j = 25°C, L = 440μHy, R_{gs} = 50Ω, Ipeak = 28A, see Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2420

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C unless otherwise specified.*

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	VGS = 0 V ID = 0.25 mA	100	–	–	V
Gate-Threshold Voltage	VGS(th)	VDS = VGS ID = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	IDSS	Tj = 25°C Tj = 125°C VDS = 100 V, VGS = 0 V	– –	20 100	250 1000	µA
Gate-Source Leakage Current	IGSS	VGS = 20 V VDS = 0 V	–	10	100	nA
Drain-Source on Resistance	rDS(on)	VGS = 10 V ID = 9 A	–	0.09	0.1	Ω
Forward Transconductance	gfs	VDS = 25 V ID = 9 A	4	8	–	S
Input Capacitance	Ciss	VGS = 0 V	–	1500	2000	pF
Output Capacitance	Coss	VDS = 25 V	–	450	700	pF
Reverse Transfer Capacitance	Crss	f = 1 MHZ	–	150	240	pF
Turn-On Time ton	td(on)	Vcc = 30 V	–	30	45	ns
(ton = td(on) + tr)	tr	ID = 3 A	–	50	75	ns
Turn-Off Time toff	td(off)	VGS = 10 V	–	170	220	ns
(toff = td(off) = tr)	tr	RGS = 50 Ω	–	80	110	ns
Thermal Resistance, Junction-to-Case	RθJC			≤ 1.67		°C/W
Thermal Resistance, Junction-to-Ambient	RθJA			≤ 75		°C/W

*VDD = 25 V, starting Tj = 25°C, L = 440 µHy, Rgs = 50 Ω, Ipeak = 28 A, see figure 14 & 15.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	IDR	Tc = 25°C	–	–	19	A
Pulsed Reverse Drain Current	IDRM		–	–	75	A
Diode Forward Voltage	VSD	IF = 2 x IDR VGS = 0 V, Tj = 25°C	–	1.5	2.1	V
Reverse Recovery Time	trr	Tj = 25°C, IF = IDR	–	200	–	ns
Reverse Recovered Charge	QRR	dIF/dt = 100 A/µs, VR = 30 V	–	0.25	–	µC

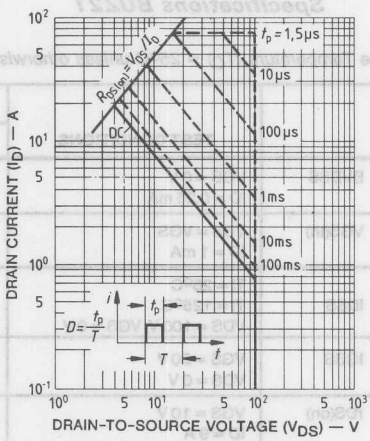


Figure 1 – Maximum safe operating areas for all types.

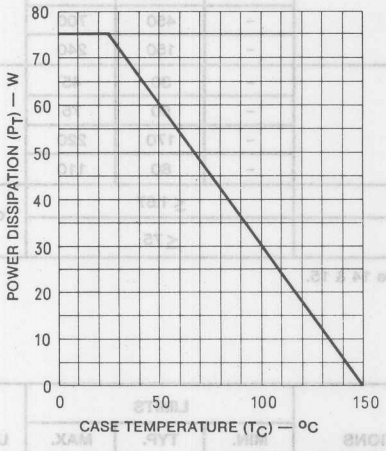


Figure 2 – Power vs temperature derating curve for all types.

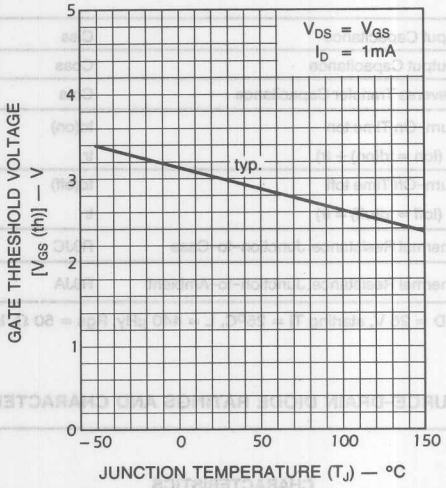


Figure 3 – Normalized gate threshold voltage as a function of junction temperature for all types.

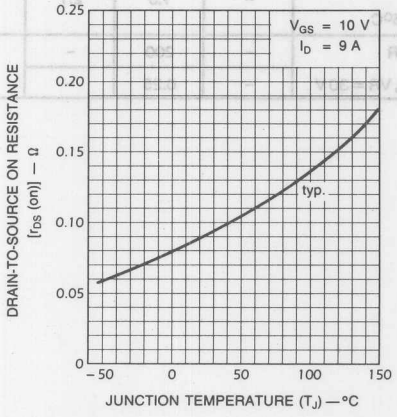


Figure 4 – Normalized drain-to-source on resistance to junction temperature for all types.

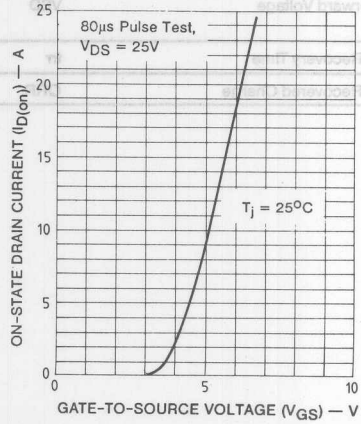


Figure 5 – Typical transfer characteristics for all types.

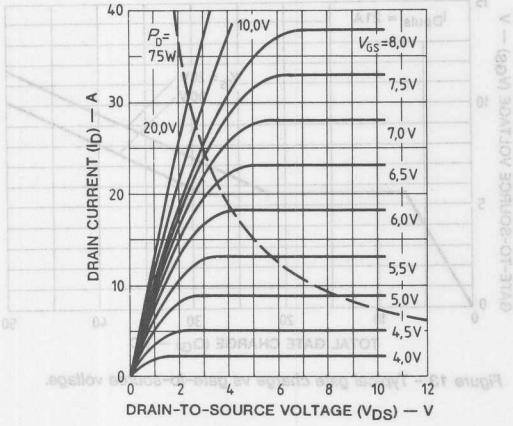


Figure 6 – Typical output characteristics.

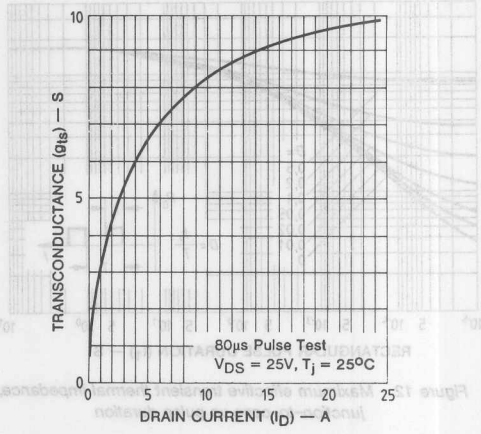


Figure 7 – Typical transconductance vs drain current.

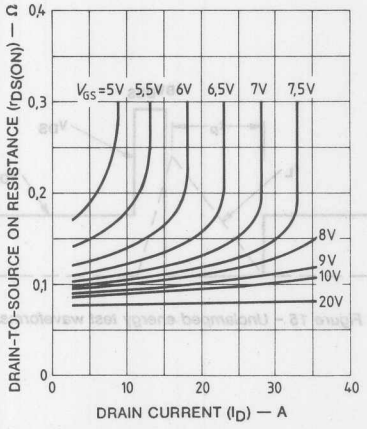


Figure 8 – Typical on-resistance vs drain current.

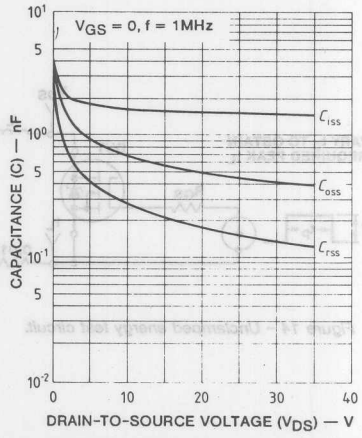


Figure 9 – Typical capacitance vs drain-to-source voltage.

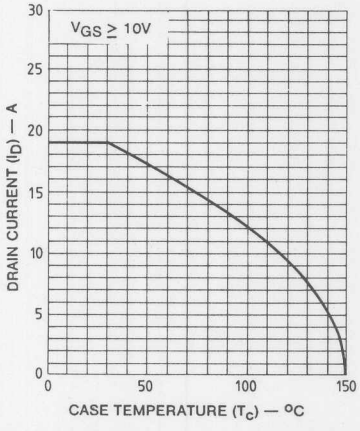


Figure 10 – Maximum drain current vs case temperature.

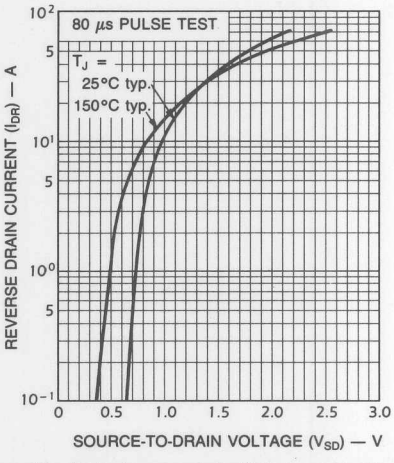


Figure 11 – Typical source-drain diode forward voltage.

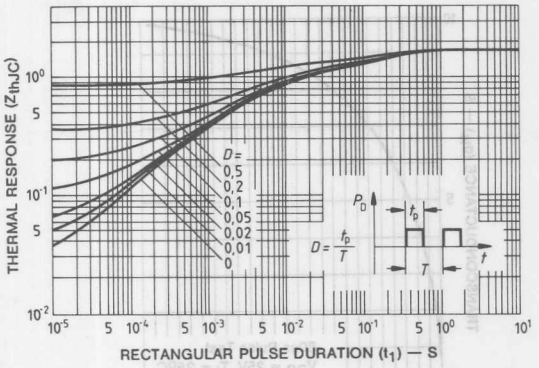


Figure 12 – Maximum effective transient thermal impedance, junction-to-case vs pulse duration

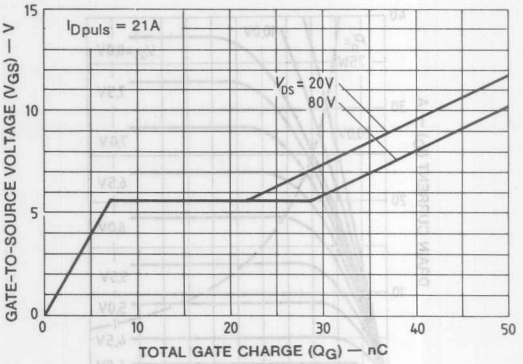


Figure 13 – Typical gate charge vs gate-to-source voltage.

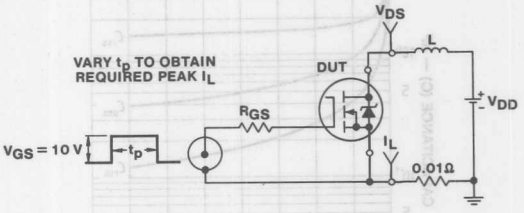


Figure 14 – Unclamped energy test circuit.

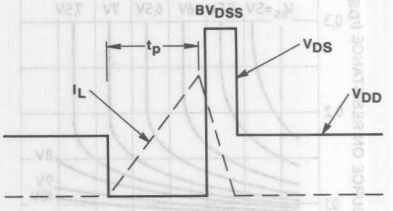


Figure 15 – Unclamped energy test waveforms.

BUZ32

N-Channel Enhancement-Mode Power Field-Effect Transistor

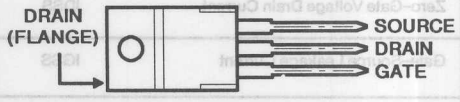
August 1991

Features

- 9.5A, 200V
- $r_{DS(on)} = 0.4\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-220AB
TOP VIEW



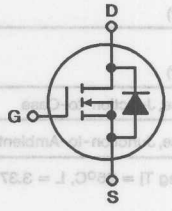
Description

The BUZ32 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ32 is supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4

N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ32	UNITS
Drain-Source Voltage	V_{DS}	200	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	200	V
Continuous Drain Current T_C = +55°C	I_D	9.5	A
Pulsed Drain Current T_C = +25°C	I_{DM}	38	A
Single Pulse Avalanche Energy*, EAS		150	mj
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

*V_{DD} = 20V, starting T_j = 25°C, L = 3.3(μHy, R_{gs} = 50Ω, I_{peak} = 9A, see Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2416

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C unless otherwise specified.*

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain–Source Breakdown Voltage	BVDSS	VGS = 0 V ID = 0.25 mA	200	–	–	V
Gate–Threshold Voltage	VGS(th)	VDS = VGS ID = 1 mA	2.1	3	4	
Zero–Gate Voltage Drain Current	IDSS	Tj = 25°C Tj = 125°C VDS = 200 V, VGS = 0 V	– –	20 100	250 1000	µA
Gate–Source Leakage Current	IGSS	VGS = 20 V VDS = 0 V	–	10	100	nA
Drain–Source on Resistance	rDS(on)	VGS = 10 V ID = 4.5 A	–	0.35	0.4	Ω
Forward Transconductance	gfs	VDS = 25 V ID = 4.5 A	2.2	5.0	–	S
Input Capacitance	Ciss	VGS = 0 V	–	1500	2000	pF
Output Capacitance	Coss	VDS = 25 V	–	250	400	
Reverse Transfer Capacitance	Crss	f = 1 MHZ	–	70	120	
Turn–On Time ton	td(on)	Vcc = 30 V	–	30	45	ns
(ton = td(on) + tr)	tr	ID = 2.9 A	–	40	60	
Turn–Off Time toff	td(off)	VGS = 10 V	–	110	140	
(toff = td(off) = tr)	tr	RGS = 50 Ω	–	60	80	
Thermal Resistance, Junction–to–Case	RθJC			≤ 1.67		°C/W
Thermal Resistance, Junction–to–Ambient	RθJA			≤ 75		

*VDD = 20 V, starting Tj = 25°C, L = 3.37 µHy, Rgs = 50 Ω, Ipeak = 9 A, see figure 14 & 15.

SOURCE–DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	IDR	Tc = 25°C	–	–	9.5	A
Pulsed Reverse Drain Current	IDRM		–	–	38	
Diode Forward Voltage	VSD	IF = 2 x IDR VGS = 0 V, Tj = 25°C	–	1.3	1.7	V
Reverse Recovery Time	trr	Tj = 25°C, IF = IDR	–	400	–	ns
Reverse Recovered Charge	QRR	dIF/dt = 100 A/µs, VR = 100 V	–	6.0	–	µC

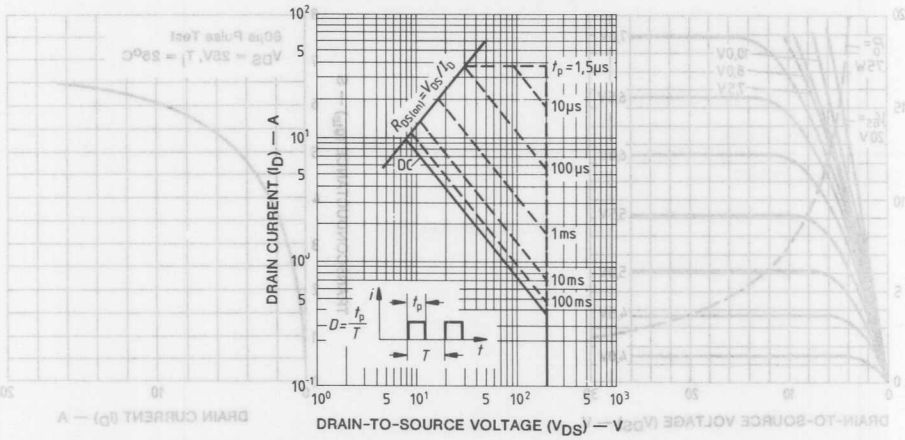


Figure 1 – Maximum safe operating areas for all types.

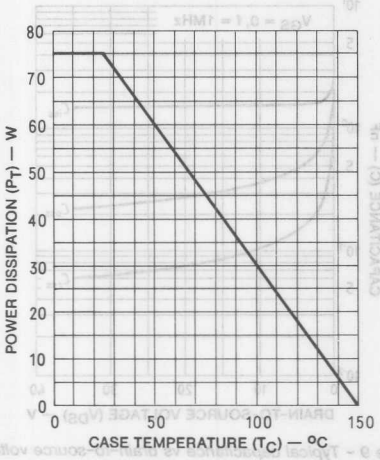


Figure 2 – Power vs temperature derating curve for all types.

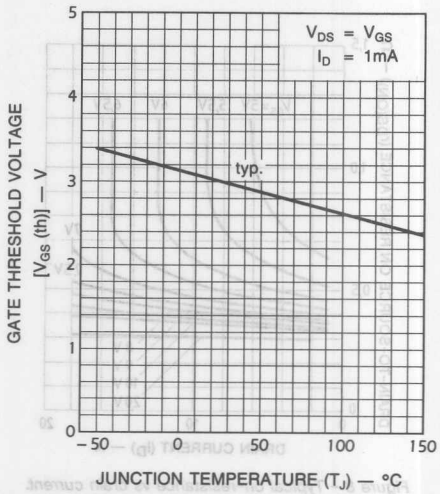


Figure 3 – Normalized gate threshold voltage as a function of junction temperature for all types.

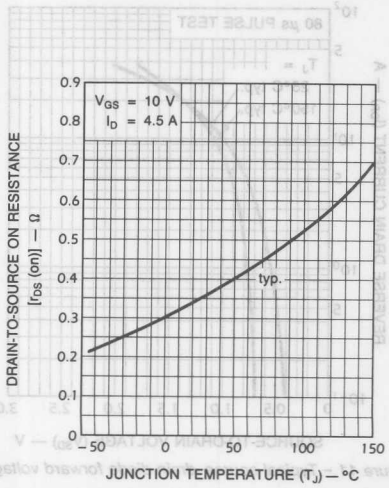


Figure 4 – Normalized drain-to-source on resistance to junction temperature for all types.

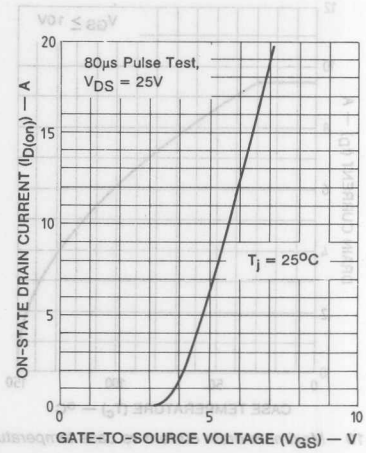


Figure 5 – Typical transfer characteristics for all types.

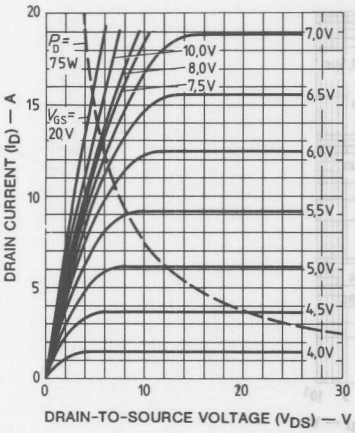


Figure 6 – Typical output characteristics.

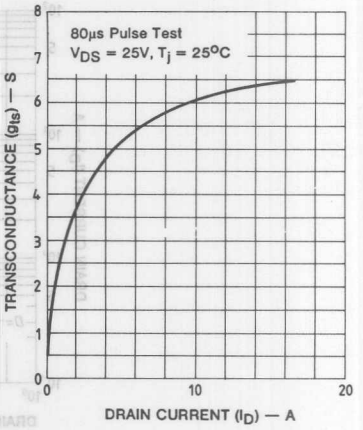


Figure 7 – Typical transconductance vs drain current.

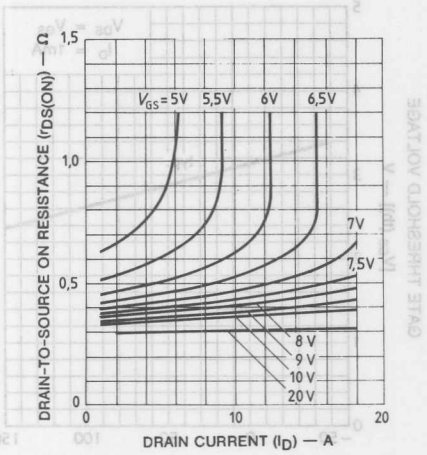


Figure 8 – Typical on-resistance vs drain current.

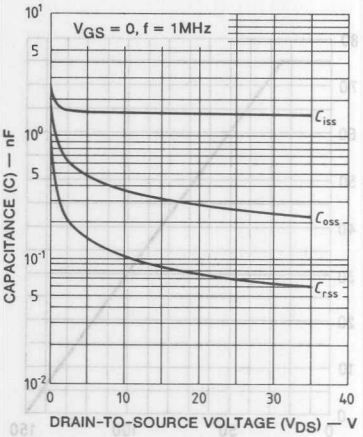


Figure 9 – Typical capacitance vs drain-to-source voltage.

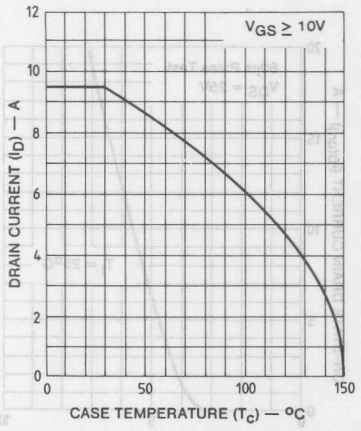


Figure 10 – Maximum drain current vs case temperature.

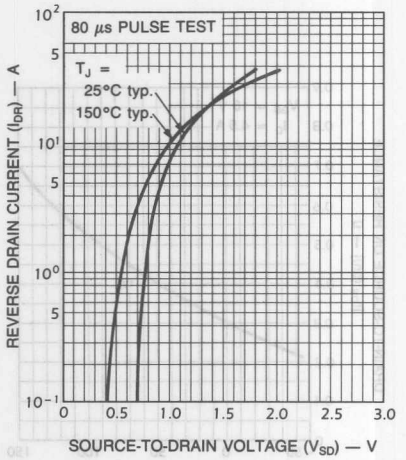


Figure 11 – Typical source-drain diode forward voltage.

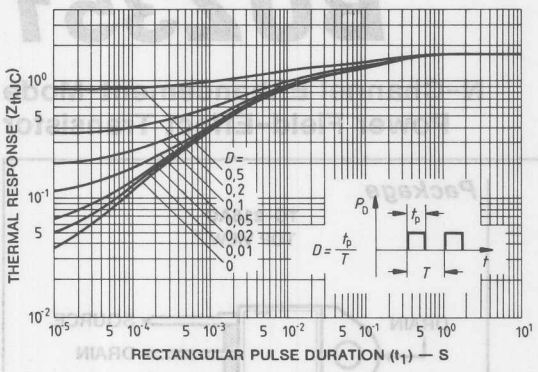


Figure 12 – Maximum effective transient thermal impedance, junction-to-case vs pulse duration

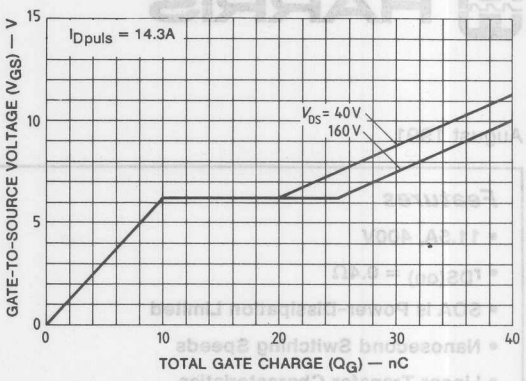


Figure 13 – Typical gate charge vs gate-to-source voltage.

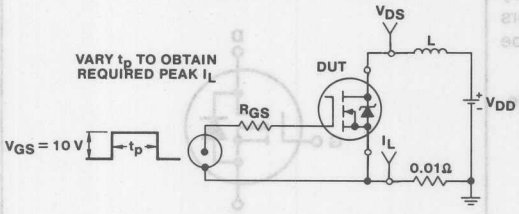


Figure 14 – Unclamped energy test circuit.

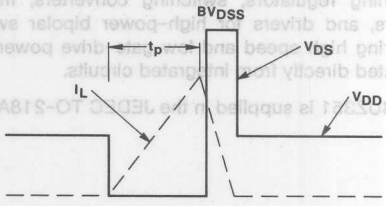


Figure 15 – Unclamped energy test waveforms.

HARRIS

BUZ351

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 11.5A, 400V
- $r_{DS(on)} = 0.4\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

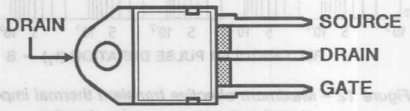
Description

The BUZ351 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ351 is supplied in the JEDEC TO-218AC plastic package.

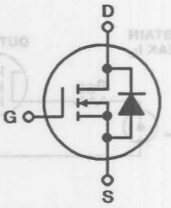
Package

TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ351	UNITS
Drain-Source Voltage	V_{DS}	400	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400	V
Continuous Drain Current T_C = +30°C	I_D	11.5	A
Pulsed Drain Current T_C = +25°C	I_{DM}	46	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	125	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2266

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V, $I_D = 0.25$ mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1$ mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C, $V_{DS} = 400$ V, $V_{GS} = 0$ V	—	20	250	μA
		$T_j = 125$ °C, $V_{DS} = 400$ V, $V_{GS} = 0$ V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V, $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 5.5$ A	—	0.35	0.4	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V, $I_D = 5.5$ A	3.3	4.5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	—	3.8	4.9	nF
Output Capacitance	C_{oss}		—	300	500	pF
Reverse Transfer Capacitance	C_{rss}		—	120	200	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	$V_{CC} = 30$ V, $I_D = 2.9$ A, $V_{GS} = 10$ V, $R_{GS} = 50$ Ω	—	50	75	ns
	t_r		—	80	120	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$		—	330	430	ns
	t_r		—	110	140	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 1		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 45		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	11.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	46	A
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$, $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.3	1.7	V
Reverse Recovery Time	t_{rr}	$T_j = 25$° C, $I_F = I_{DR}$, $dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	1	—	ns
Reverse Recovered Charge	Q_{RR}		—	10	—	μC

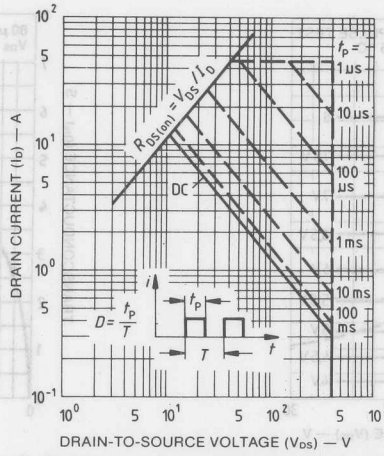


Fig. 1 - Maximum safe operating areas for all types.

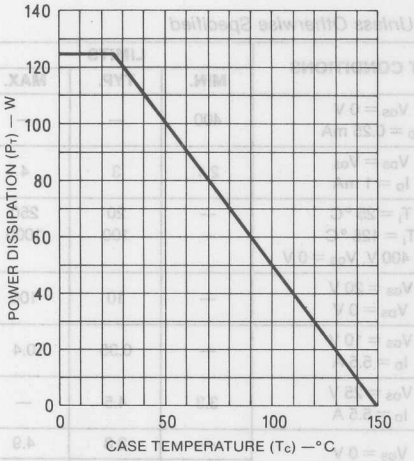


Fig. 2 - Power vs. temperature derating curve for all types.

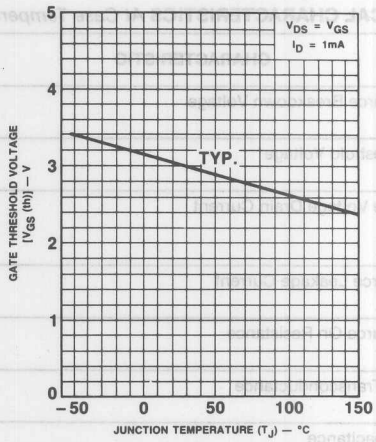


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

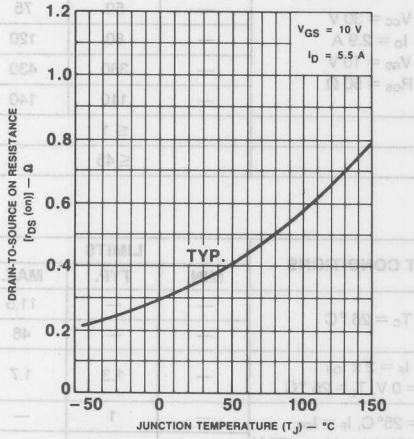


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

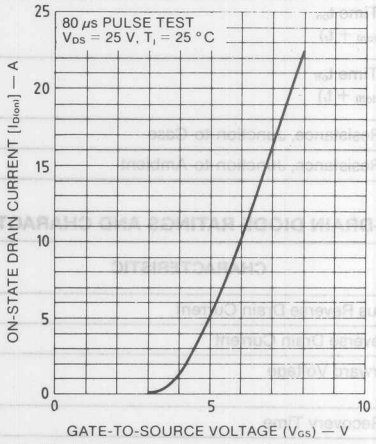


Fig. 5 - Typical transfer characteristics for all types.

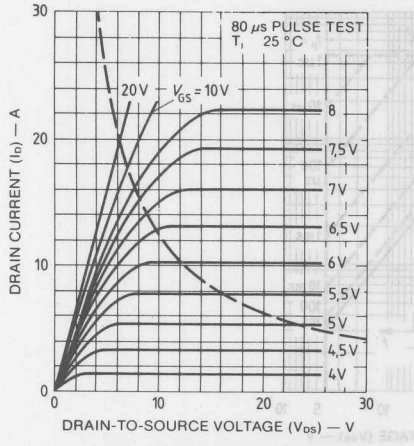


Fig. 6 - Typical output characteristics.

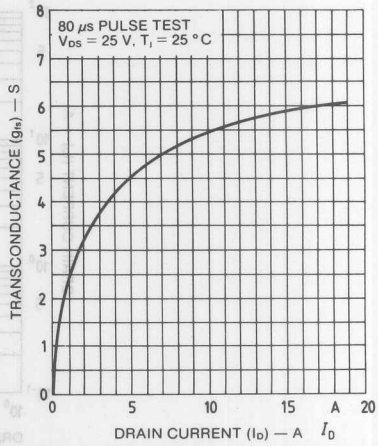


Fig. 7 - Typical transconductance vs. drain current.

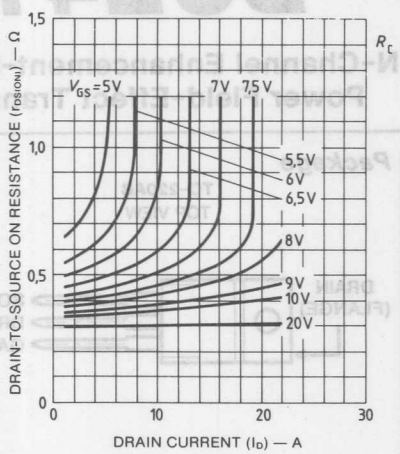


Fig. 8 - Typical on-resistance vs. drain current.

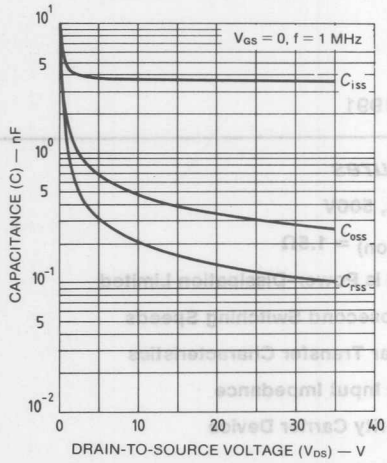


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

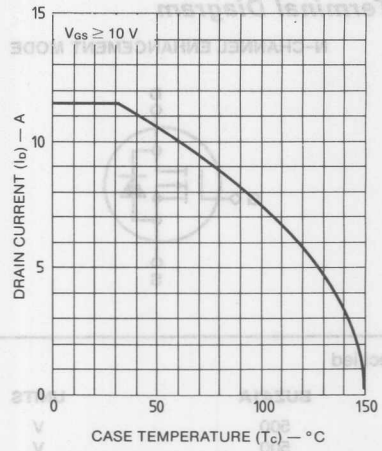


Fig. 10 - Maximum drain current vs. case temperature.

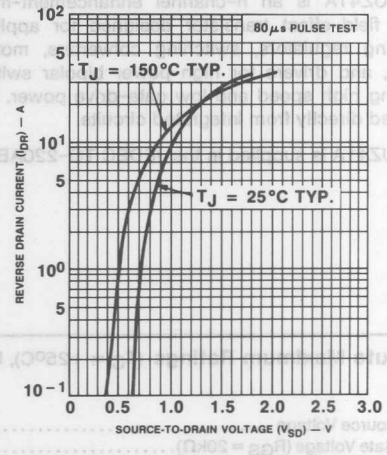


Fig. 11 - Typical source-drain diode forward voltage.

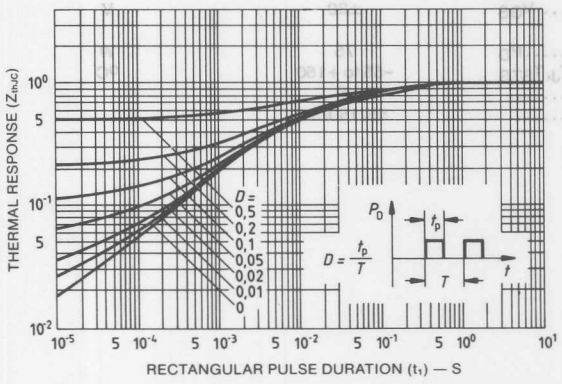


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

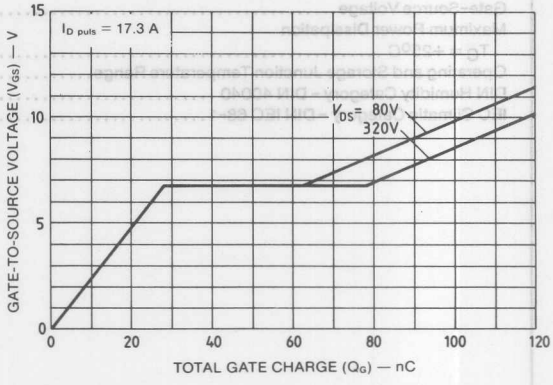


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ41A

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 4.5A, 500V
- $r_{DS(on)} = 1.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

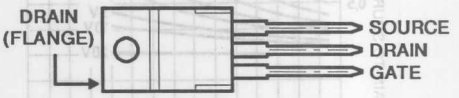
Description

The BUZ41A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ41A is supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ41A	UNITS
Drain-Source Voltage	V_{DS}	500	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500	V
Continuous Drain Current			
T_C = +35°C	I_D	4.5	A
Pulsed Drain Current			
T_C = +25°C	I_{DM}	18	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C, V_{DS} = 500 V, V_{GS} = 0 V	—	20	250	μA
		T_j = 125 °C, V_{DS} = 500 V, V_{GS} = 0 V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 2.5 A	—	1.4	1.5	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 2.5 A	1.5	2.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	—	1500	2000	pF
Output Capacitance	C_{oss}		—	110	170	pF
Reverse Transfer Capacitance	C_{rss}		—	40	70	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	V_{CC} = 30 V, I_D = 2.6 A, V_{GS} = 10 V, R_{GS} = 50 Ω	—	30	45	ns
	t_r		—	40	60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$		—	110	140	ns
	t_r		—	50	65	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 1.67		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 75		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	4.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	18	A
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR}, V_{GS} = 0 V, T_j = 25 °C	—	1.1	1.5	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DR}, dI_F/dt = 100 A/μs, V_R = 100 V	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}		—	6	—	μC

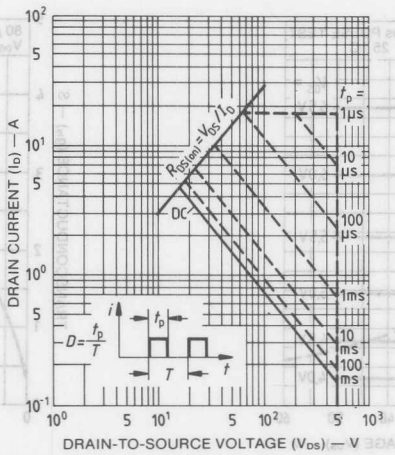


Fig. 1 - Maximum safe operating areas for all types.

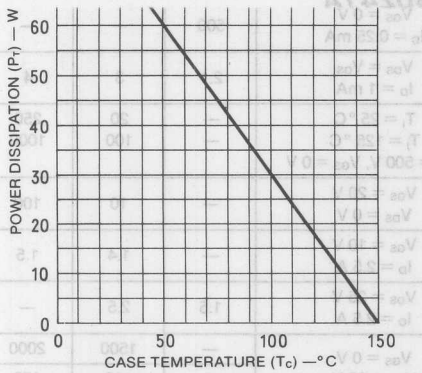


Fig. 2 - Power vs. temperature derating curve for all types.

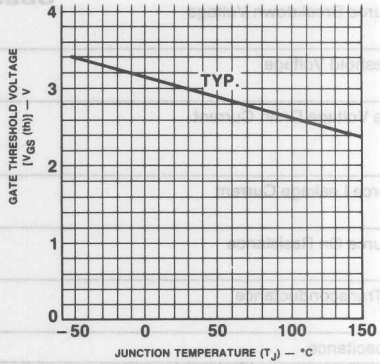


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

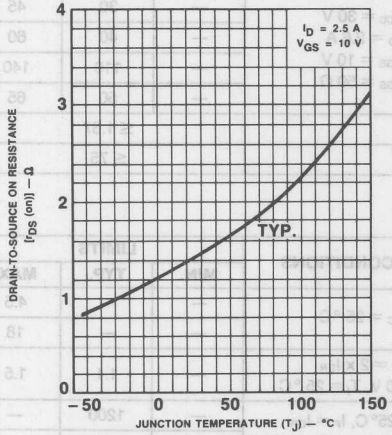


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

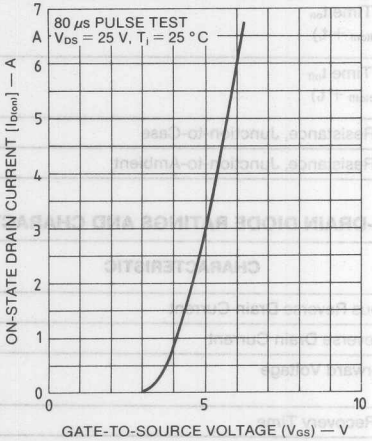


Fig. 5 - Typical transfer characteristics for all types.

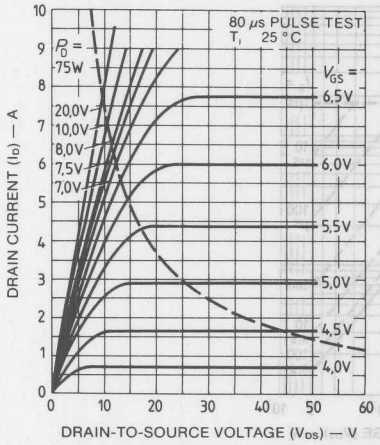


Fig. 6 - Typical output characteristics.

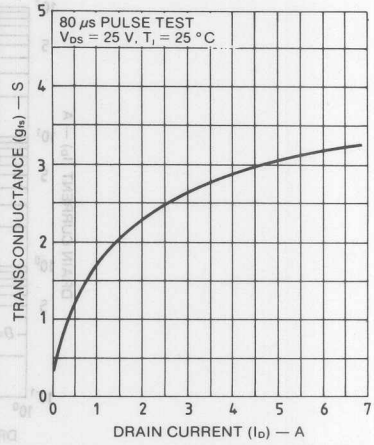


Fig. 7 - Typical transconductance vs. drain current.

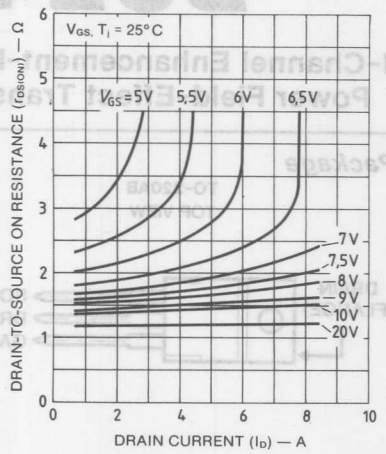


Fig. 8 - Typical on-resistance vs. drain current.

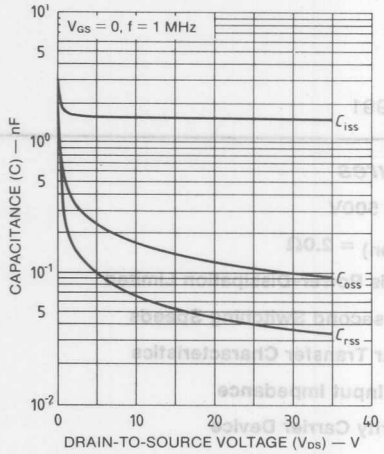


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

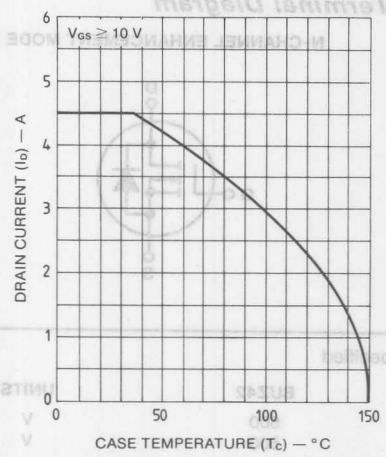


Fig. 10 - Maximum drain current vs. case temperature.

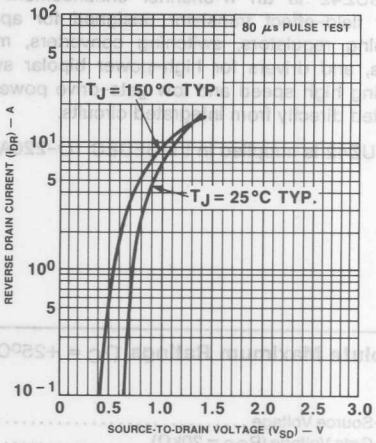


Fig. 11 - Typical source-drain diode forward voltage.

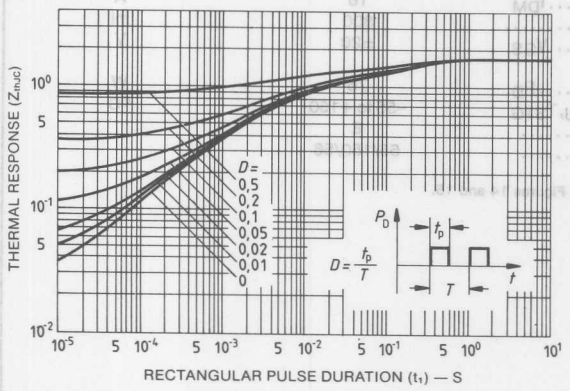


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

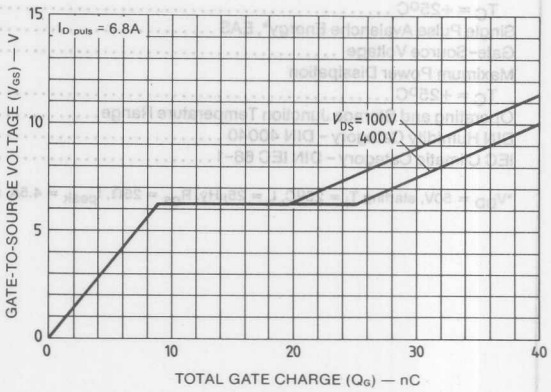


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

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BUZ42

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 4.0A, 500V
- $r_{DS(on)} = 2.0\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

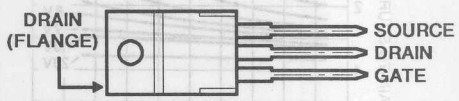
Description

The BUZ42 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ42 is supplied in the JEDEC TO-220AB plastic package.

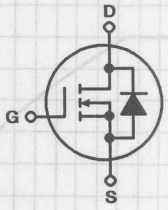
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ42	UNITS
Drain-Source Voltage	V_{DS}	500	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500	V
Continuous Drain Current T_C = +55°C	I_D	40	A
Pulsed Drain Current T_C = +25°C	I_{DM}	16	A
Single Pulse Avalanche Energy*, EAS		300	mj
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

*V_{DD} = 50V, starting T_j = 25°C, L = 25μHy, R_{gs} = 25Ω, I_{peak} = 4.5A, see Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2417

Specifications BUZ42

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C unless otherwise specified.*

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	VGS = 0 V ID = 0.25 mA	500	–	–	V
Gate-Threshold Voltage	VGS(th)	VDS = VGS ID = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	IDSS	Tj = 25°C Tj = 125°C VDS = 500 V, VGS = 0 V	– –	20 100	250 1000	µA
Gate-Source Leakage Current	IGSS	VGS = 20 V VDS = 0 V	–	10	100	nA
Drain-Source on Resistance	rDS(on)	VGS = 10 V ID = 2.5 A	–	1.6	2.0	Ω
Forward Transconductance	gfs	VDS = 25 V ID = 2.5 A	1.5	2.5	–	S
Input Capacitance	Ciss	VGS = 0 V	–	1500	2000	pF
Output Capacitance	Coss	VDS = 25 V	–	110	170	pF
Reverse Transfer Capacitance	Crss	f = 1 MHZ	–	40	70	pF
Turn-On Time ton	td(on)	Vcc = 30 V	–	30	45	ns
(ton = td(on) + tr)	tr	ID = 2.5 A	–	40	60	ns
Turn-Off Time toff	td(off)	VGS = 10 V	–	110	140	ns
(toff = td(off) = tr)	tr	RGS = 50 Ω	–	50	65	ns
Thermal Resistance, Junction-to-Case	RθJC			≤ 1.67		°C/W
Thermal Resistance, Junction-to-Ambient	RθJA			≤ 75		°C/W

*VDD = 50 V, starting Tj = 25°C, L = 25 µHy, Rgs = 25Ω, Ipeak = 4.5 A, see figure 14 & 15.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	IDR	Tc = 25°C	–	–	4.0	A
Pulsed Reverse Drain Current	IDRM		–	–	16	A
Diode Forward Voltage	VSD	IF = 2 x IDR VGS = 0 V, Tj = 25°C	–	1.1	1.5	V
Reverse Recovery Time	trr	Tj = 25°C, IF = IDR	–	1200	–	ns
Reverse Recovered Charge	QRR	dIF/dt = 100 A/µs, VR = 100 V	–	6.0	–	µC

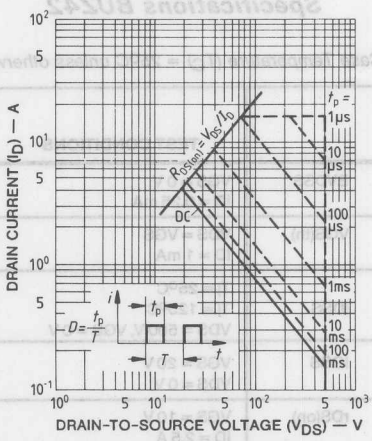


Figure 1 – Maximum safe operating areas for all types.

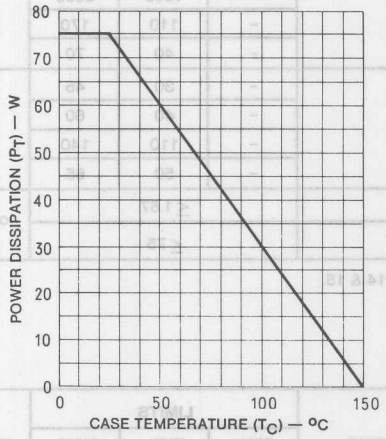


Figure 2 – Power vs temperature derating curve for all types.

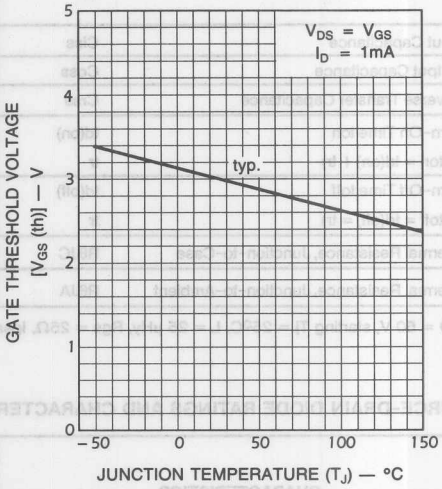


Figure 3 – Normalized gate threshold voltage as a function of junction temperature for all types.

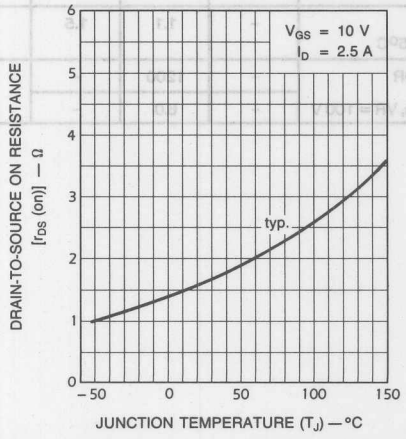


Figure 4 – Normalized drain-to-source on resistance to junction temperature for all types.

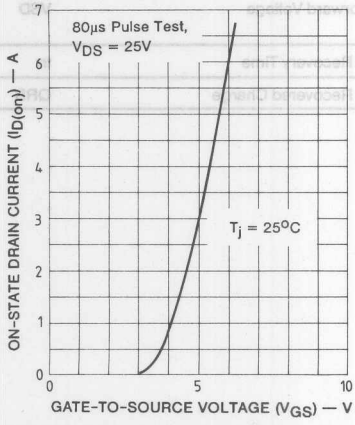


Figure 5 – Typical transfer characteristics for all types.

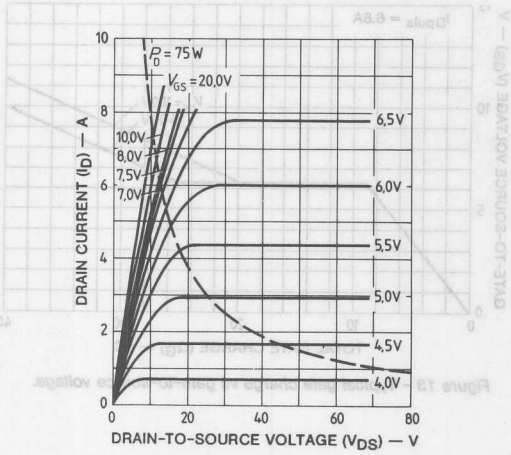


Figure 6 - Typical output characteristics.

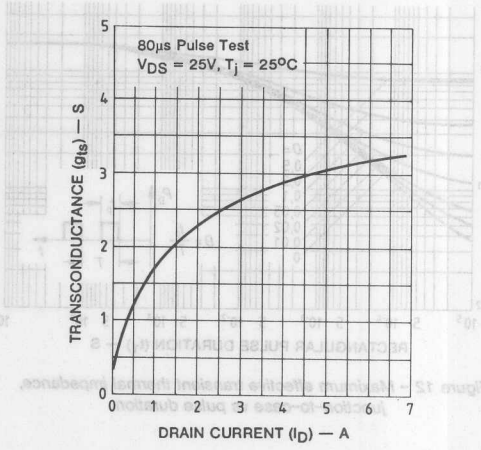


Figure 7 - Typical transconductance vs drain current.

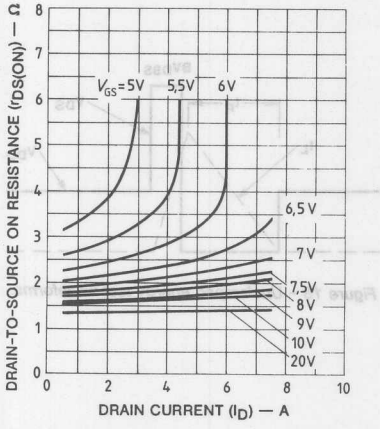


Figure 8 - Typical on-resistance vs drain current.

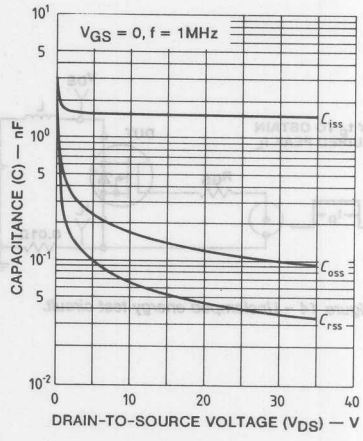


Figure 9 - Typical capacitance vs drain-to-source voltage.

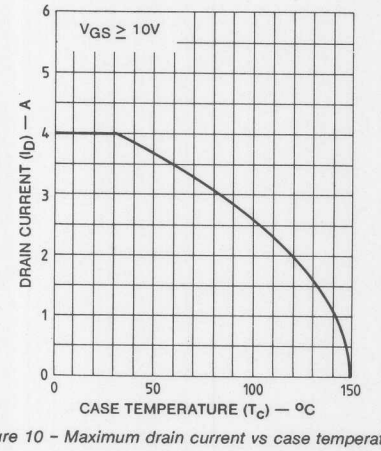


Figure 10 - Maximum drain current vs case temperature.

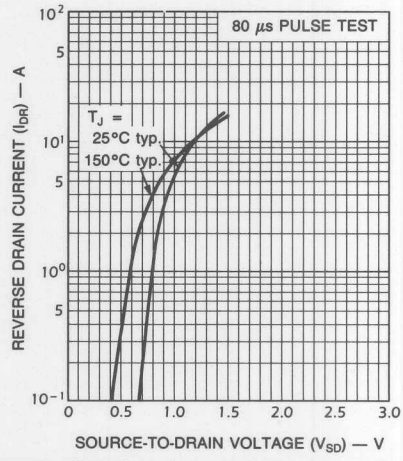


Figure 11 - Typical source-drain diode forward voltage.

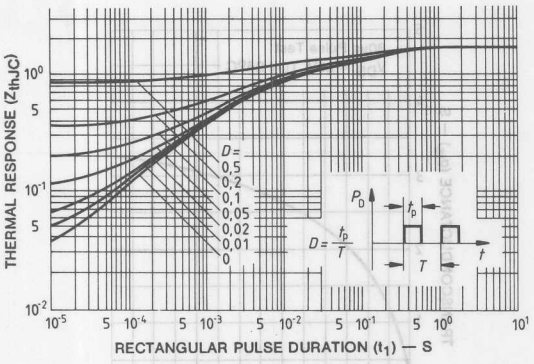


Figure 12 – Maximum effective transient thermal impedance, junction-to-case vs pulse duration

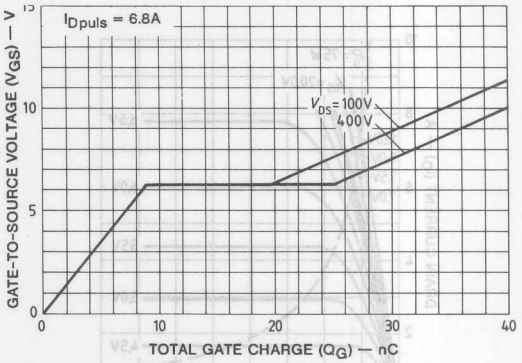


Figure 13 – Typical gate charge vs gate-to-source voltage.

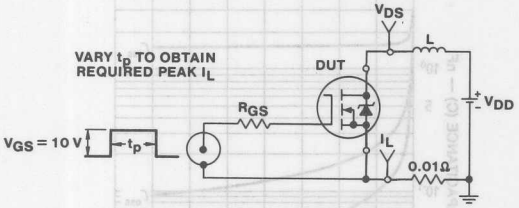


Figure 14 – Unclamped energy test circuit.

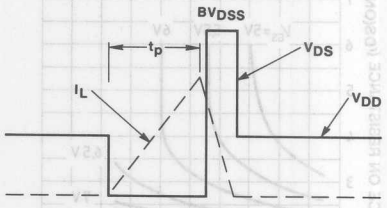


Figure 15 – Unclamped energy test waveforms.

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BUZ45

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 9.6A, 500V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

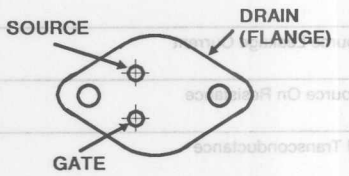
Description

The BUZ45 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ45 is supplied in the JEDEC TO-204AA plastic package.

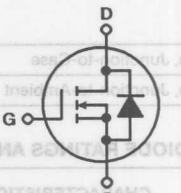
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		BUZ45	UNITS
Drain-Source Voltage	V_{DS}	500	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500	V
Continuous Drain Current			
T_C = +25°C	I_D	9.6	A
Pulsed Drain Current			
T_C = +25°C	I_{DM}	38	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	125	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2257

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C, V_{DS} = 500 V, V_{GS} = 0 V	—	20	250	μA
		T_j = 125 °C, V_{DS} = 500 V, V_{GS} = 0 V	—	100	1000	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A	—	0.55	0.6	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 5 A	2.7	5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	—	3800	4900	pF
Output Capacitance	C_{oss}		—	250	400	
Reverse Transfer Capacitance	C_{rss}		—	100	170	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	V_{CC} = 30 V, I_D = 2.8 A, V_{GS} = 10 V, R_{GS} = 50 Ω	—	50	75	ns
	t_r		—	80	120	
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$		—	330	430	
	t_r		—	110	140	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 35			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	9.6	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	38	
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR}, V_{GS} = 0 V, T_j = 25 °C	—	1.3	1.7	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DR}, dI_F/dt = 100 A/μs, V_R = 100 V	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}		—	12	—	μC

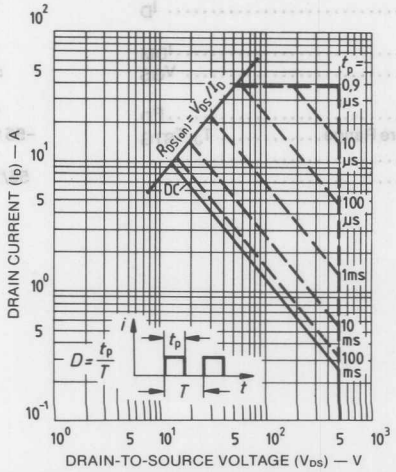


Fig. 1 - Maximum safe operating areas for all types.

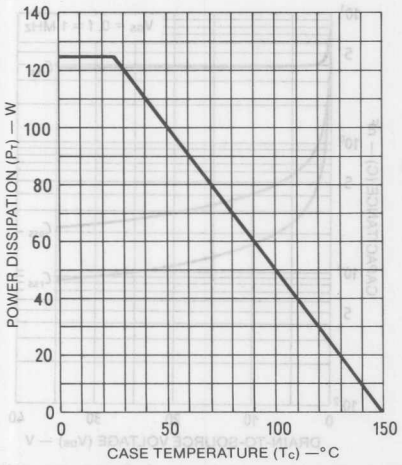


Fig. 2 - Power vs. temperature derating curve for all types.

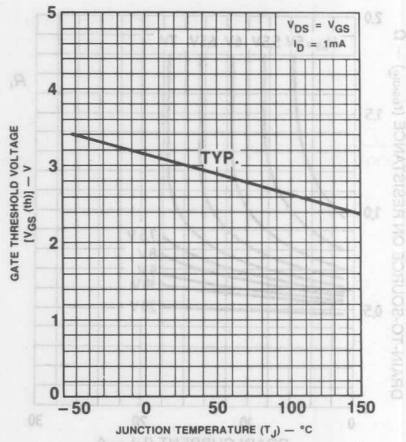


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

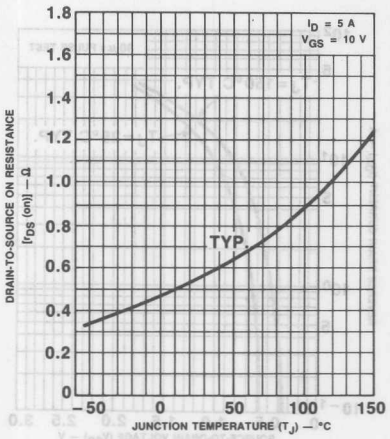


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

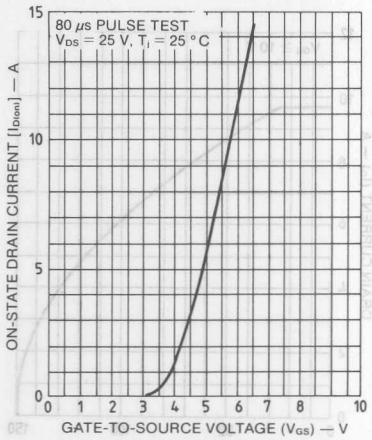


Fig. 5 - Typical transfer characteristics for all types.

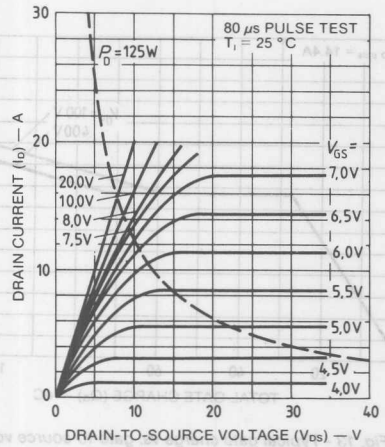


Fig. 6 - Typical output characteristics.

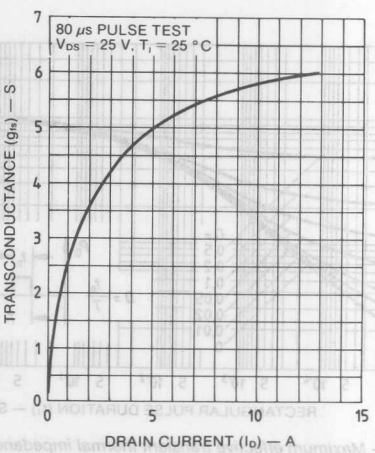


Fig. 7 - Typical transconductance vs. drain current.

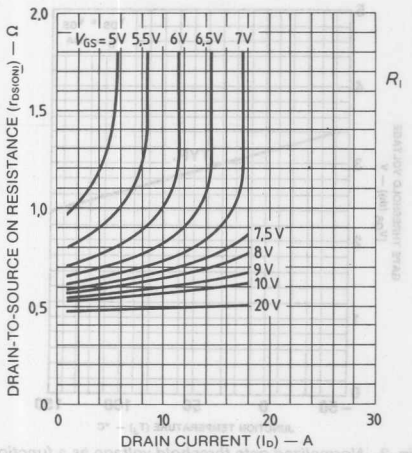


Fig. 8 - Typical on-resistance vs. drain current.

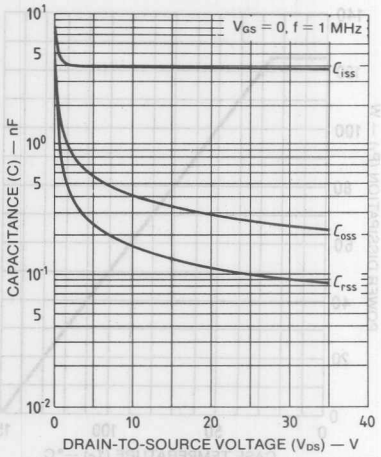


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

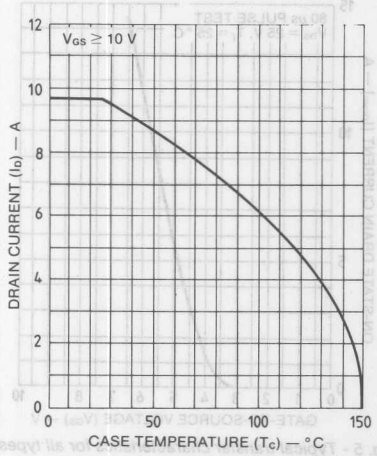


Fig. 10 - Maximum drain current vs. case temperature.

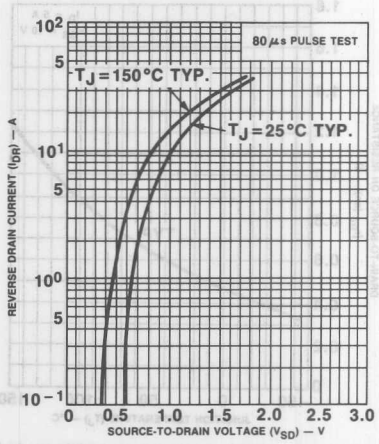


Fig. 11 - Typical source-drain diode forward voltage.

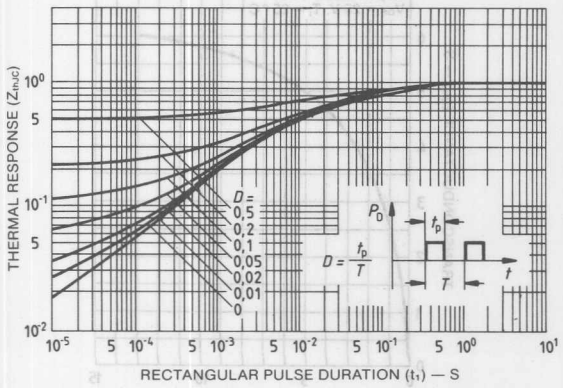


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

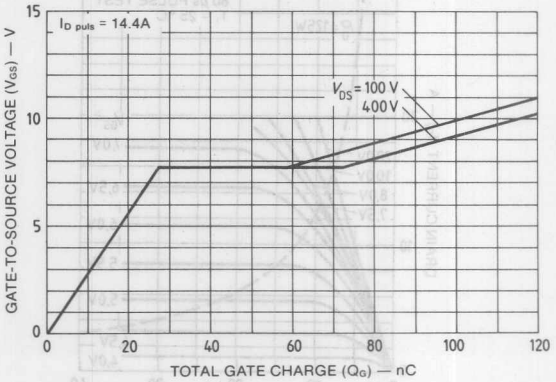


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ45A

August 1991

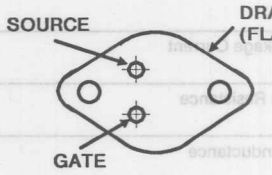
N-Channel Enhancement-Mode Power Field-Effect Transistor

Features

- 8.3A, 500V
- $r_{DS(on)} = 0.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AA
BOTTOM VIEW



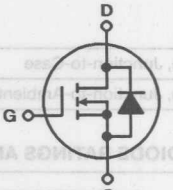
Description

The BUZ45A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ45A is supplied in the JEDEC TO-204AA plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4

N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ45A	UNITS
Drain-Source Voltage	V_{DS}	500	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500	V
Continuous Drain Current			
T_C = +25°C	I_D	8.3	A
Pulsed Drain Current			
T_C = +25°C	I_{DM}	33	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	125	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2258

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C, V_{DS} = 500 V, V_{GS} = 0 V	—	20	250	μA
		T_j = 125 °C, V_{DS} = 500 V, V_{GS} = 0 V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A	—	0.7	0.8	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 5 A	2.7	5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	—	3800	4900	pF
Output Capacitance	C_{oss}		—	250	400	pF
Reverse Transfer Capacitance	C_{rss}		—	100	170	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	V_{CC} = 30 V, I_D = 2.8 A, V_{GS} = 10 V, R_{GS} = 50 Ω	—	50	75	ns
	t_r		—	80	120	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$		—	330	430	ns
	t_f		—	110	140	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 1		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 35		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	8.3	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	33	A
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR}, V_{GS} = 0 V, T_j = 25 °C	—	1.3	1.6	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DR}, dI_F/dt = 100 A/μs, V_R = 100 V	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}		—	12	—	μC

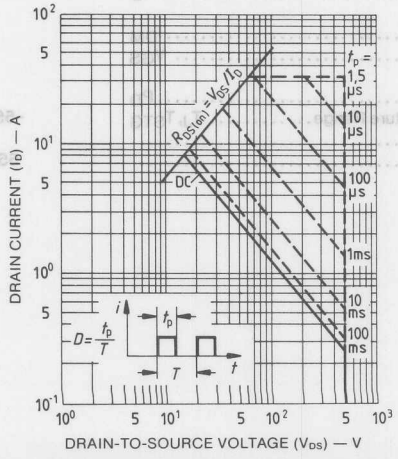


Fig. 1 - Maximum safe operating areas for all types.

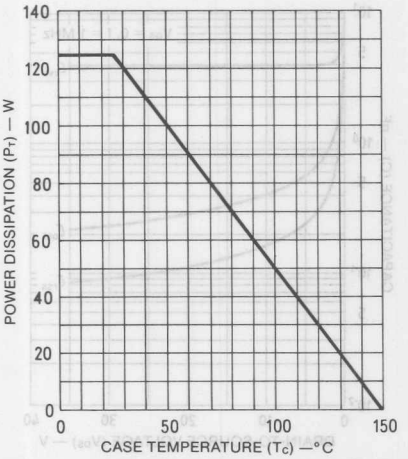


Fig. 2 - Power vs. temperature derating curve for all types.

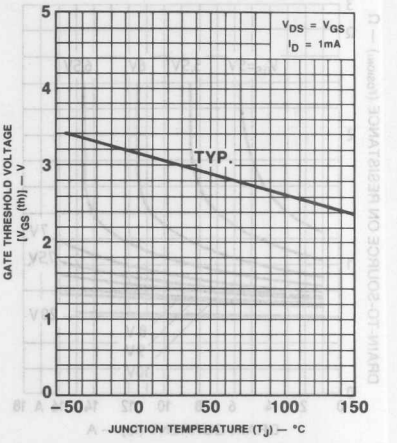


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

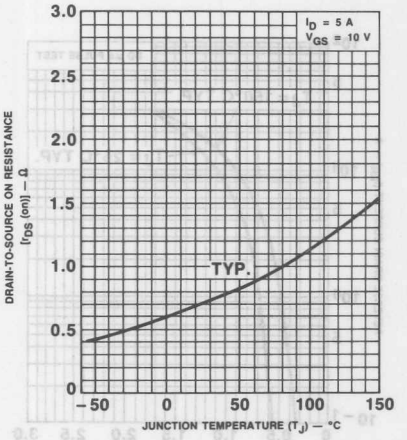


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

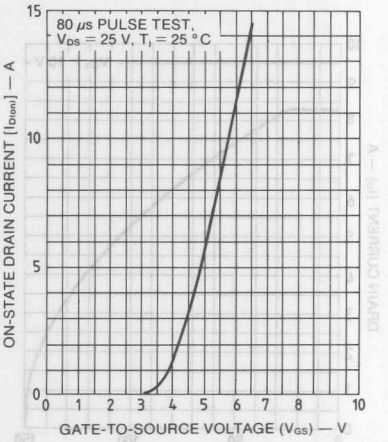


Fig. 5 - Typical transfer characteristics for all types.

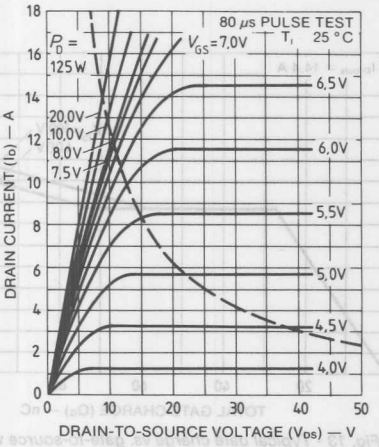


Fig. 6 - Typical output characteristics.

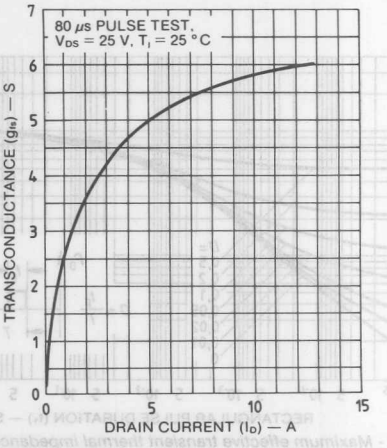


Fig. 7 - Typical transconductance vs. drain current.

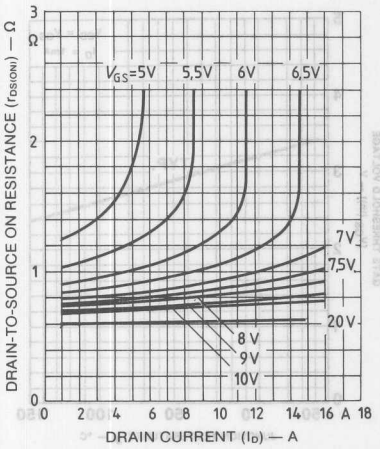


Fig. 8 - Typical on-resistance vs. drain current.

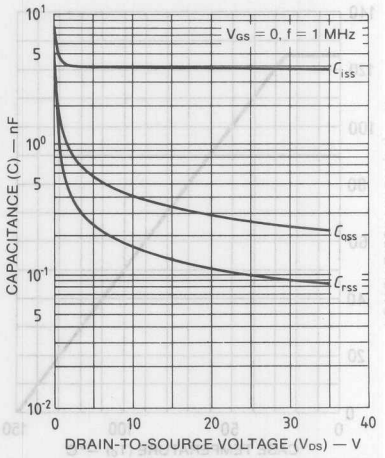


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

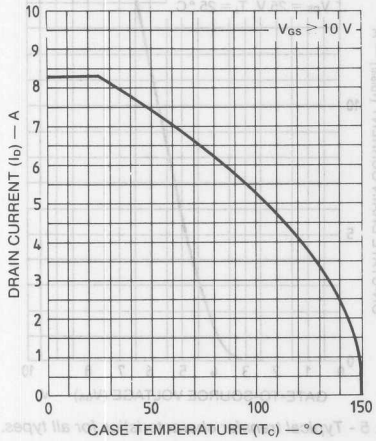


Fig. 10 - Maximum drain current vs. case temperature.

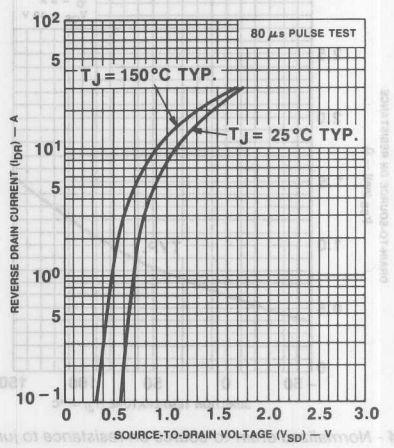


Fig. 11 - Typical source-drain diode forward voltage.

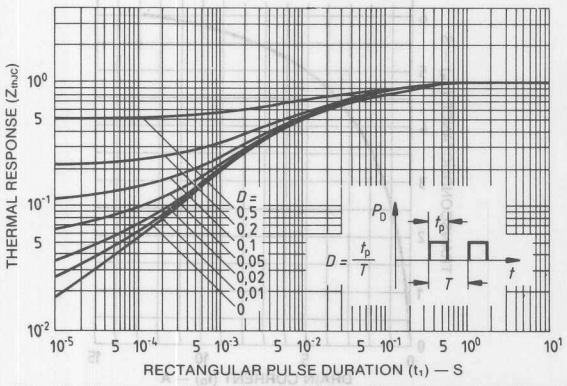


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

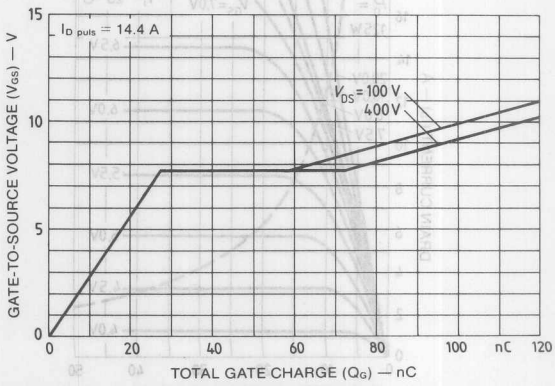


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ45B

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 10A, 500V
- $r_{DS(on)} = 0.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

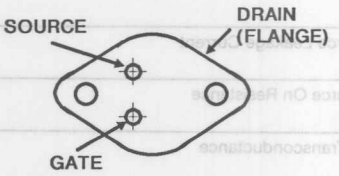
Description

The BUZ45B is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ45B is supplied in the JEDEC TO-204AA plastic package.

Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4

N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		BUZ45B	UNITS
Drain-Source Voltage	V_{DS}	500	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500	V
Continuous Drain Current T_C = +35°C	I_D	10	A
Pulsed Drain Current T_C = +25°C	I_{DM}	40	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	125	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2259**

Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V, $I_D = 0.25$ mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1$ mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C, $V_{DS} = 500$ V, $V_{GS} = 0$ V	—	20	250	μA
		$T_j = 125$ °C, $V_{DS} = 500$ V, $V_{GS} = 0$ V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V, $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 5$ A	—	0.49	0.50	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V, $I_D = 5$ A	2.7	5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1$ MHz	—	3800	4900	pF
Output Capacitance	C_{oss}		—	250	400	pF
Reverse Transfer Capacitance	C_{rss}		—	100	170	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	$V_{CC} = 30$ V, $I_D = 2.9$ A, $V_{GS} = 10$ V, $R_{GS} = 50$ Ω	—	50	75	ns
	t_r		—	80	120	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$		—	330	430	ns
	t_r		—	110	140	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 1		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 35		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	10	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	40	A
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$, $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.3	1.7	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$, $dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}		—	12	—	μC

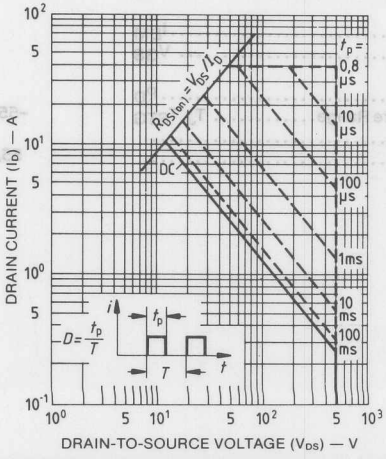


Fig. 1 - Maximum safe operating areas for all types.

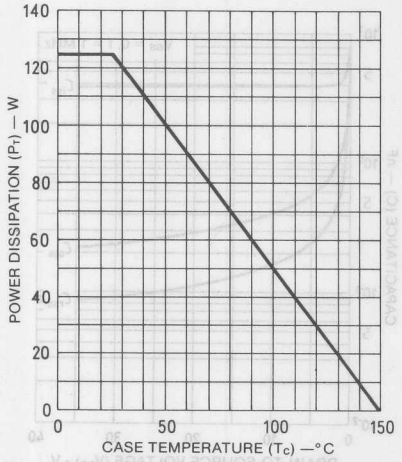


Fig. 2 - Power vs. temperature derating curve for all types.

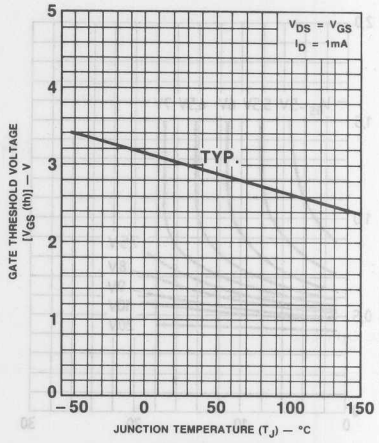


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

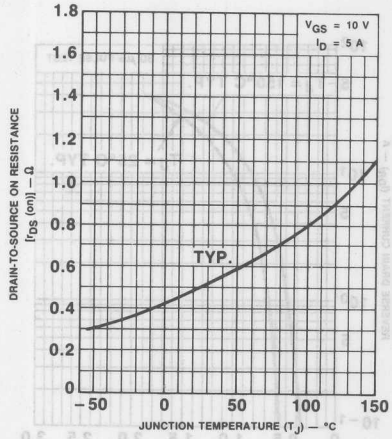


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

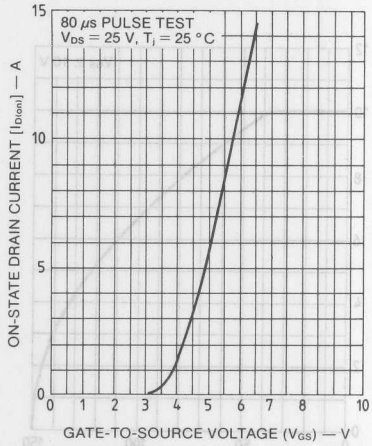


Fig. 5 - Typical transfer characteristics for all types.

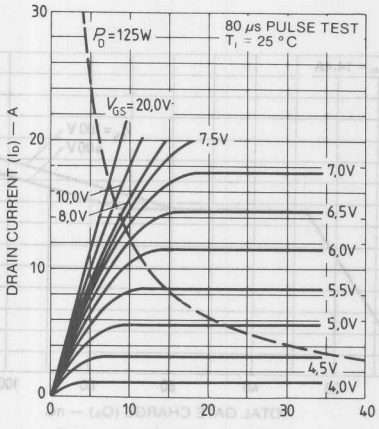


Fig. 6 - Typical output characteristics.

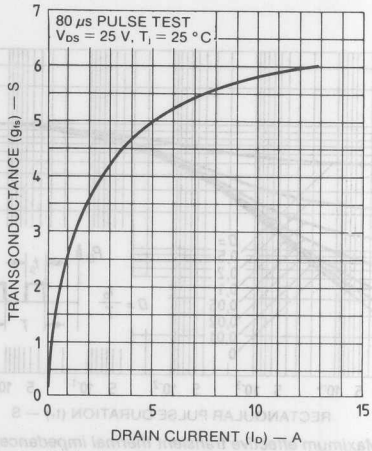


Fig. 7 - Typical transconductance vs. drain current.

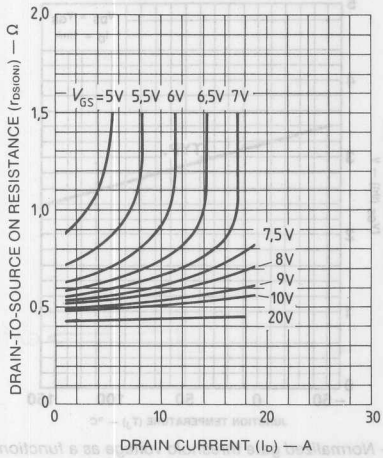


Fig. 8 - Typical on-resistance vs. drain current.

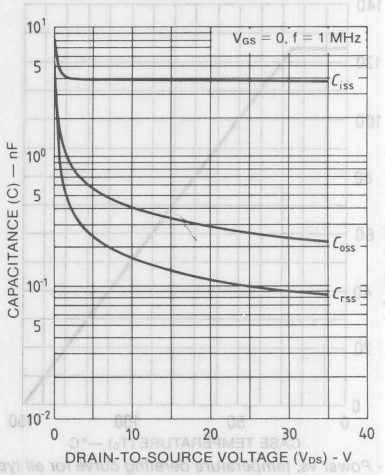


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

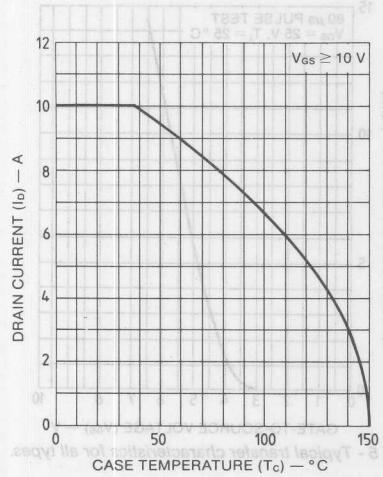


Fig. 10 - Maximum drain current vs. case temperature.

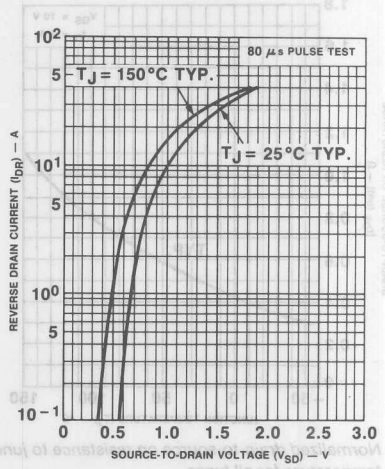


Fig. 11 - Typical source-drain diode forward voltage.

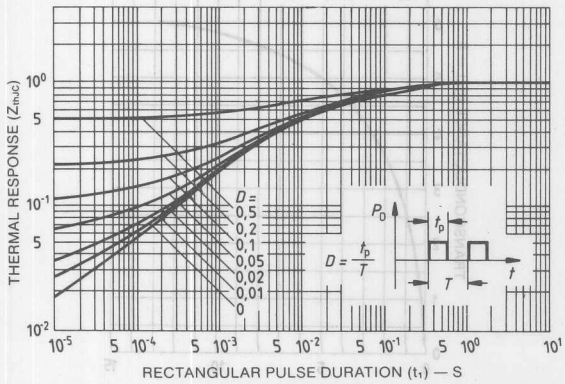


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

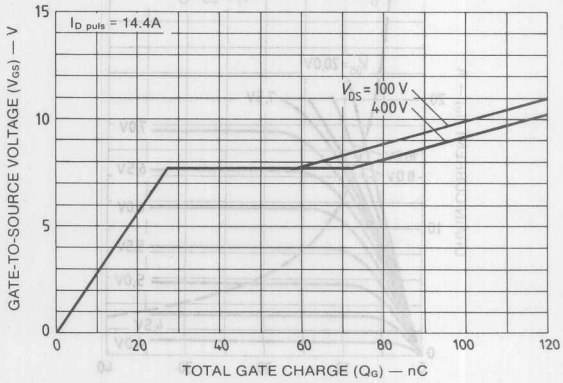


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ60

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 5.5A, 400V
- $r_{DS(on)} = 1.0\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

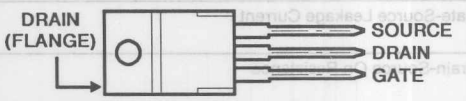
Description

The BUZ60 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ60 is supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ60	UNITS
Drain-Source Voltage	V_{DS}	400	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400	V
Continuous Drain Current			
T_C = +35°C	I_D	5.5	A
Pulsed Drain Current			
T_C = +25°C	I_{DM}	22	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2260

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C, V_{DS} = 400 V, V_{GS} = 0 V	—	20	250	μA
		T_j = 125 °C, V_{DS} = 400 V, V_{GS} = 0 V	—	100	1000	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 2.5 A	—	0.9	1	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 2.5 A	1.7	2.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	—	1.5	2	pF
Output Capacitance	C_{oss}		—	120	180	
Reverse Transfer Capacitance	C_{rss}		—	35	60	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	V_{CC} = 30 V, I_D = 2.7 A, V_{GS} = 10 V, R_{GS} = 50 Ω	—	30	45	ns
	t_r		—	40	60	
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$		—	110	140	
	t_f		—	50	65	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 1.67		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 75		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	5.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	22	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$, V_{GS} = 0 V, T_j = 25 °C	—	1.15	1.6	V
Reverse Recovery Time	t_{rr}	T_j = 25° C, $I_F = I_{DR}$, dI_F/dt = 100 A/μs, V_R = 100 V	—	1000	—	ns
Reverse Recovered Charge	Q_{RR}		—	5	—	μC

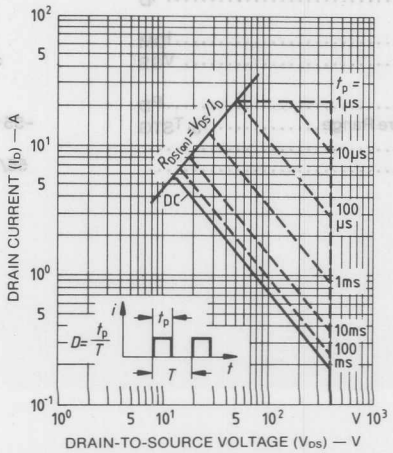


Fig. 1 - Maximum safe operating areas for all types.

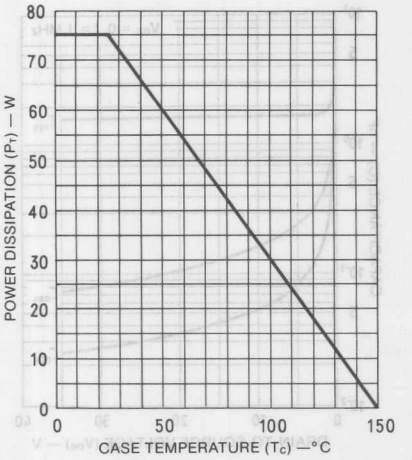


Fig. 2 - Power vs. temperature derating curve for all types.

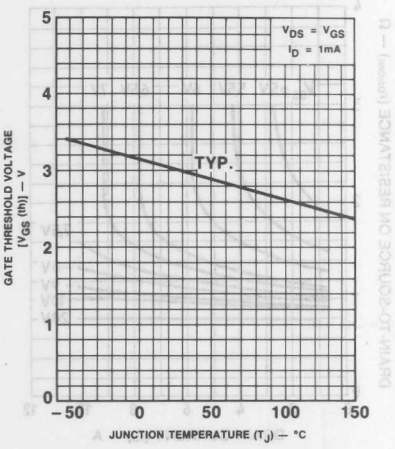


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

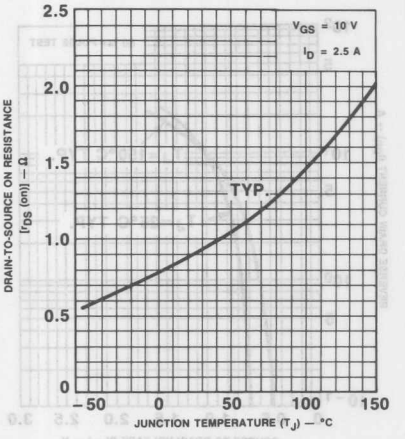


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

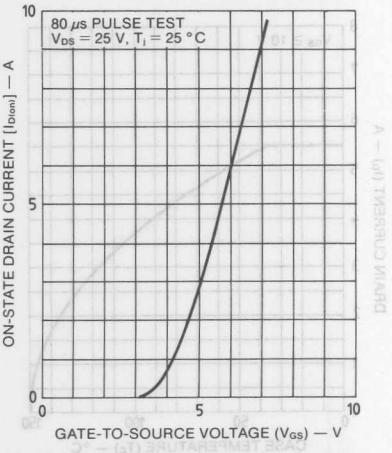


Fig. 5 - Typical transfer characteristics for all types.

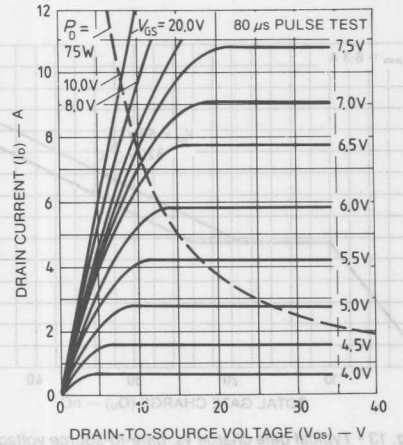


Fig. 6 - Typical output characteristics.

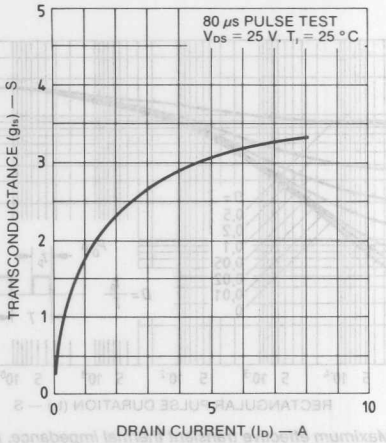


Fig. 7 - Typical transconductance vs. drain current.

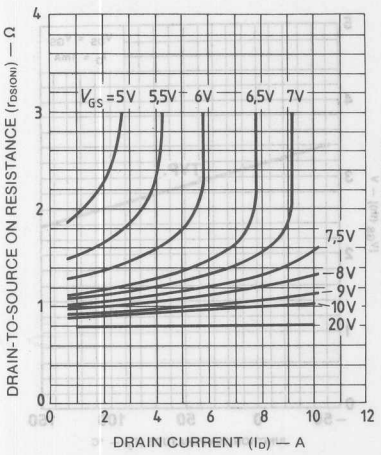


Fig. 8 - Typical on-resistance vs. drain current.

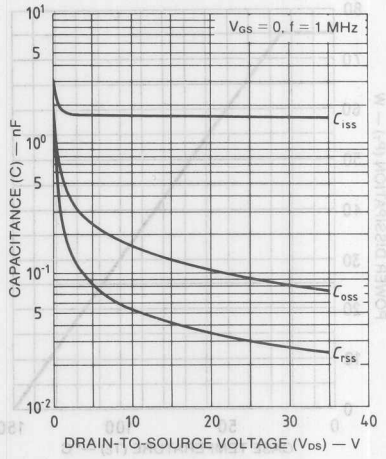


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

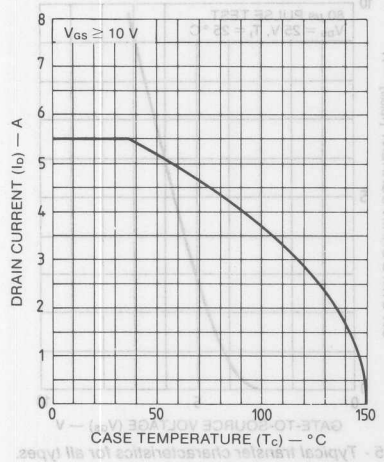


Fig. 10 - Maximum drain current vs. case temperature.

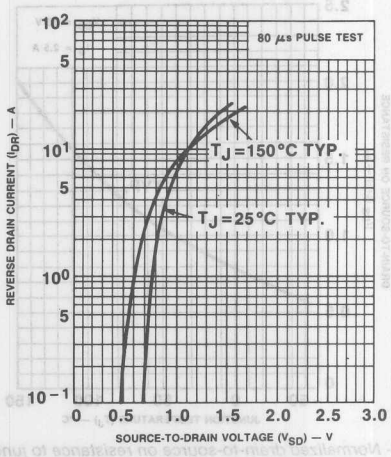


Fig. 11 - Typical source-drain diode forward voltage.

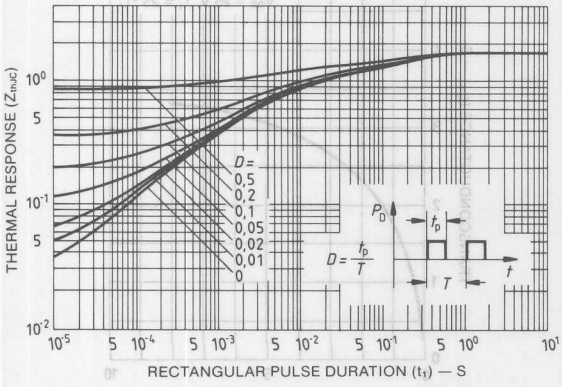


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

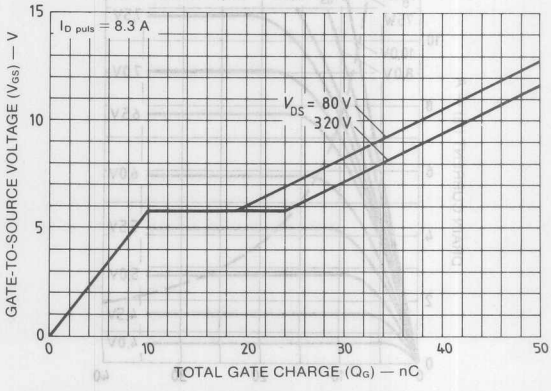


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ60B

August 1991

N-Channel Enhancement-Mode Power Field-Effect Transistor

Features

- 4.5A, 400V
- $r_{DS(on)} = 1.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

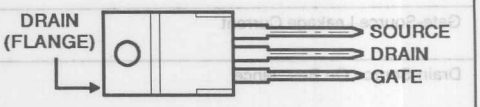
Description

The BUZ60B is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ60B is supplied in the JEDEC TO-220AB plastic package.

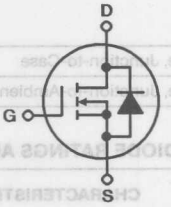
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ60B	UNITS
Drain-Source Voltage	V_{DS}	400	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400	V
Continuous Drain Current			
T_C = +35°C	I_D	4.5	A
Pulsed Drain Current			
T_C = +25°C	I_{DM}	18	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2261

Specifications BUZ60B

Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 400$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 2.5$ A	—	1.2	1.5	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 2.5$ A	1.7	2.5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V $f = 1$ MHz	—	1.5	2	pF
Output Capacitance	C_{oss}		—	120	180	
Reverse Transfer Capacitance	C_{rss}		—	35	60	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30$ V $I_D = 2.6$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	— —	30 40	45 60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		— —	110 50	140 65	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1.67			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	1.7	4.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	18	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.15	1.50	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$ $dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	1000	—	ns
Reverse Recovered Charge	Q_{RR}		—	5	—	μC

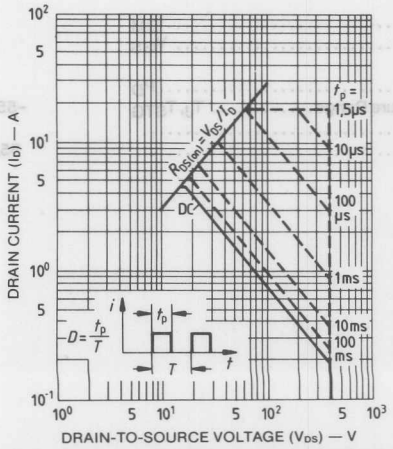


Fig. 1 - Maximum safe operating areas for all types.

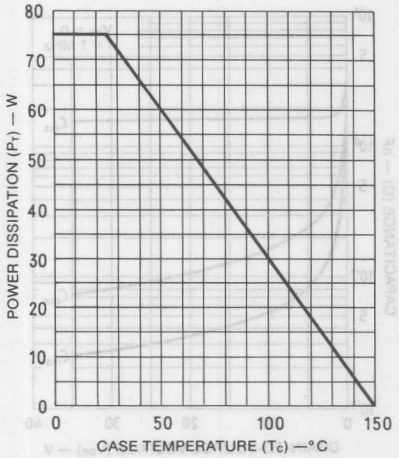


Fig. 2 - Power vs. temperature derating curve for all types.

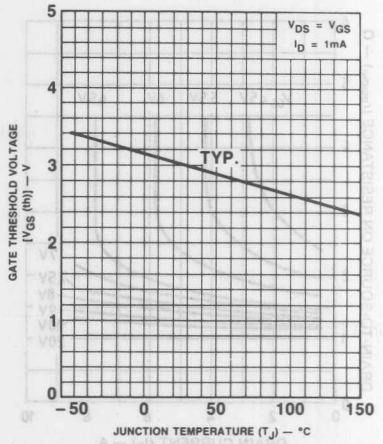


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

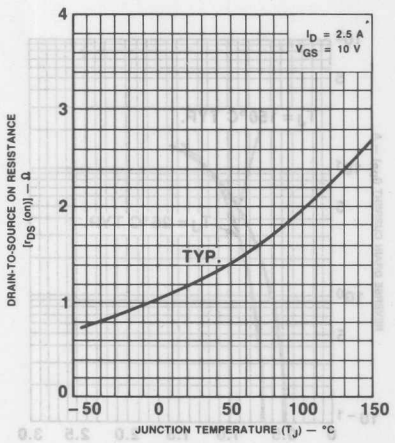


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

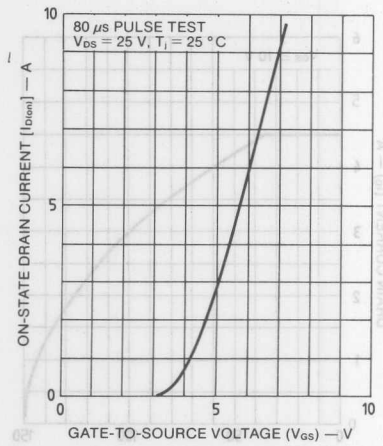


Fig. 5 - Typical transfer characteristics for all types.

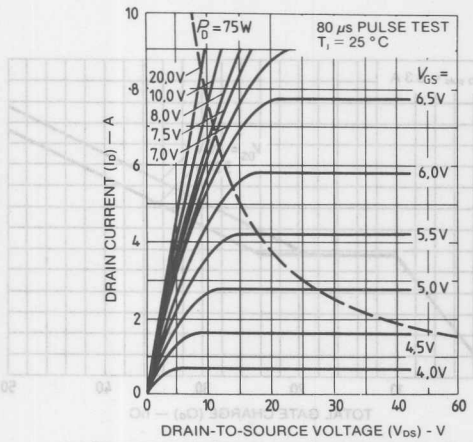


Fig. 6 - Typical output characteristics.

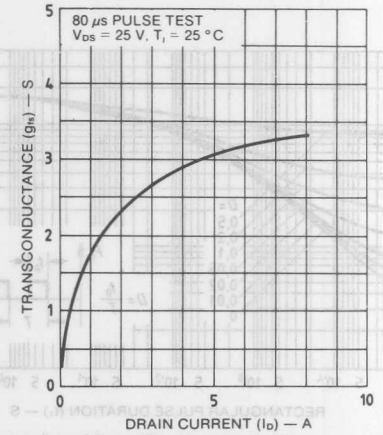


Fig. 7 - Typical transconductance vs. drain current.

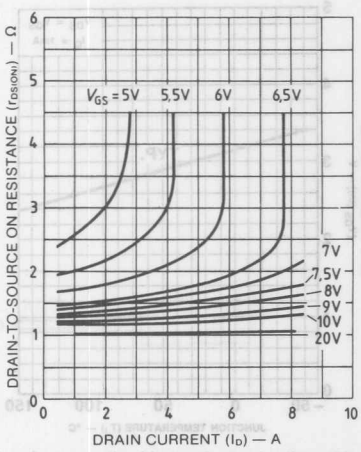


Fig. 8 - Typical on-resistance vs. drain current.

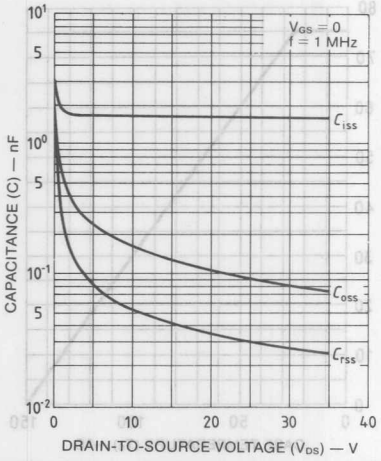


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

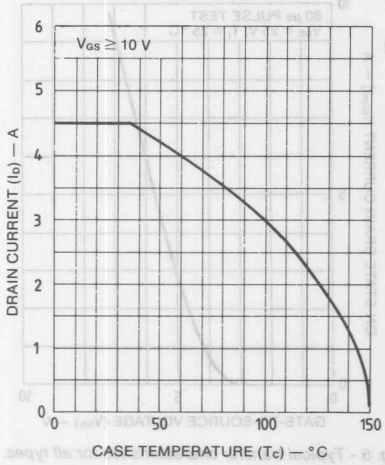


Fig. 10 - Maximum drain current vs. case temperature.

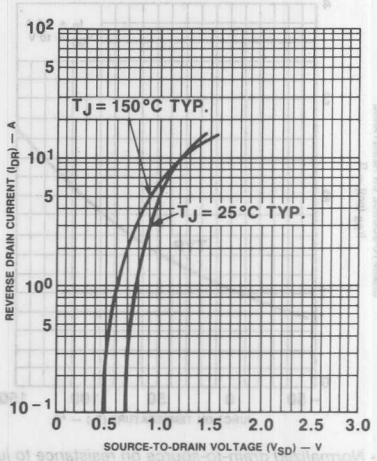


Fig. 11 - Typical source-drain diode forward voltage.

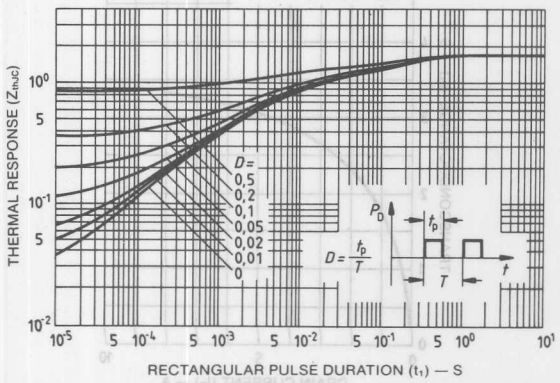


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

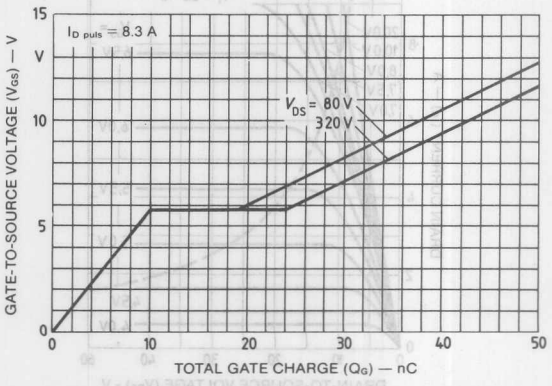


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ71

August 1991

N-Channel Enhancement-Mode Power Field-Effect Transistor

Features

- 14A, 50V
- $r_{DS(on)} = 0.1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

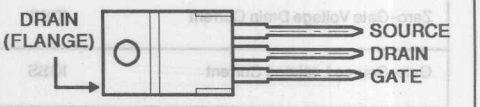
Description

The BUZ71 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ71 is supplied in the JEDEC TO-220AB plastic package.

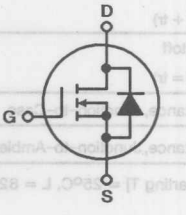
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ71	UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	50	V
Continuous Drain Current T_C = +55°C	I_D	14	A
Pulsed Drain Current T_C = +25°C	I_{DM}	56	A
Single Pulse Avalanche Energy*, EAS		100	mj
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

*V_{DD} = 10V, starting T_j = 25°C, L = 820μHy, I_{peak} = 14A, see Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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ELECTRICAL CHARACTERISTICS At Case Temperature (T_C) = +25°C Unless Otherwise Specified.

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	VGS = 0 V ID = 0.25 mA	50	–	–	V
Gate-Threshold Voltage	VGS(th)	VDS = VGS ID = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	IDSS	Tj = 25°C Tj = 125°C VDS = 50 V, VGS = 0 V	– –	20 100	250 1000	µA
Gate-Source Leakage Current	IGSS	VGS = 20 V VDS = 0 V	–	10	100	nA
Drain-Source on Resistance	rDS(on)	VGS = 10 V ID = 9A	–	0.09	0.1	Ω
Forward Transconductance	gfs	VDS = 25 V ID = 9 A	3.0	5.2	–	S
Input Capacitance	Ciss	VGS = 0 V	–	480	650	pF
Output Capacitance	Coss	VDS = 25 V	–	280	450	pF
Reverse Transfer Capacitance	Crss	f = 1 MHZ	–	160	280	pF
Turn-On Time ton	td(on)	Vcc = 30 V	–	20	30	ns
(ton = td(on) + tr)	tr	ID = 3 A	–	55	85	ns
Turn-Off Time toff	td(off)	VGS = 10 V	–	70	90	ns
(toff = td(off) = tr)	tr	RGS = 50 Ω	–	80	110	ns
Thermal Resistance, Junction-to-Case	RθJC			≤3.1		°C/W
Thermal Resistance, Junction-to-Ambient	RθJA			≤75		°C/W

*VDD = 10 V, starting Tj = 25°C, L = 820 µHy, Ipeak = 14 A, see figure 14 & 15.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	IDR	Tc = 25°C	–	–	14	A
Pulsed Reverse Drain Current	IDRM		–	–	56	A
Diode Forward Voltage	VSD	IF = 2 x IDR VGS = 0 V, Tj = 25°C	–	1.6	1.8	V
Reverse Recovery Time	trr	Tj = 25°C, IF = IDR	–	120	–	ns
Reverse Recovered Charge	QRR	dIF/dt = 100 A/µs, VR = 30 V	–	0.15	–	µC

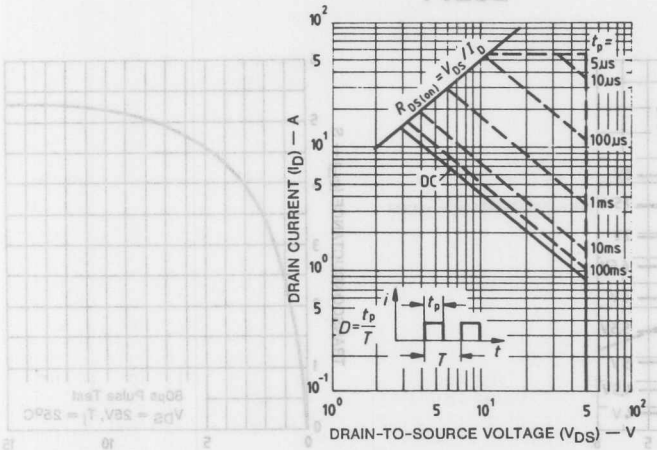


Figure 1 – Maximum safe operating areas for all types.

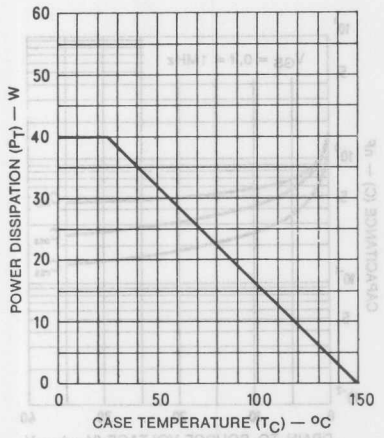


Figure 2 – Power vs temperature derating curve for all types.

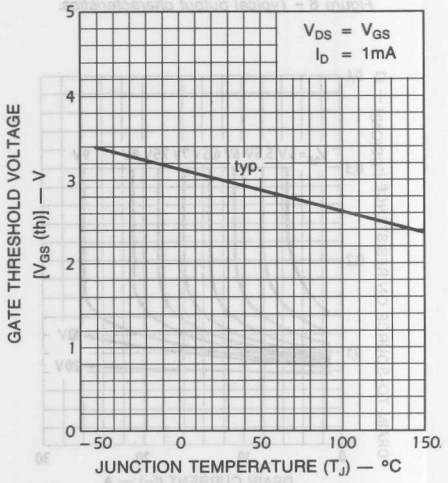


Figure 3 – Normalized gate threshold voltage as a function of junction temperature for all types.

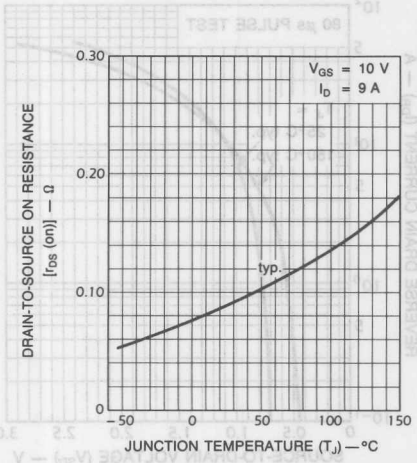


Figure 4 – Normalized drain-to-source on resistance to junction temperature for all types.

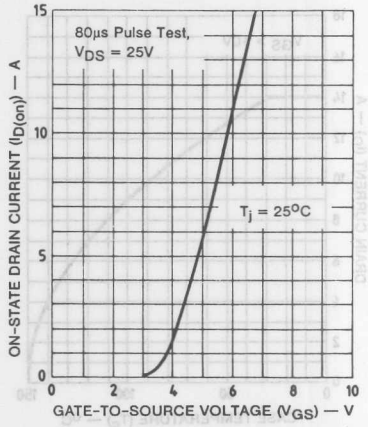


Figure 5 – Typical transfer characteristics for all types.

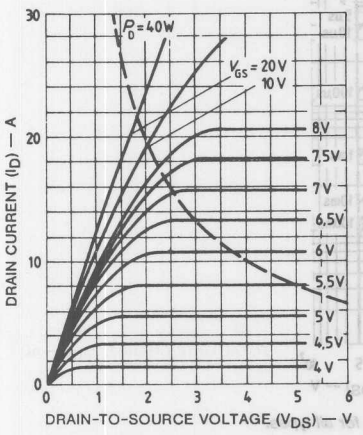


Figure 6 - Typical output characteristics.

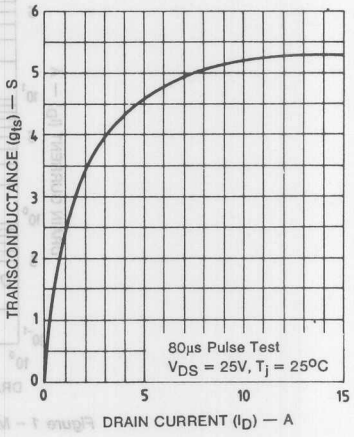


Figure 7 - Typical transconductance vs drain current.

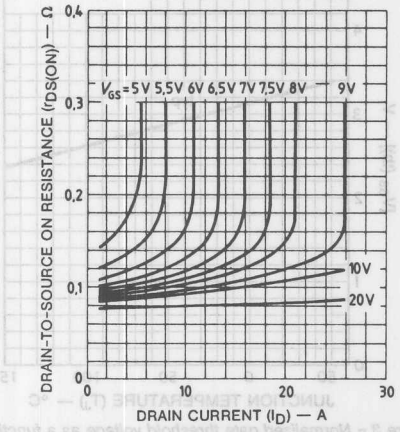


Figure 8 - Typical on-resistance vs drain current.

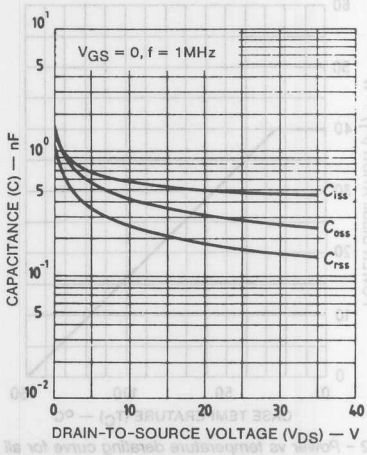


Figure 9 - Typical capacitance vs drain-to-source voltage.

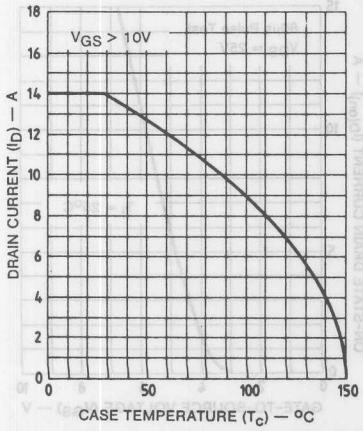


Figure 10 - Maximum drain current vs case temperature.

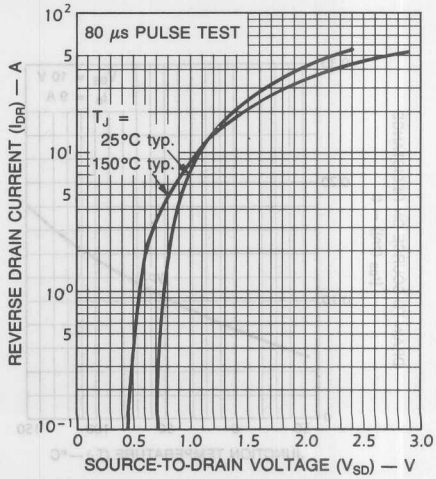


Figure 11 - Typical source-drain diode forward voltage.

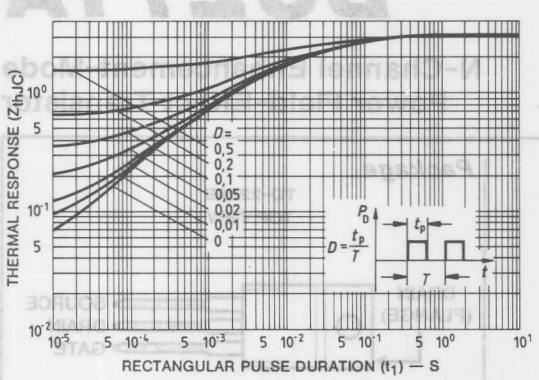


Figure 12 – Maximum effective transient thermal impedance, junction-to-case vs pulse duration

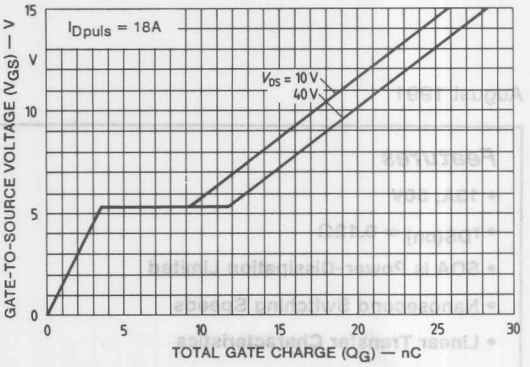


Figure 13 – Typical gate charge vs gate-to-source voltage.

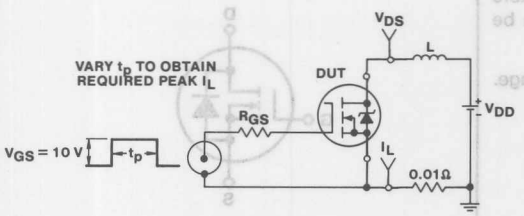


Figure 14 – Unclamped energy test circuit.

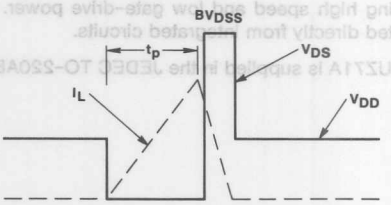


Figure 15 – Unclamped energy test waveforms.

Features

- 13A, 50V
- $r_{DS(on)} = 0.12\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

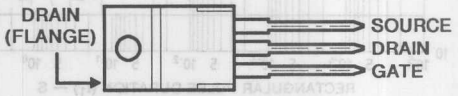
Description

The BUZ71A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ71A is supplied in the JEDEC TO-220AB plastic package.

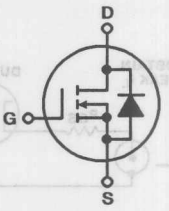
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ71A	UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	50	V
Continuous Drain Current T_C = +55°C	I_D	13	A
Pulsed Drain Current T_C = +25°C	I_{DM}	48	A
Single Pulse Avalanche Energy*, EAS		100	mj
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

*V_{DD} = 10V, starting T_j = +25°C, L = 820μHy, I_{peak} = 14A, see Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2419**

ELECTRICAL CHARACTERISTICS At Case Temperature (T_C) = +25°C Unless Otherwise Specified.

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	VGS = 0 V ID = 0.25 mA	50	–	–	V
Gate-Threshold Voltage	VGS(th)	VDS = VGS ID = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	IDSS	Tj = 25°C Tj = 125°C VDS = 50 V, VGS = 0 V	– –	20 100	250 1000	µA
Gate-Source Leakage Current	IGSS	VGS = 20 V VDS = 0 V	–	10	100	nA
Drain-Source on Resistance	rDS(on)	VGS = 10 V ID = 9A	–	0.11	0.12	Ω
Forward Transconductance	gfs	VDS = 25 V ID = 9 A	3.0	5.2	–	S
Input Capacitance	Ciss	VGS = 0 V	–	480	650	pF
Output Capacitance	Coss	VDS = 25 V	–	280	450	pF
Reverse Transfer Capacitance	Crss	f = 1 MHZ	–	160	280	pF
Turn-On Time ton	td(on)	Vcc = 30 V	–	20	30	ns
(ton = td(on) + tr)	tr	ID = 3 A	–	55	85	ns
Turn-Off Time toff	td(off)	VGS = 10 V	–	70	90	ns
(toff = td(off) = tr)	tr	RGS = 50 Ω	–	80	110	ns
Thermal Resistance, Junction-to-Case	RθJC			≤3.1		°C/W
Thermal Resistance, Junction-to-Ambient	RθJA			≤75		°C/W

*VDD = 10 V, starting Tj = 25°C, L = 820 µHy, Ipeak = 14 A, see figure 14 & 15.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	IDR	Tc = 25°C	–	–	13	A
Pulsed Reverse Drain Current	IDRM		–	–	52	A
Diode Forward Voltage	VSD	IF = 2 x IDR VGS = 0 V, Tj = 25°C	–	1.6	2.2	V
Reverse Recovery Time	trr	Tj = 25°C, IF = IDR	–	120	–	ns
Reverse Recovered Charge	QRR	dIF/dt = 100 A/µs, VR = 30 V	–	0.15	–	µC

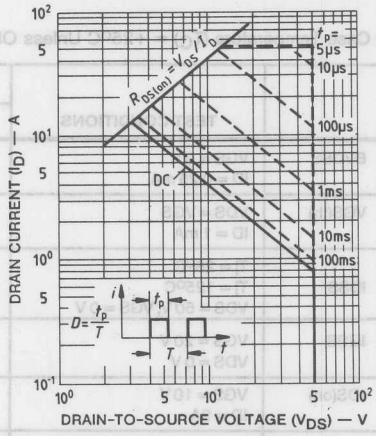


Figure 1 – Maximum safe operating areas for all types.

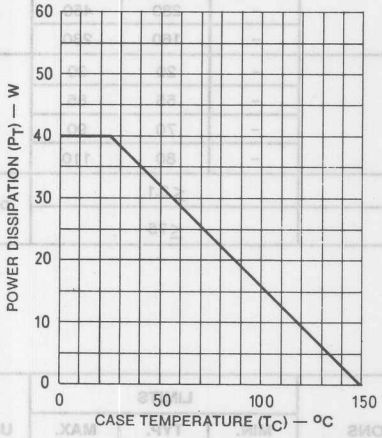


Figure 2 – Power vs temperature derating curve for all types.

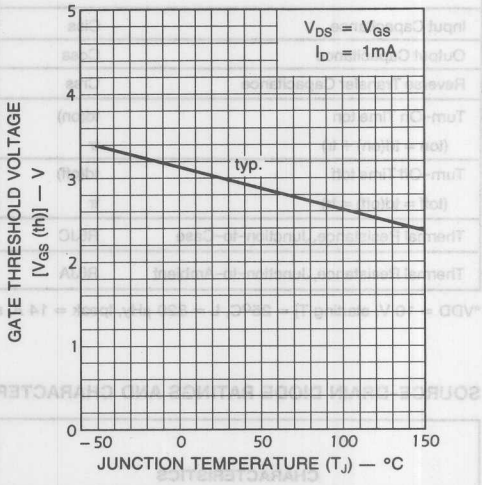


Figure 3 – Normalized gate threshold voltage as a function of junction temperature for all types.

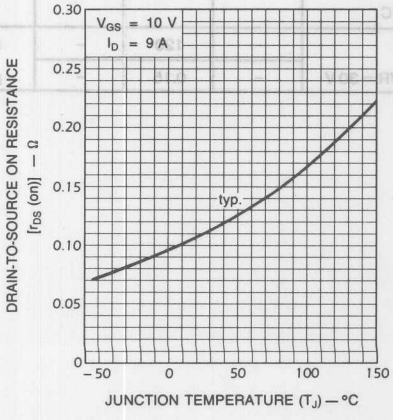


Figure 4 – Normalized drain-to-source on resistance to junction temperature for all types.

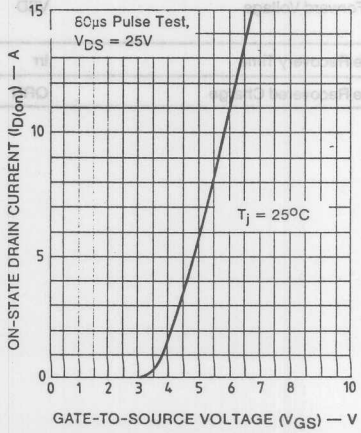


Figure 5 – Typical transfer characteristics for all types.

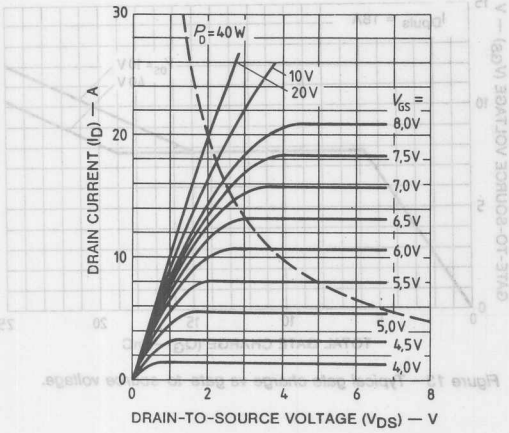


Figure 6 – Typical output characteristics.

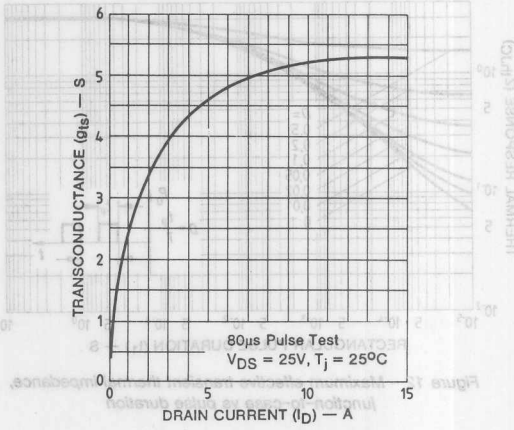


Figure 7 – Typical transconductance vs drain current.

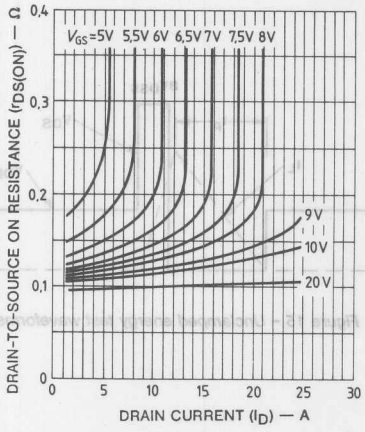


Figure 8 – Typical on-resistance vs drain current.

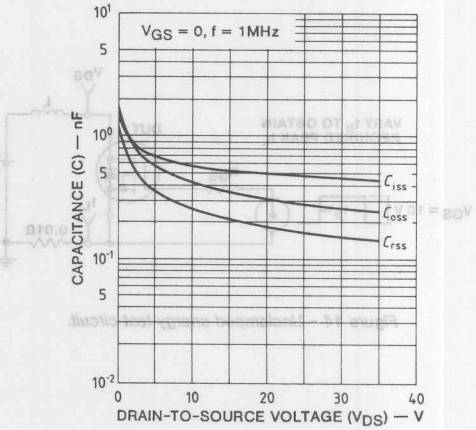


Figure 9 – Typical capacitance vs drain-to-source voltage.

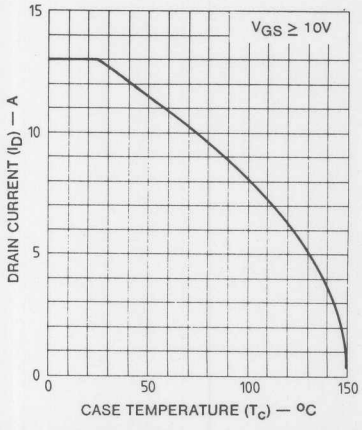


Figure 10 – Maximum drain current vs case temperature.

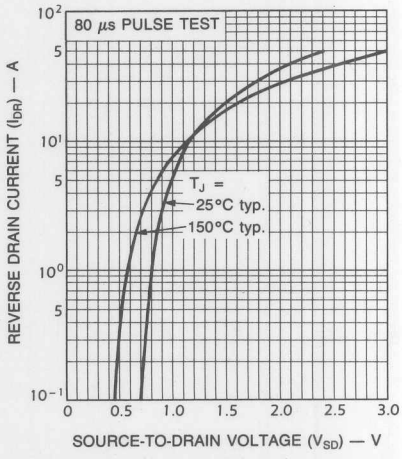


Figure 11 – Typical source-drain diode forward voltage.

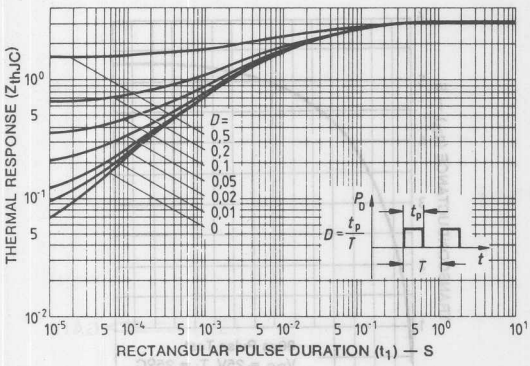


Figure 12 – Maximum effective transient thermal impedance, junction-to-case vs pulse duration

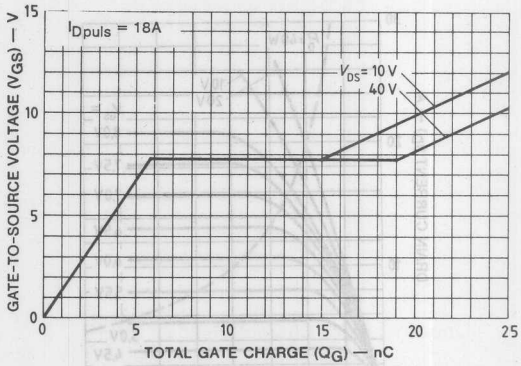


Figure 13 – Typical gate charge vs gate-to-source voltage.

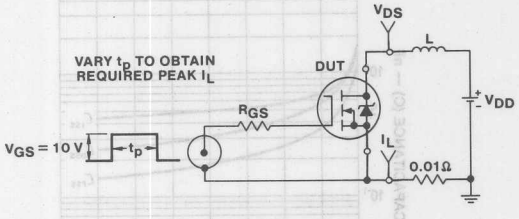


Figure 14 – Unclamped energy test circuit.

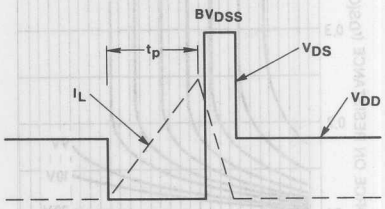


Figure 15 – Unclamped energy test waveforms.

HARRIS

BUZ72A

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 9A, 100V
- $r_{DS(on)} = 0.25\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

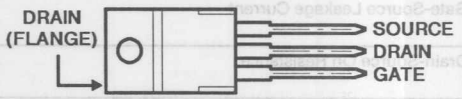
Description

The BUZ72A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ72A is supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ72A	UNITS
Drain-Source Voltage	V_{DS}	100	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	100	V
Continuous Drain Current, T_C = +25°C	I_D	9	A
Pulsed Drain Current, T_C = +25°C	I_{DM}	36	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation, T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2262

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	100	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C, V_{DS} = 100 V, V_{GS} = 0 V	—	20	250	μA
		T_j = 125 °C, V_{DS} = 100 V, V_{GS} = 0 V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A	—	0.23	0.25	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 5 A	2.7	3.8	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	—	450	600	pF
Output Capacitance	C_{oss}		—	150	240	pF
Reverse Transfer Capacitance	C_{rss}		—	80	130	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	V_{CC} = 30 V, I_D = 2.9 A, V_{GS} = 10 V, R_{GS} = 50 Ω	—	20	30	ns
	t_r		—	45	70	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$		—	70	90	ns
	t_f		—	55	70	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 3.1		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 75		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	9	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	36	A
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR}, V_{GS} = 0 V, T_j = 25 °C	—	1.5	2	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DR}, dI_F/dt = 100 A/μs, V_R = 30 V	—	170	—	ns
Reverse Recovered Charge	Q_{RR}		—	0.30	—	μC

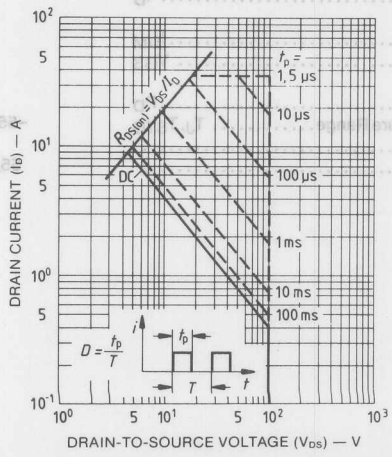


Fig. 1 - Maximum safe operating areas for all types.

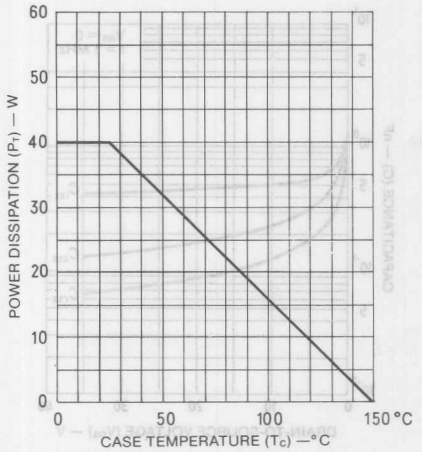


Fig. 2 - Power vs. temperature derating curve for all types.

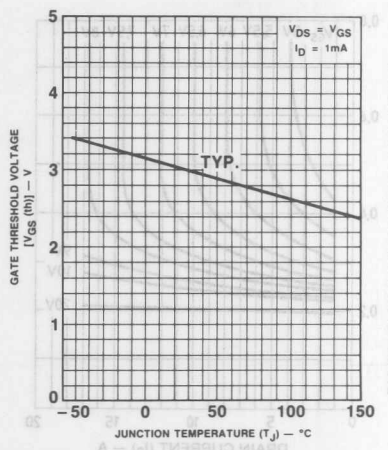


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

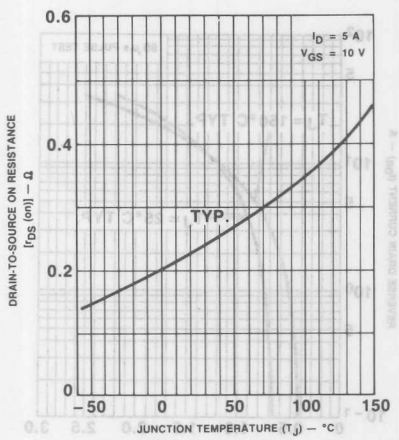


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

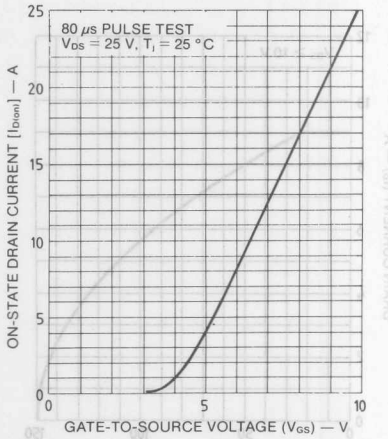


Fig. 5 - Typical transfer characteristics for all types.

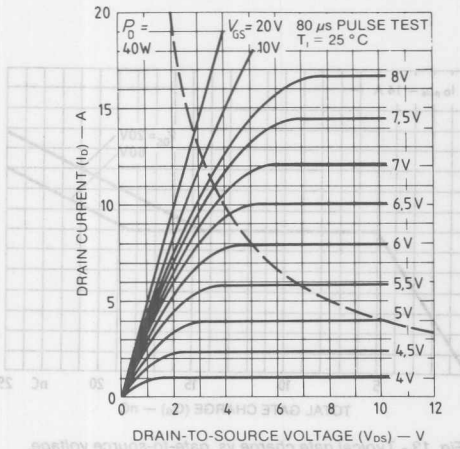


Fig. 6 - Typical output characteristics.

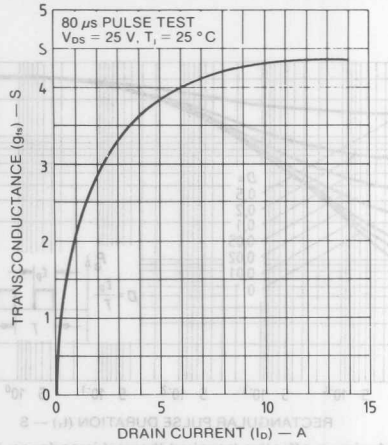


Fig. 7 - Typical transconductance vs. drain current.

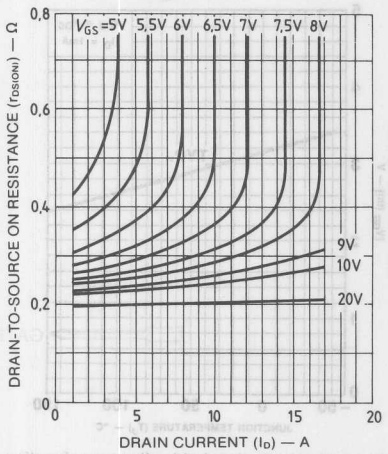


Fig. 8 - Typical on-resistance vs. drain current.

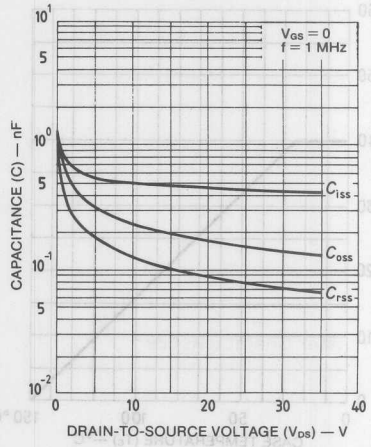


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

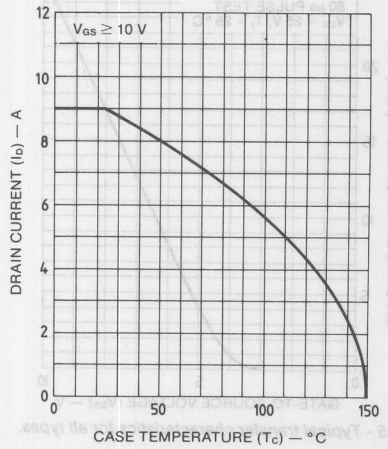


Fig. 10 - Maximum drain current vs. case temperature.

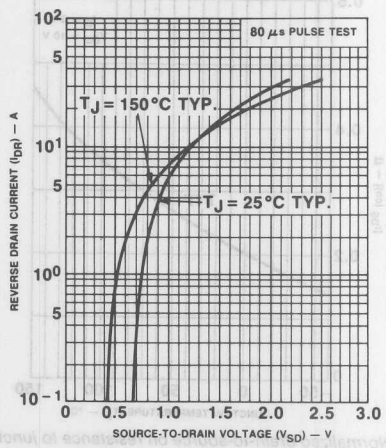


Fig. 11 - Typical source-drain diode forward voltage.

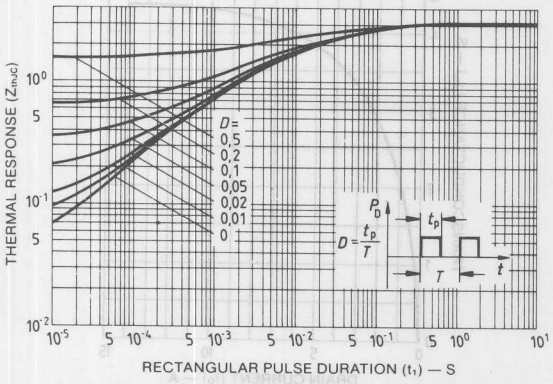


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

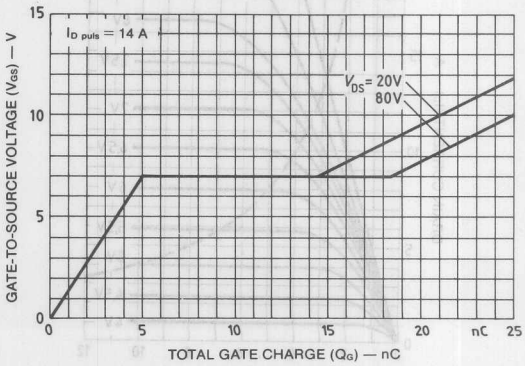


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ73A

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 5.8A, 200V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

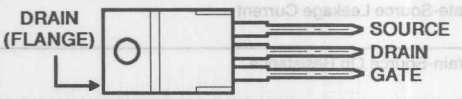
Description

The BUZ73A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ73A is supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		BUZ73A	UNITS
Drain-Source Voltage	V_{DS}	200	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	200	V
Continuous Drain Current T_C = +25°C	I_D	5.8	A
Pulsed Drain Current T_C = +25°C	I_{DM}	23	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2263

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	200	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C, V_{DS} = 200 V, V_{GS} = 0 V	—	20	250	μA
		T_j = 125 °C, V_{DS} = 200 V, V_{GS} = 0 V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3.5 A	—	0.5	0.6	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 3.5 A	2.2	3.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	—	450	600	pF
Output Capacitance	C_{oss}		—	100	160	pF
Reverse Transfer Capacitance	C_{rss}		—	50	80	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	V_{CC} = 30 V, I_D = 2.8 A, V_{GS} = 10 V, R_{GS} = 50 Ω	—	15	20	ns
	t_r		—	40	60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$		—	70	90	ns
	t_f		—	40	55	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 3.1		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 75		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	5.8	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	23	A
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$, V_{GS} = 0 V, T_j = 25 °C	—	1.4	1.7	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, $I_F = I_{DR}$, dI_F/dt = 100 A/μs, V_R = 100 V	—	200	—	ns
Reverse Recovered Charge	Q_{RR}		—	0.6	—	μC

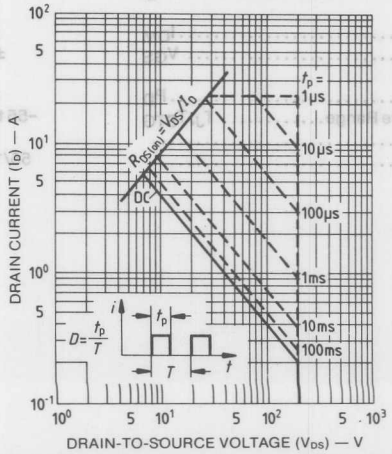


Fig. 1 - Maximum safe operating areas for all types.

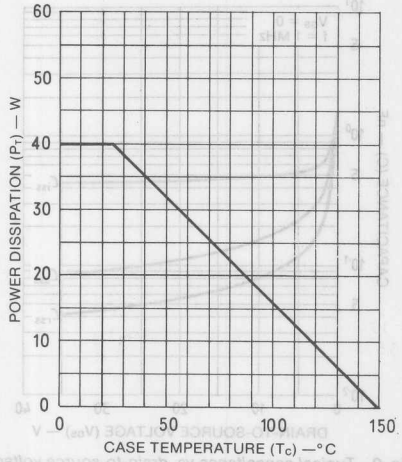


Fig. 2 - Power vs. temperature derating curve for all types.

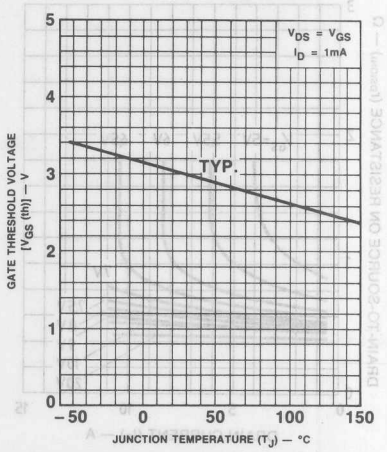


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

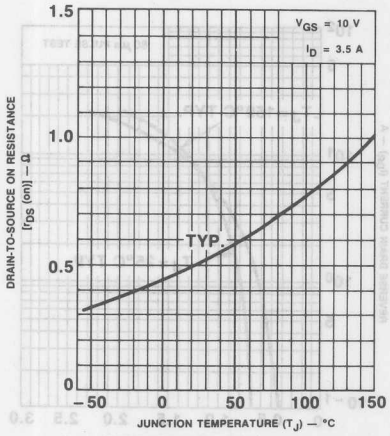


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

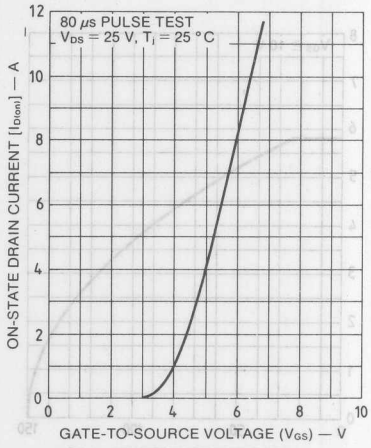


Fig. 5 - Typical transfer characteristics for all types.

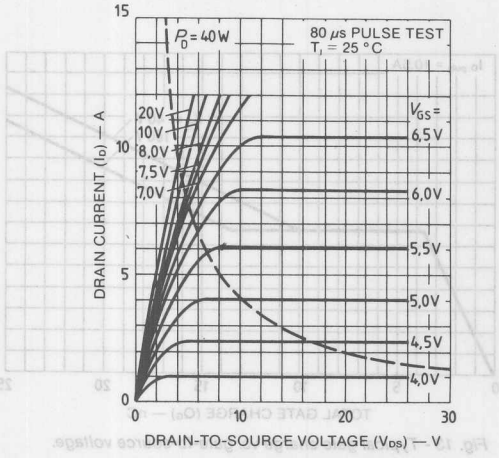


Fig. 6 - Typical output characteristics.

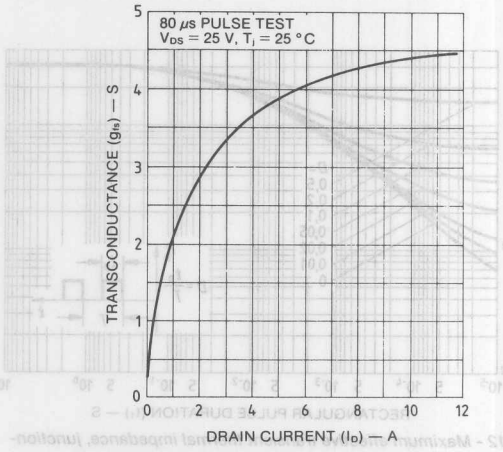


Fig. 7 - Typical transconductance vs. drain current.

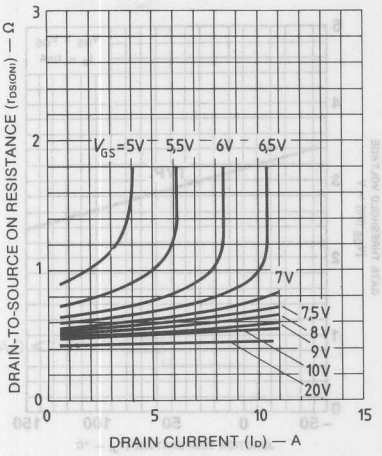


Fig. 8 - Typical on-resistance vs. drain current.

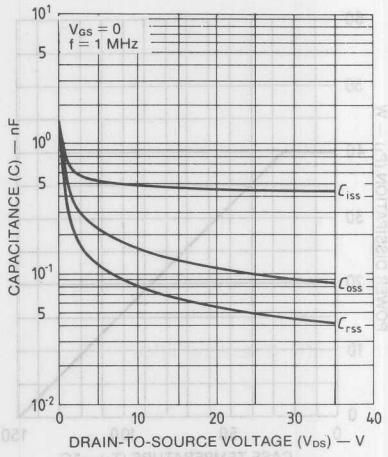


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

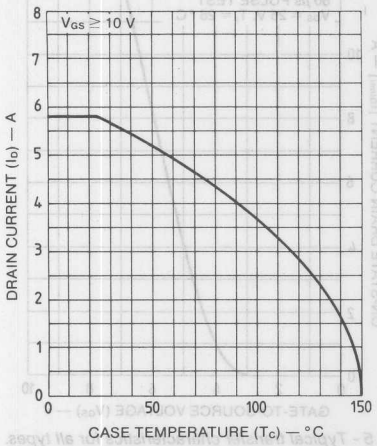


Fig. 10 - Maximum drain current vs. case temperature.

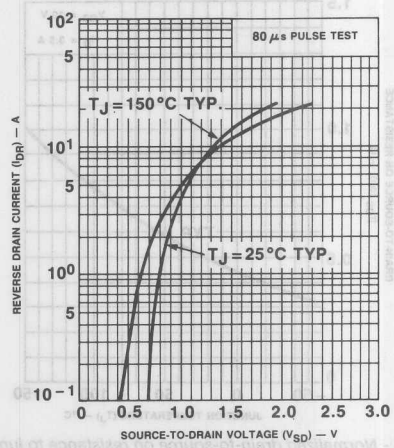


Fig. 11 - Typical source-drain diode forward voltage.

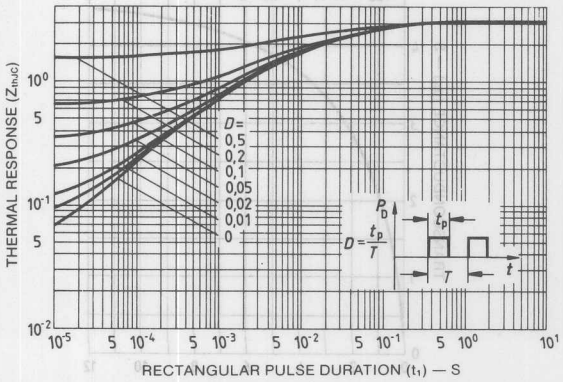


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

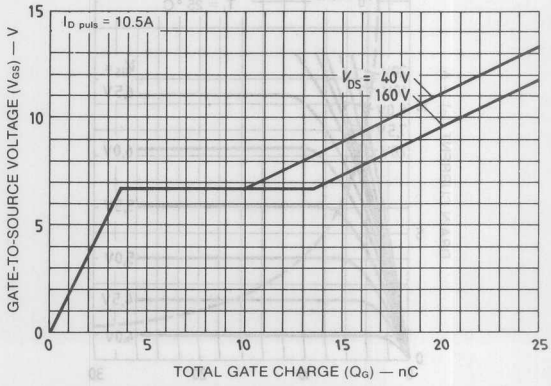


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ76

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 3A, 400V
- $r_{DS(on)} = 1.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

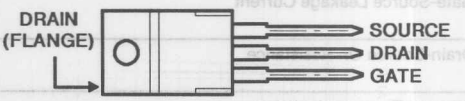
Description

The BUZ76 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ76 is supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4

N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ76	UNITS
Drain-Source Voltage	V_{DS}	400	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400	V
Continuous Drain Current			
T_C = +35°C	I_D	3	A
Pulsed Drain Current			
T_C = +25°C	I_{DM}	12	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2264

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 400$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 1.5$ A	—	1.65	1.8	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 3$ A	2.1	2.5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V $f = 1$ MHz	—	300	500	pF
Output Capacitance	C_{oss}		—	50	80	
Reverse Transfer Capacitance	C_{rss}		—	35	60	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30$ V $I_D = 2.5$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	— —	15 40	20 60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$ t_f		— —	50 30	65 40	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 3.1		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 75		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	3	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	12	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.1	1.4	V
Reverse Recovery Time	t_{rr}	$T_j = 25$° C, $I_F = I_{DR}$ $dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	300	—	ns
Reverse Recovered Charge	Q_{RR}		—	2.5	—	μC

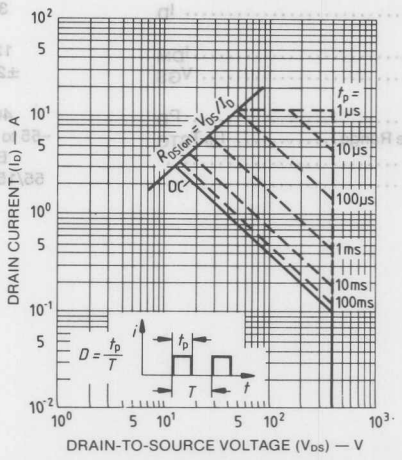


Fig. 1 - Maximum safe operating areas for all types.

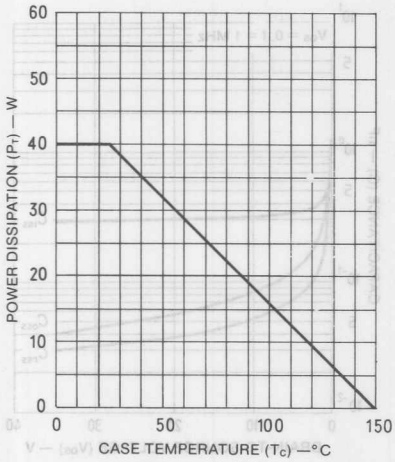


Fig. 2 - Power vs. temperature derating curve for all types.

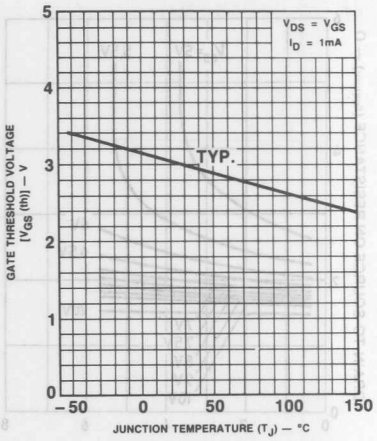


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

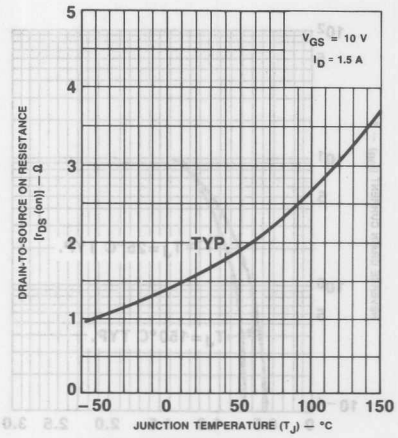


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

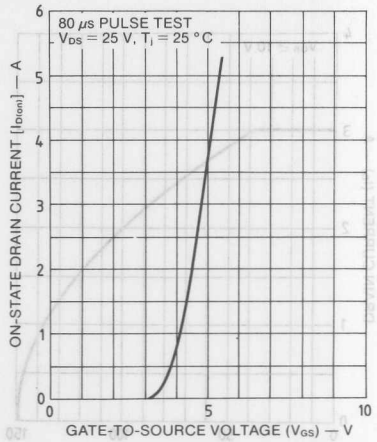


Fig. 5 - Typical transfer characteristics for all types.

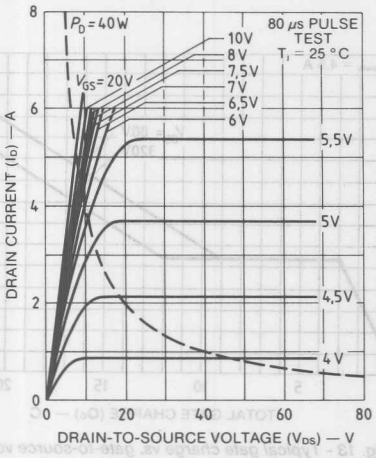


Fig. 6 - Typical output characteristics.

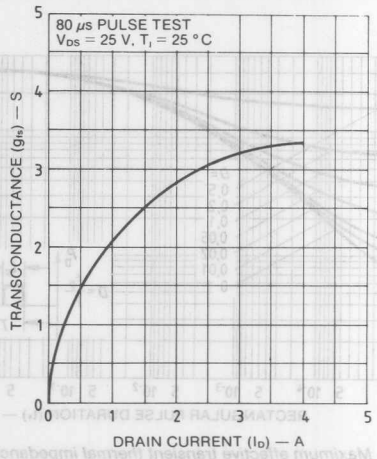


Fig. 7 - Typical transconductance vs. drain current.

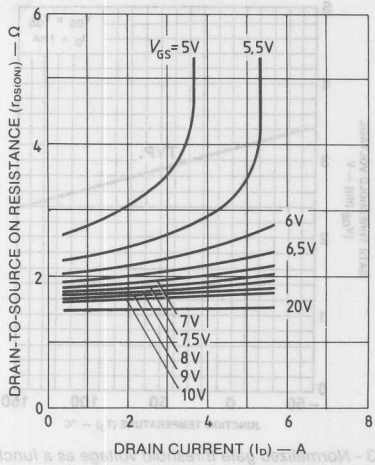


Fig. 8 - Typical on-resistance vs. drain current.

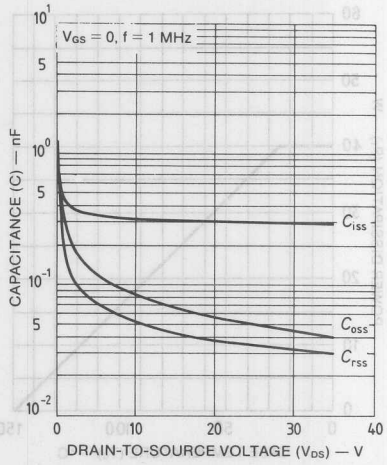


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

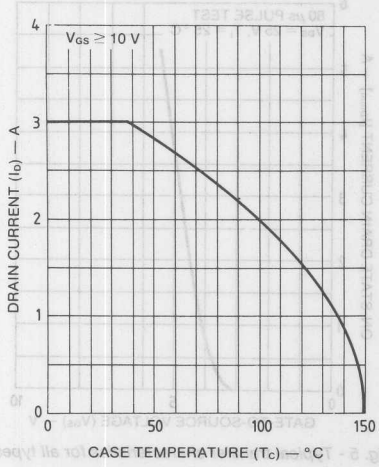


Fig. 10 - Maximum drain current vs. case temperature.

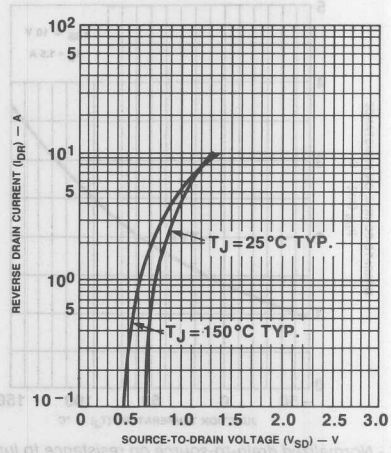


Fig. 11 - Typical source-drain diode forward voltage.

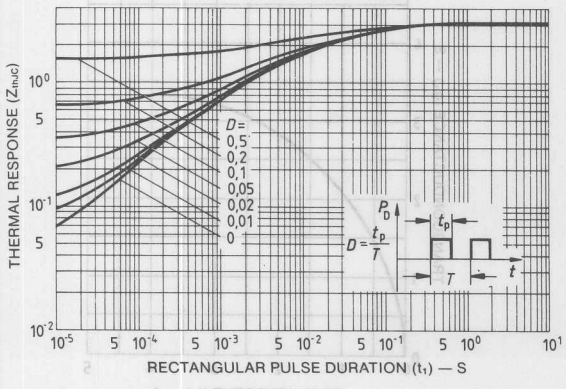


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

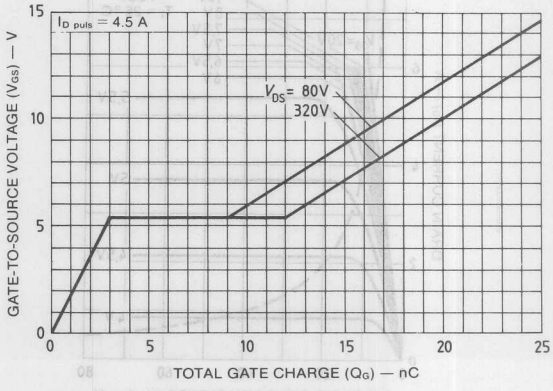


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ76A

August 1991

N-Channel Enhancement-Mode Power Field-Effect Transistor

Features

- 2.6A, 400V
- $r_{DS(on)} = 2.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

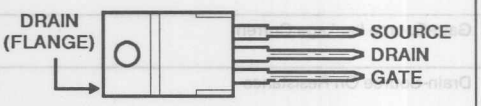
Description

The BUZ76A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ76A is supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4

N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ76A	UNITS
Drain-Source Voltage	V_{DS}	400	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400	V
Continuous Drain Current			
T_C = +30°C	I_D	2.6	A
Pulsed Drain Current			
T_C = +25°C	I_{DM}	10	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2265

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V, $I_D = 0.25$ mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1$ mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C, $V_{DS} = 400$ V, $V_{GS} = 0$ V	—	20	250	μA
		$T_j = 125$ °C, $V_{DS} = 400$ V, $V_{GS} = 0$ V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V, $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 1.5$ A	—	2.2	2.5	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V, $I_D = 1.5$ A	2.1	2.5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = 25$ V, f = 1 MHz	—	300	500	pF
Output Capacitance	C_{oss}		—	50	80	pF
Reverse Transfer Capacitance	C_{rss}		—	35	60	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	$V_{CC} = 30$ V, $I_D = 2.4$ A, $V_{GS} = 10$ V, $R_{GS} = 50$ Ω	—	15	20	ns
	t_r		—	40	60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$		—	50	65	ns
	t_r		—	30	40	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 3.1		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 75		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	2.6	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	10	A
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$, $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.1	1.4	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$, $dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	300	—	ns
Reverse Recovered Charge	Q_{RR}		—	2.5	—	μC

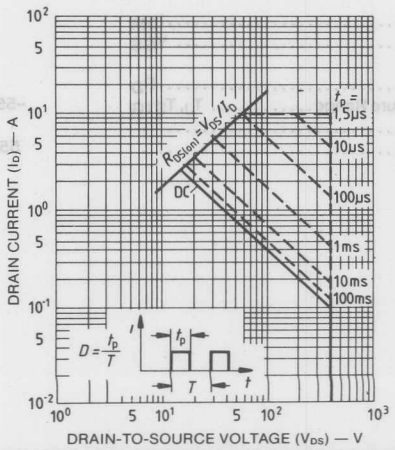


Fig. 1 - Maximum safe operating areas for all types.

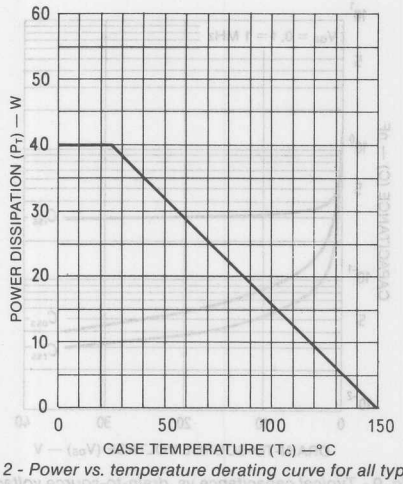


Fig. 2 - Power vs. temperature derating curve for all types.

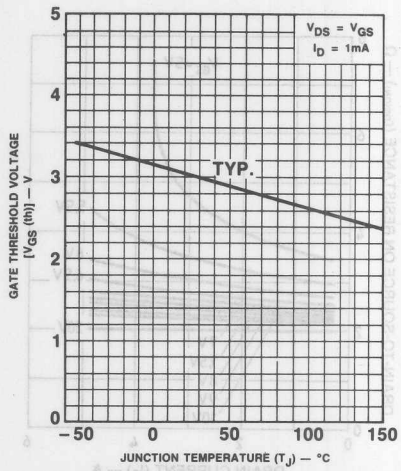


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

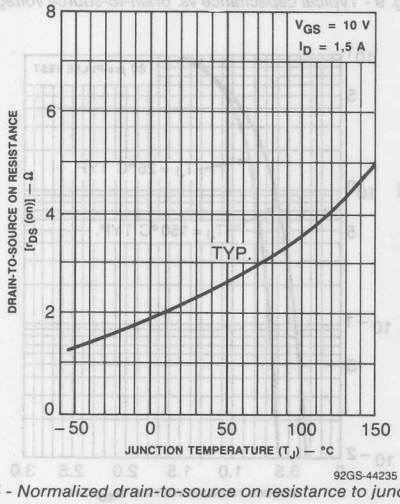


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

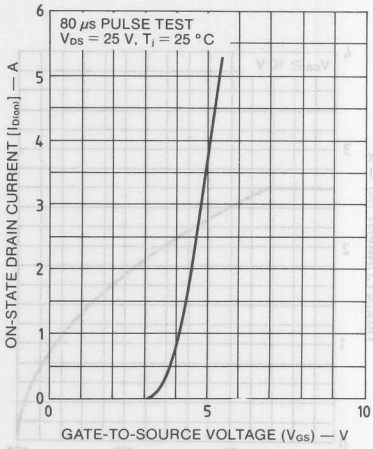


Fig. 5 - Typical transfer characteristics for all types.

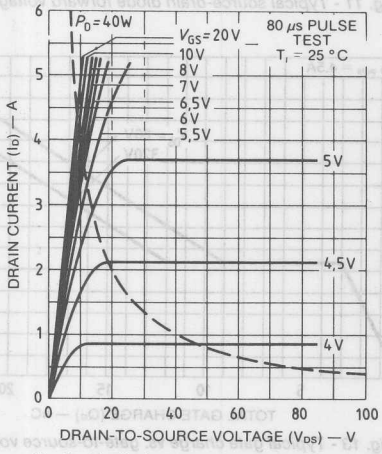


Fig. 6 - Typical output characteristics.

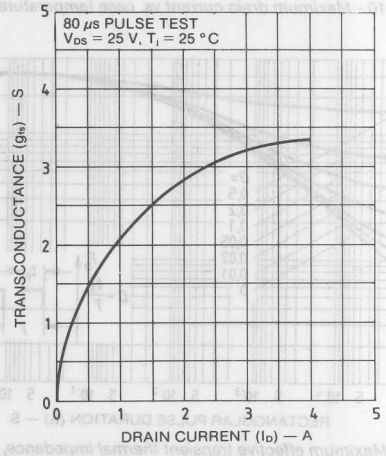


Fig. 7 - Typical transconductance vs. drain current.

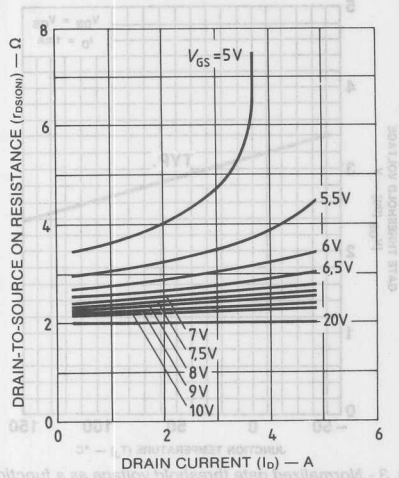


Fig. 8 - Typical on-resistance vs. drain current.

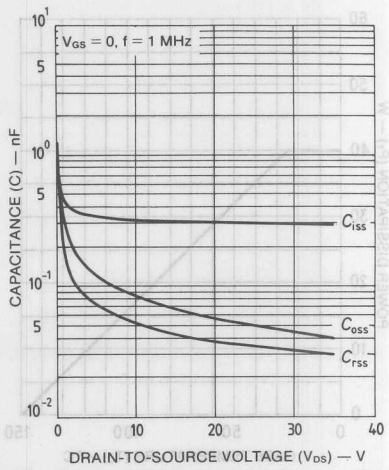


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

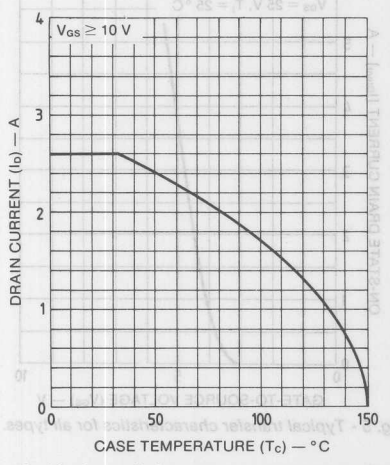


Fig. 10 - Maximum drain current vs. case temperature.

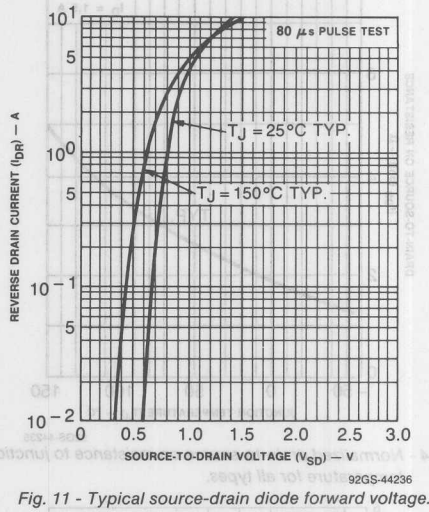


Fig. 11 - Typical source-drain diode forward voltage.

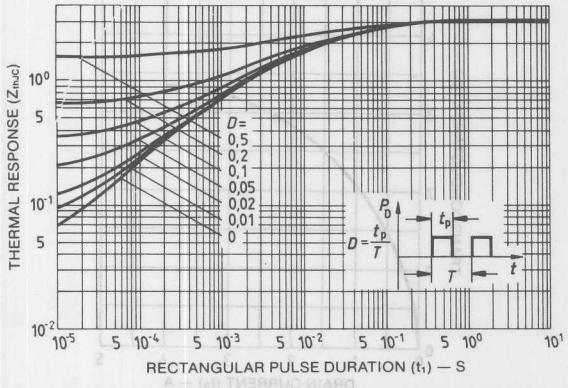


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

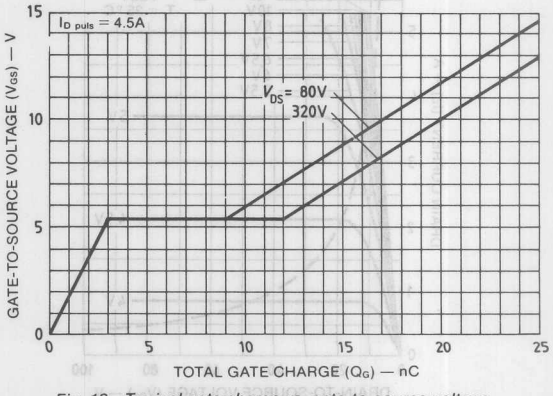


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

IRF120, IRF121 IRF122, IRF123

N-Channel Enhancement-Mode Power Field-Effect Transistors

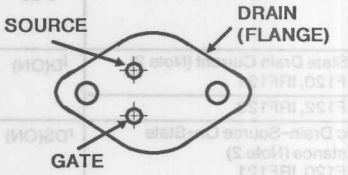
August 1991

Features

- 8.0A and 9.2A, 80V - 100V
- $r_{DS(on)}$ = 0.27Ω and 0.36Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AA
BOTTOM VIEW



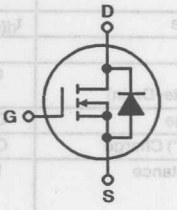
Description

The IRF120, IRF121, IRF122, and IRF123 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF120	IRF121	IRF122	IRF123	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	9.2	9.2	8.0	8.0	A
T_C = +100°C ..... I_D	6.5	6.5	5.6	5.6	A
Pulsed Drain Current (3) ..... I_{DM}	37	37	32	32	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	60	60	60	60	W
Linear Derating Factor	0.4	0.4	0.4	0.4	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figures 14 and 15, L = 100μH)	32	32	28	28	A
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

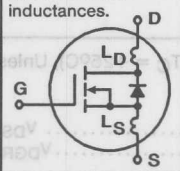
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

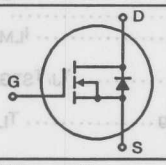
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File Number 1565.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF120, IRF122	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	100	-	-	V
IRF121, IRF123			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +150°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF120, IRF121	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, V_{GS} = 10V	9.2	-	-	A
IRF122, IRF123			8.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF120, IRF121	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.6A	-	0.25	0.27	Ω
IRF122. IRF123			-	0.27	0.36	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, I_D = 5.6A	2.9	4.0	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	350	-	pF
Output Capacitance	C_{OSS}		-	130	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	36	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D = 9.2A, rd = 5.1Ω, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	8.8	13	ns
Rise Time	t_r		-	30	45	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	19	29	ns
Fall Time	t_f		-	20	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 5.6A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	9.7	15	nC
Gate-Source Charge	Q_{gs}		-	2.2	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	2.3	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	2.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	8.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = 9.2A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 9.2A, dI_F/dt = 100A/μs	55	110	240	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 9.2A, dI_F/dt = 100A/μs	0.25	0.53	1.10	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES:
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5)

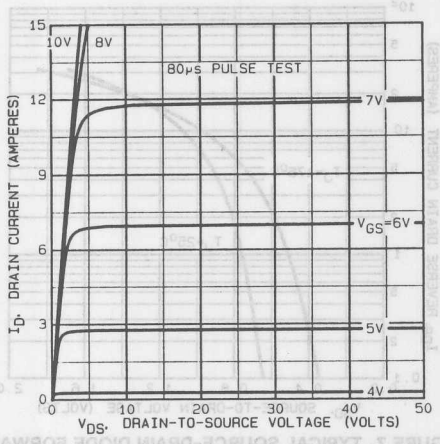


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

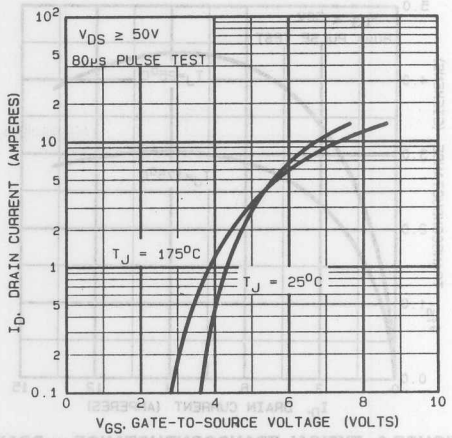


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

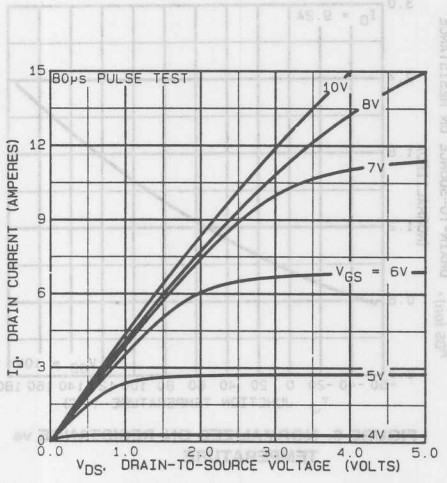


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

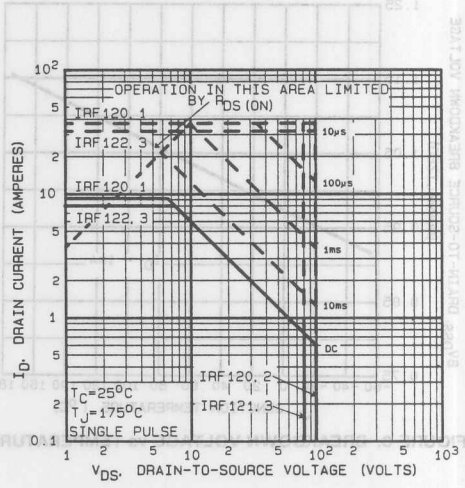


FIGURE 4. MAXIMUM SAFE OPERATING AREA

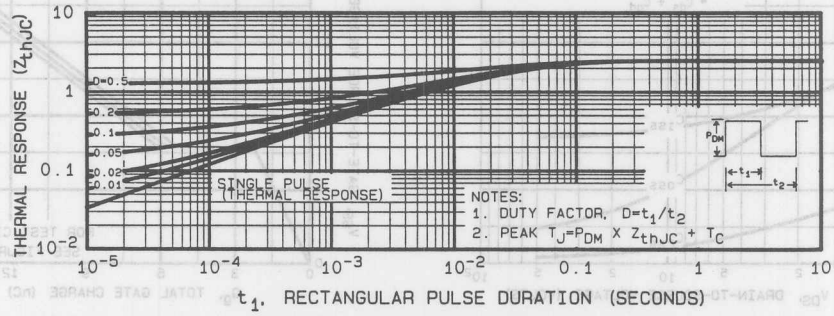


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE vs PULSE DURATION

4

N-CHANNEL POWER MOSFETs

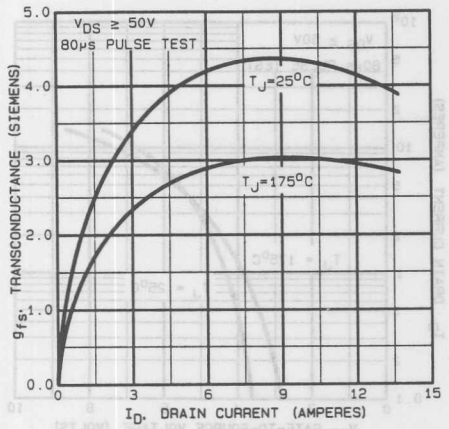


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

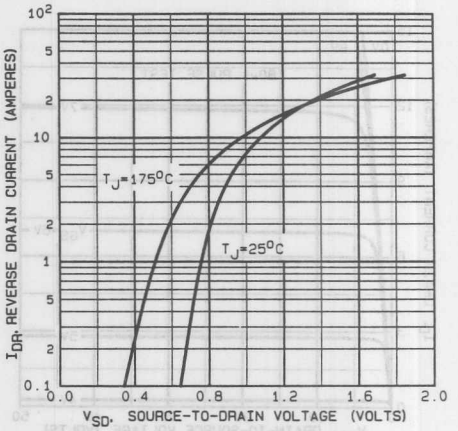


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

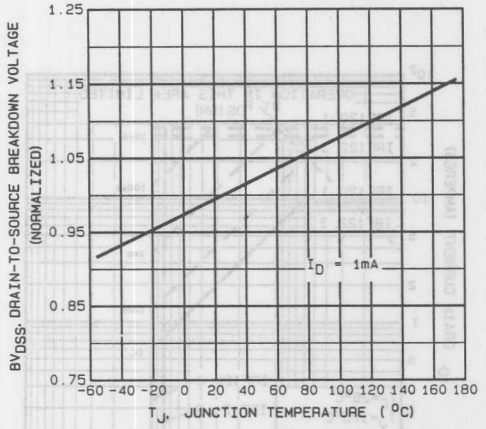


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

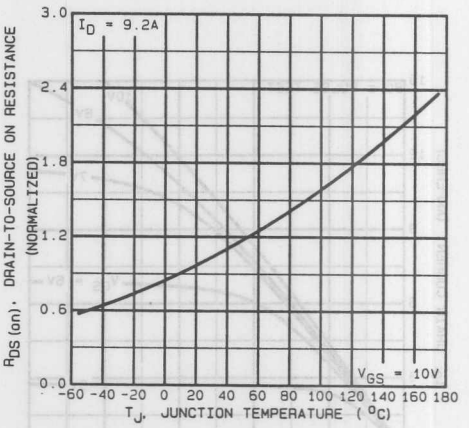


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

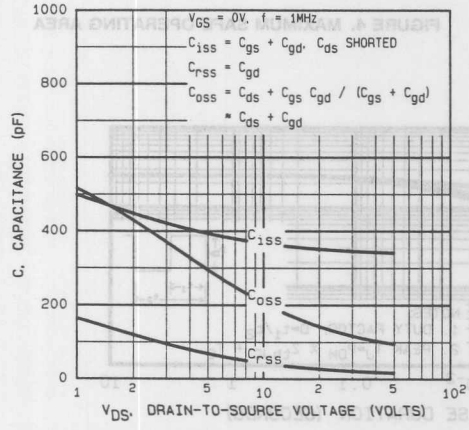


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

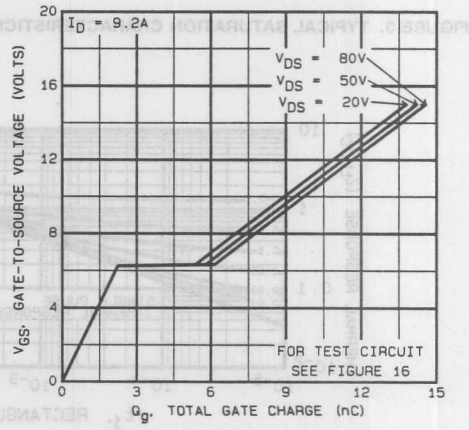


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

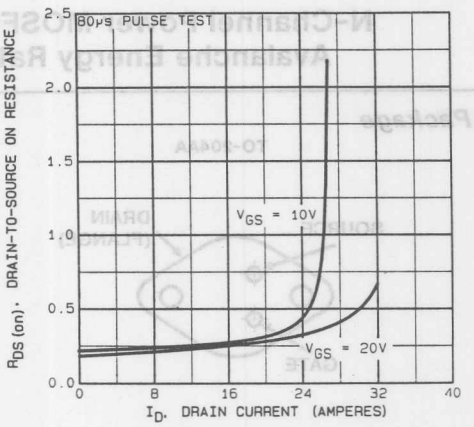


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

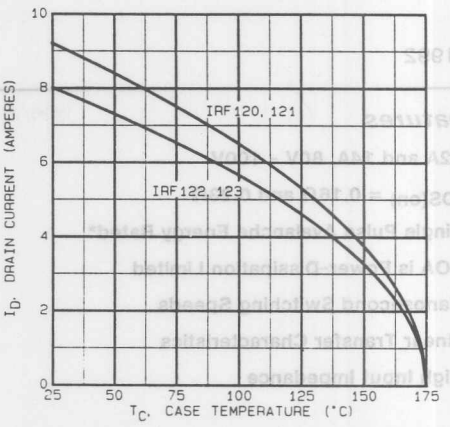


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

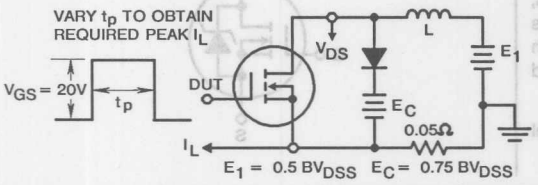


FIGURE 14. CLAMPED INDUCTIVE TEST CIRCUIT

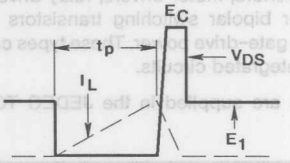


FIGURE 15. CLAMPED INDUCTIVE WAVEFORMS

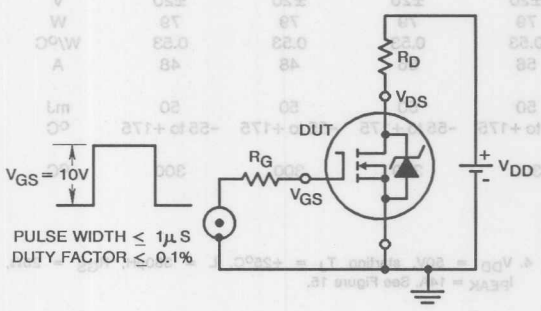


FIGURE 16. SWITCHING TIME TEST CIRCUIT

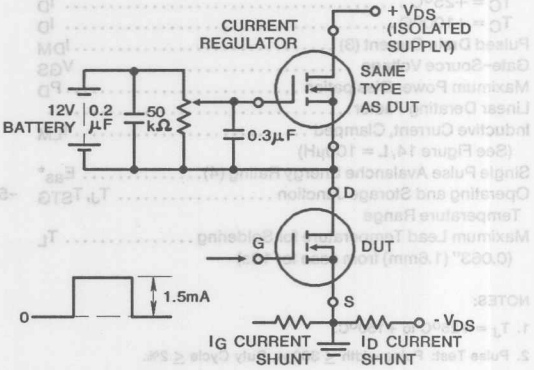


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF130/131/132/133
IRF130R/131R/132R/133R

N-Channel Power MOSFETs
Avalanche Energy Rated*

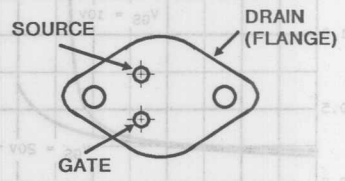
May 1992

Features

- 12A and 14A, 80V - 100V
- $r_{DS(on)}$ = 0.16Ω and 0.23Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AA



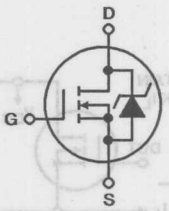
Description

The IRF130, IRF131, IRF132, and IRF133 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF130R, IRF131R, IRF132R, and IRF133R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF130 IRF130R	IRF131 IRF131R	IRF132 IRF132R	IRF133 IRF133R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	10	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	14	14	12	12	A
T_C = +100°C ..... I_D	9.9	9.9	8.3	8.3	A
Pulsed Drain Current (3) ..... I_{DM}	56	56	48	48	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D	79	79	79	79	W
Linear Derating Factor	0.53	0.53	0.53	0.53	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	56	56	48	48	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	50	50	50	50	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max junction temp. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 380μH, R_{GS} = 25Ω, I_{PEAK} = 14A. See Figure 15.

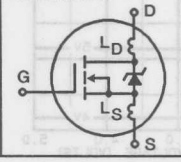
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

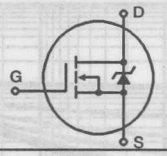
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File Number 1566.2

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF130/132, IRF130R/132R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	-	-	V
IRF131/133, IRF131R/133R			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRF130/131, IRF130R/131R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, V_{GS} = 10V	14	-	-	A
IRF132/133, IRF132R/133R			12	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF130/131, IRF130R/131R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8.3A	-	0.12	0.16	Ω
IRF132/133, IRF132R/133R			-	0.16	0.23	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 8.3A	4.6	6.9	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D = 14A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	-	30	ns
Rise Time	t_r		-	-	75	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	40	ns
Fall Time	t_f		-	-	45	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	18	26	nC
Gate-Source Charge	Q_{gs}		-	5.5	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	11	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.9	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	14	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	56	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 14A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/µs	55	120	250	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/µs	0.26	0.58	1.3	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 380µH, R_{GS} = 25Ω, I_{PEAK} = 145A (See Figure 15)

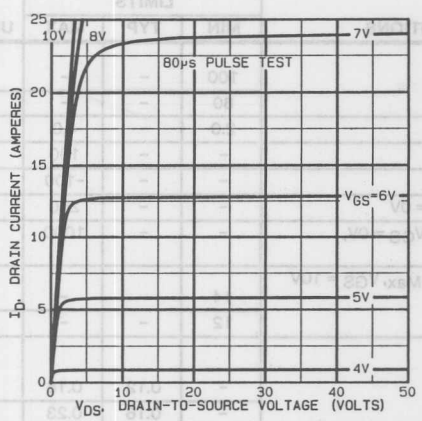


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

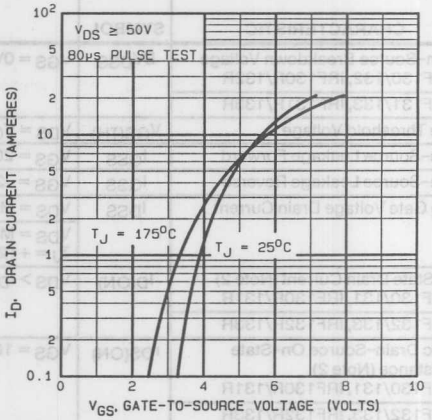


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

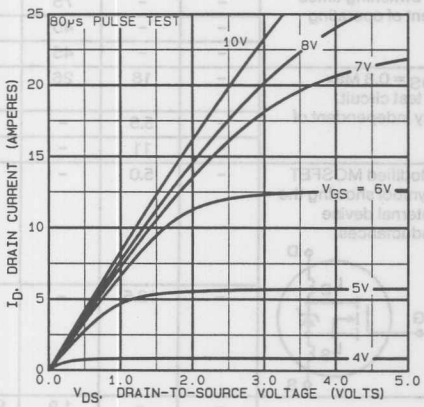


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

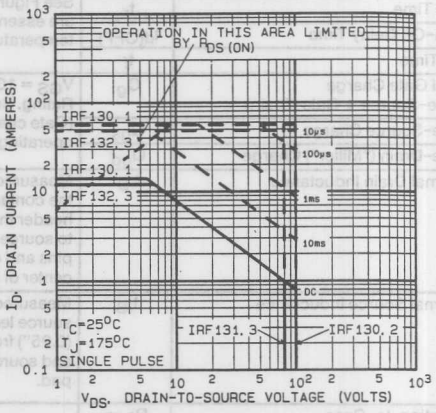


FIGURE 4. MAXIMUM SAFE OPERATING AREA

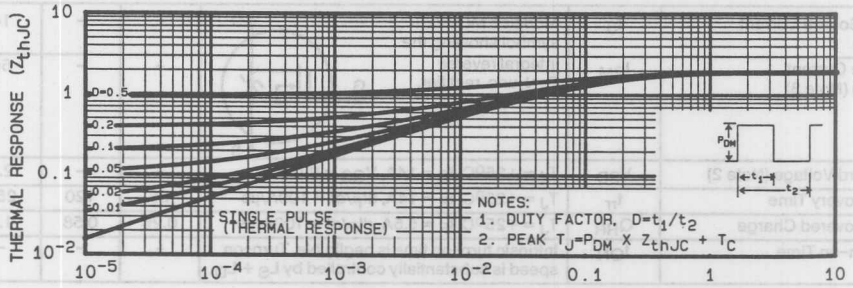


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

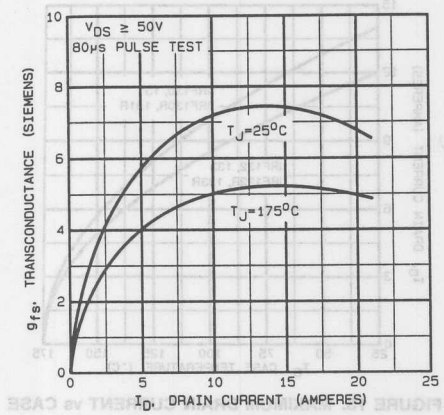


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

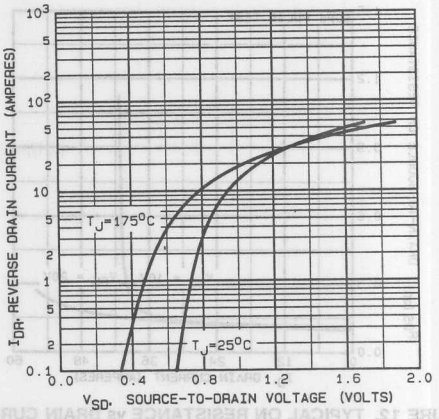


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

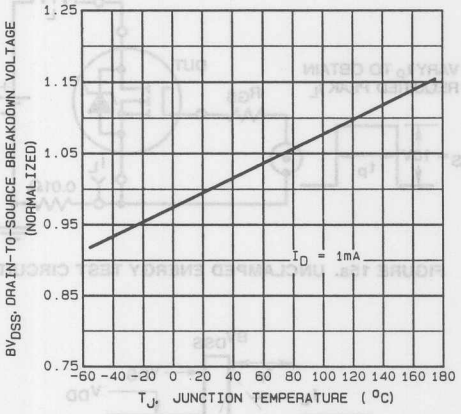


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

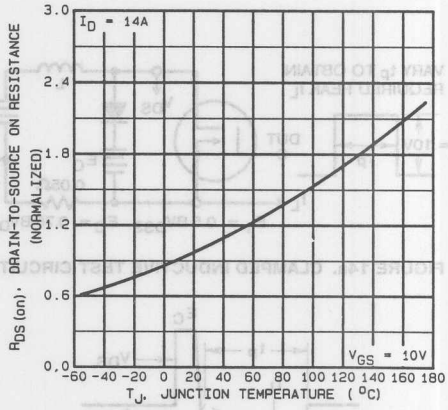


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

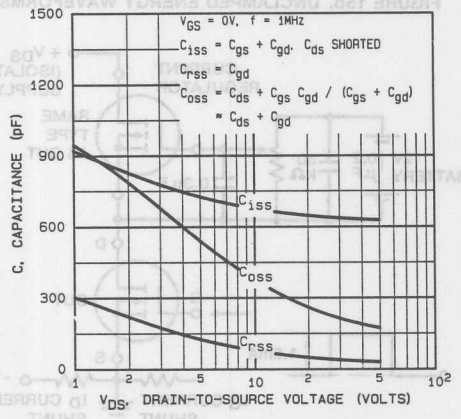


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

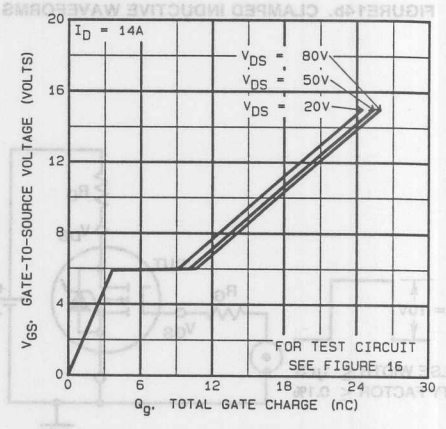


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

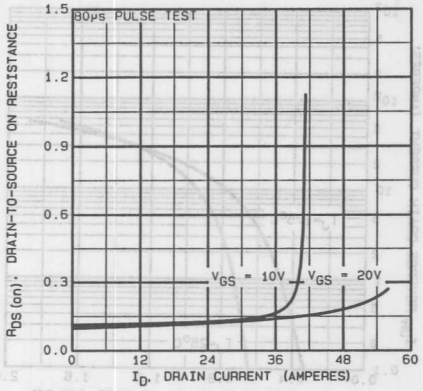


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

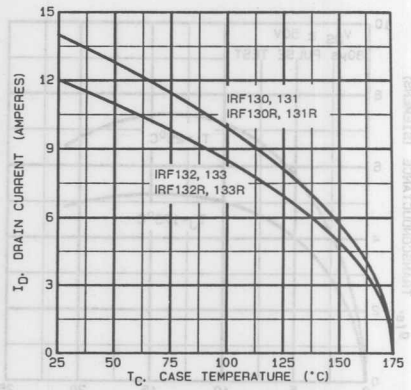


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

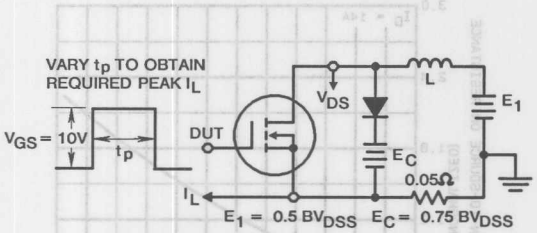


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

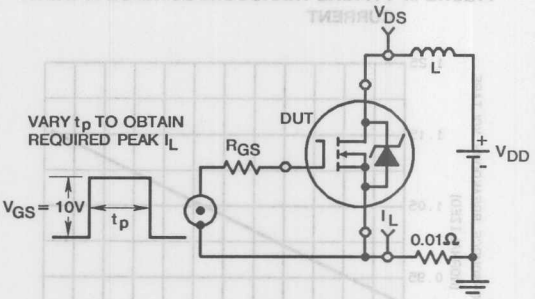


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

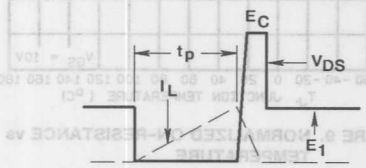


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

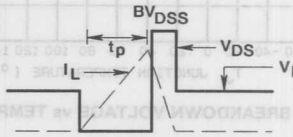


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

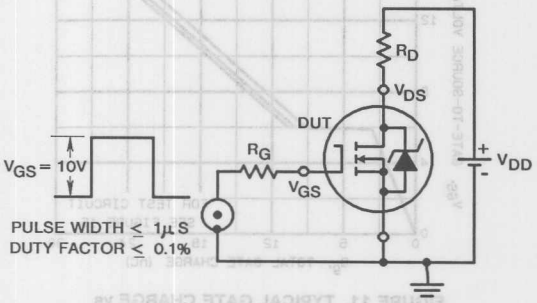


FIGURE 16. SWITCHING TIME TEST CIRCUIT

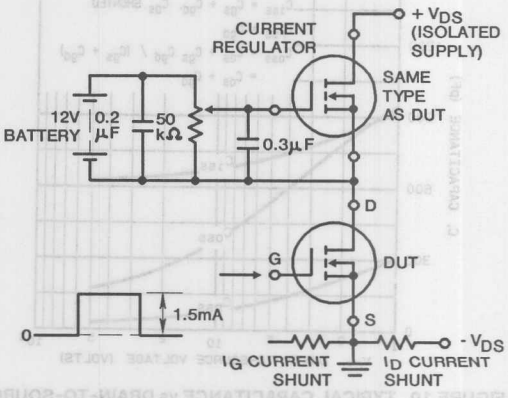


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS IRF140/141/142/143 IRF140R/141R/142R/143R

N-Channel Power MOSFETs Avalanche Energy Rated*

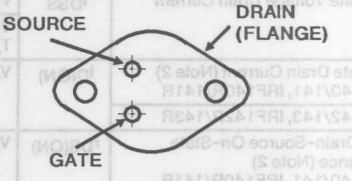
August 1991

Features

- 28A and 25A, 80V - 100V
- $r_{DS(on)}$ = 0.077Ω and 0.10Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AE



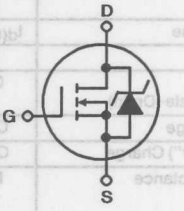
Description

The IRF140, IRF141, IRF142, and IRF143 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF140R, IRF141R, IRF142R, and IRF143R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AE steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF140 IRF140R	IRF141 IRF141R	IRF142 IRF142R	IRF143 IRF143R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	28	28	25	25	A
T_C = +100°C ..... I_D	20	20	17	17	A
Pulsed Drain Current (3) ..... I_{DM}	110	110	100	100	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D	150	150	150	150	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	108	108	96	96	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	100	100	100	100	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max junction temp. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 190μH, R_{GS} = 25Ω, I_{PEAK} = 28A. See Figure 15.

* R Suffix Types Only

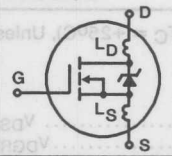
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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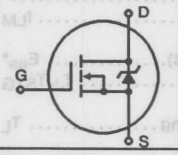
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF140/142, IRF140R/142R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	-	-	V
IRF141/143, IRF141R/143R			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRF140/141, IRF140R/141R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	28	-	-	A
IRF142/143, IRF142R/143R			25	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF140/141, IRF140R/141R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 17A	-	0.07	0.077	Ω
IRF142/143, IRF142R/143R			-	0.09	0.100	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 17A	8.7	13	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	1275	-	pF
Output Capacitance	C_{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	160	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D = 28A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	16	23	ns
Rise Time	t_r		-	27	110	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	38	60	ns
Fall Time	t_f		-	14	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 28A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	38	59	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	21	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	28	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	110	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 28A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 28A, dI_F/dt = 100A/µs	70	150	300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/µs	0.44	0.9	1.9	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 190µH, R_{GS} = 25Ω, I_{PEAK} = 28A (See Figure 15)

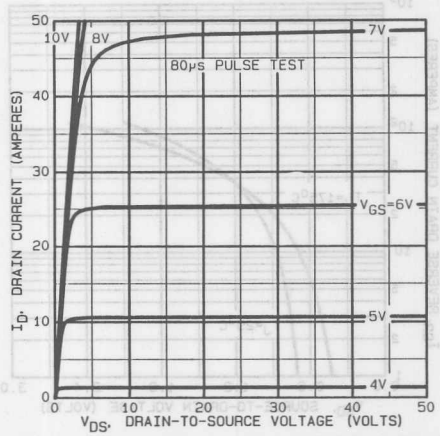


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

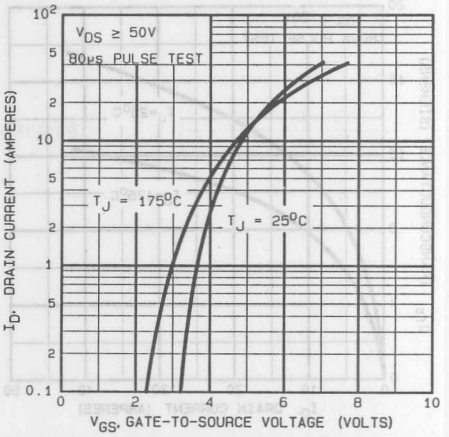


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

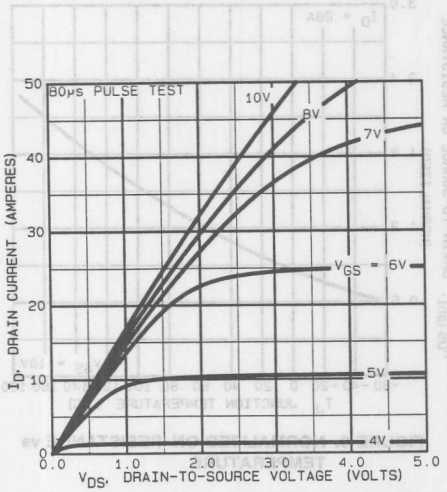


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

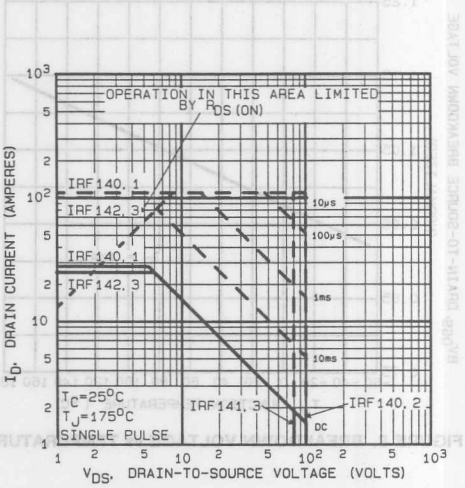


FIGURE 4. MAXIMUM SAFE OPERATING AREA

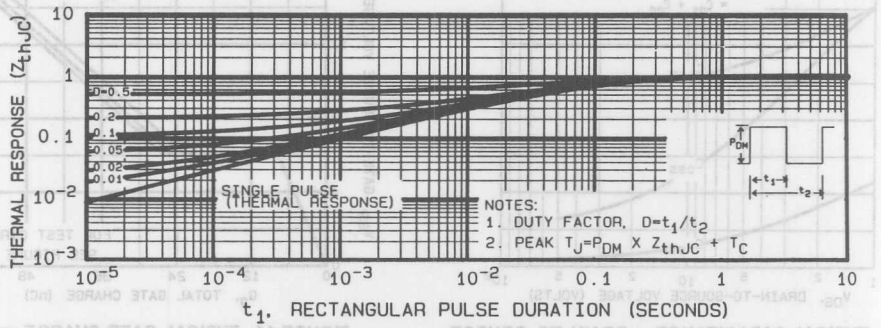


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

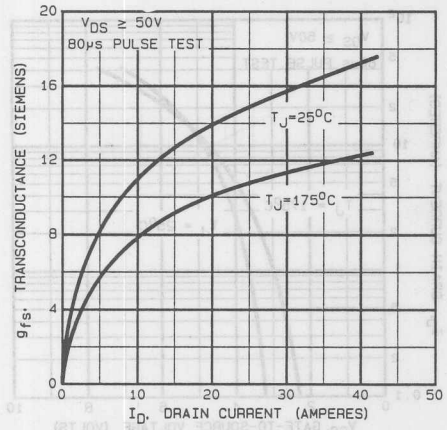


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

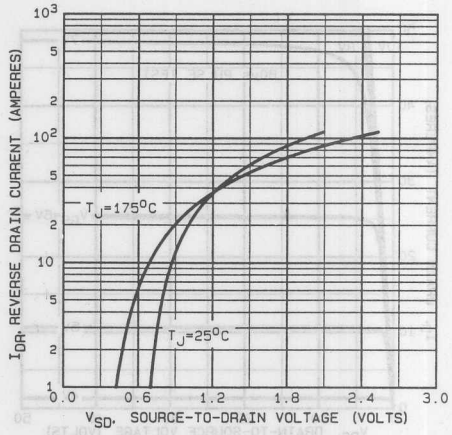


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

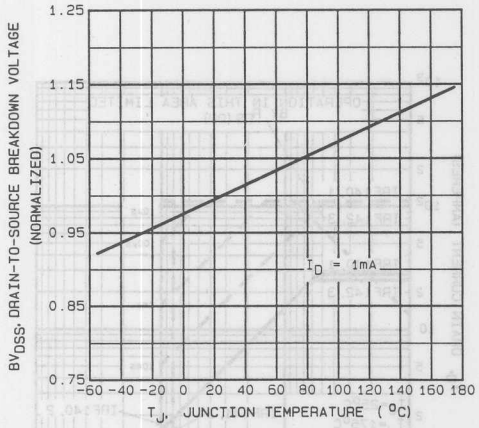


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

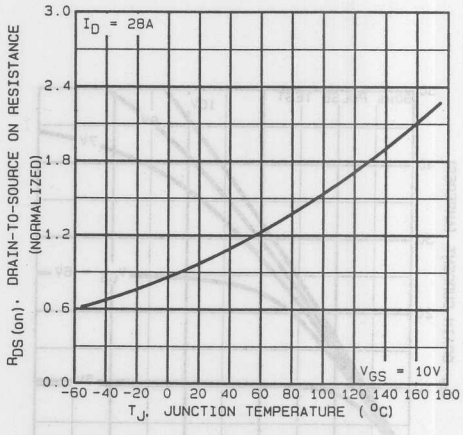


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

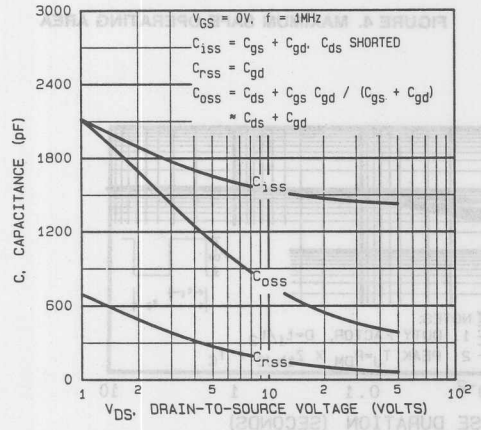


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

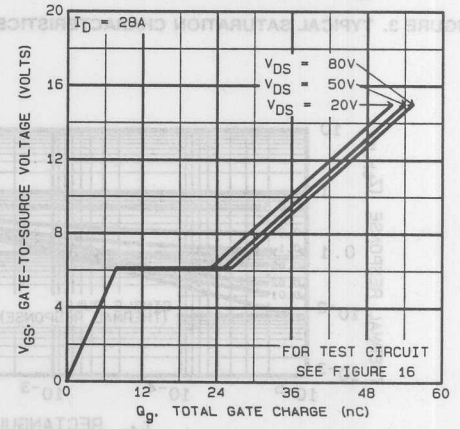


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

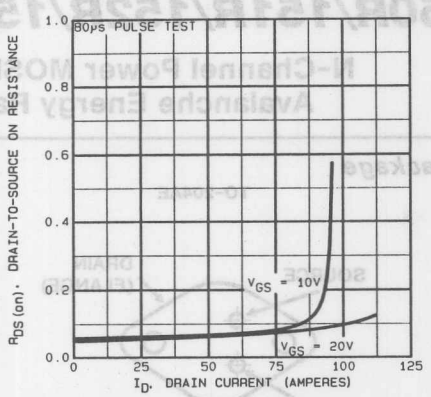


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

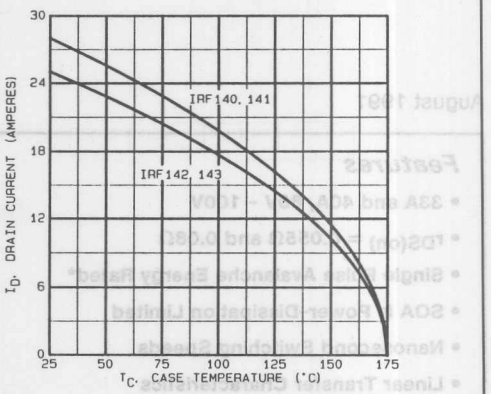


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

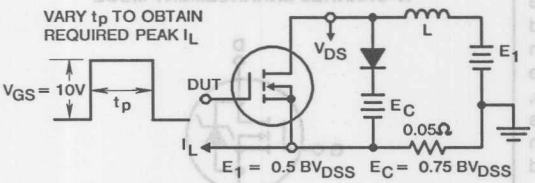


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

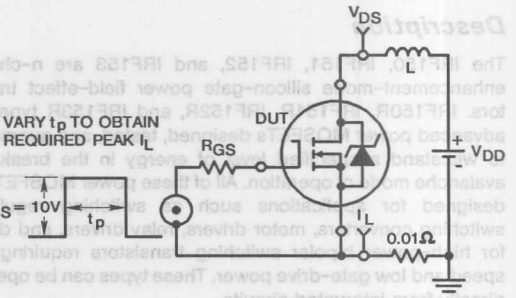


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

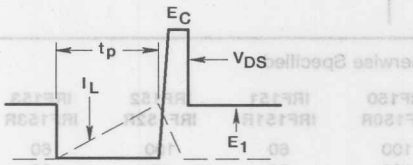


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

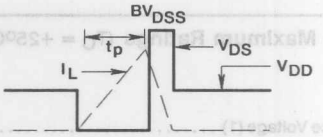


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

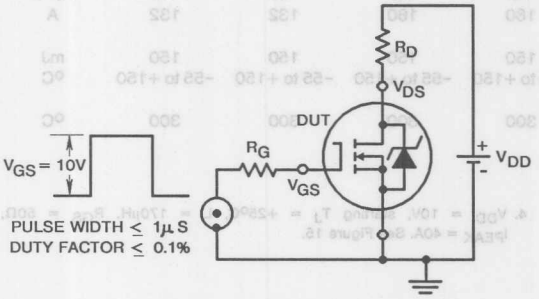


FIGURE 16. SWITCHING TIME TEST CIRCUIT

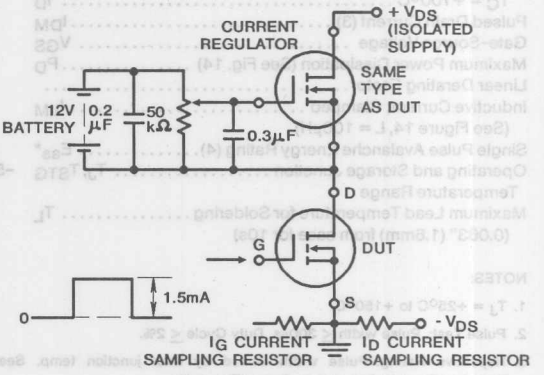


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF150/151/152/153
IRF150R/151R/152R/153R

N-Channel Power MOSFETs
Avalanche Energy Rated*

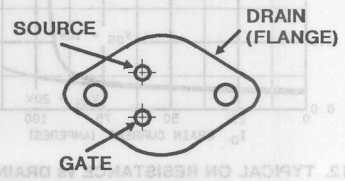
August 1991

Features

- 33A and 40A, 60V - 100V
- $r_{DS(on)}$ = 0.055Ω and 0.08Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AE



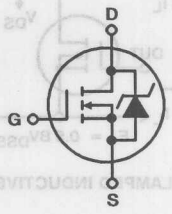
Description

The IRF150, IRF151, IRF152, and IRF153 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF150R, IRF151R, IRF152R, and IRF153R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AE steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF150 IRF150R	IRF151 IRF151R	IRF152 IRF152R	IRF153 IRF153R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	60	100	60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	60	10	60	V
Continuous Drain Current					
T_C = +25°C ..... I_D	40	40	33	33	A
T_C = +100°C ..... I_D	25	25	20	20	A
Pulsed Drain Current (3) ..... I_{DM}	160	160	132	132	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation (See Fig. 14) ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	160	160	132	132	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	150	150	150	150	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max junction temp. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 10V, starting T_J = +25°C, L = 170μH, R_{GS} = 50Ω, I_{PEAK} = 40A. See Figure 15.

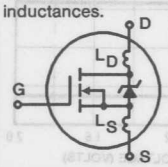
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

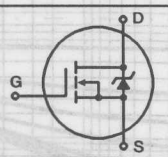
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File Number 1824.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF150/152, IRF150R/152R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	–	–	V
IRF151/153, IRF151R/153R			60	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF150/151, IRF150R/151R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	40	–	–	A
IRF152/153, IRF152R/153R			33	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF150/151, IRF150R/151R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 20A	–	0.045	0.055	Ω
IRF152/153, IRF152R/153R			–	0.06	0.08	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 20A	9.0	11	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2000	–	pF
Output Capacitance	C_{OSS}		–	1000	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	350	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 24V, I_D = 20A, Z_0 = 4.7Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	–	35	ns
Rise Time	t_r		–	–	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	–	125	ns
Fall Time	t_f		–	–	100	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 50A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	63	120	nC
Gate-Source Charge	Q_{gs}		–	27	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	36	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.8	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	40	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	160	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 40A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 40A, dI_F/dt = 100A/µs	–	600	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/µs	–	3.3	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 10V, Start T_J = +25°C, L = 170µH, R_{GS} = 50Ω, I_{PEAK} = 40A (See Figure 15)

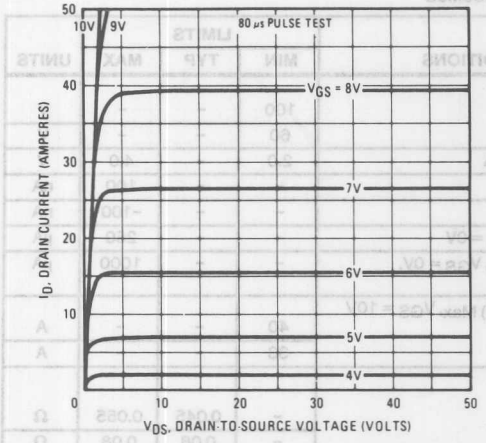


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

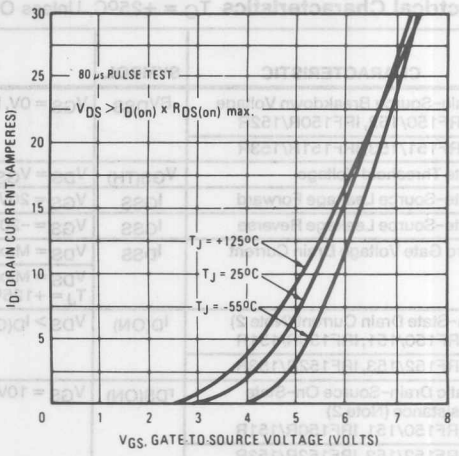


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

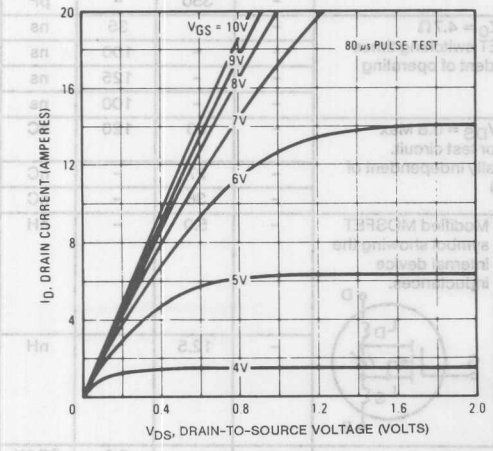


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

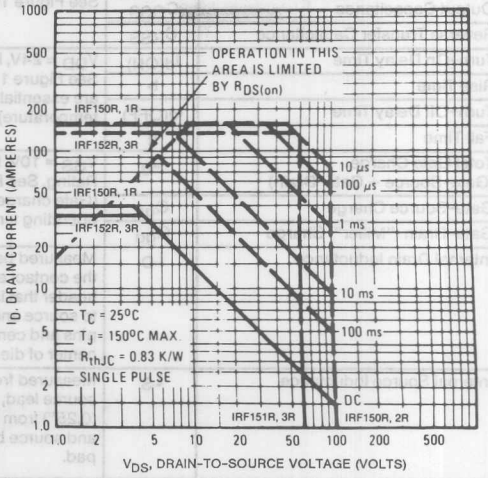


FIGURE 4. MAXIMUM SAFE OPERATING AREA

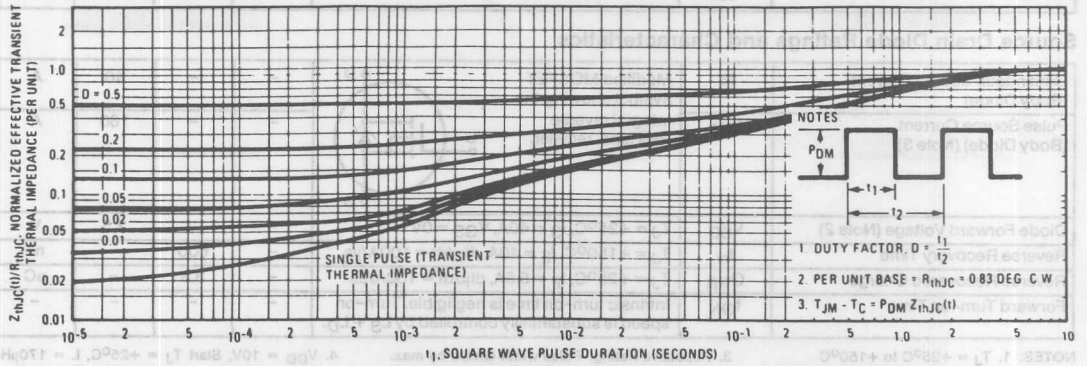


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

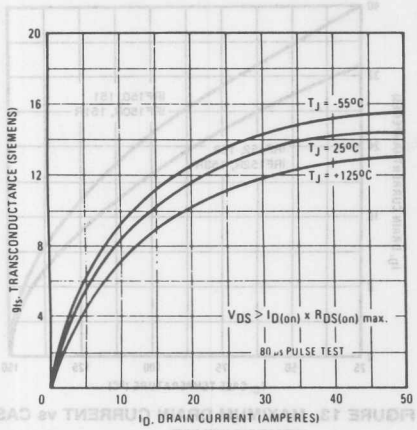


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

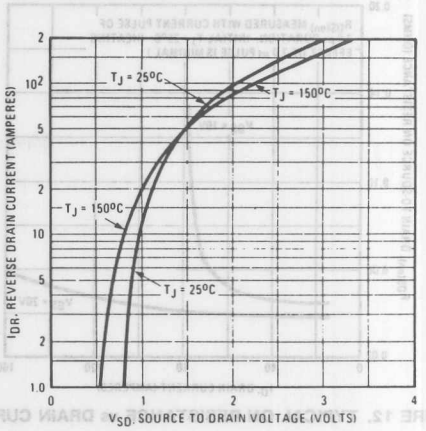


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

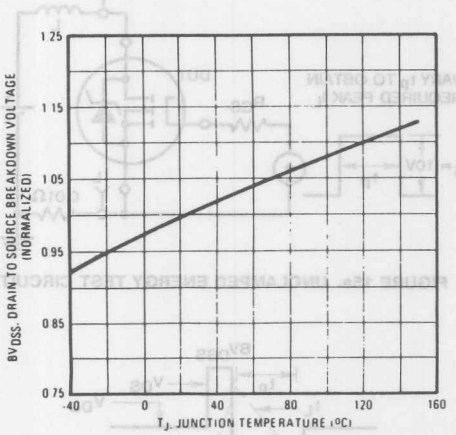


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

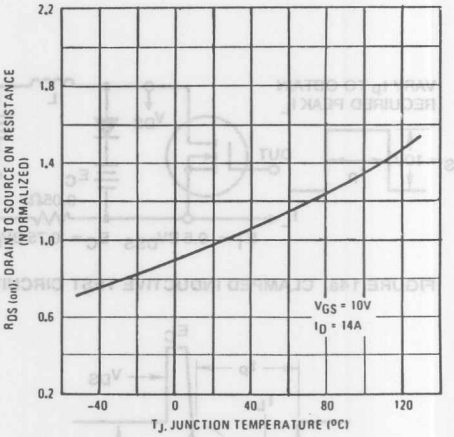


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

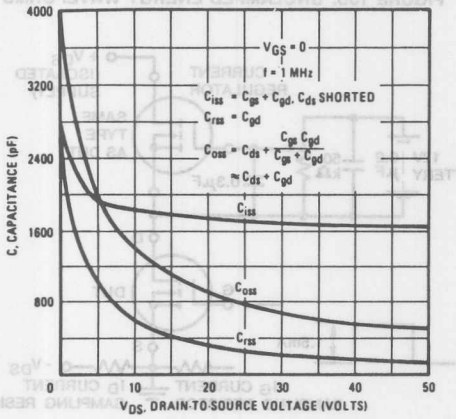


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

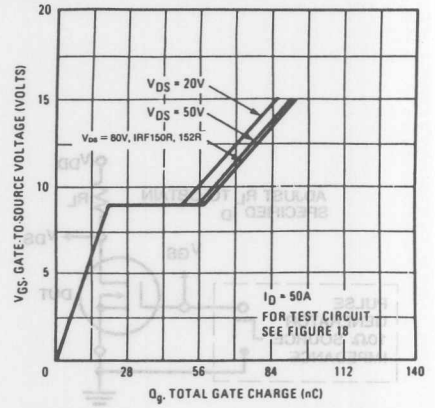


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

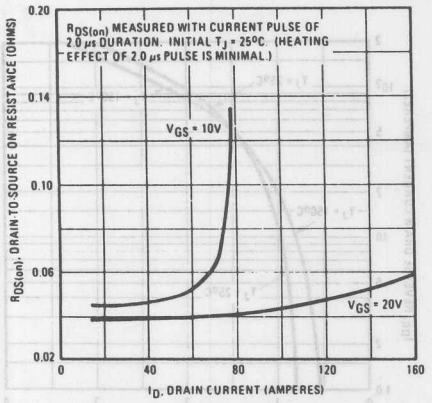


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

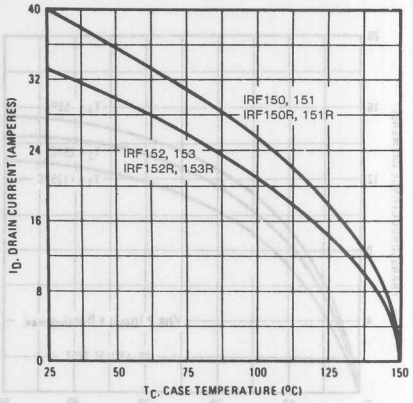


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

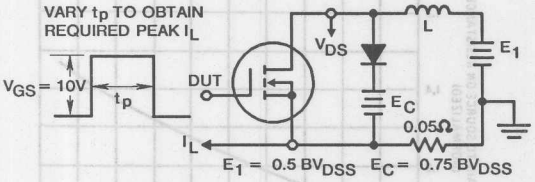


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

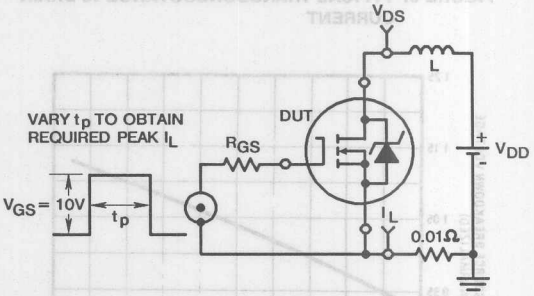


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

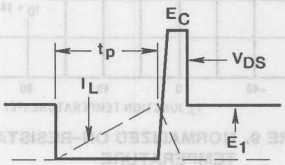


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

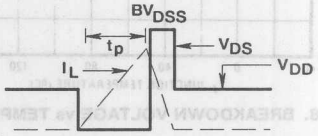


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

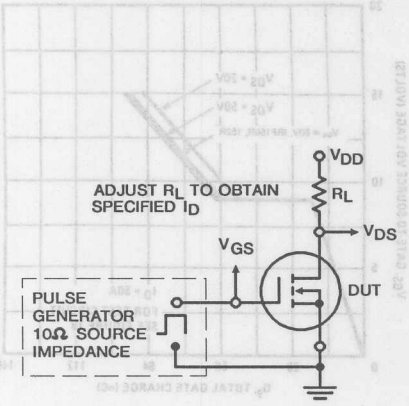


FIGURE 16. SWITCHING TIME TEST CIRCUIT

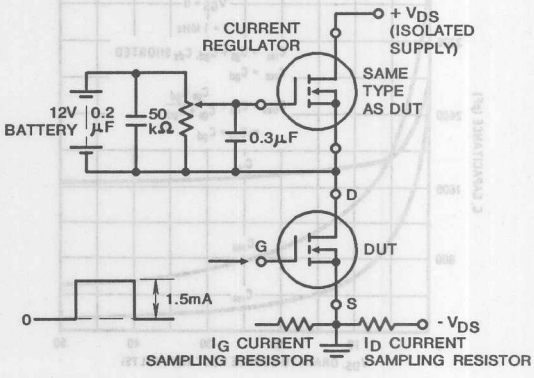


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRF220, IRF221
IRF222, IRF223

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 4.0A and 5.0A, 150V - 200V
- $r_{DS(on)}$ = 0.8Ω and 1.2Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

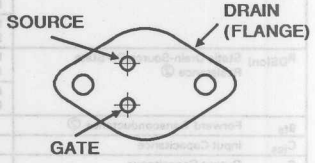
Description

The IRF220, IRF221, IRF222, and IRF223 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

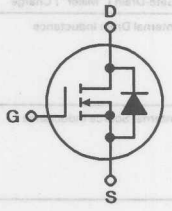
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		IRF220	IRF221	IRF222	IRF223	UNITS
Drain-Source Voltage (1)	V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	200	150	200	150	V
Continuous Drain Current						
T_C = +25°C	I_D	5.0	5.0	4.0	4.0	A
T_C = +100°C	I_D	3.0	3.0	2.5	2.5	A
Pulsed Drain Current (3)	I_{DM}	20	20	16	16	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C (See Figure 14)	P_D	40	40	40	40	W
Linear Derating Factor (See Figure 14)		0.32	0.32	0.32	0.32	W/°C
Inductive Current, Clamped (See Figures 14 and 15, L = 100μH)	I_{LM}	20	20	16	16	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-50 to +150	-50 to +150	-50 to +150	-50 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

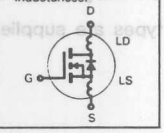
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File Number **1567.1**

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF220 IRF222	200	–	–	V	V_{GS} = 0V
		IRF221 IRF223	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF220 IRF221	5.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		IRF222 IRF223	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF220 IRF221	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF222 IRF223	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF220 IRF221	–	–	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF222 IRF223	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF220 IRF221	–	–	20	A	
		IRF222 IRF223	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF220 IRF221	–	–	2.0	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
		IRF222 IRF223	–	–	1.8	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	350	–	ns	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.3	–	μC	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

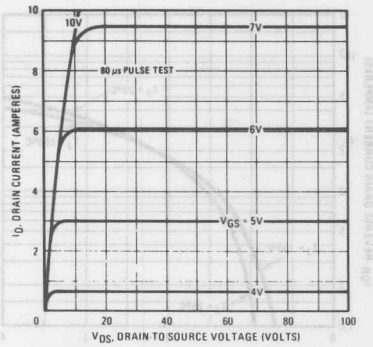


Fig. 1 – Typical Output Characteristics

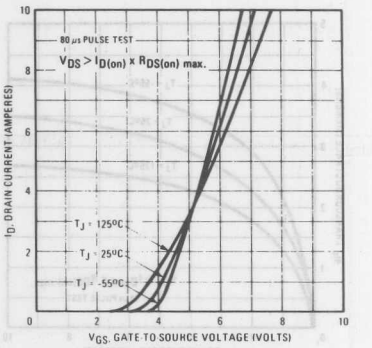


Fig. 2 – Typical Transfer Characteristics

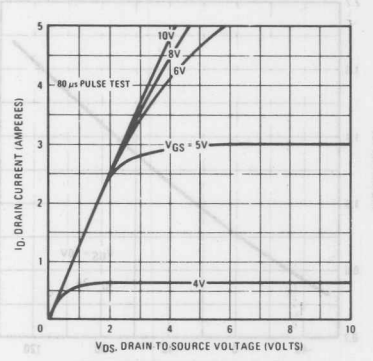


Fig. 3 – Typical Saturation Characteristics

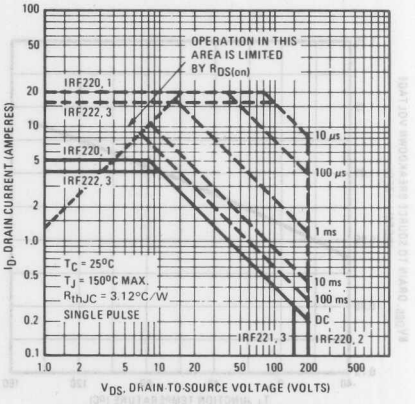


Fig. 4 – Maximum Safe Operating Area

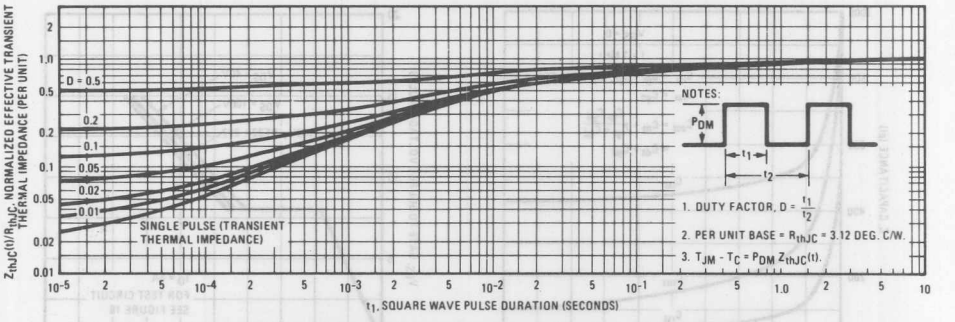


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

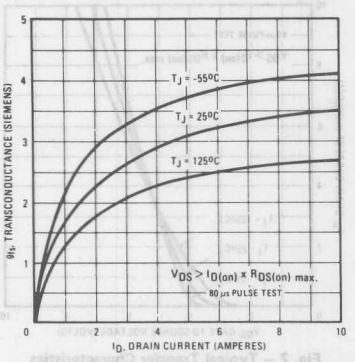


Fig. 6 – Typical Transconductance Vs. Drain Current

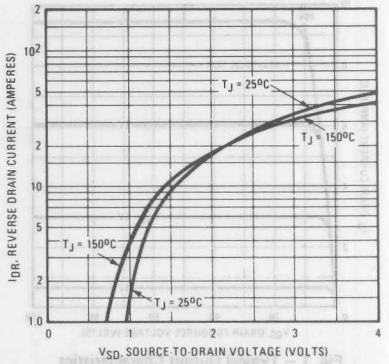


Fig. 7 – Typical Source-Drain Diode Forward Voltage

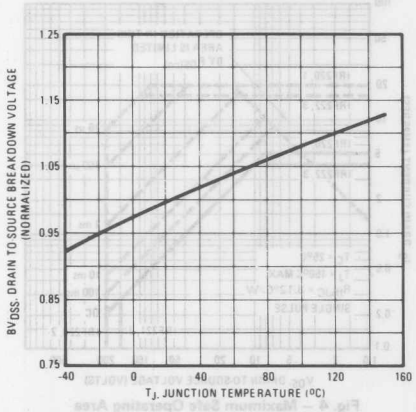


Fig. 8 – Breakdown Voltage Vs. Temperature

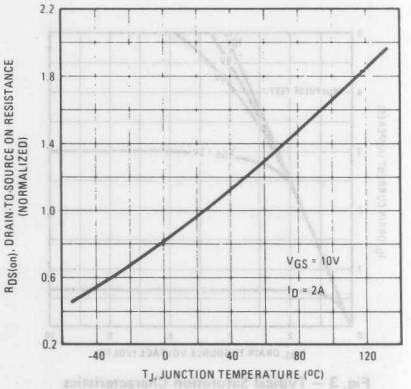


Fig. 9 – Normalized On-Resistance Vs. Temperature

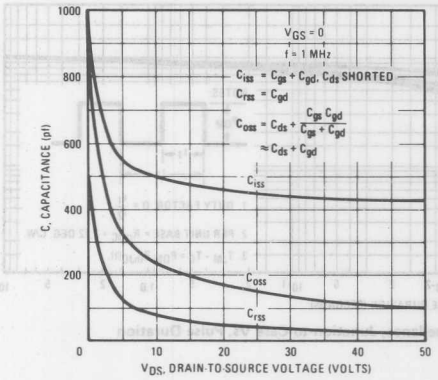


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

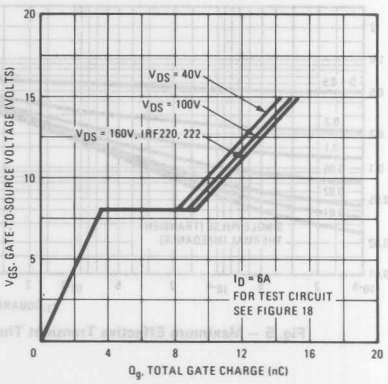


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

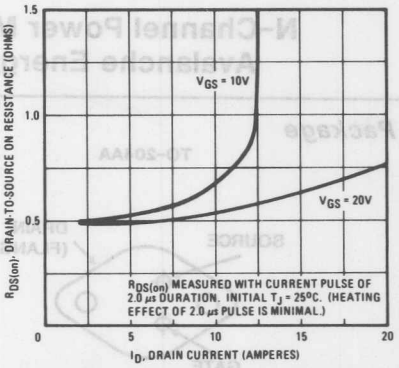


Fig. 12 – Typical On-Resistance Vs. Drain Current

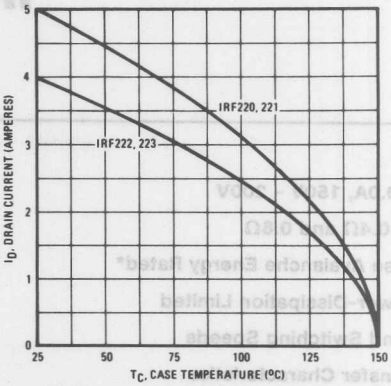


Fig. 13 – Maximum Drain Current Vs. Case Temperature

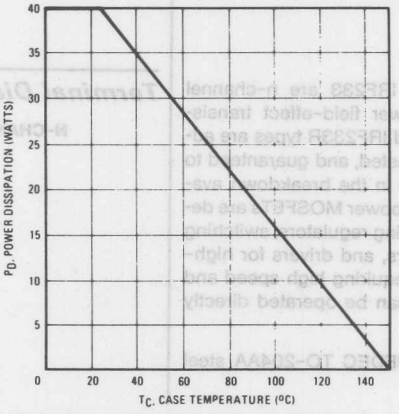


Fig. 14 – Power Vs. Temperature Derating Curve

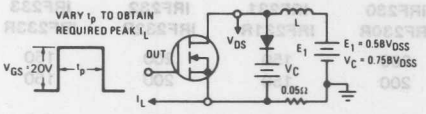


Fig. 15 – Clamped Inductive Test Circuit



Fig. 16 – Clamped Inductive Waveforms

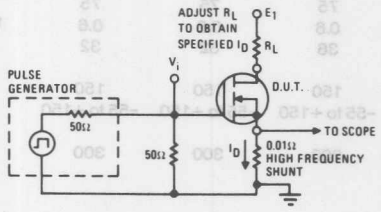


Fig. 17 – Switching Time Test Circuit

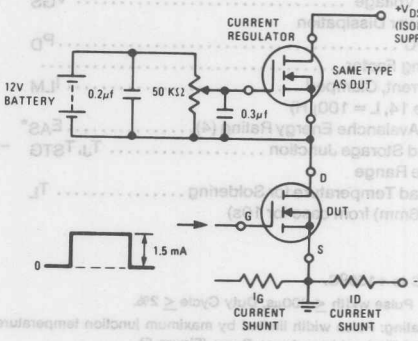


Fig. 18 – Gate Charge Test Circuit

HARRIS

IRF230/231/232/233
IRF230R/231R/232R/233R

N-Channel Power MOSFETs
Avalanche Energy Rated*

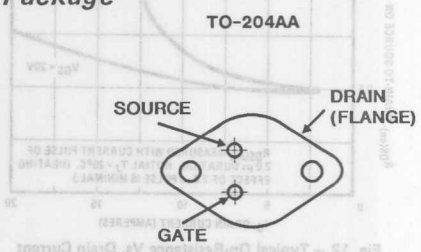
August 1991

Features

- 8.0A and 9.0A, 150V - 200V
- $r_{DS}(on)$ = 0.4Ω and 0.6Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AA



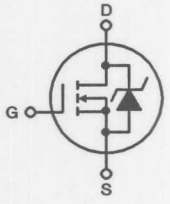
Description

The IRF230, IRF231, IRF232, and IRF233 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF230R, IRF231R, IRF232R and IRF233R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	IRF230 IRF230R	IRF231 IRF231R	IRF232 IRF232R	IRF233 IRF233R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	9.0	9.0	8.0	8.0	A
T_C = +100°C ..... I_D	6.0	6.0	5.0	5.0	A
Pulsed Drain Current (3) ..... I_{DM}	36	36	32	32	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	36	36	32	32	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	150	150	150	150	mj
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 20V, starting T_J = +25°C, L = 3.37mH, R_{GS} = 50Ω, I_{PEAK} = 9A. See Figure 15.

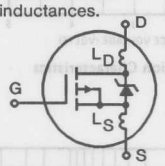
*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

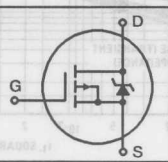
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File Number **1568.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF230/232, IRF230R/232R	BV_{DSS}	V_{GS} = 0V, I_D = -250µA	200	-	-	V
IRF231/233, IRF231R/233R			150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRF230/231, IRF230R/231R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	9.0	-	-	A
IRF232/233, IRF232R/233R			8.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF230/231, IRF230R/231R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.0A	-	0.25	0.4	Ω
IRF232/233, IRF232R/233R			-	0.4	0.6	Ω
Forward Transconductance (Note 2)	g_{ts}	V_{DS} > 50V, I_D = 5.0A	3.0	4.8	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	250	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	80	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 90V, I_D = 5.0A, Zo = 15Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature)	-	-	30	ns
Rise Time	t_r		-	-	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	50	ns
Fall Time	t_f		-	-	40	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8V Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	19	30	nC
Gate-Source Charge	Q_{gs}		-	10	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	9.0	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.6	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	9.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	36	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 9A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 9.0A, dI_F/dt = 100A/µs	-	450	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 9.0A, dI_F/dt = 100A/µs	-	3.0	-	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 20V, Start T_J = +25°C, L = 3.37mH, R_{GS} = 50Ω, I_{PEAK} = 9A (See Figure 15)

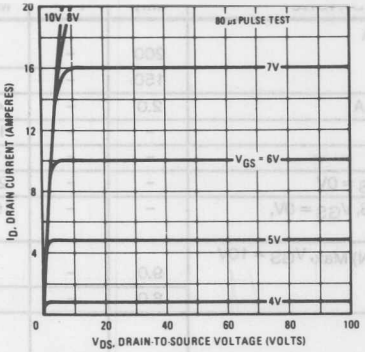


Fig. 1 – Typical Output Characteristics

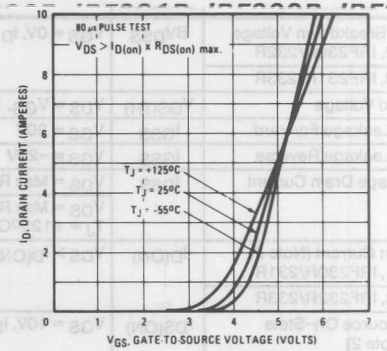


Fig. 2 – Typical Transfer Characteristics

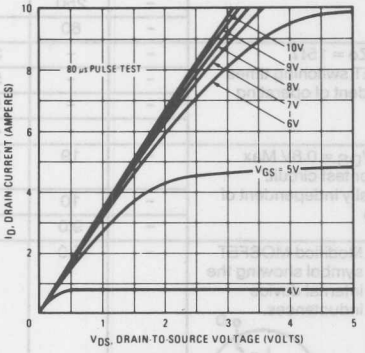


Fig. 3 – Typical Saturation Characteristics

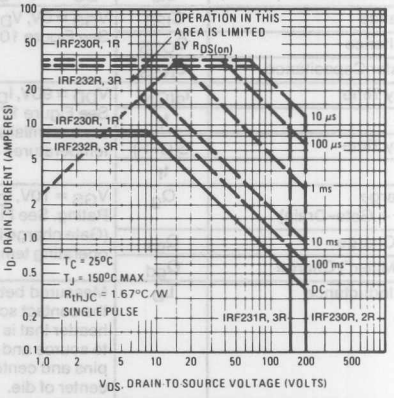


Fig. 4 – Maximum Safe Operating Area

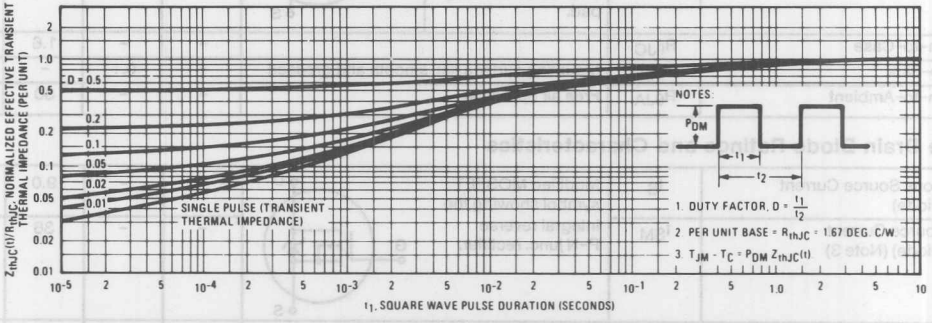


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

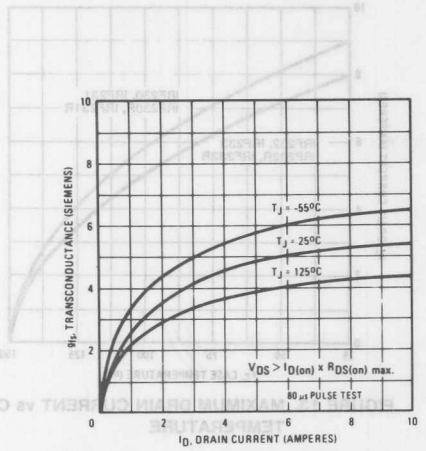


Fig. 6 – Typical Transconductance Vs. Drain Current

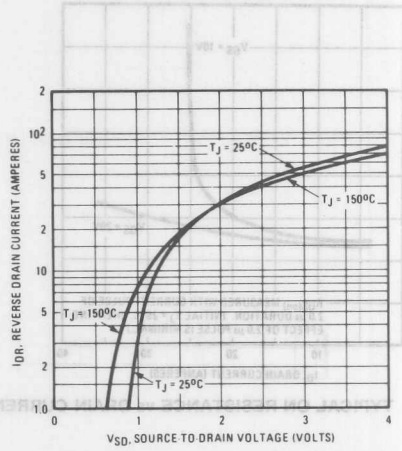


Fig. 7 – Typical Source-Drain Diode Forward Voltage

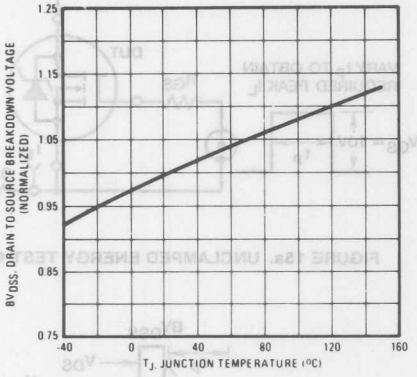


Fig. 8 – Breakdown Voltage Vs. Temperature

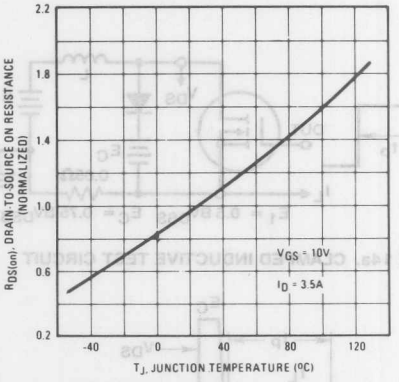


Fig. 9 – Normalized On-Resistance Vs. Temperature

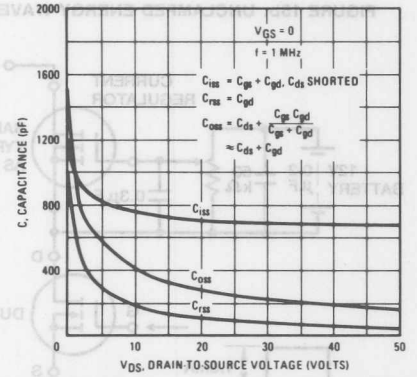


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

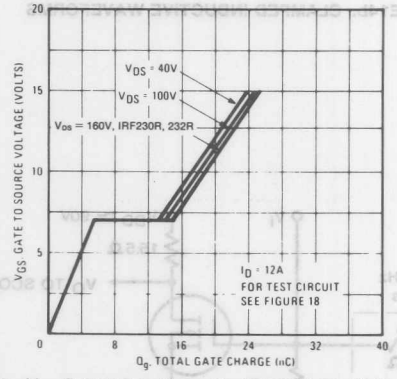


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

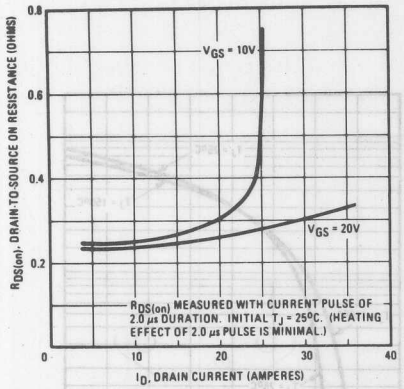


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

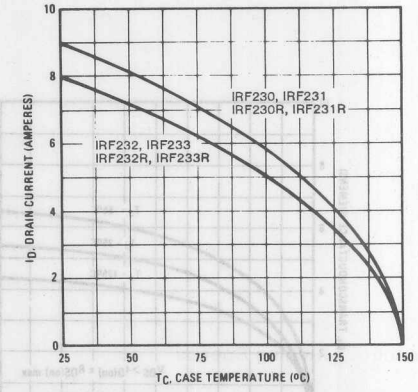


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

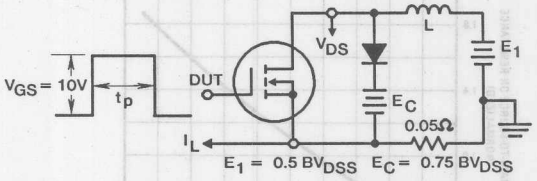


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

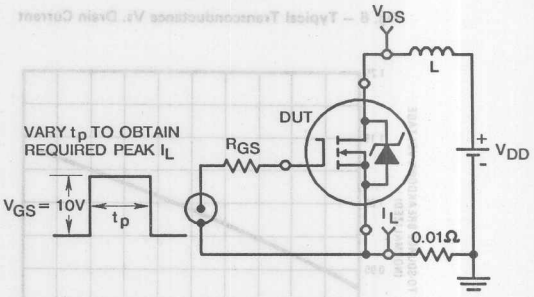


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

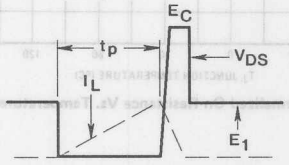


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

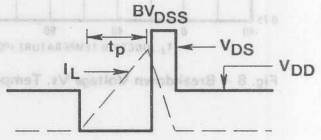


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

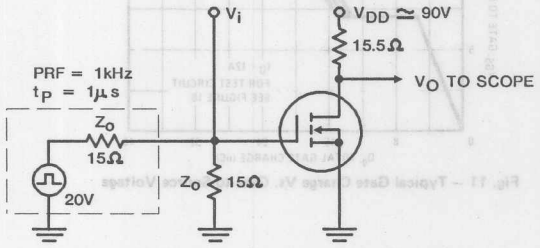


FIGURE 16. SWITCHING TIME TEST CIRCUIT

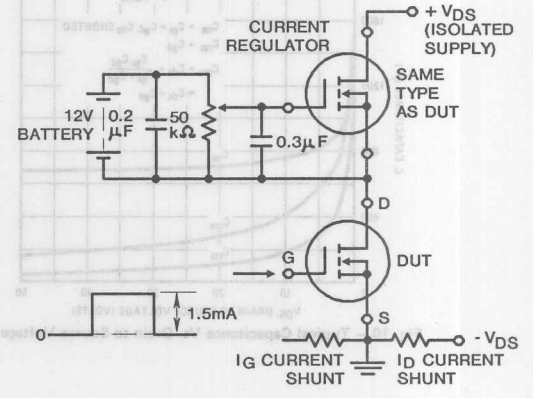


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF234, IRF235 IRF236, IRF237

N-Channel Power MOSFETs Avalanche-Energy Rated

May 1992

Features

- 8.1A and 6.5A, 275V - 250V
- $r_{DS}(on)$ = 0.45Ω and 0.68Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275V, 250V Rating - 120V AC Line System Operation

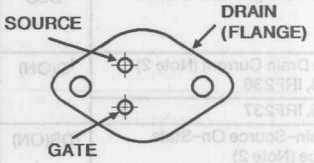
Description

The IRF234, IRF235, IRF236, and IRF237 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

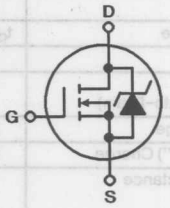
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		IRF234	IRF235	IRF236	IRF237	UNITS
Drain-Source Voltage (1)	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current						
T_C = +25°C	I_D	8.1	6.5	8.1	6.5	A
T_C = +100°C	I_D	5.1	4.1	5.1	4.1	A
Pulsed Drain Current (3)	I_{DM}	32	26	32	26	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	75	75	75	75	W
Linear Derating Factor		0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{AS}	180	180	180	180	mj
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

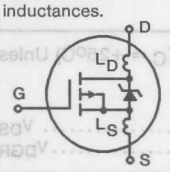
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 8.1A. See Figures 14 & 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

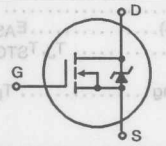
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File Number 2208.2

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF236, IRF237	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	275	-	-	V
IRF234, IRF235			250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF234, IRF236	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, V_{GS} = 10V	8.1	-	-	A
IRF235, IRF237			6.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF234, IRF236	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.1A	-	0.32	0.45	Ω
IRF235, IRF237			-	0.48	0.68	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 2 X V_{GS}, I_D = 4.1A	2.9	4.3	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	180	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	52	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 8.1A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	9.1	14	ns
Rise Time	t_r		-	23	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	31	47	ns
Fall Time	t_f		-	19	29	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8.1A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	24	35	nC
Gate-Source Charge	Q_{gs}		-	5.1	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	8.1	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.1A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 8.1A, dI_F/dt = 100A/μs	92	180	390	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 8.1A, dI_F/dt = 100A/μs	0.63	1.3	2.7	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 8.1A (See Figures 14 & 15)

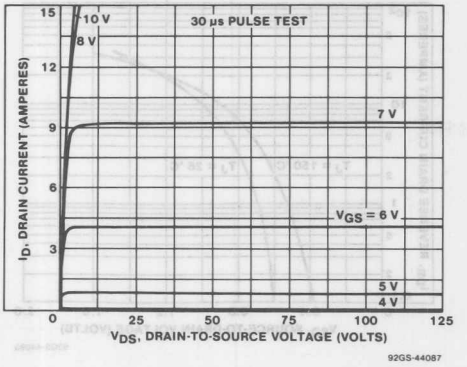


Fig. 1 - Typical output characteristics.

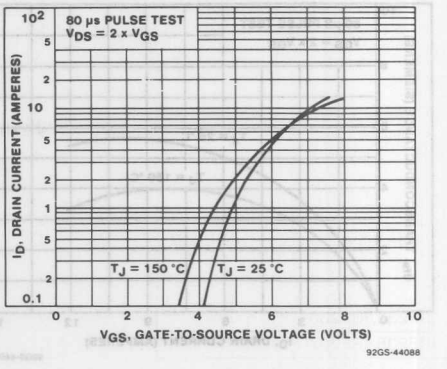


Fig. 2 - Typical transfer characteristics.

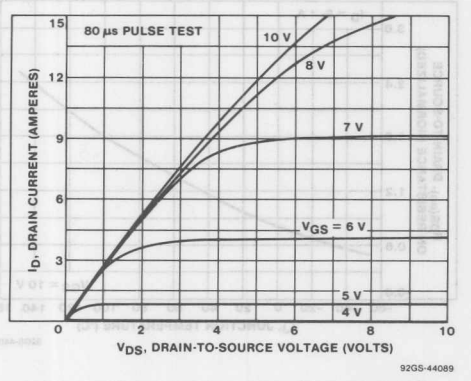


Fig. 3 - Typical saturation characteristics.

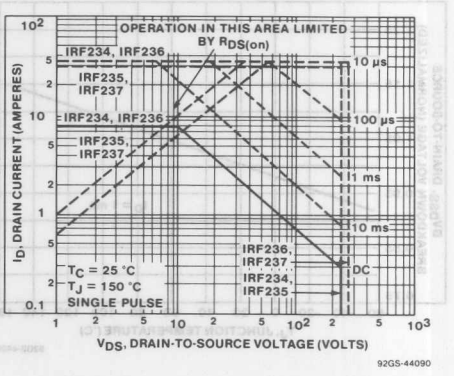


Fig. 4 - Maximum safe operating area.

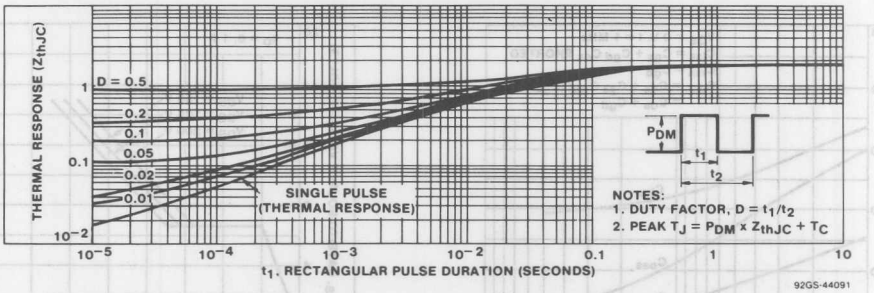


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

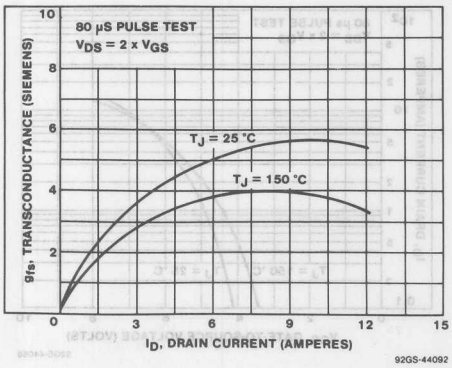


Fig. 6 - Typical transconductance vs. drain current.

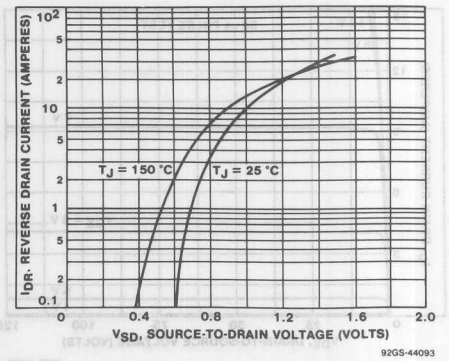


Fig. 7 - Typical source-drain diode forward voltage.

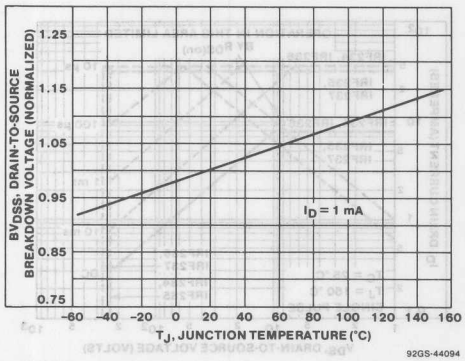


Fig. 8 - Breakdown voltage vs. temperature.

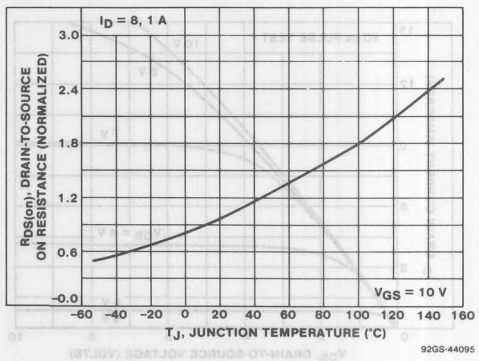


Fig. 9 - Normalized on-resistance vs. temperature.

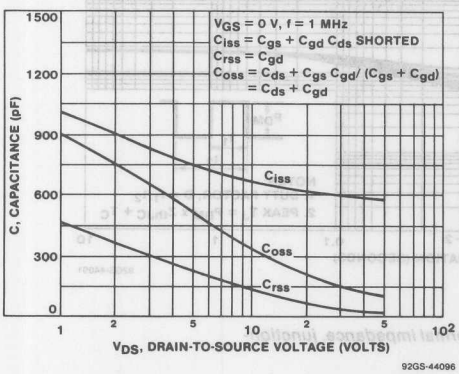


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

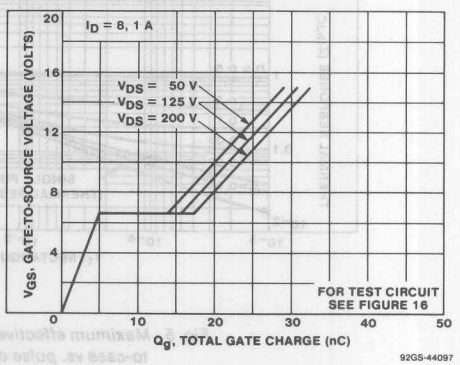


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

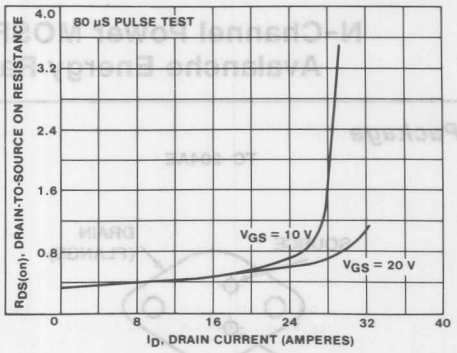


Figure 12. Typical On Resistance vs Drain Current

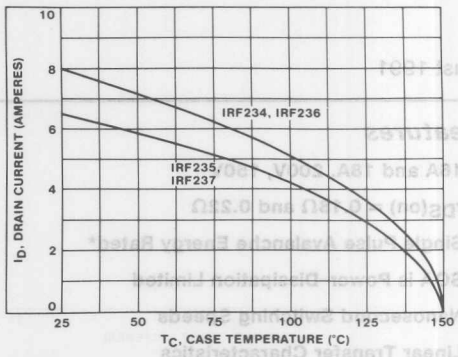


Figure 13. Maximum Drain Current vs Case Temperature

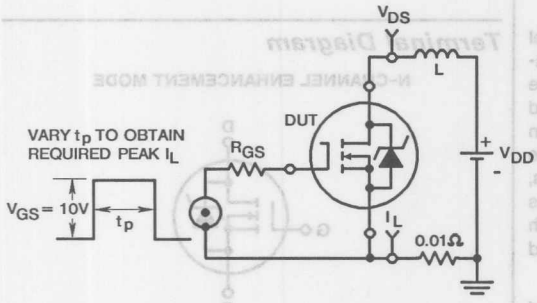


Figure 14. Unclamped Energy Test Circuit

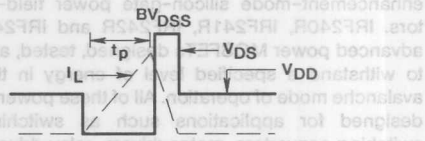


Figure 15. Unclamped Energy Waveforms

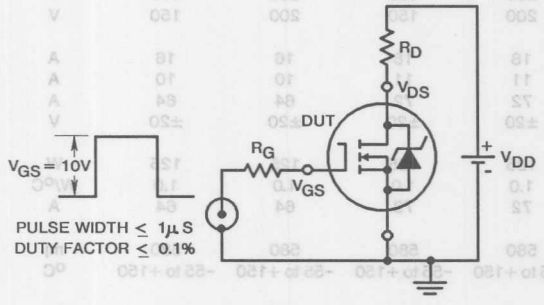


Figure16. Switching Time Test Circuit

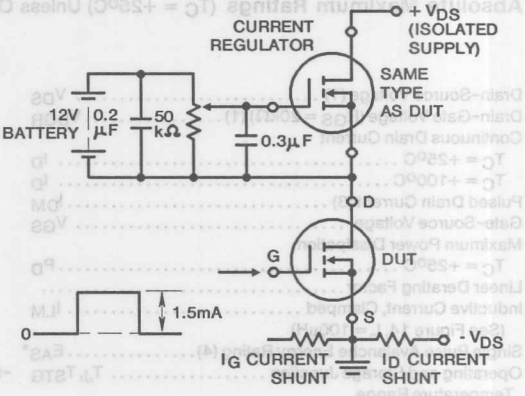


Figure 17. Gate Charge Test Circuit

HARRIS

IRF240/241/242/243
IRF240R/241R/242R/243R

N-Channel Power MOSFETs
Avalanche Energy Rated*

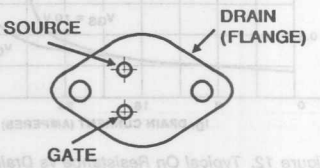
August 1991

Features

- 16A and 18A, 200V, 150V
- $r_{DS}(on)$ = 0.18Ω and 0.22Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AE



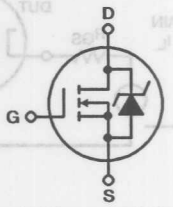
Description

The IRF240, IRF241, IRF242, and IRF243 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF240R, IRF241R, IRF242R and IRF243R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	IRF240 IRF240R	IRF241 IRF241R	IRF242 IRF242R	IRF243 IRF243R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	18	18	16	16	A
T_C = +100°C ..... I_D	11	11	10	10	A
Pulsed Drain Current (3) ..... I_{DM}	72	72	64	64	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	72	72	64	64	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	580	580	580	580	mj
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 2.7mH, R_{GS} = 25Ω, I_{PEAK} = 9A. See Figure 15.

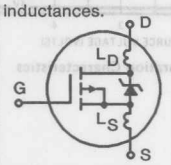
*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

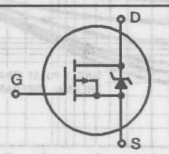
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File Number **1584.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF240/242, IRF240R/242R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRF241/243, IRF241R/243R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF240/241, IRF240R/241R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\,Max}$, V_{GS} = 10V	18	–	–	A
IRF242/243, IRF242R/243R			16	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF240/241, IRF240R/241R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 10A	–	0.14	0.18	Ω
IRF242/243, IRF242R/243R			–	0.20	0.22	Ω
Forward Transconductance (Note 2)	g_{ts}	V_{DS} > ID(ON) x $r_{DS(ON)Max}$, I_D = 10A	6.7	9.0	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1275	–	pF
Output Capacitance	C_{OSS}		–	500	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	160	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, I_D = 18A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	16	30	ns
Rise Time	t_r		–	27	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	40	80	ns
Fall Time	t_f		–	31	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	43	60	nC
Gate-Source Charge	Q_{gs}		–	8	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	27	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	18	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	72	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 18A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 18A, dI_F/dt = 100A/µs	–	650	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 18A, dI_F/dt = 100A/µs	–	4.1	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 2.7mH, R_{GS} = 25Ω, I_{PEAK} = 18A (See Figure 15)

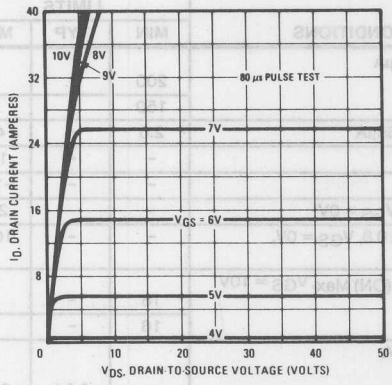


Fig. 1 – Typical Output Characteristics

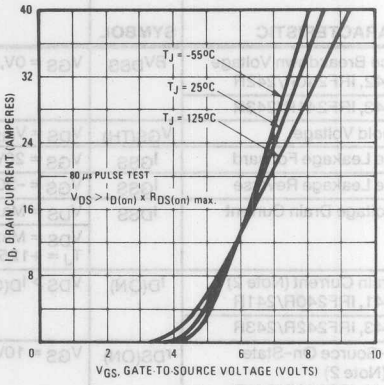


Fig. 2 – Typical Transfer Characteristics

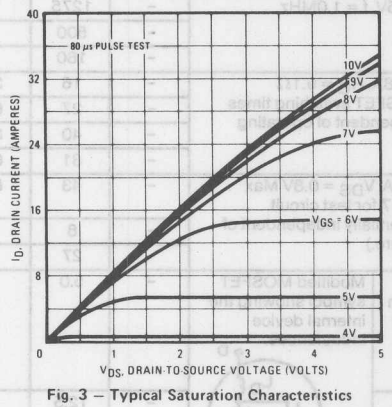


Fig. 3 – Typical Saturation Characteristics

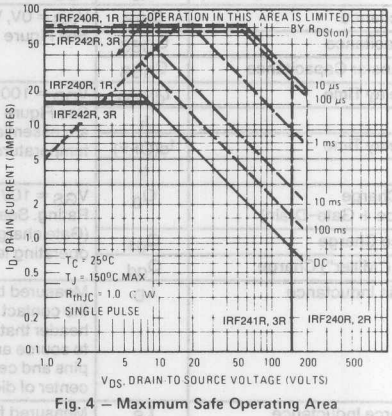


Fig. 4 – Maximum Safe Operating Area

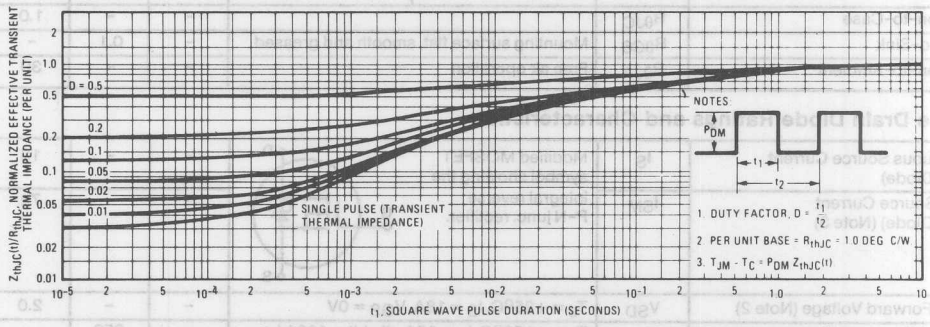


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

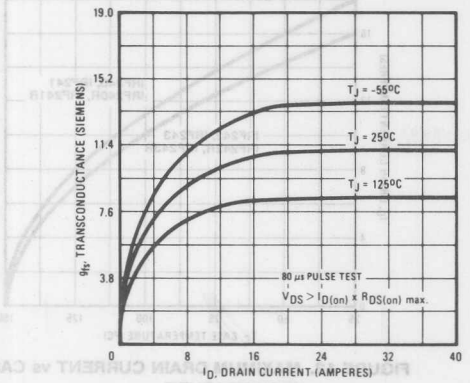


Fig. 6 – Typical Transconductance Vs. Drain Current

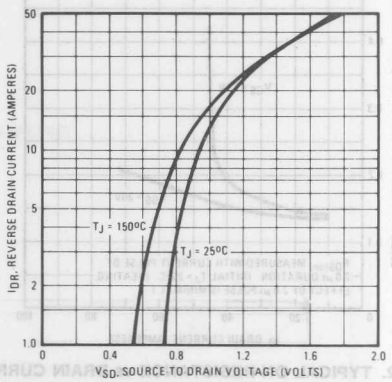


Fig. 7 – Typical Source-Drain Diode Forward Voltage

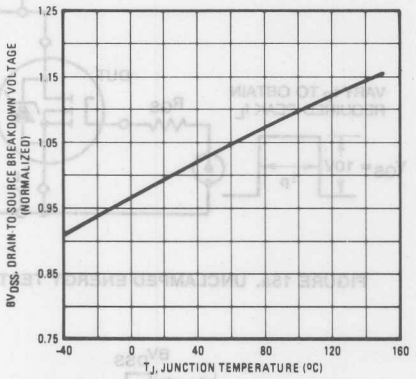


Fig. 8 – Breakdown Voltage Vs. Temperature

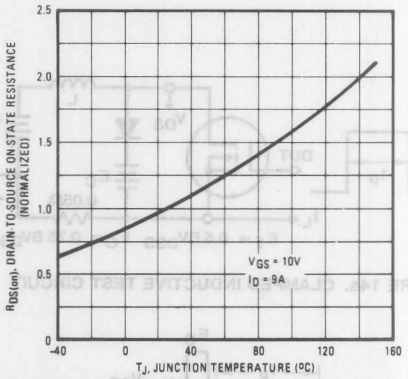


Fig. 9 – Normalized On-Resistance Vs. Temperature

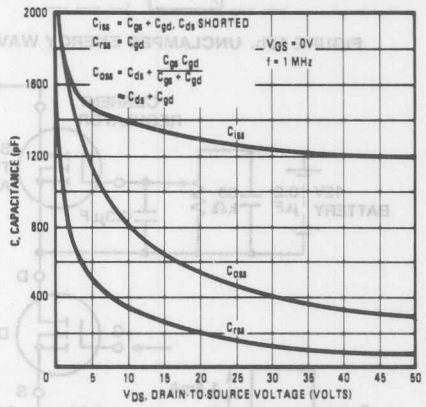


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

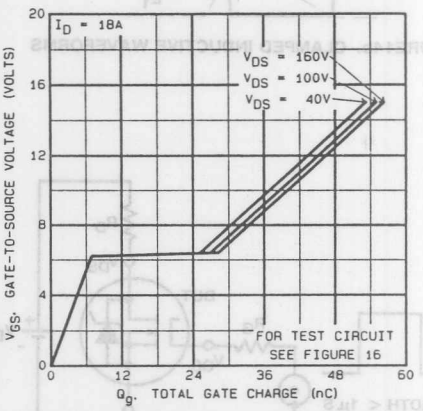


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

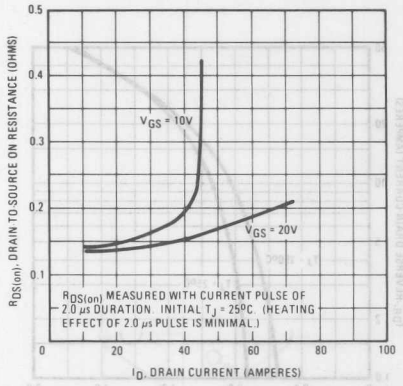


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

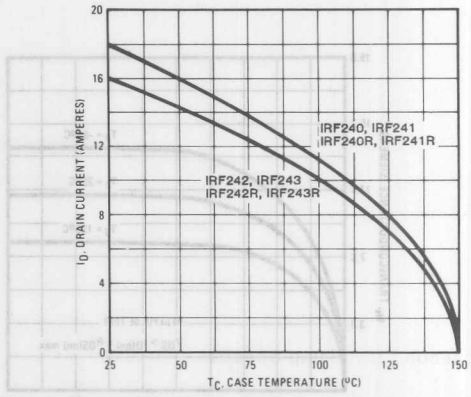


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

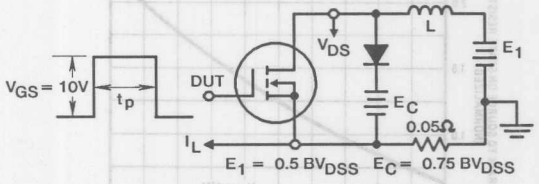


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

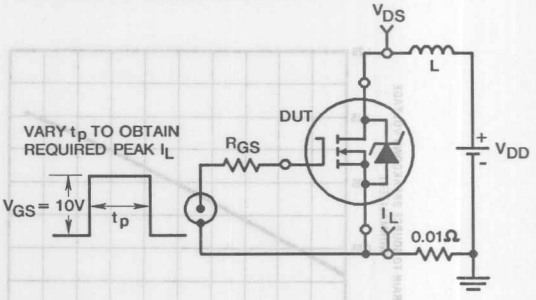


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

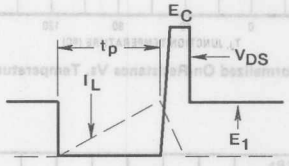


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

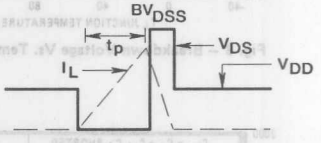


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

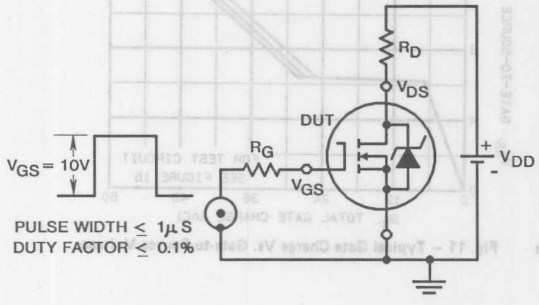


FIGURE 16. SWITCHING TIME TEST CIRCUIT

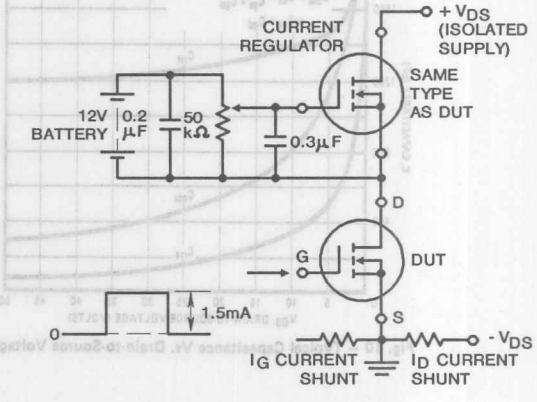


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF244, IRF245
IRF246, IRF247

N-Channel Power MOSFETs
Avalanche Energy Rated

August 1991

Features

- 14A and 13A, 275V - 250V
- $r_{DS(on)}$ = 0.28Ω and 0.34Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275, 250V DC Rated - 120V AC Line System Operation

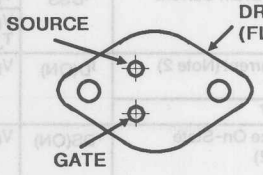
Description

The IRF244, IRF245, IRF246, and IRF247 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

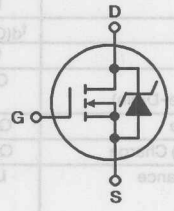
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF244	IRF245	IRF246	IRF247	UNITS
Drain-Source Voltage (1)	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current						
T_C = +25°C	I_D	14	13	14	13	A
T_C = +100°C	I_D	8.8	8.0	8.8	8.0	A
Pulsed Drain Current (3)	I_{DM}	56	52	56	52	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	125	125	125	125	W
Linear Derating Factor		1.0	1.0	1.0	1.0	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	550	550	550	550	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

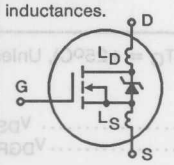
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, Starting T_J = +25°C, L = 4.5mH, R_G = 25Ω, Peak I_L = 14A (See Figures 14 & 15).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

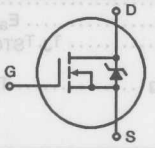
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File Number 2209.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF244, 1RF245	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	250	–	–	V
IRF246, IRF247			275	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF244, IRF246	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	14	–	–	A
1RF245, IRF247			13	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF244, IRF246	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4A	–	0.20	0.28	Ω
1RF245. IRF247			–	0.24	0.34	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 4A	6.7	10	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1300	–	pF
Output Capacitance	C_{OSS}		–	320	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	69	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 14A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	16	24	ns
Rise Time	t_r		–	67	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	53	80	ns
Fall Time	t_f		–	49	74	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	39	59	nC
Gate-Source Charge	Q_{gs}		–	6.6	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	20	–	nC
Internal Drain Inductance	L_D	Measured from the source lead, 6mm (0.25 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	14	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	56	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 14A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/μs	150	300	640	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/μs	1.6	3.4	7.2	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, Starting T_J = +25°C, L = 4.5mH, R_G = 25Ω, Peak I_L = 14A (See Figures 14 & 15).

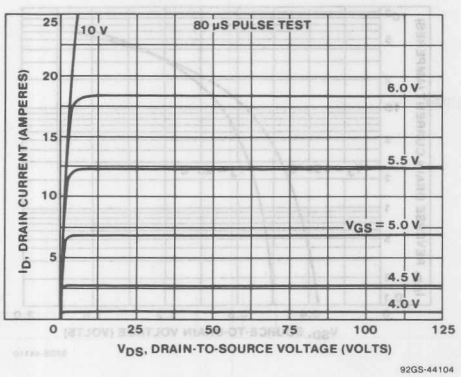


Fig. 1 - Typical output characteristics.

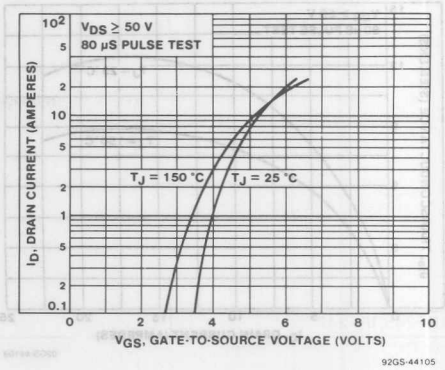


Fig. 2 - Typical transfer characteristics.

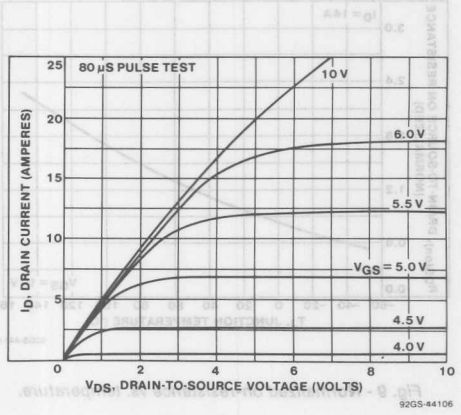


Fig. 3 - Typical saturation characteristics.

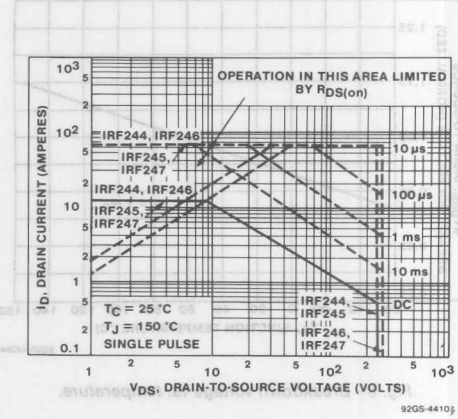


Fig. 4 - Maximum safe operating area.

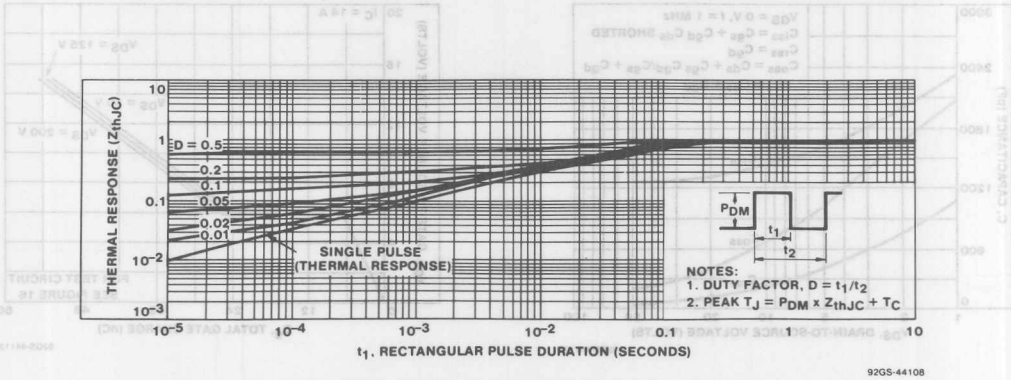


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

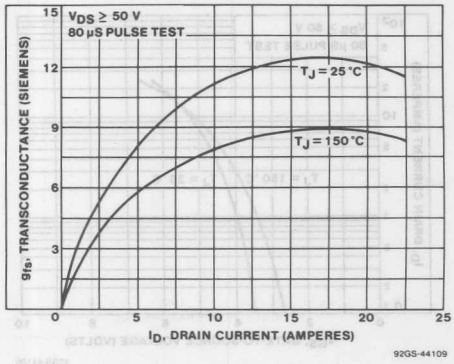


Fig. 6 - Typical transconductance vs. drain current.

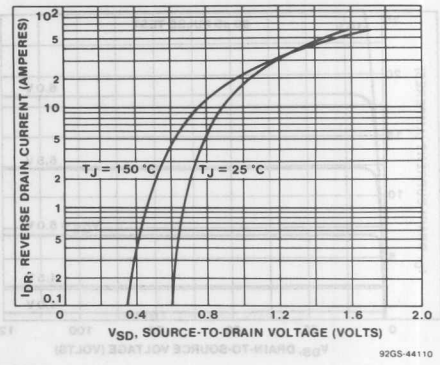


Fig. 7 - Typical source-drain diode forward voltage.

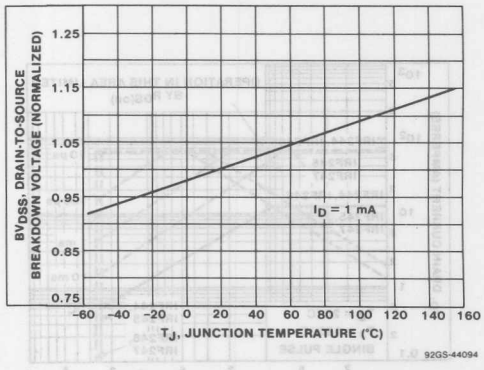


Fig. 8 - Breakdown voltage vs. temperature.

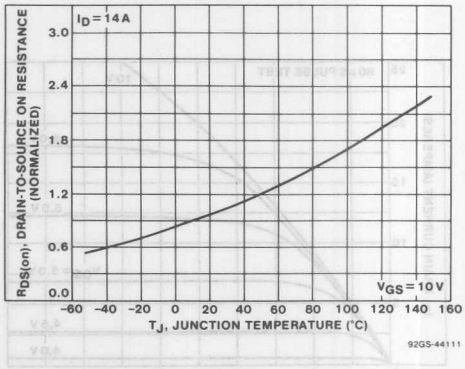


Fig. 9 - Normalized on-resistance vs. temperature.

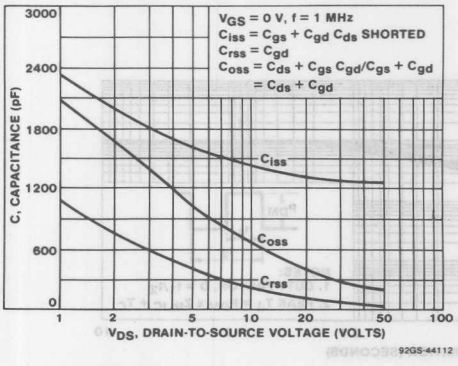


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

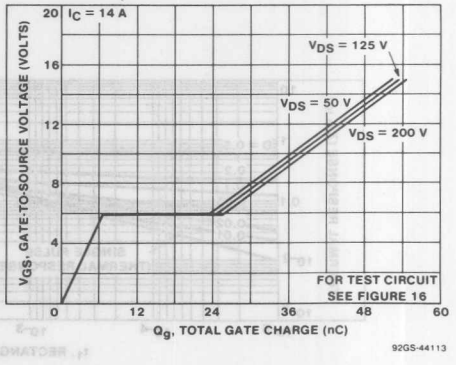


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

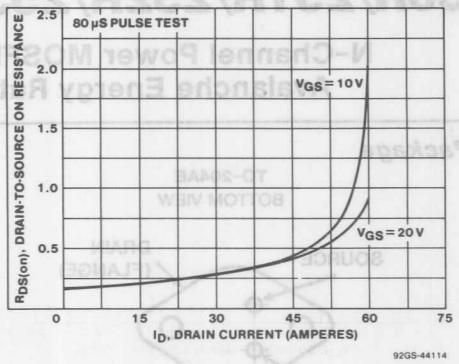


Figure 12. Typical On Resistance vs Drain Current

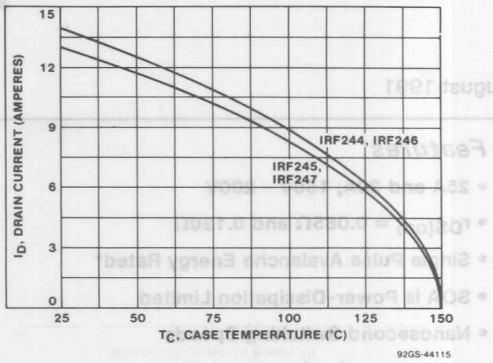


Figure 13. Maximum Drain Current vs Case Temperature

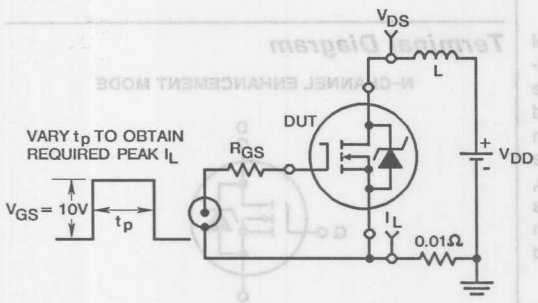


Figure 14. Unclamped Energy Test Circuit

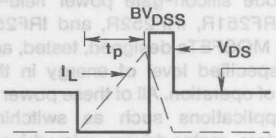


Figure 15. Unclamped Energy Waveforms

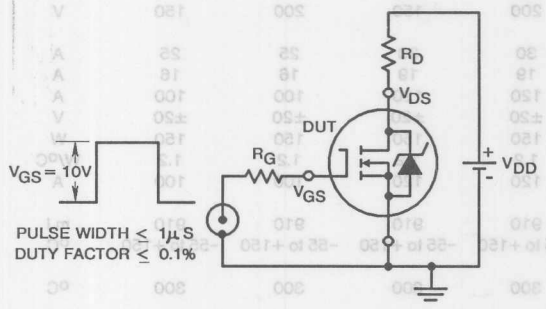


Figure16. Switching Time Test Circuit

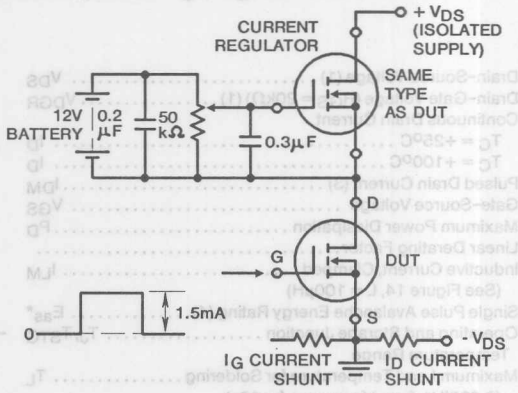


Figure 17. Gate Charge Test Circuit

HARRIS

IRF250/251/252/253
IRF250R/251R/252R/253R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 25A and 30A, 150V - 200V
- $r_{DS(on)}$ = 0.085Ω and 0.120Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

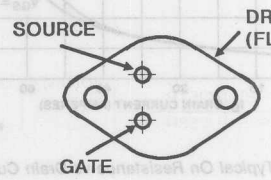
Description

The IRF250, IRF251, IRF252, and IRF253 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF250R, IRF251R, IRF252R, and IRF253R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AE steel package.

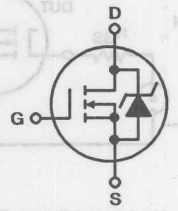
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF250 IRF250R	IRF251 IRF251R	IRF252 IRF252R	IRF253 IRF253R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	30	30	25	25	A
T_C = +100°C ..... I_D	19	19	16	16	A
Pulsed Drain Current (3) ..... I_{DM}	120	120	100	100	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	120	120	100	100	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	910	910	910	910	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max junction temp. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 1.5mH, R_{GS} = 25Ω, I_{PEAK} = 30A. See Figure 15.

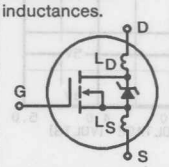
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

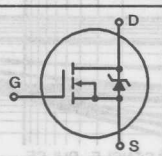
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File Number **1825.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF250/252, IRF250R/252R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRF251/253, IRF251R/253R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF250/251, IRF250R/251R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	30	–	–	A
IRF252/253, IRF252R/253R			25	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF250/251, IRF250R/251R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 16A	–	0.07	0.085	Ω
IRF252/253, IRF252R/253R			–	0.09	0.120	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 16A	13	19	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2000	–	pF
Output Capacitance	C_{OSS}		–	800	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	300	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, $I_D \approx$ 30A, R_G = 6.2Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	20	30	ns
Rise Time	t_r		–	120	180	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	70	100	ns
Fall Time	t_f		–	80	120	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 30A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	79	120	nC
Gate-Source Charge	Q_{gs}		–	13	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	42	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	30	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	120	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 30A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 30A, dI_F/dt = 100A/µs	140	350	630	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 30A, dI_F/dt = 100A/µs	1.8	4.7	8.1	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 1.5mH, R_{GS} = 25Ω, I_{PEAK} = 30A (See Figure 15)

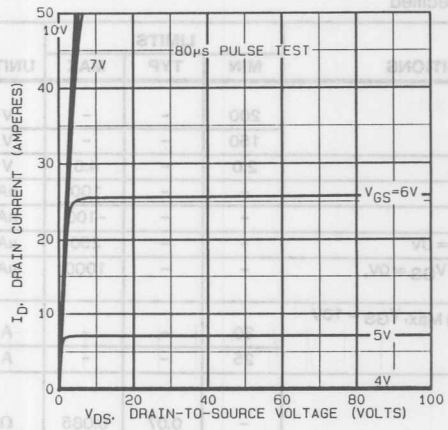


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

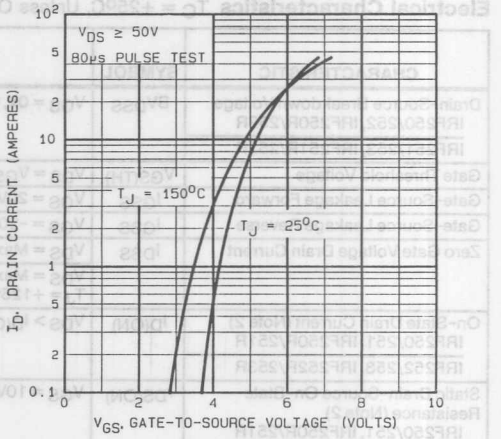


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

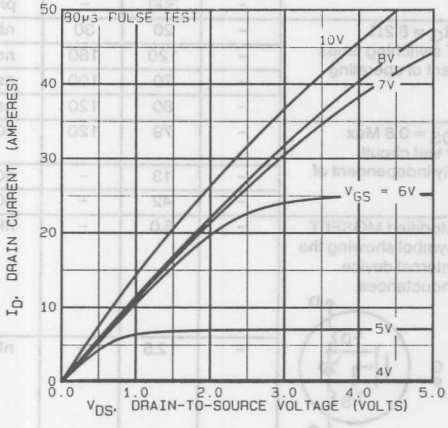


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

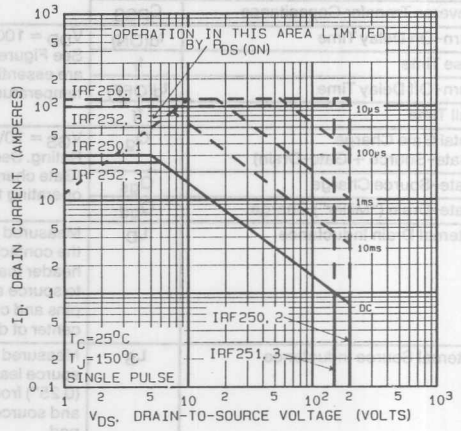


FIGURE 4. MAXIMUM SAFE OPERATING AREA

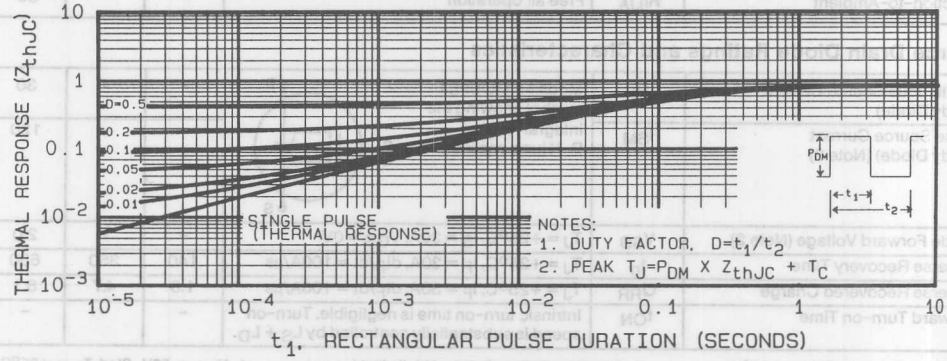


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

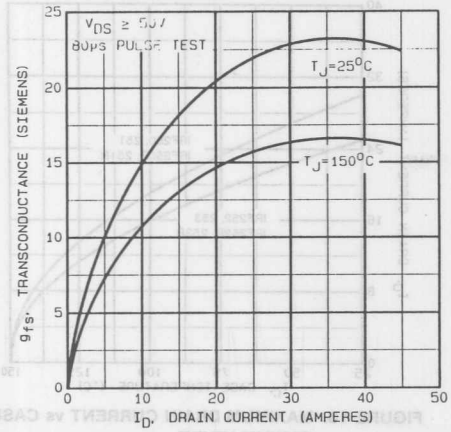


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

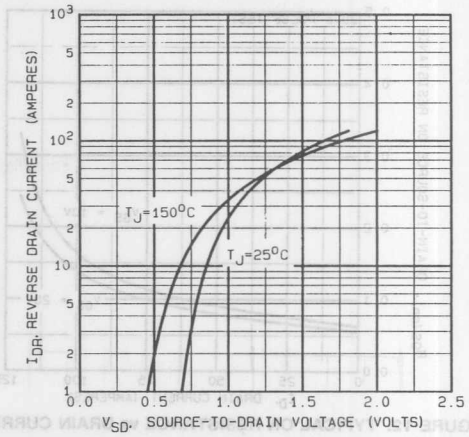


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

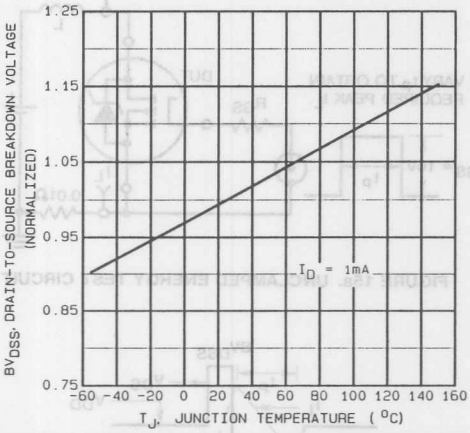


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

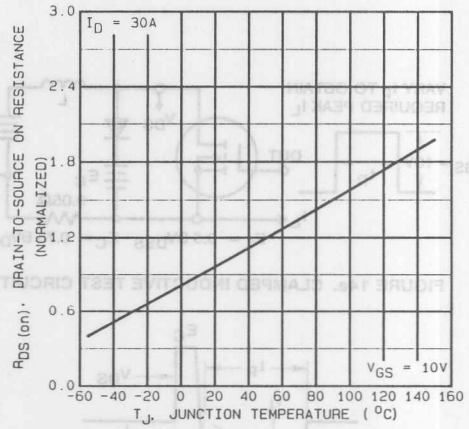


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

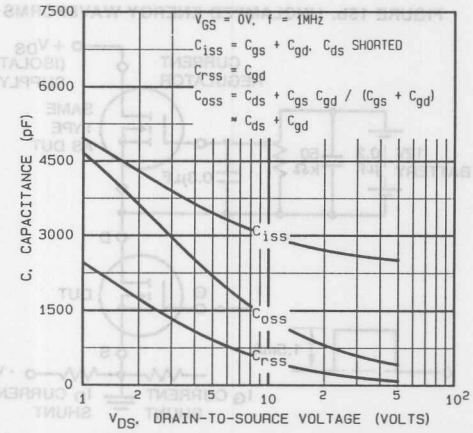


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

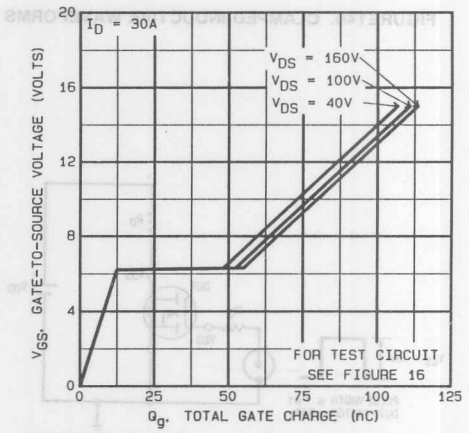


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

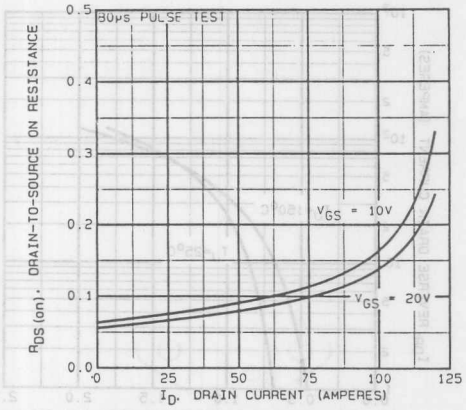


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

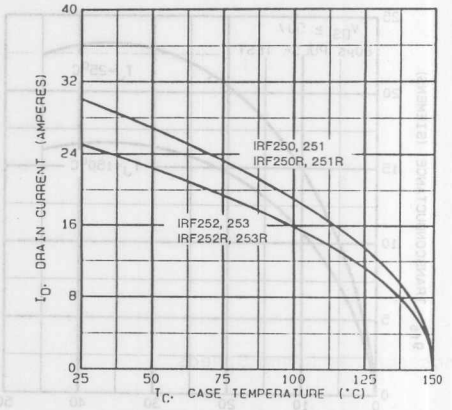


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

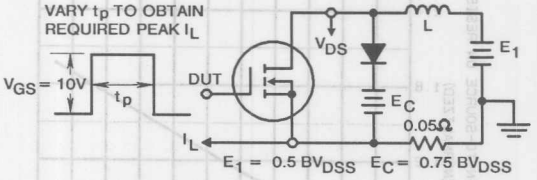


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

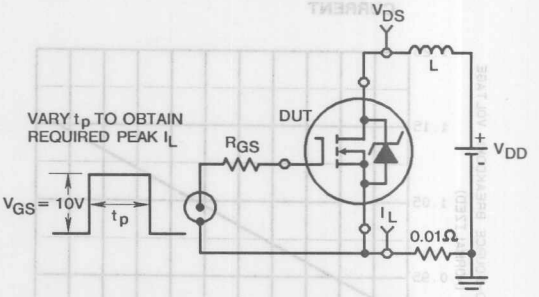


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

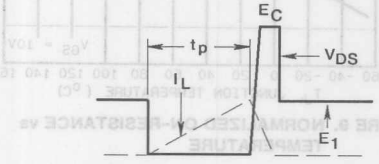


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

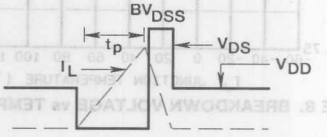


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

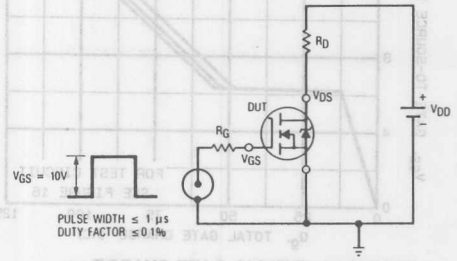


FIGURE 16. SWITCHING TIME TEST CIRCUIT

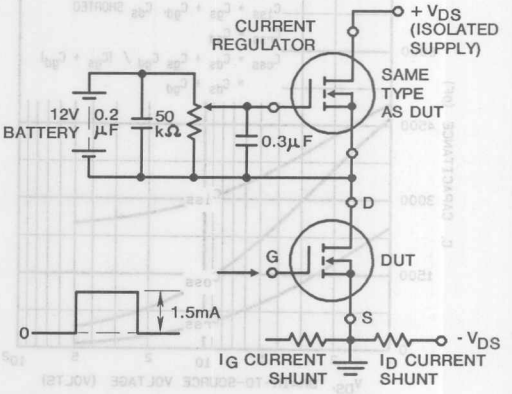


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF254, IRF255 IRF256, IRF257

N-Channel Power MOSFETs Avalanche Energy Rated

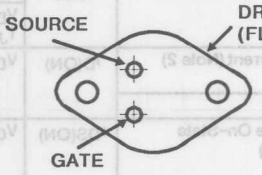
August 1991

Features

- 22A and 20A, 275V - 250V
- $r_{DS(on)}$ = 0.14Ω and 0.17Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275, 250V DC Rated - 120V AC Line System Operation

Package

TO-204AE
BOTTOM VIEW



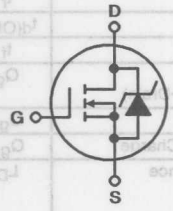
Description

The IRF254, IRF255, IRF256, and IRF257 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AE steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF254	IRF255	IRF256	IRF257	UNITS
Drain-Source Voltage (1) ..... V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	250	250	275	275	V
Continuous Drain Current					
T_C = +25°C ..... I_D	22	20	22	20	A
T_C = +100°C ..... I_D	14	12	14	12	A
Pulsed Drain Current (3) ..... I_{DM}	88	80	88	80	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	1000	1000	1000	1000	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

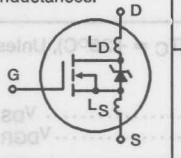
NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, Starting T_J = +25°C, L = 3.3mH, R_G = 25Ω, Peak I_L = 22A (See Figures 14 & 15).

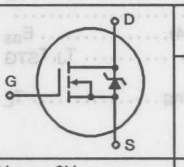
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2300.2

Drain-Source Breakdown Voltage IRF254, 1RF255	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	250	-	-	V
IRF256, IRF257			275	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF254, IRF256	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	22	-	-	A
1RF255, IRF257			20	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF254, IRF256	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 12A	-	0.11	0.14	Ω
1RF255. IRF257			-	0.14	0.17	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 12A	11	17	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	2700	-	pF
Output Capacitance	C_{OSS}		-	580	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	130	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 22A, R_G = 6.2Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	19	29	ns
Rise Time	t_r		-	84	130	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	75	110	ns
Fall Time	t_f		-	65	98	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	87	130	nC
Gate-Source Charge	Q_{gs}		-	14	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	73	-	nC
Internal Drain Inductance	L_D	Measured from the source lead, 6mm (0.25 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.10	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	22	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	88	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 22A, V_{GS} = 0V	-	-	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 22A, dI_F/dt = 100A/μs	150	310	650	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 22A, dI_F/dt = 100A/μs	1.9	4	8.4	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, Starting T_J = +25°C, L = 3.3mH, R_G = 25Ω, Peak I_L = 22A (See Figures 14 & 15).

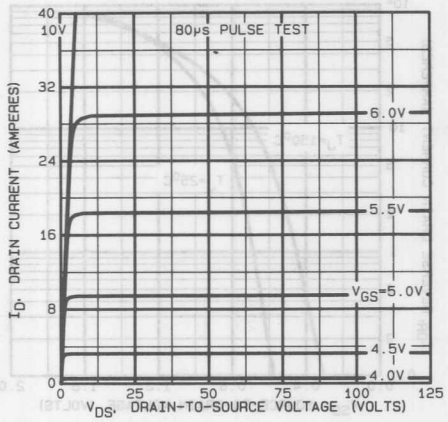


Fig. 1 - Typical output characteristics.

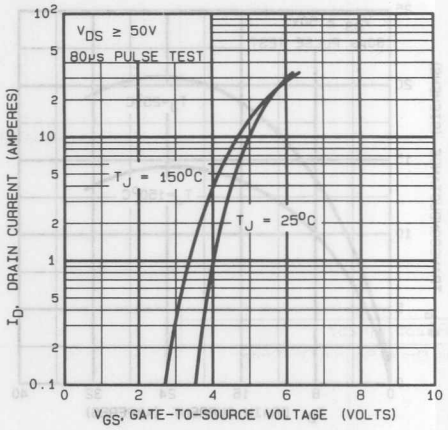


Fig. 2 - Typical transfer characteristics.

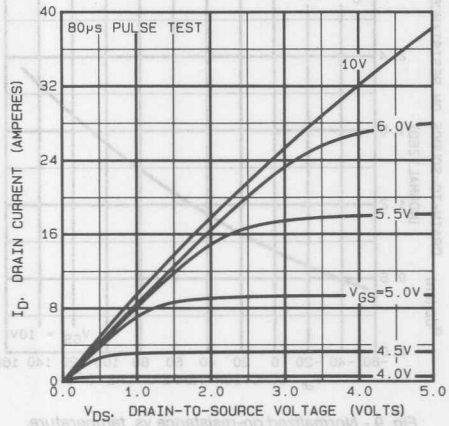


Fig. 3 - Typical saturation characteristics.

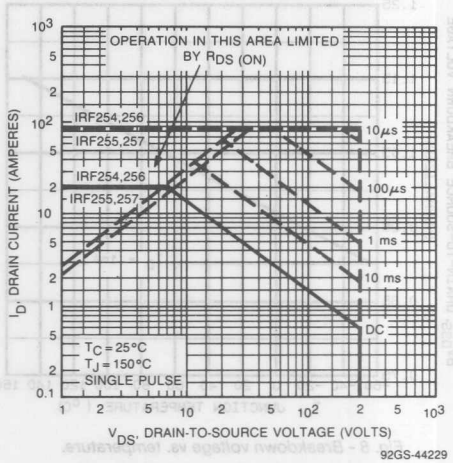


Fig. 4 - Maximum safe operating area.

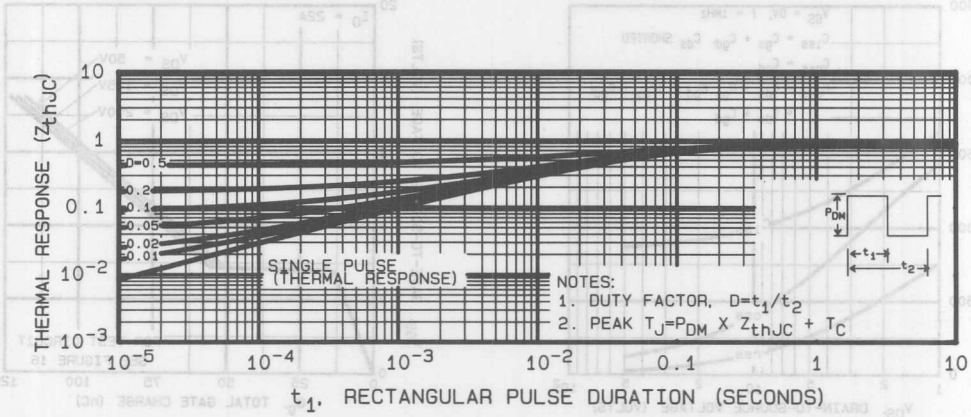


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

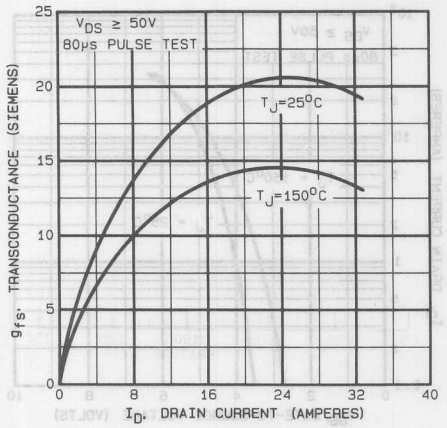


Fig. 6 - Typical transconductance vs. drain current.

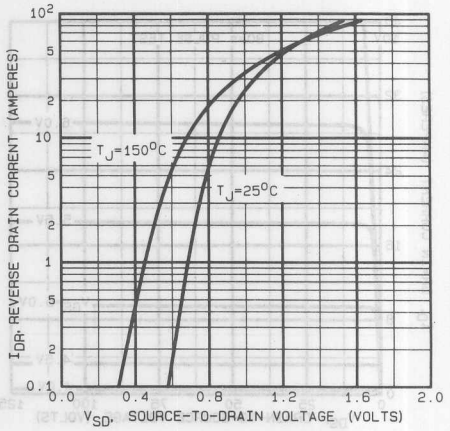


Fig. 7 - Typical source-drain diode forward voltage.

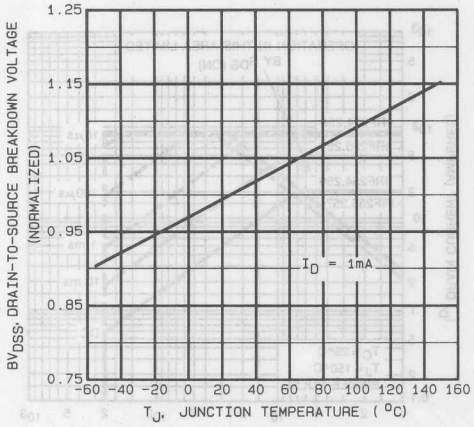


Fig. 8 - Breakdown voltage vs. temperature.

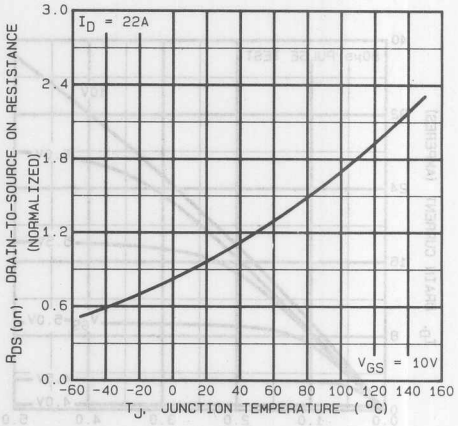


Fig. 9 - Normalized on-resistance vs. temperature.

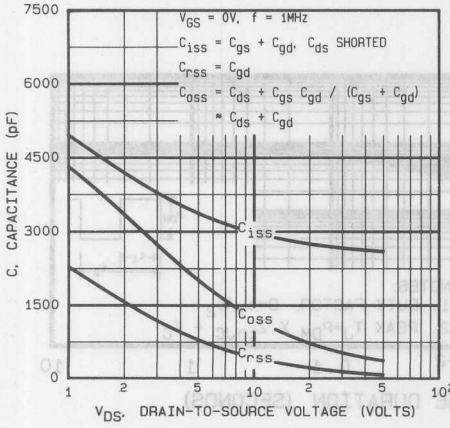


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

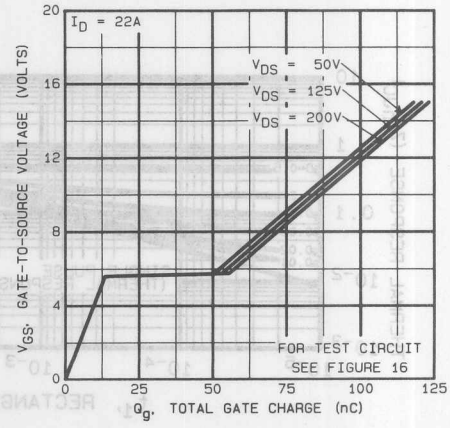


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

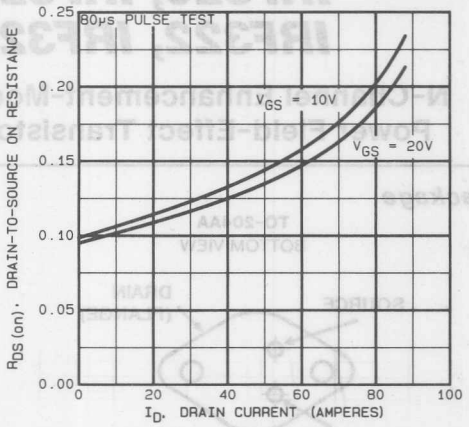


Figure 12. Typical On Resistance vs Drain Current

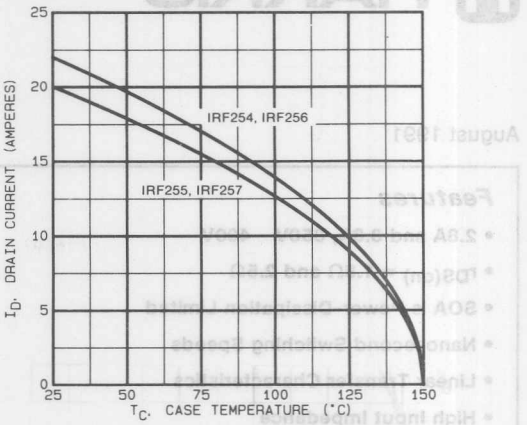


Figure 13. Maximum Drain Current vs Case Temperature

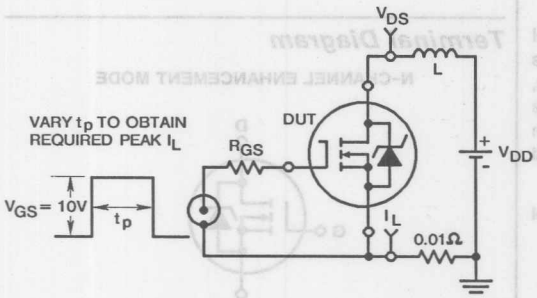


Figure 14. Unclamped Energy Test Circuit

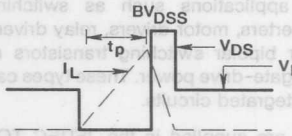


Figure 15. Unclamped Energy Waveforms

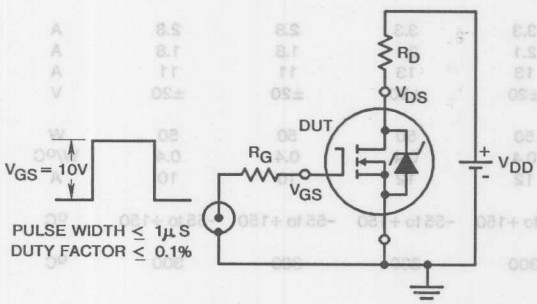


Figure16. Switching Time Test Circuit

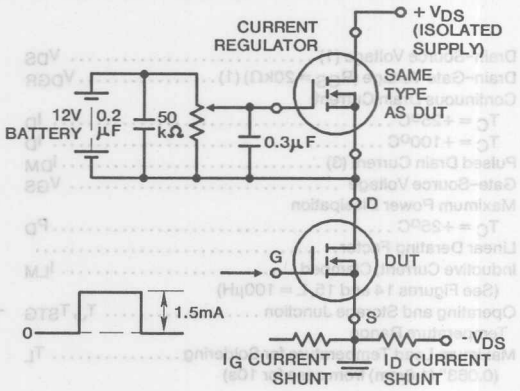


Figure 17. Gate Charge Test Circuit

HARRIS

IRF320, IRF321 IRF322, IRF323

N-Channel Enhancement-Mode Power Field-Effect Transistors

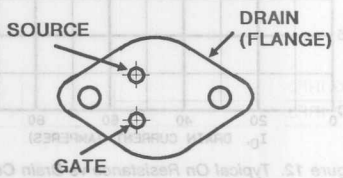
August 1991

Features

- 2.8A and 3.3A, 350V - 400V
- $r_{DS(on)}$ = 1.8Ω and 2.5Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AA
BOTTOM VIEW



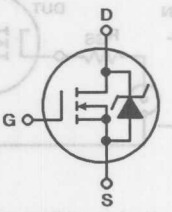
Description

The IRF320, IRF321, IRF322, and IRF323 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF320	IRF321	IRF322	IRF323	UNITS
Drain-Source Voltage (1)	V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	400	350	400	350	V
Continuous Drain Current						
T_C = +25°C	I_D	3.3	3.3	2.8	2.8	A
T_C = +100°C	I_D	2.1	2.1	1.8	1.8	A
Pulsed Drain Current (3)	I_{DM}	13	13	11	11	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	50	50	50	50	W
Linear Derating Factor		0.4	0.4	0.4	0.4	W/°C
Inductive Current, Clamped (See Figures 14 and 15, L = 100μH)	I_{LM}	12	12	10	10	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

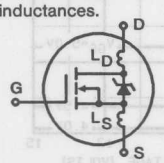
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

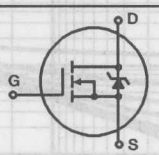
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File Number **1569.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF320, IRF322	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	–	–	V
IRF321, IRF323			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF320, IRF321	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)\ Max}$, V_{GS} = 10V	3.3	–	–	A
IRF322, IRF323			2.8	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF320, IRF321	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.8A	–	1.5	1.8	Ω
IRF322, IRF323			–	1.8	2.5	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 1.8A	1.8	2.7	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	450	–	pF
Output Capacitance	C_{OSS}		–	100	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 3.3A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	10	15	ns
Rise Time	t_r		–	14	20	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	30	45	ns
Fall Time	t_f		–	13	20	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.3A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	12	20	nC
Gate-Source Charge	Q_{gs}		–	3.3	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	11	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	2.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	3.3	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	13	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = 3.3A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 3.3A, dI_F/dt = 100A/µs	120	270	600	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 3.3A, dI_F/dt = 100A/µs	0.64	1.4	3.0	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES:
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5)

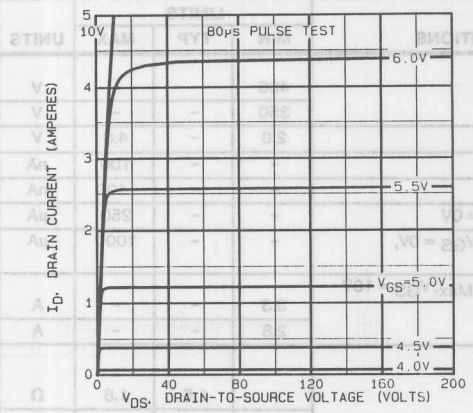


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

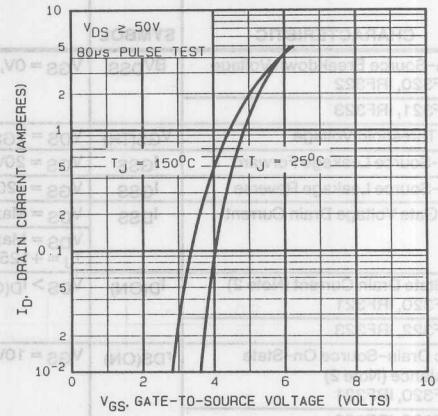


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

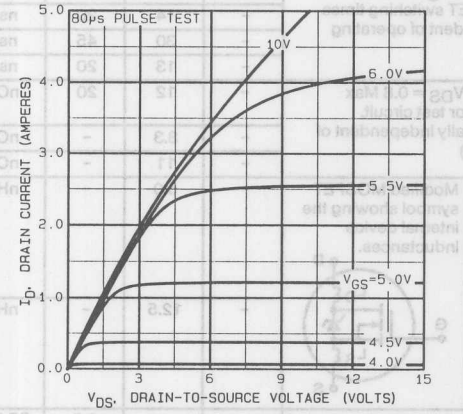


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

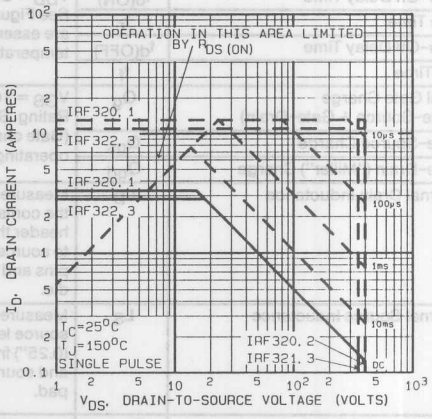


FIGURE 4. MAXIMUM SAFE OPERATING AREA

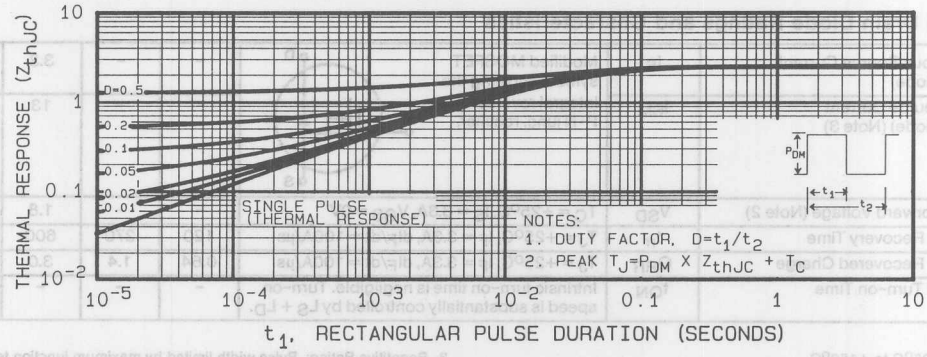


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

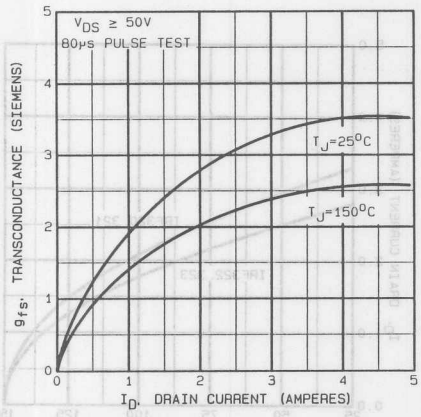


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

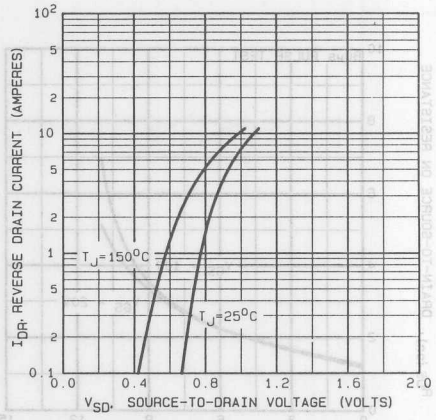


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

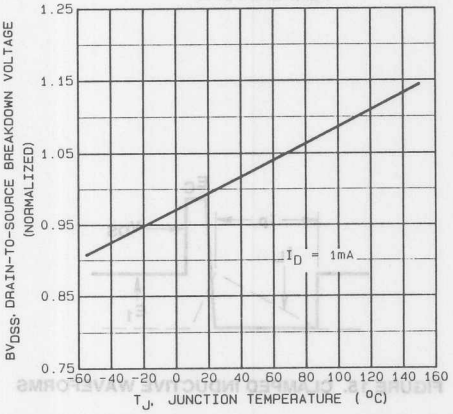


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

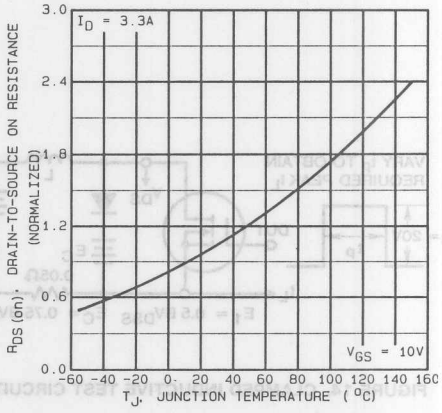


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

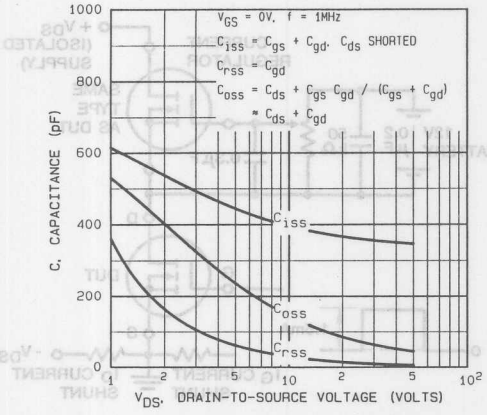


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

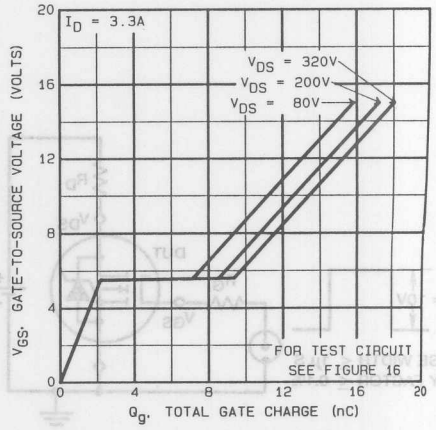


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

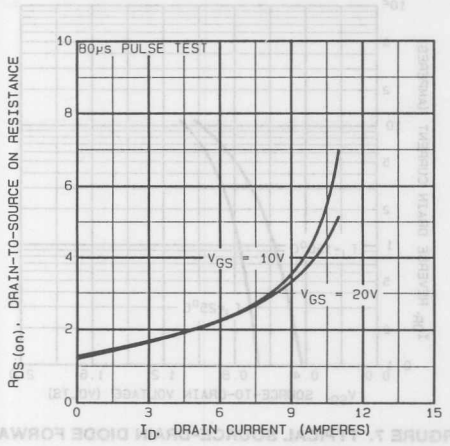


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

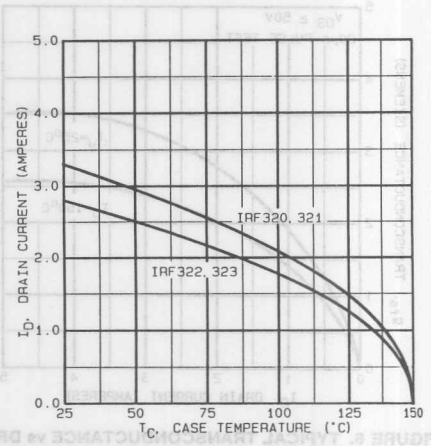


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

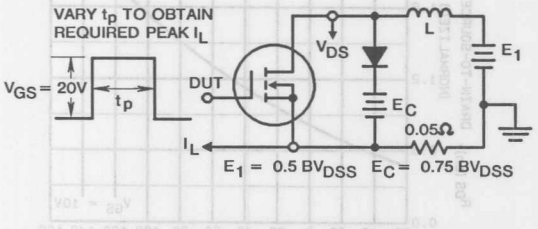


FIGURE 14. CLAMPED INDUCTIVE TEST CIRCUIT

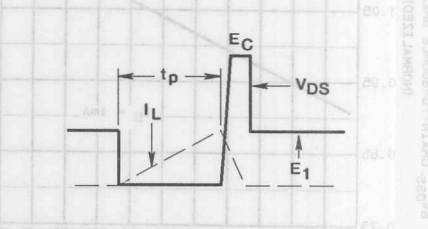


FIGURE 15. CLAMPED INDUCTIVE WAVEFORMS

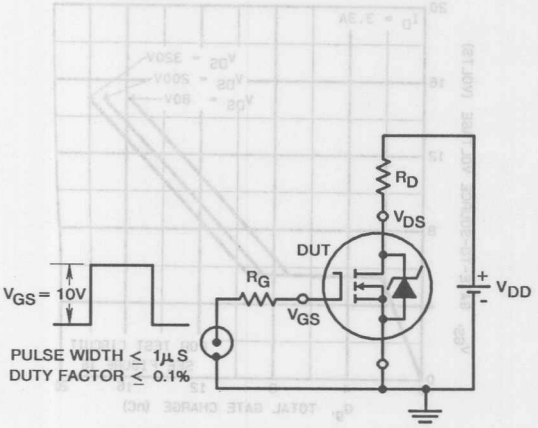


FIGURE 16. SWITCHING TIME TEST CIRCUIT

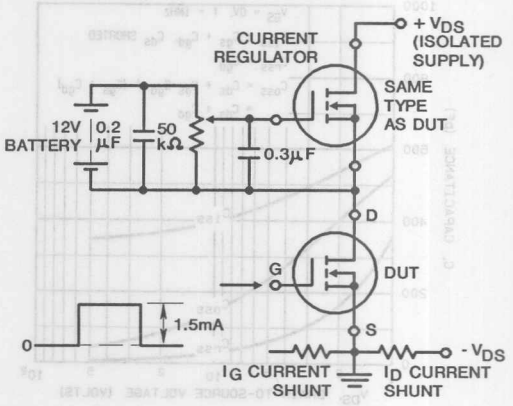


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRF330/331/332/333
IRF330R/331R/332R/333R

N-Channel Power MOSFETs
Avalanche Energy Rated*

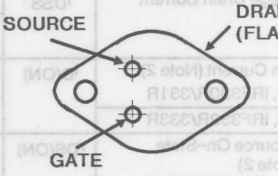
August 1991

Features

- 4.5A and 5.5A, 350V - 400V
- $r_{DS(on)}$ = 1.0Ω and 1.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AA
BOTTOM VIEW



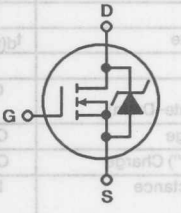
Description

The IRF330, IRF331, IRF332, and IRF333 are n-channel enhancement mode silicon gate power field effect transistors. IRF330R, IRF331R, IRF332R, and IRF333R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of the power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	IRF330 IRF330R	IRF331 IRF331R	IRF332 IRF332R	IRF333 IRF333R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	5.5	5.5	4.5	4.5	A
T_C = +100°C ..... I_D	3.5	3.5	3.0	3.0	A
Pulsed Drain Current (3) ..... I_{DM}	22	22	18	18	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L 100μH)	22	22	18	18	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	300	300	300	300	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

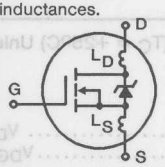
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max junction temp. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 17mH, R_{GS} = 25Ω, I_{PEAK} = 5.5A. See Figure 15.

* R Suffix Types Only

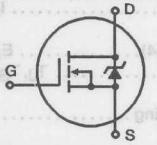
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1570.1

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage IRF330/332, IRF330R/332R	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	400	-	-	V
IRF331/333, IRF331R/333R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF330/331, IRF330R/331R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	5.5	-	-	A
IRF332/333, IRF332R/333R			4.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF330/331, IRF330R/331R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.0A	-	0.8	1.0	Ω
IRF332/333, IRF332R/333R			-	1.0	1.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 3.0A	2.9	4.0	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	700	-	pF
Output Capacitance	C_{OSS}		-	150	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	40	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D ≈ 5.5A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	11	17	ns
Rise Time	t_r		-	20	29	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	35	56	ns
Fall Time	t_f		-	15	24	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 5.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	21	35	nC
Gate-Source Charge	Q_{gs}		-	4	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	17	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	5.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	22	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 5.5A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/μs	140	400	660	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/μs	0.93	2.4	4.3	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 17mH, R_{GS} = 25Ω, I_{PEAK} = 5.5A (See Figure 15)

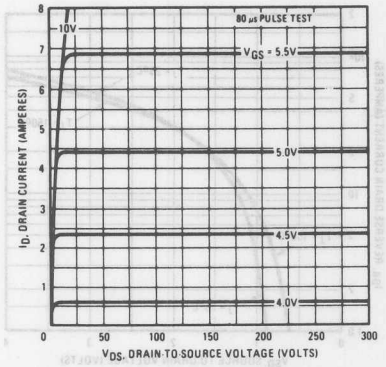


Fig. 1 – Typical Output Characteristics

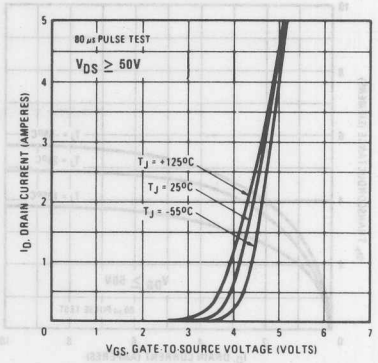


Fig. 2 – Typical Transfer Characteristics

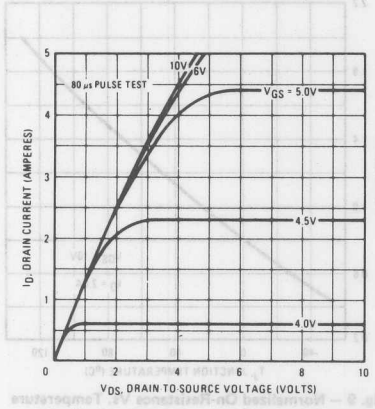


Fig. 3 – Typical Saturation Characteristics

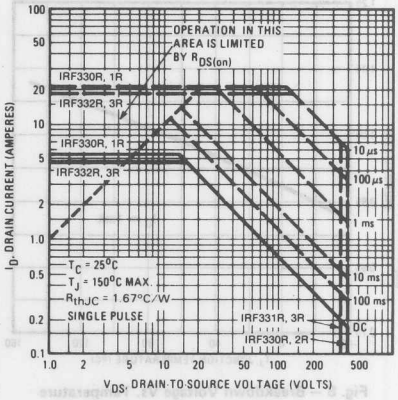


Fig. 4 – Maximum Safe Operating Area

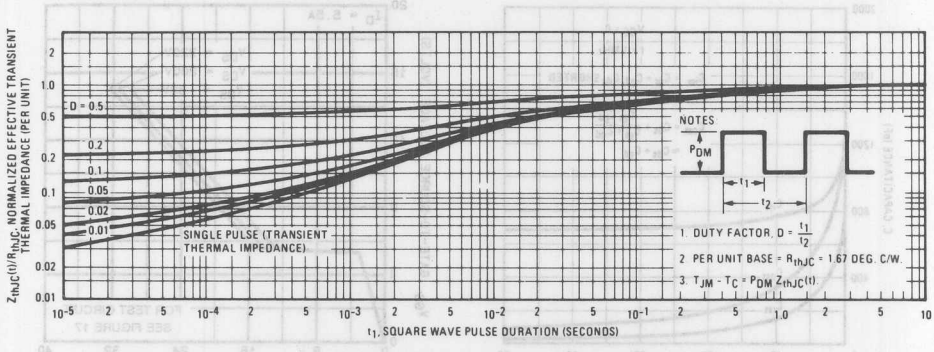


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

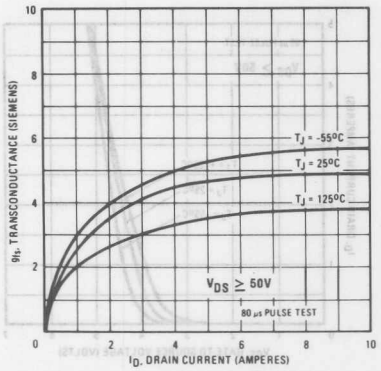


Fig. 6 – Typical Transconductance Vs. Drain Current

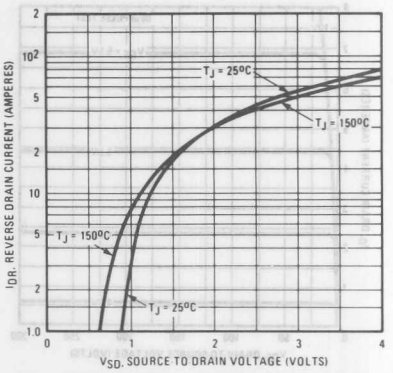


Fig. 7 – Typical Source-Drain Diode Forward Voltage

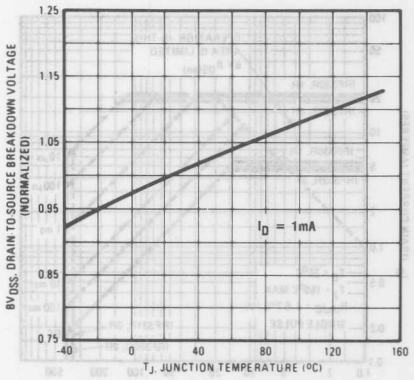


Fig. 8 – Breakdown Voltage Vs. Temperature

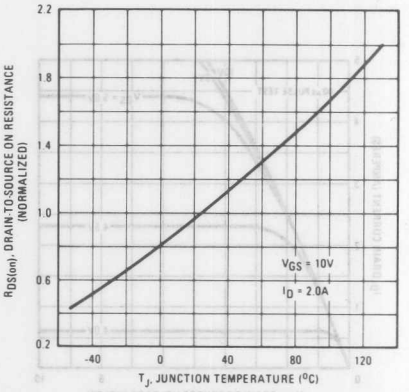


Fig. 9 – Normalized On-Resistance Vs. Temperature

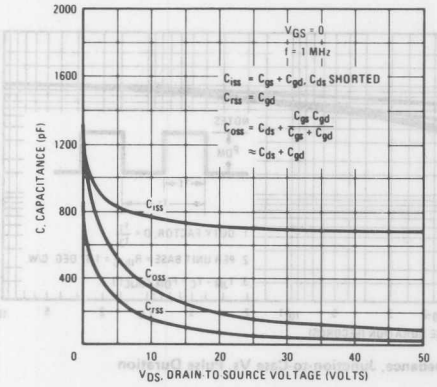


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

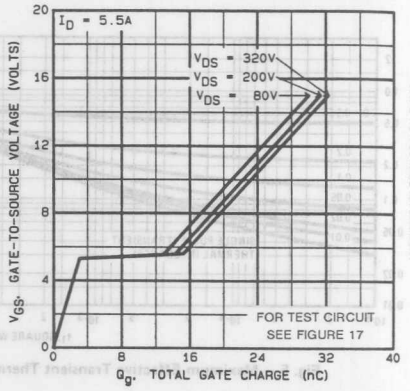


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

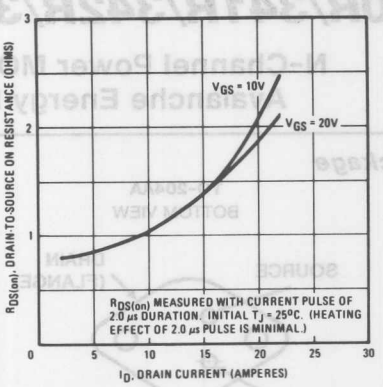


Fig. 12 - Typical On Resistance vs Drain Current

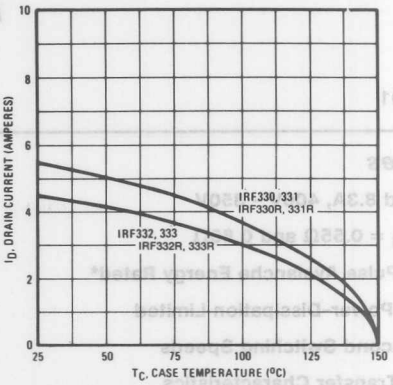


Fig. 13 - Maximum Drain Current vs Case Temperature

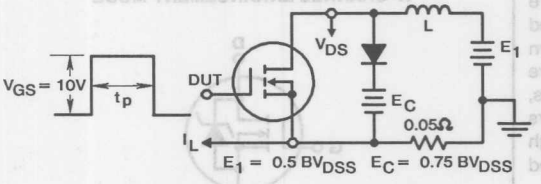


Fig. 14a - Clamped Inductive Test Circuit

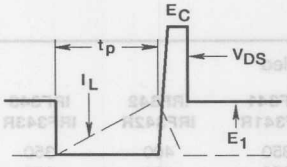


Fig. 14b - Clamped Inductive Waveforms

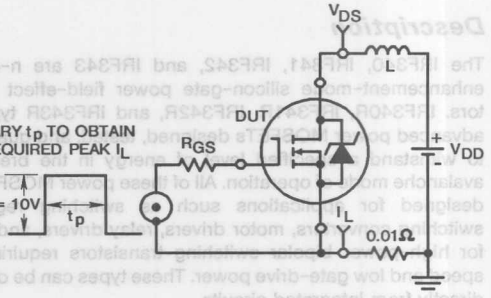


Fig. 15a - Unclamped Energy Test Circuit

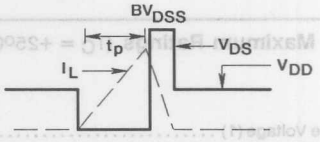


Fig. 15b - Unclamped Energy Waveforms

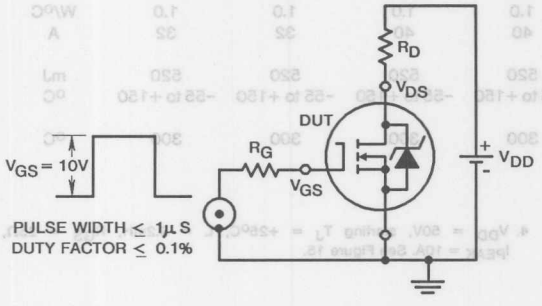


Fig. 16 - Switching Time Test Circuit

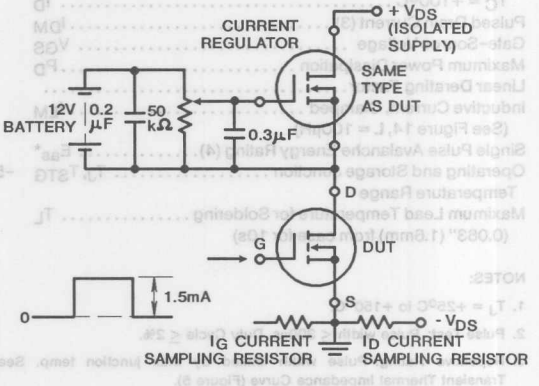


Fig. 17 - Gate Charge Test Circuit

4 N-CHANNEL POWER MOSFETs

IRF340/341/342/343
IRF340R/341R/342R/343R

N-Channel Power MOSFETs
Avalanche Energy Rated*

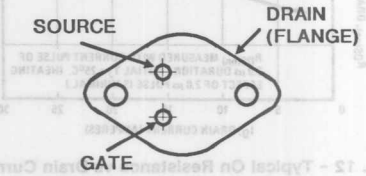
August 1991

Features

- 10A and 8.3A, 400V - 350V
- $r_{DS(on)}$ = 0.55Ω and 0.80Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AA
BOTTOM VIEW



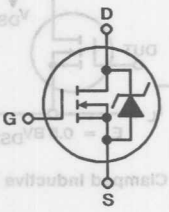
Description

The IRF340, IRF341, IRF342, and IRF343 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF340R, IRF341R, IRF342R, and IRF343R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF340 IRF340R	IRF341 IRF341R	IRF342 IRF342R	IRF343 IRF343R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	10	10	8.3	8.3	A
T_C = +100°C ..... I_D	6.3	6.3	5.2	5.2	A
Pulsed Drain Current (3) ..... I_{DM}	40	40	33	33	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	40	40	32	32	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	520	520	520	520	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max junction temp. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 9.2mH, R_{GS} = 25Ω, I_{PEAK} = 10A. See Figure 15.

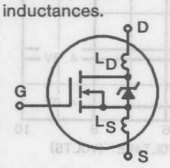
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

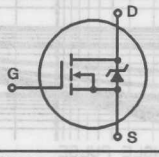
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File Number **2307.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF340/342, IRF340R/342R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	–	–	V
IRF341/343, IRF341R/343R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF340/341, IRF340R/341R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\,Max}$, V_{GS} = 10V	10	–	–	A
IRF342/343, IRF342R/343R			8.3	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF340/341, IRF340R/341R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.2A	–	0.4	0.55	Ω
IRF342/343, IRF342R/343R			–	0.5	0.80	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 5.2A	5.8	8	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1250	–	pF
Output Capacitance	C_{OSS}		–	300	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	80	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D ≈ 10A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	17	21	ns
Rise Time	t_r		–	27	41	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	45	75	ns
Fall Time	t_f		–	20	36	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	41	63	nC
Gate-Source Charge	Q_{gs}		–	7	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	23	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	10	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	40	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 10A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 10A, dI_F/dt = 100A/µs	170	350	790	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 10A, dI_F/dt = 100A/µs	1.6	4.0	8.2	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 9.2mH, R_{GS} = 25Ω, I_{PEAK} = 10A (See Figure 15)

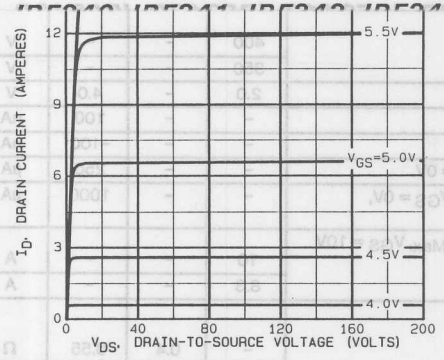


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

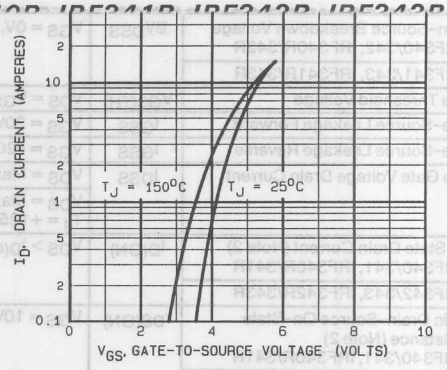


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

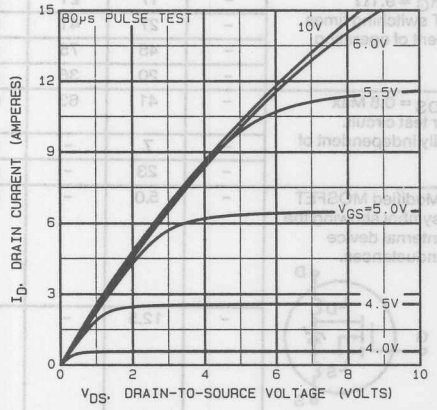


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

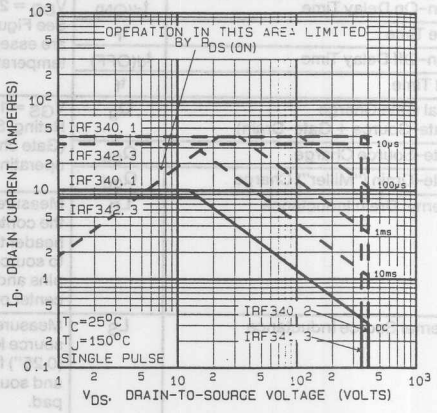


FIGURE 4. MAXIMUM SAFE OPERATING AREA

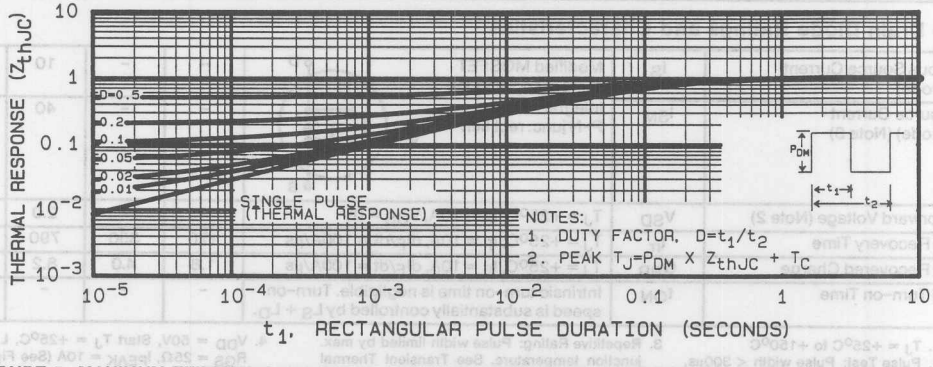


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

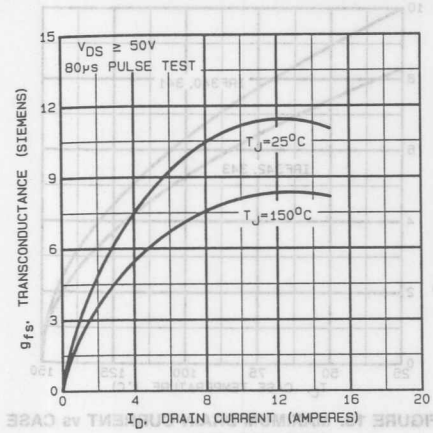


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

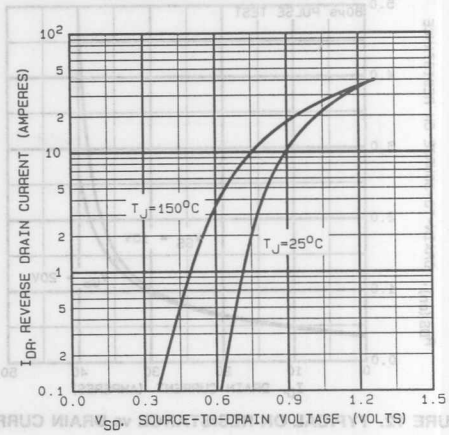


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

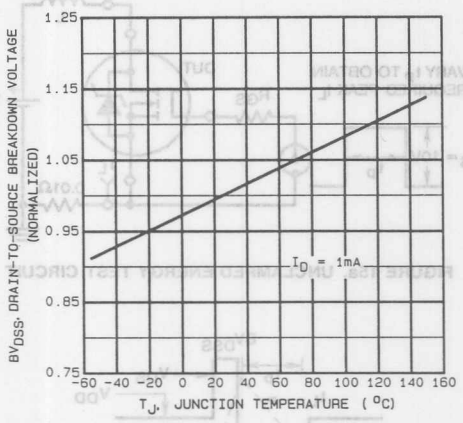


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

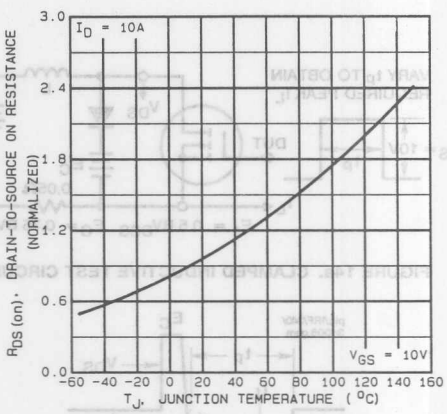


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

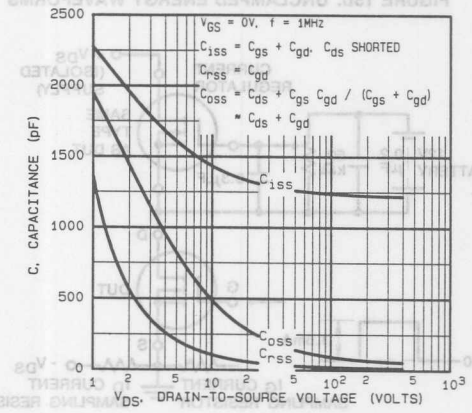


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

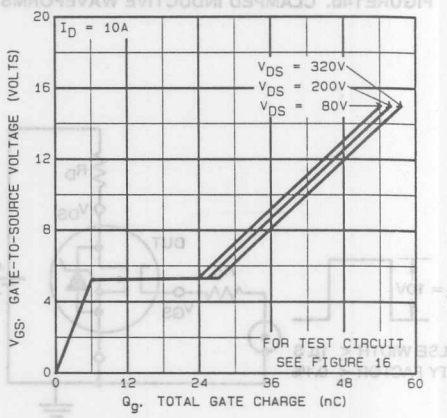


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

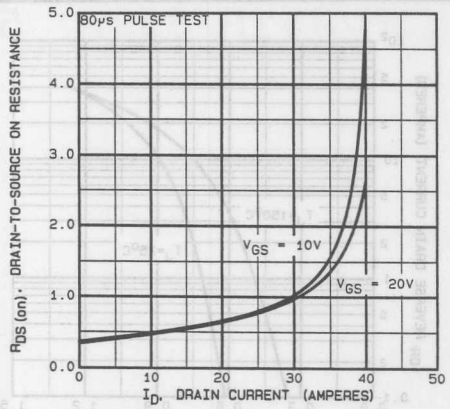


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

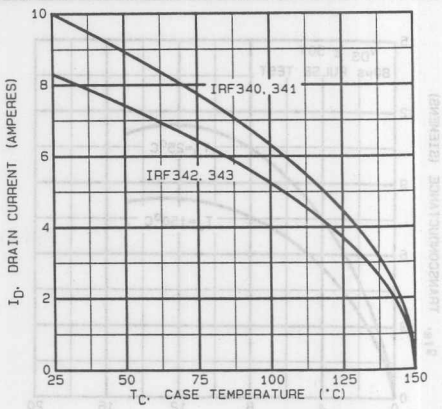


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

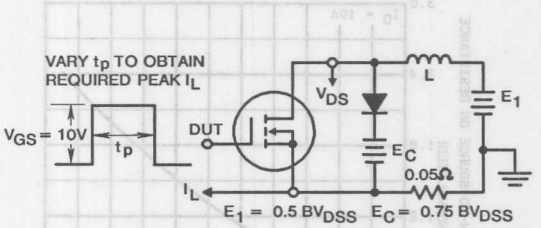


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

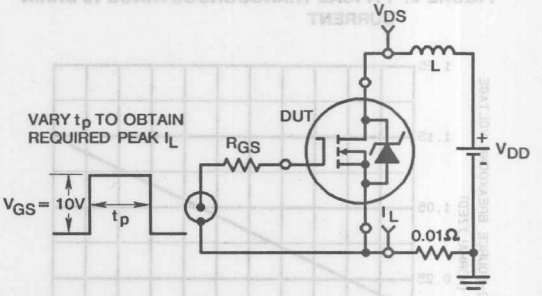


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

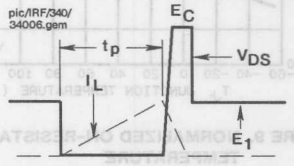


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

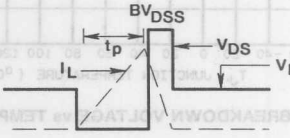


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

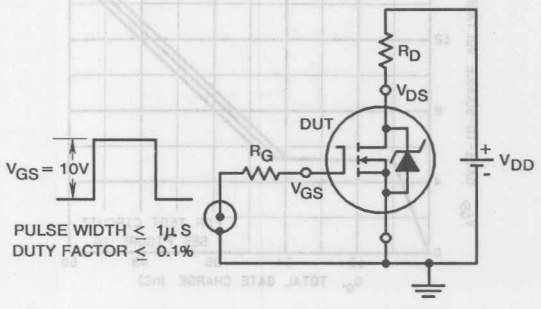


FIGURE 16. SWITCHING TIME TEST CIRCUIT

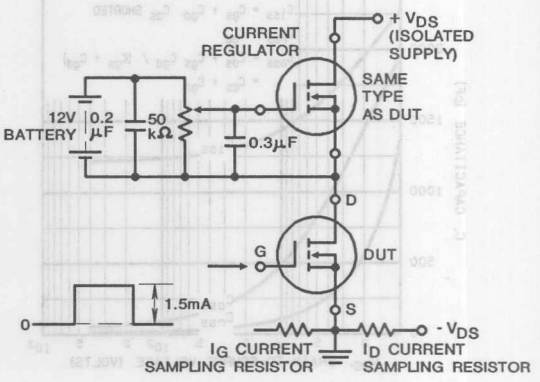


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS IRF350/351/352/353 IRF350R/351R/352R/353R

N-Channel Power MOSFETs Avalanche Energy Rated*

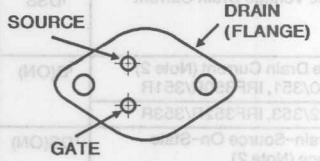
August 1991

Features

- 13A and 15.0A, 350V - 400V
- $r_{DS}(on)$ = 0.3Ω and 0.4Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AA



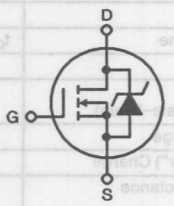
Description

The IRF350, IRF351, IRF352, and IRF353 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF350R, IRF351R, IRF352R and IRF353R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF350 IRF350R	IRF351 IRF351R	IRF352 IRF352R	IRF353 IRF353R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	15	15	13	13	A
T_C = +100°C ..... I_D	9.0	9.0	8.0	8.0	A
Pulsed Drain Current (3) ..... I_{DM}	60	60	52	52	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	60	60	52	52	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	700	700	700	700	mj
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 5.66mH, R_{GS} = 50Ω, I_{PEAK} = 15A. See Figure 15.

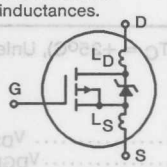
*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

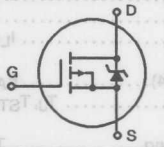
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File Number 1826.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF350/352, IRF350R/352R	BV_{DSS}	V_{GS} = 0V, I_D = -250µA	400	-	-	V
IRF351/353, IRF351R/353R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRF350/351, IRF350R/351R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	15	-	-	A
IRF352/353, IRF352R/353R			13	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF350/351, IRF350R/351R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8.0A	-	0.25	0.3	Ω
IRF352/353, IRF352R/353R			-	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)Max}$, I_D = 8.0A	8.0	10	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	2000	-	pF
Output Capacitance	C_{OSS}		-	400	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 180V, I_D = 8.0A, Zo = 4.7Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	-	35	ns
Rise Time	t_r		-	-	65	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	150	ns
Fall Time	t_f		-	-	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	79	120	nC
Gate-Source Charge	Q_{gs}		-	38	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	41	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	15	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	60	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 15A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 15A, dI_F/dt = 100A/µs	-	1000	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 15A, dI_F/dt = 100A/µs	-	6.6	-	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 40V, Start T_J = +25°C, L = 5.66mH, R_{GS} = 50Ω, I_{PEAK} = 15A (See Figure 15)

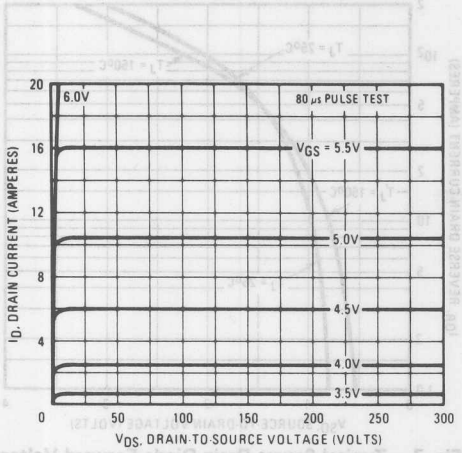


Fig. 1 – Typical Output Characteristics

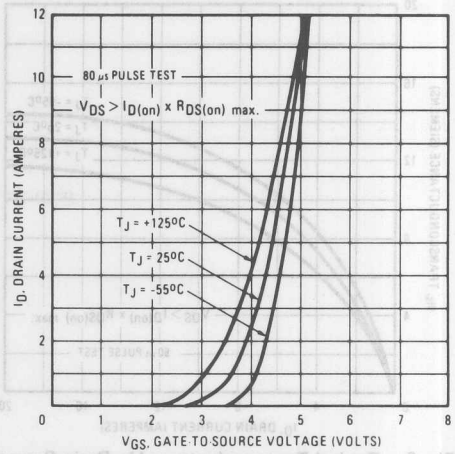


Fig. 2 – Typical Transfer Characteristics

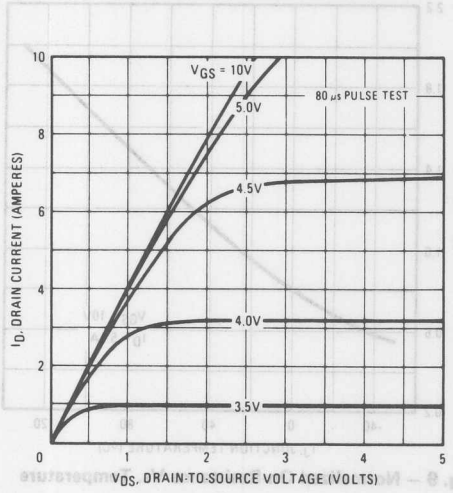


Fig. 3 – Typical Saturation Characteristics

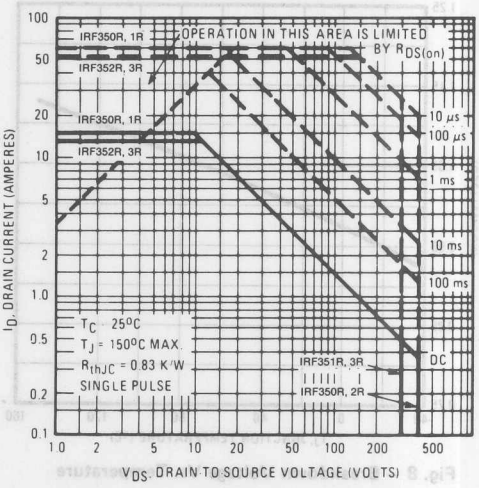


Fig. 4 – Maximum Safe Operating Area

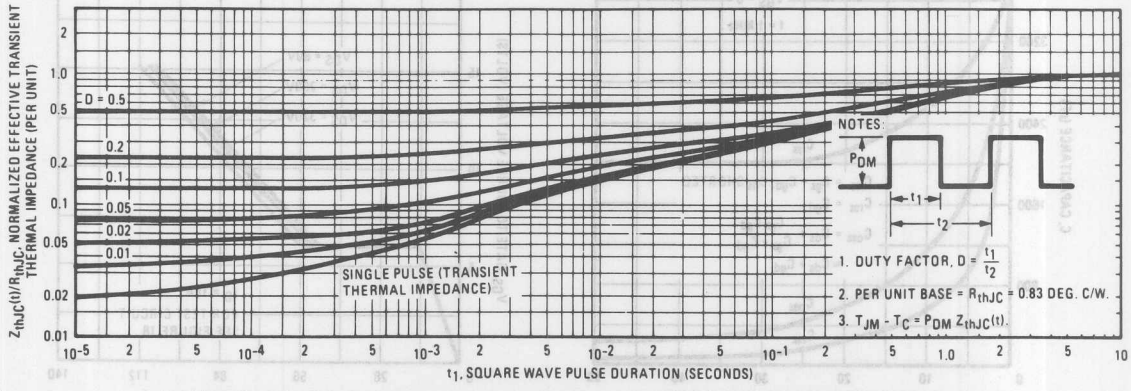


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

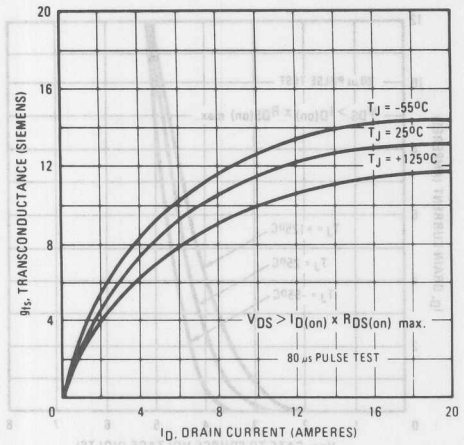


Fig. 6 — Typical Transconductance Vs. Drain Current

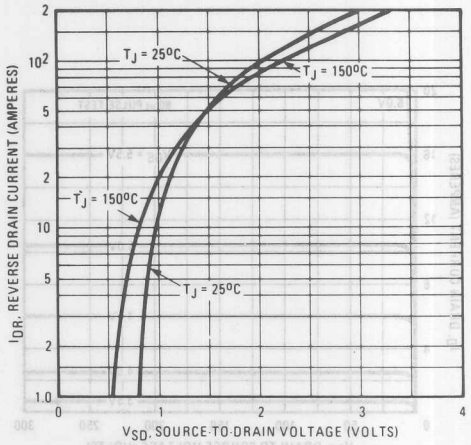


Fig. 7 — Typical Source-Drain Diode Forward Voltage

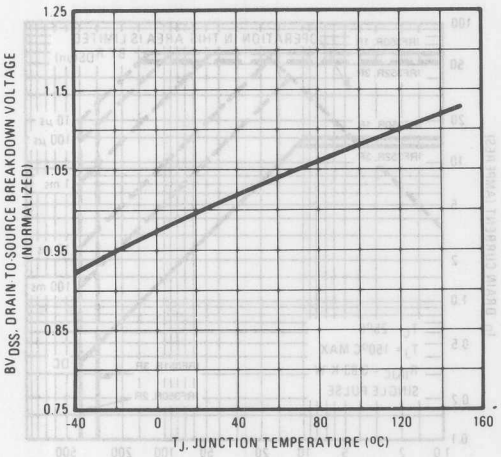


Fig. 8 — Breakdown Voltage Vs. Temperature

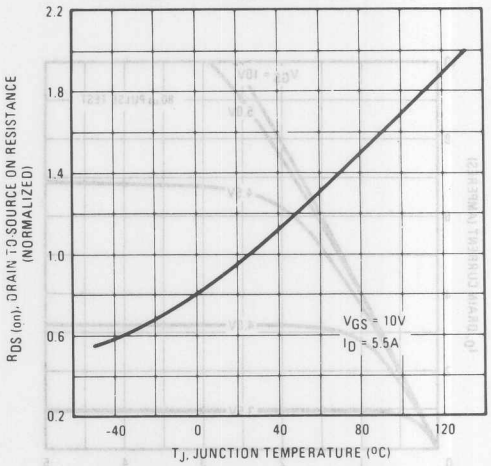


Fig. 9 — Normalized On-Resistance Vs. Temperature

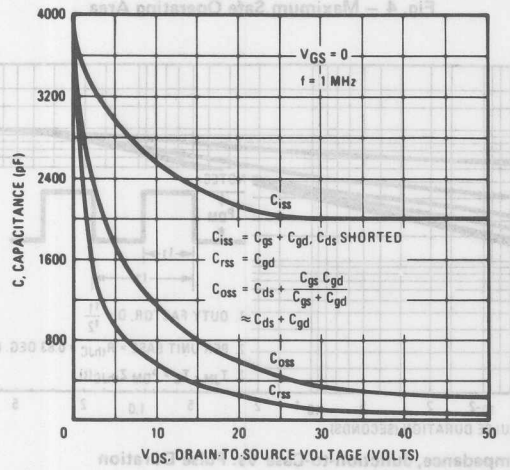


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

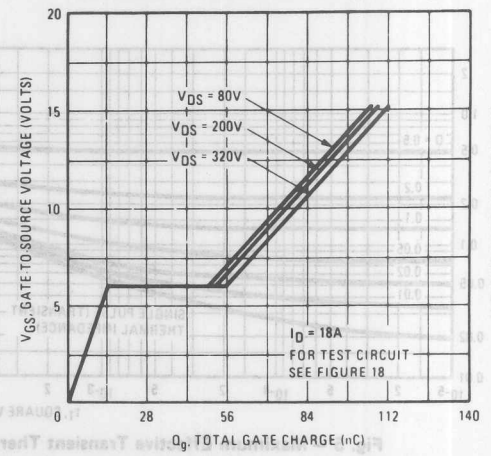


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

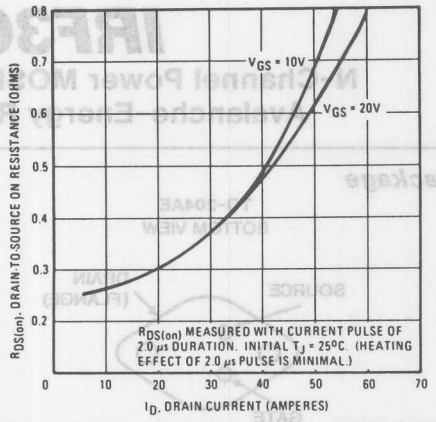


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

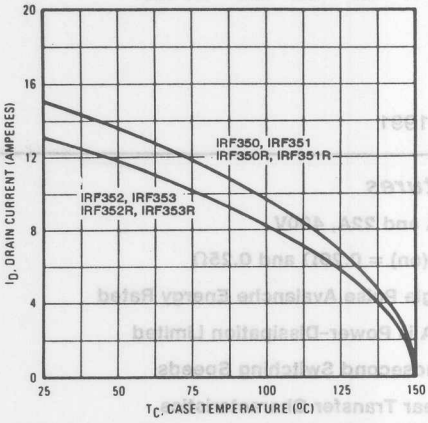


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

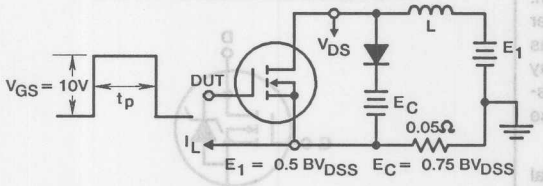


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

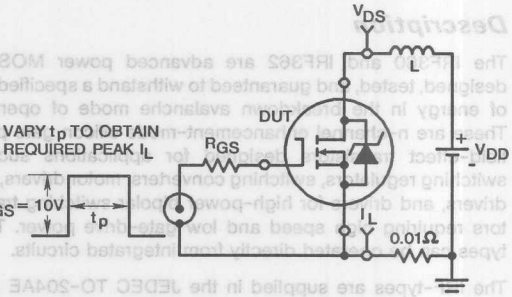


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

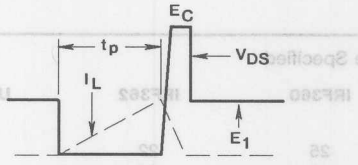


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

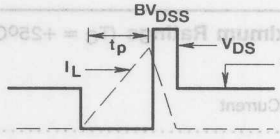


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

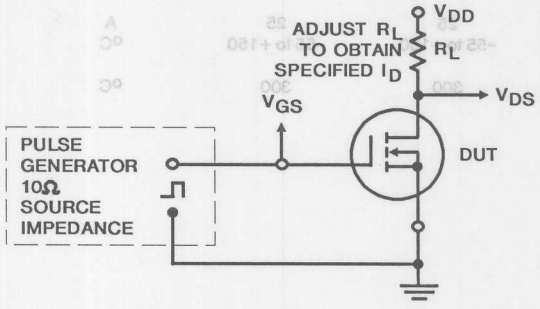


FIGURE 16. SWITCHING TIME TEST CIRCUIT

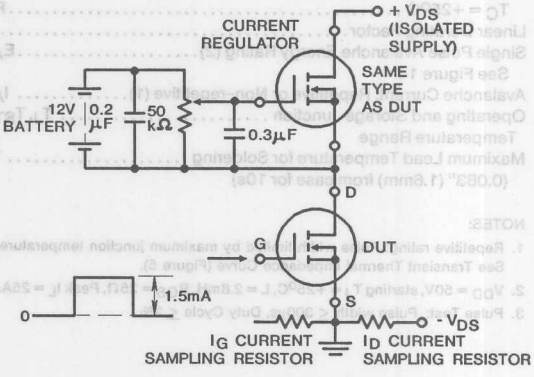


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF360
IRF362

N-Channel Power MOSFETs
Avalanche-Energy Rated

August 1991

Features

- 25A and 22A, 400V
- $r_{DS}(on)$ = 0.20Ω and 0.25Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

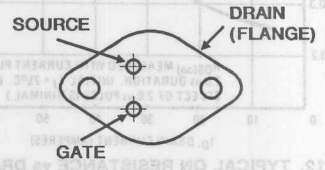
Description

The IRF360 and IRF362 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

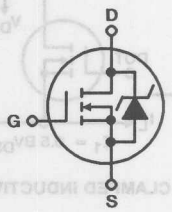
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF360	IRF362	UNITS
Continuous Drain Current				
T_C = +25°C	I_D	25	22	A
T_C = +100°C	I_D	16	14	A
Pulsed Drain Current (1)	I_{DM}	100	88	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	300	300	W
Linear Derating Factor		2.4	2.4	W/°C
Single Pulse Avalanche Energy Rating (2) See Figure 14	E_{AS}	980	980	mj
Avalanche Current, Repetitive or Non-repetitive (1)	I_{AR}	25	25	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

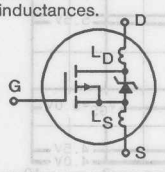
1. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
2. V_{DD} = 50V, starting T_J = +25°C, L = 2.8mH, R_{GS} = 25Ω, Peak I_L = 25A.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

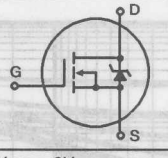
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File Number **2276.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 3) IRF360	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	25	–	–	A
IRF362			22	–	–	A
Static Drain-Source On-State Resistance (Note 3) IRF360	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 14A	–	0.18	0.20	Ω
IRF362			–	0.20	0.25	Ω
Forward Transconductance (Note 3)	g_{fs}	I_{DS} = 14A, V_{DS} ≥ 50V	14	21	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	4000	–	pF
Output Capacitance	C_{OSS}		–	550	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	97	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 25A, R_G = 4.3Ω R_D = 7.5Ω. (MOSFET switching times are essentially independent of operating temperature)	–	22	33	ns
Rise Time	t_r		–	94	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	80	120	ns
Fall Time	t_f		–	66	99	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 25A, V_{DS} = 0.8V x Max Rating. See Figure 16 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	120	170	nC
Gate-Source Charge	Q_{gs}		–	19	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	60	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	13	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.42	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.10	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	25	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	100	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 25A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/µs	200	460	1000	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/µs	3.1	7.1	16	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES:
1. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
2. V_{DD} = 50V, Starting T_J = +25°C, L = 2.8mH, I_L = 25A
3. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%

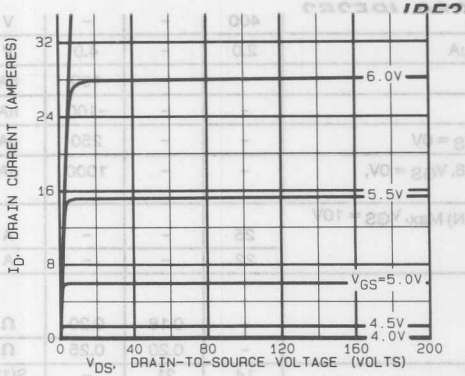


Fig. 1 - Typical output characteristics.

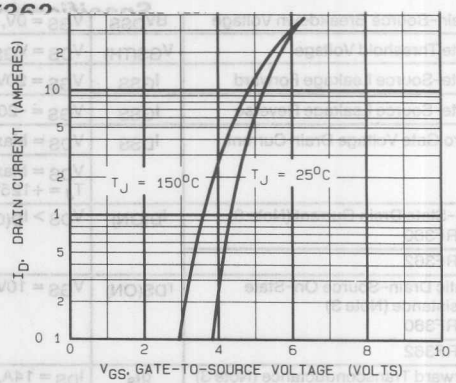


Fig. 2 - Typical transfer characteristics.

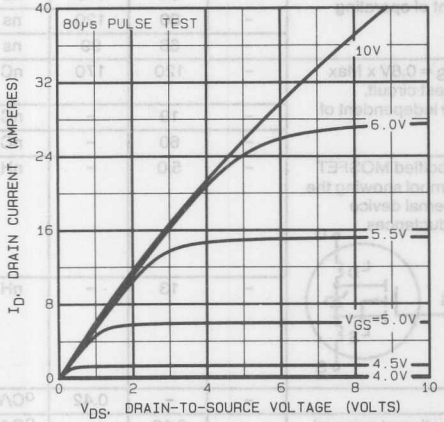


Fig. 3 - Typical saturation characteristics.

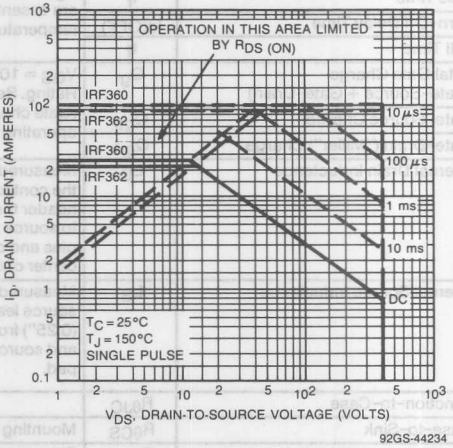
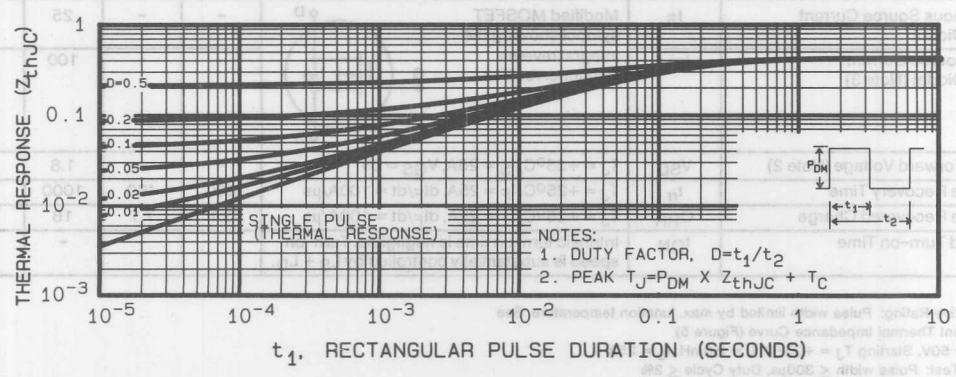


Fig. 4 - Maximum safe operating area.



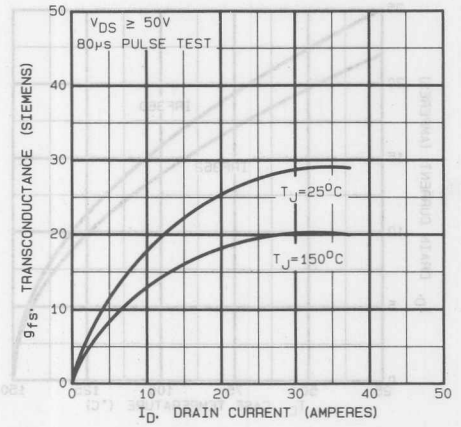


Fig. 6 - Typical transconductance vs. drain current.

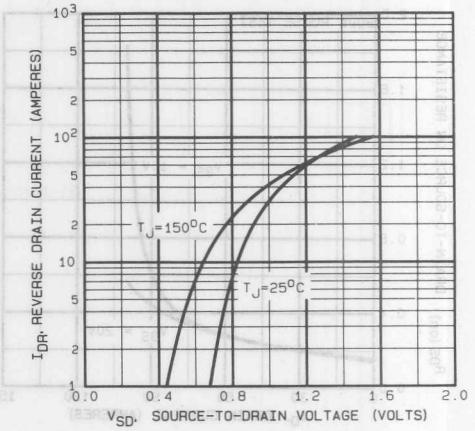


Fig. 7 - Typical source-drain diode forward voltage.

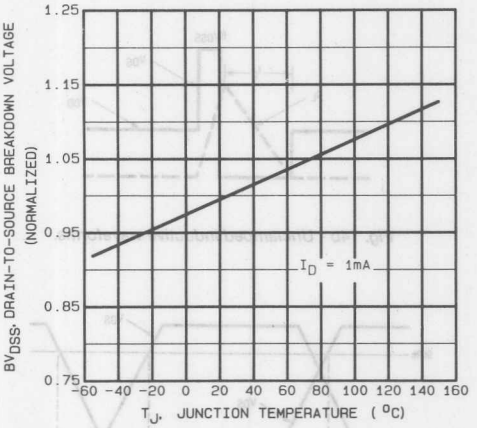


Fig. 8 - Breakdown voltage vs. temperature.

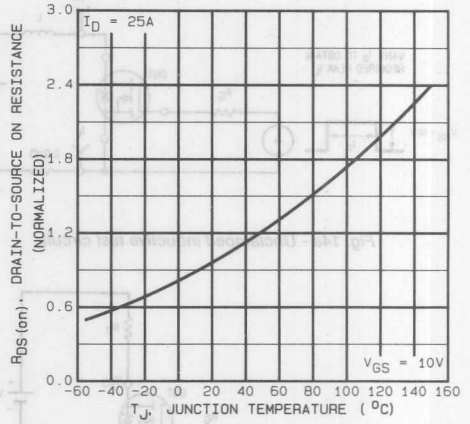


Fig. 9 - Normalized on-resistance vs. temperature.

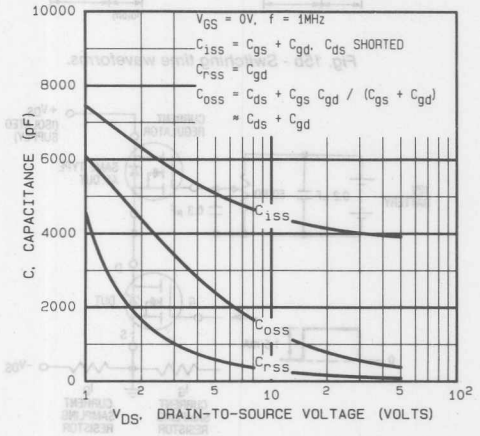


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

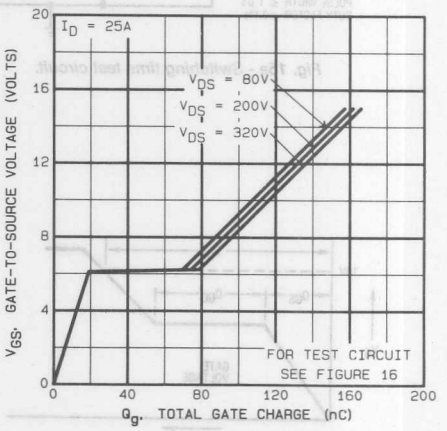


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

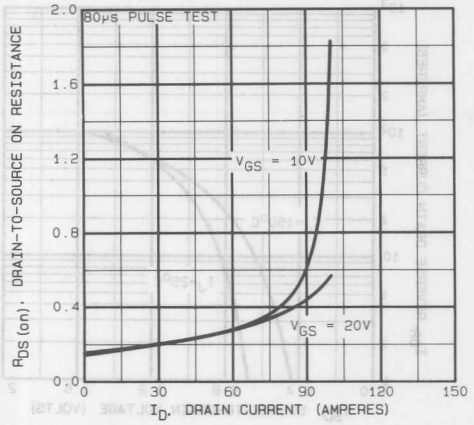


Fig. 12 - Typical on-resistance vs. drain current.

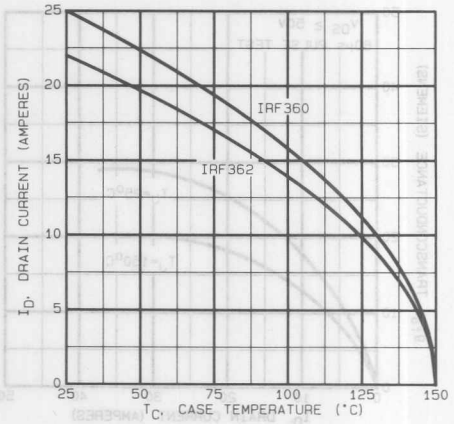


Fig. 13 - Maximum drain current vs. case temperature.

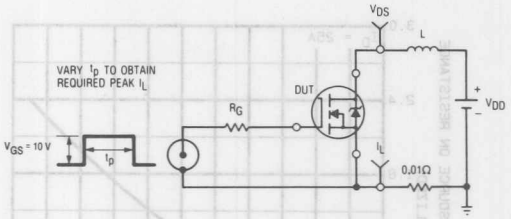


Fig. 14a - Unclamped inductive test circuit.

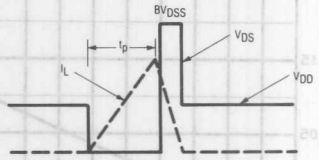


Fig. 14b - Unclamped inductive waveforms.

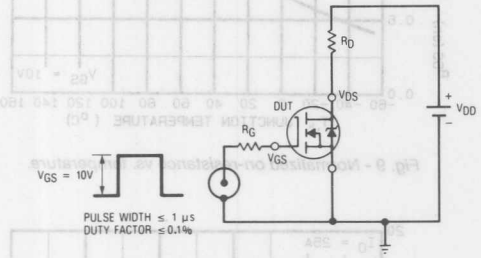


Fig. 15a - Switching time test circuit.

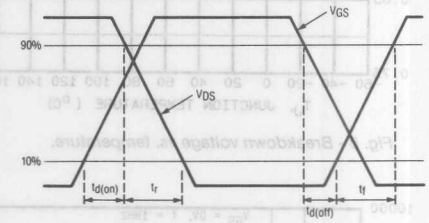


Fig. 15b - Switching time waveforms.

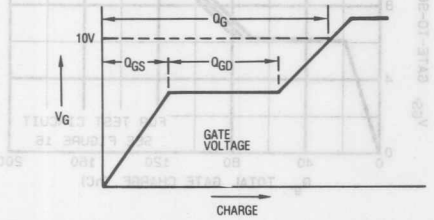


Fig. 16a - Basic gate charge waveform.

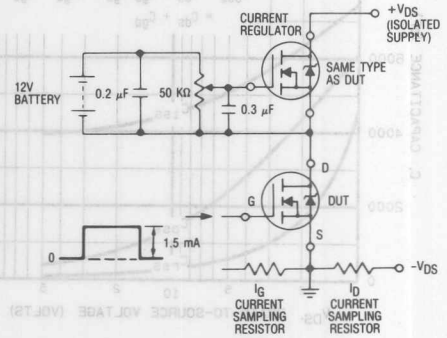


Fig. 16b - Gate charge test circuit.

IRF420, IRF421
IRF422, IRF423

N-Channel Enhnancement Mode Power Field-Effect Transistors

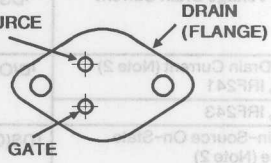
August 1991

Features

- 2.2A and 2.5A, 450V - 500V
- $r_{DS(on)}$ = 3.0Ω and 4.0Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AA
BOTTOM VIEW



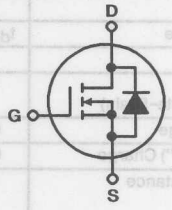
Description

The IRF420, IRF421, IRF422, and IRF423 are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF420	IRF421	IRF422	IRF423	UNITS
Drain-Source Voltage (1)	V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	500	450	500	450	V
Continuous Drain Current						
T_C = +25°C	I_D	2.5	2.5	2.2	2.2	A
T_C = +100°C	I_D	1.6	1.6	1.4	1.4	A
Pulsed Drain Current (3)	I_{DM}	10	10	8.0	8.0	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	50	50	50	50	W
Linear Derating Factor		0.4	0.4	0.4	0.4	W/°C
Inductive Current, Clamped (See Figures 14 & 15, L = 100μH)		10	10	8.0	8.0	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

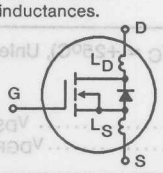
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

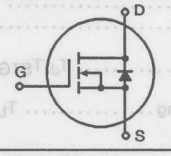
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File Number 1571.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF420, IRF422	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500	–	–	V
IRF421, IRF423			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF420, IRF241	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, V_{GS} = 10V	2.5	–	–	A
IRF242, IRF243			2.2	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF420, IRF241	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.4A	–	2.5	3.0	Ω
IRF242, IRF243			–	3.0	4.0	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 1.4A	1.5	2.3	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	300	–	pF
Output Capacitance	C_{OSS}		–	75	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 2.5A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	10	15	ns
Rise Time	t_r		–	12	18	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	28	42	ns
Fall Time	t_f		–	12	18	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 2.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	11	19	nC
Gate-Source Charge	Q_{gs}		–	5.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	6.0	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	2.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	2.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	10	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.5A, V_{GS} = 0V	–	–	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 2.5A, dI_F/dt = 100A/μs	130	270	540	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 2.5A, dI_F/dt = 100A/μs	0.57	1.2	2.3	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)

Performance Curves

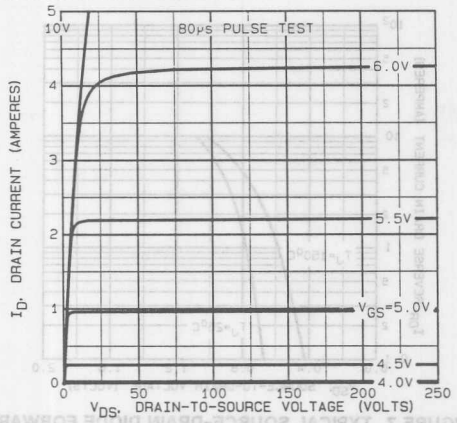


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

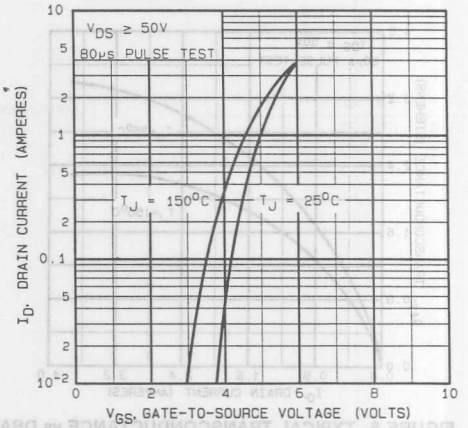


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

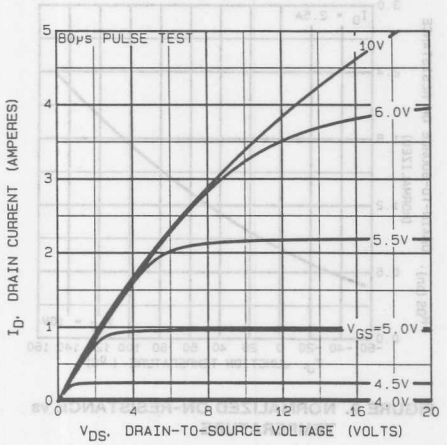


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

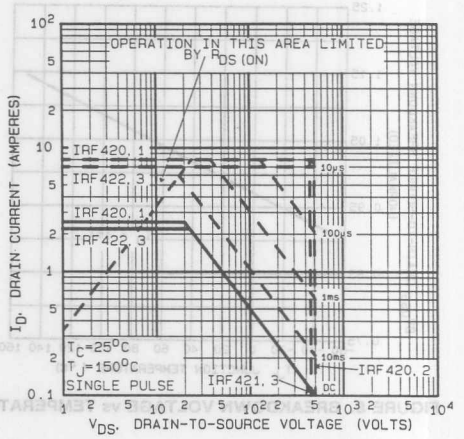


FIGURE 4. MAXIMUM SAFE OPERATING AREA

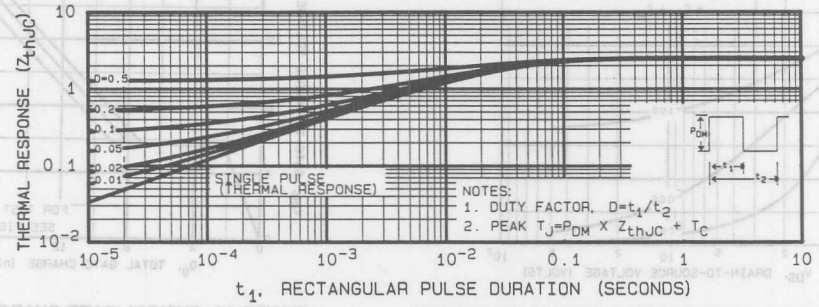


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

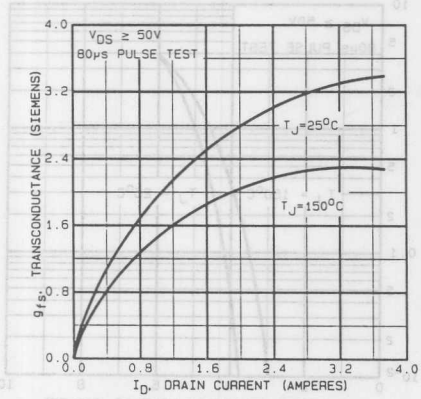


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

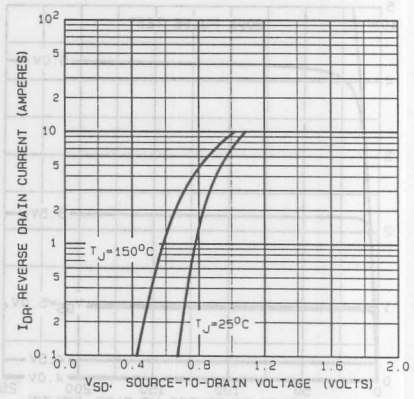


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

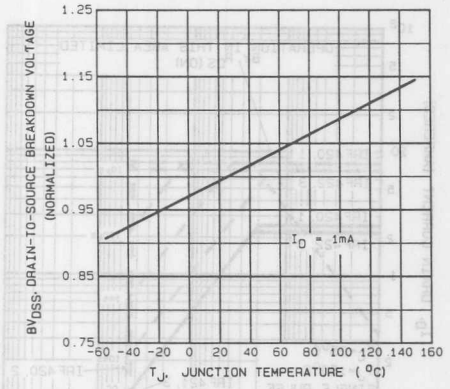


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

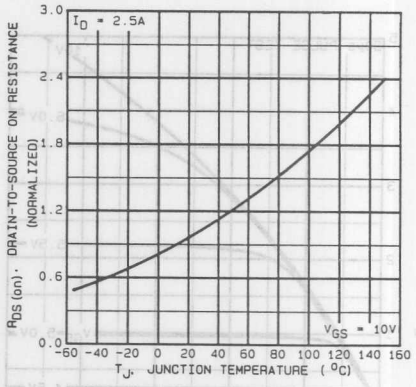


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

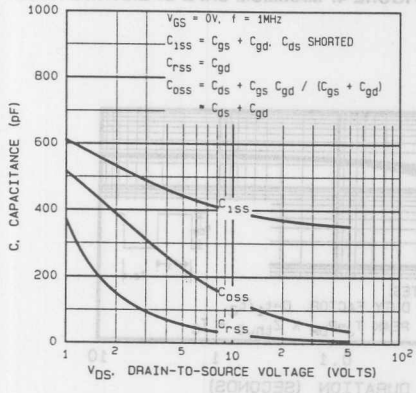


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

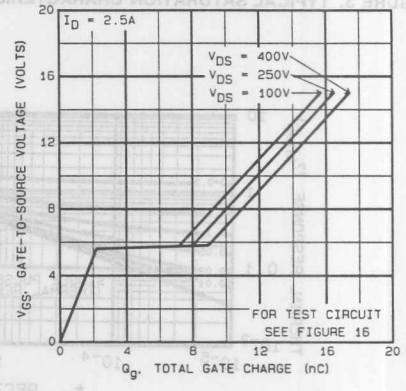


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

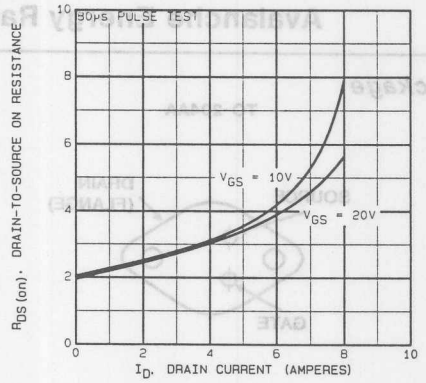


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

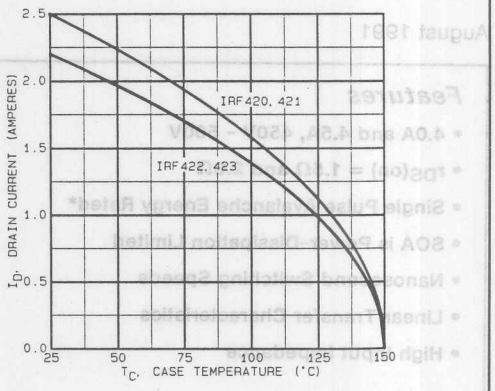


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

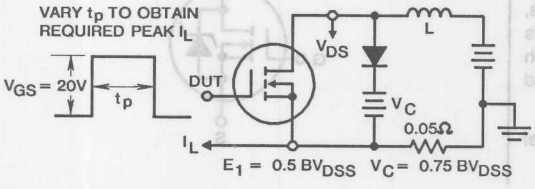


FIGURE 14. CLAMPED INDUCTIVE TEST CIRCUIT

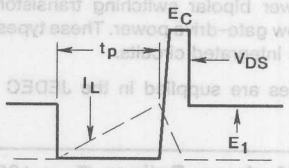


FIGURE 15. CLAMPED INDUCTIVE WAVEFORMES

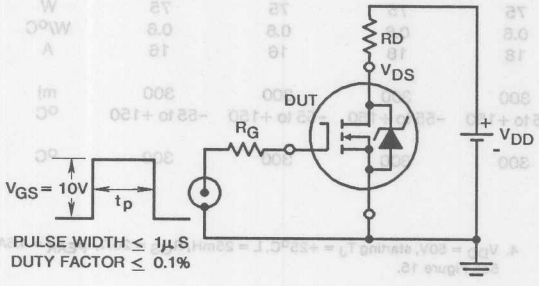


FIGURE 16. SWITCHING TIME TEST CIRCUIT

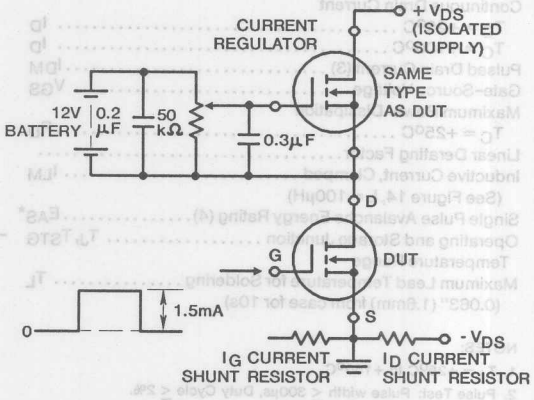


FIGURE 17. GATE CHARGE TEST CIRCUIT

Features

- 4.0A and 4.5A, 450V - 500V
- $r_{DS}(on)$ = 1.5Ω and 2.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

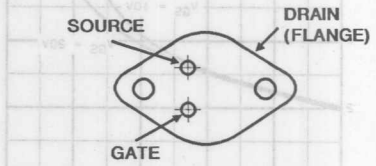
Description

The IRF430, IRF431, IRF432, and IRF433 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF430R, IRF431R, IRF432R and IRF433R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

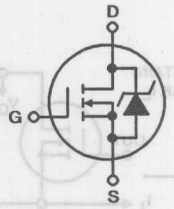
Package

TO-204AA



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF430 IRF430R	IRF431 IRF431R	IRF432 IRF432R	IRF433 IRF433R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	4.5	4.5	4.0	4.0	A
T_C = +100°C ..... I_D	3.0	3.0	2.5	2.5	A
Pulsed Drain Current (3) ..... I_{DM}	18	18	16	16	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	18	18	16	16	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	300	300	300	300	mj
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 25mH, R_{GS} = 20Ω, I_{PEAK} = 4.5A. See Figure 15.

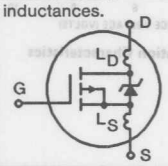
*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

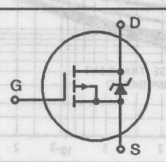
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Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF430/432, IRF430R/432R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	–	–	V
IRF431/433, IRF431R/433R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF430/431, IRF430R/431R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	4.5	–	–	A
IRF432/433, IRF432R/433R			4.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF430/431, IRF430R/431R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 2.5A	–	1.3	1.5	Ω
IRF432/433, IRF432R/433R			–	1.5	2.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 2.5A	2.7	3.2	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	100	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	30	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 4.5A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	11	17	ns
Rise Time	t_r		–	15	23	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	35	53	ns
Fall Time	t_f		–	15	23	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	22	32	nC
Gate-Source Charge	Q_{gs}		–	3.5	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	11	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	4.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	18	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 4.5A, V_{GS} = 0V	–	–	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 4.5A, dI_F/dt = 100A/µs	180	370	760	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 4.5A, dI_F/dt = 100A/µs	0.96	2	4.3	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 25mH, R_{GS} = 25Ω, I_{PEAK} = 4.5A (See Figure 15)

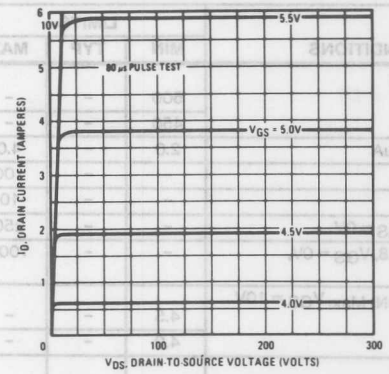


Fig. 1 – Typical Output Characteristics

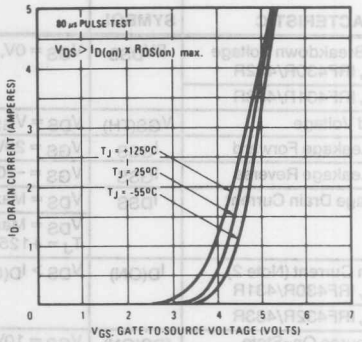


Fig. 2 – Typical Transfer Characteristics

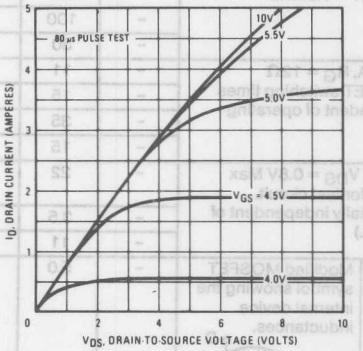


Fig. 3 – Typical Saturation Characteristics

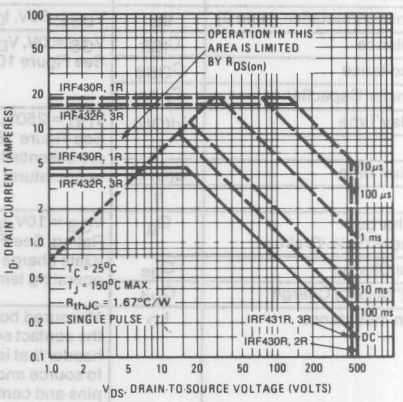


Fig. 4 – Maximum Safe Operating Area

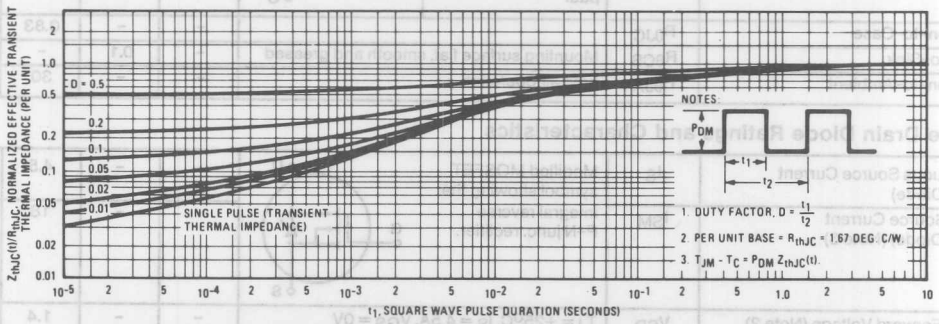


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

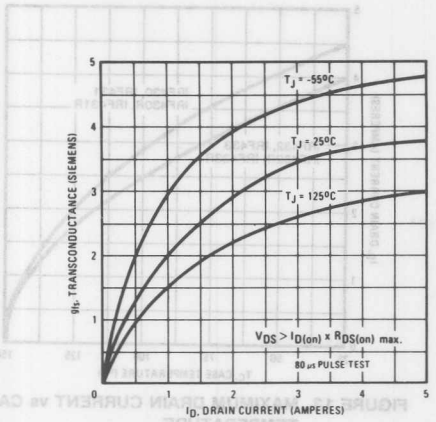


Fig. 6 – Typical Transconductance Vs. Drain Current

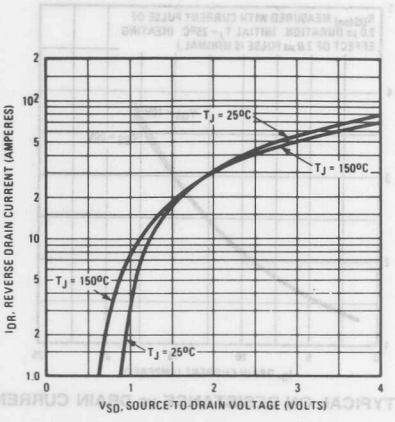


Fig. 7 – Typical Source-Drain Diode Forward Voltage

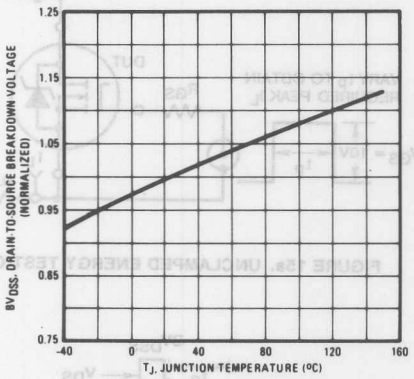


Fig. 8 – Breakdown Voltage Vs. Temperature

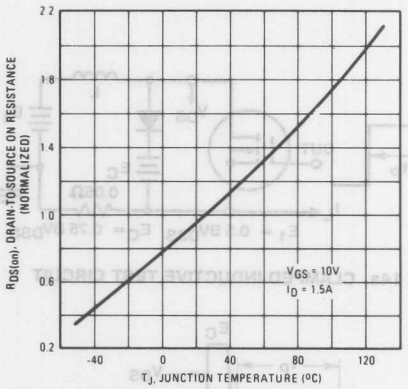


Fig. 9 – Normalized On-Resistance Vs. Temperature

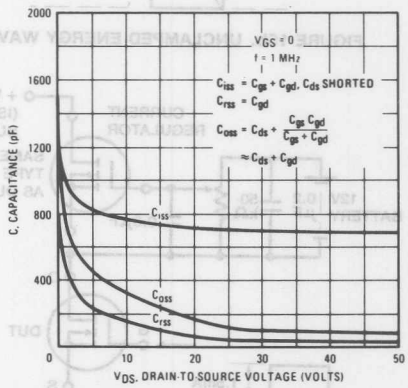


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

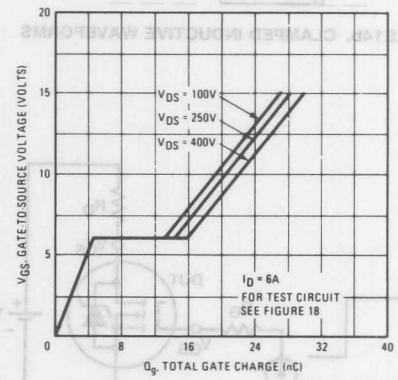


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

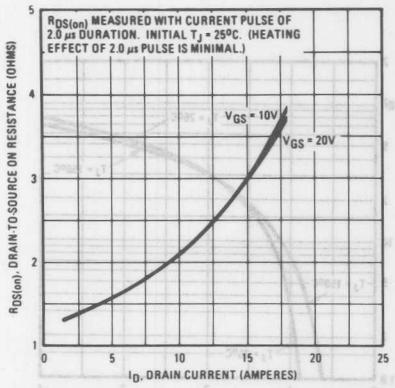


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

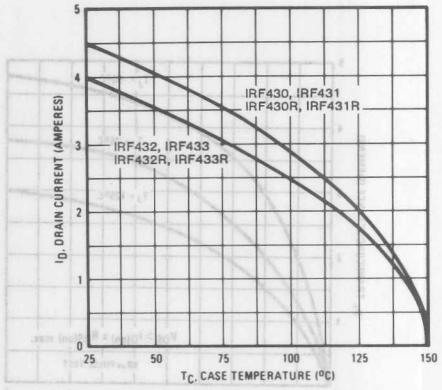


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

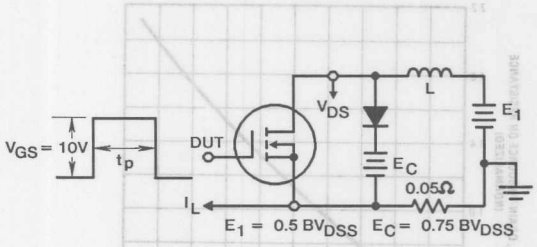


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

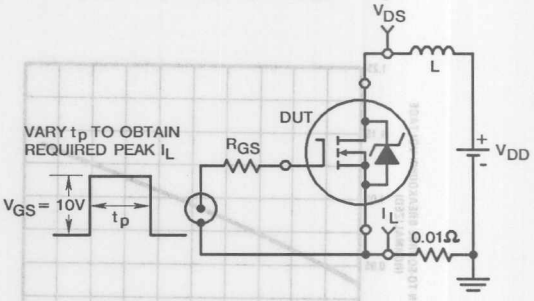


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

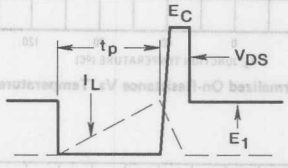


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

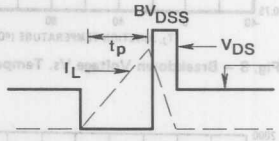


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

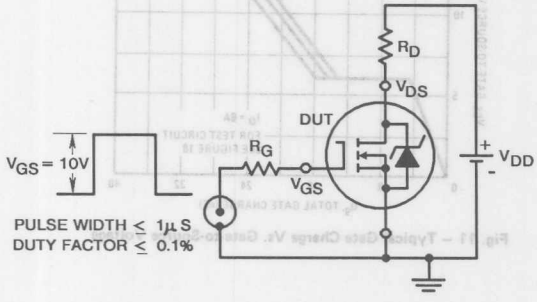


FIGURE 16. SWITCHING TIME TEST CIRCUIT

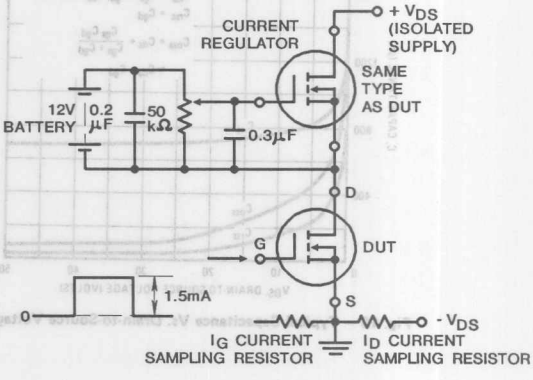


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF440/441/442/443
IRF440R/441R/442R/443R

N-Channel Power MOSFETs
Avalanche Energy Rated*

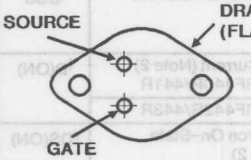
August 1991

Features

- 7A and 8A, 450V - 500V
- $r_{DS(on)}$ = 0.85Ω and 1.1Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AA
BOTTOM VIEW



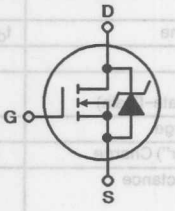
Description

The IRF440, IRF441, IRF442, and IRF443 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF440R, IRF441R, IRF442R and IRF443R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF440 IRF440R	IRF441 IRF441R	IRF442 IRF442R	IRF443 IRF443R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	8.0	8.0	7.0	7.0	A
T_C = +100°C ..... I_D	5.0	5.0	4.4	4.4	A
Pulsed Drain Current (3) ..... I_{DM}	32	32	28	28	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM}	32	32	28	28	A
(See Figure 14, L = 100μH)					
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	510	510	510	510	mj
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L	300	300	300	300	°C
(0.063" (1.6mm) from case for 10s)					

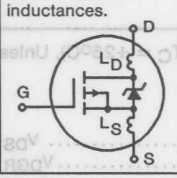
NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 14mH, R_{GS} = 25Ω, I_{PEAK} = 8A. See Figure 15.

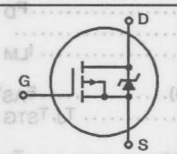
*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
Copyright © Harris Corporation 1991

File Number 2308.1

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage IRF440/442, IRF440R/442R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500	–	–	V
IRF441/443, IRF441R/443R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF440/441, IRF440R/441R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, V_{GS} = 10V	8.0	–	–	A
IRF442/443, IRF442R/443R			7.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF440/441, IRF440R/441R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.4A	–	0.70	0.85	Ω
IRF442/443, IRF442R/443R			–	0.85	1.1	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 4.4A	4.9	7.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1225	–	pF
Output Capacitance	C_{OSS}		–	200	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	85	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D ≃ 8A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	15	21	ns
Rise Time	t_r		–	22	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	49	74	ns
Fall Time	t_f		–	20	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	42	63	nC
Gate-Source Charge	Q_{gs}		–	9	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	22	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	8.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.0A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 8.0A, dI_F/dt = 100A/μs	210	460	970	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 8.0A, dI_F/dt = 100A/μs	2	4	8.9	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 14mH, R_{GS} = 25Ω, I_{PEAK} = 8A (See Figure 15)

Performance Curves

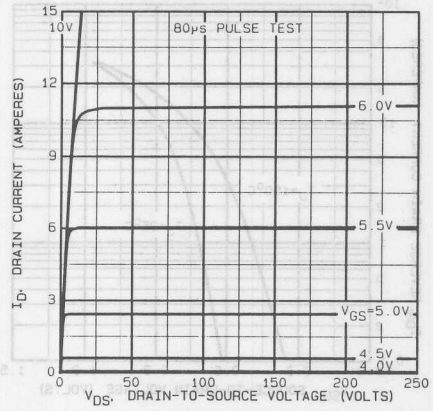


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

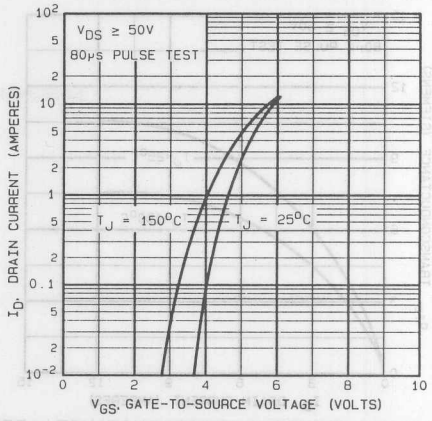


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

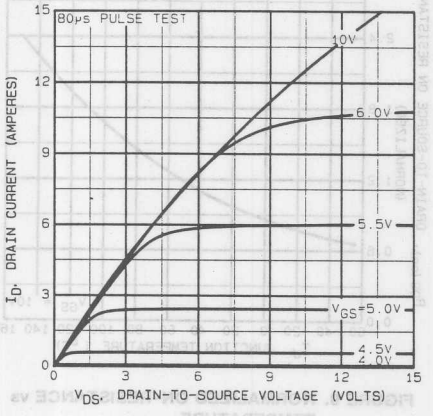


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

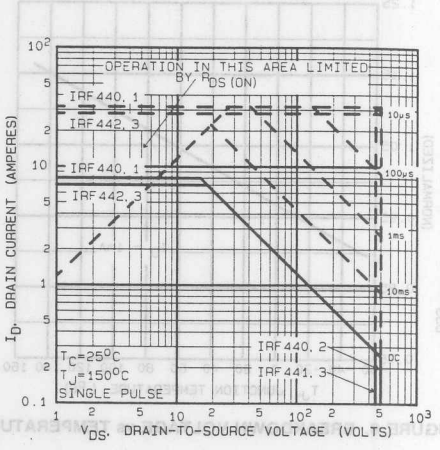


FIGURE 4. MAXIMUM SAFE OPERATING AREA

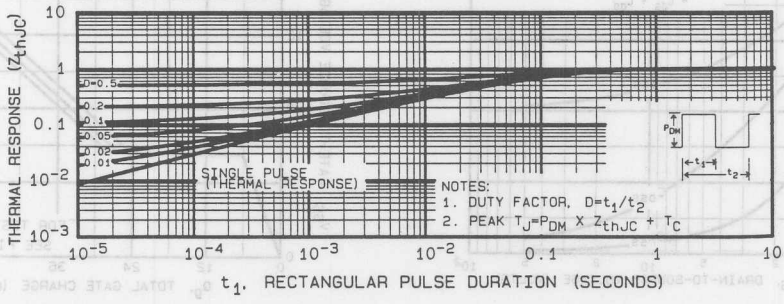


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

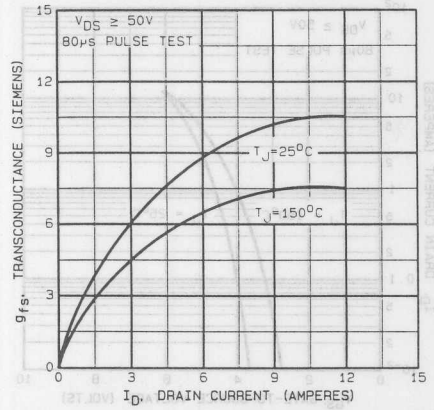


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

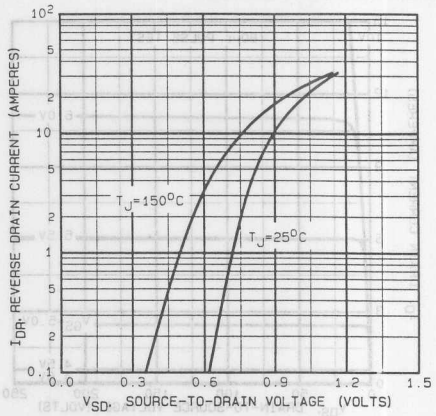


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

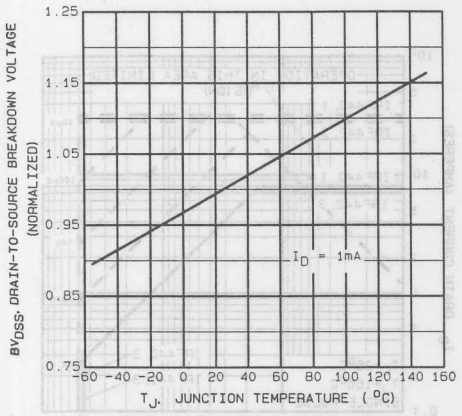


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

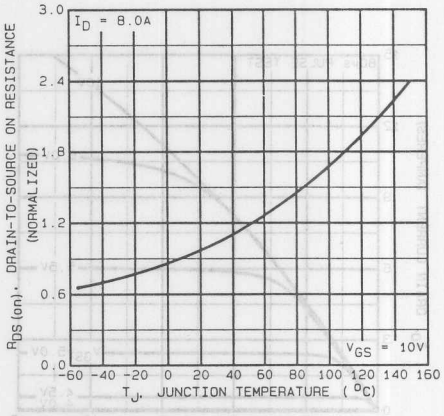


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

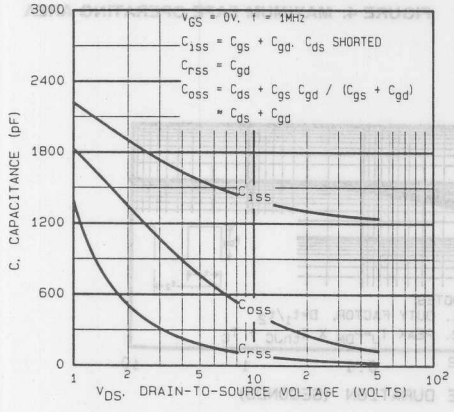


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

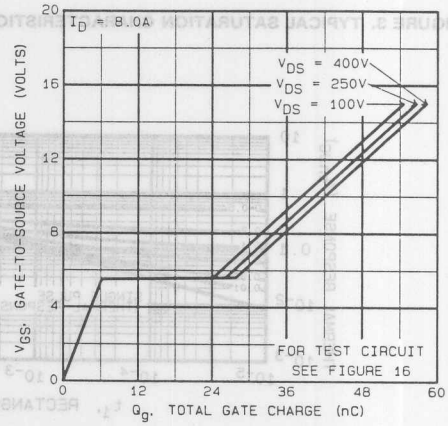


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

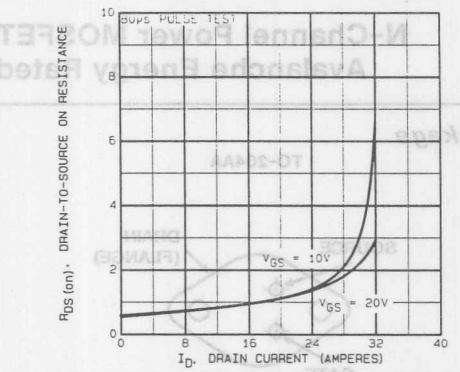


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

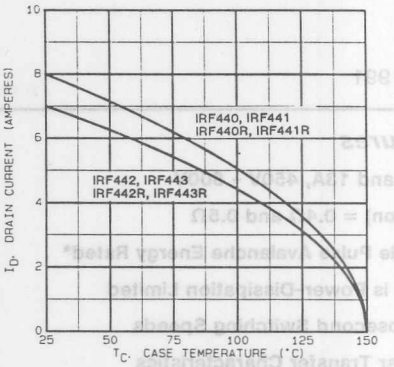


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

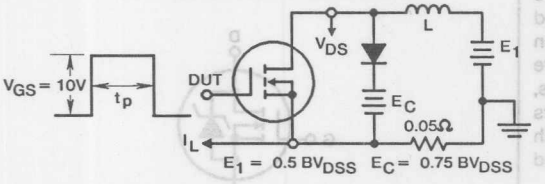


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

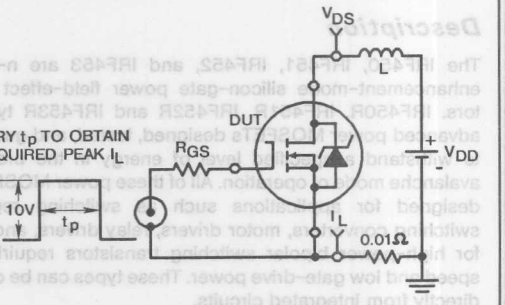


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

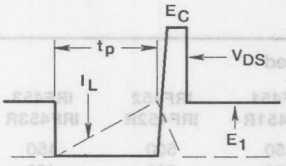


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

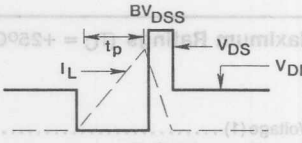


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

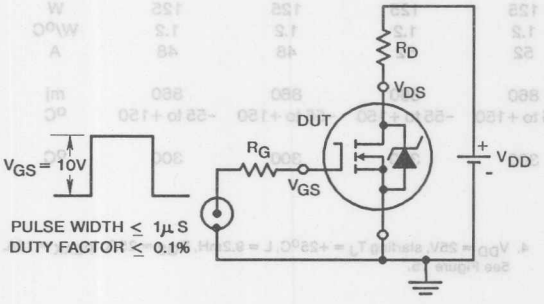


FIGURE 16. SWITCHING TIME TEST CIRCUIT

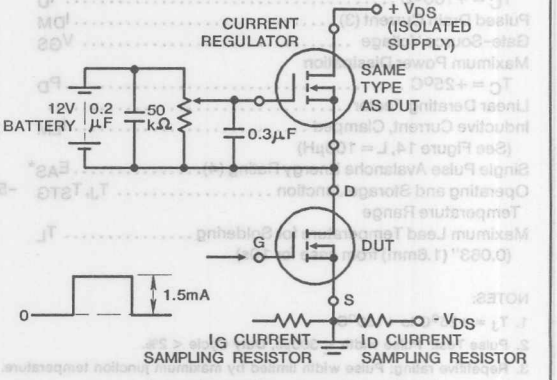


FIGURE 17. GATE CHARGE TEST CIRCUIT

4 N-CHANNEL POWER MOSFETs

HARRIS

IRF450/451/452/453
IRF450R/451R/452R/453R

N-Channel Power MOSFETs
Avalanche Energy Rated*

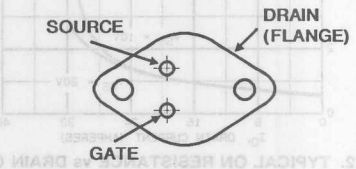
August 1991

Features

- 11A and 13A, 450V - 500V
- $r_{DS}(on)$ = 0.4Ω and 0.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AA



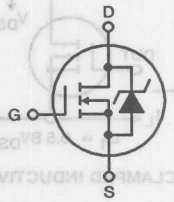
Description

The IRF450, IRF451, IRF452, and IRF453 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF450R, IRF451R, IRF452R and IRF453R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF450 IRF450R	IRF451 IRF451R	IRF452 IRF452R	IRF453 IRF453R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	13	13	11	11	A
T_C = +100°C ..... I_D	8.1	8.1	7.2	7.2	A
Pulsed Drain Current (3) ..... I_{DM}	52	52	44	44	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	52	52	48	48	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	860	860	860	860	mj
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 9.2mH, R_{GS} = 25Ω, I_{PEAK} = 13A. See Figure 15.

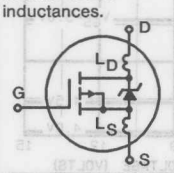
*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

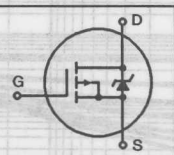
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File Number 1827.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF450/452, IRF450R/452R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	–	–	V
IRF451/453, IRF451R/453R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF450/451, IRF450R/451R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	13	–	–	A
IRF452/453, IRF452R/453R			11	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF450/451, IRF450R/451R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 7.2A	–	0.3	0.4	Ω
IRF452/453, IRF452R/453R			–	0.4	0.5	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 7.2A	6.0	11	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1800	–	pF
Output Capacitance	C_{OSS}		–	400	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	100	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, $I_D \simeq$ 13A, R_G = 6.2Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	20	27	ns
Rise Time	t_r		–	40	66	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	72	100	ns
Fall Time	t_f		–	35	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 13A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	85	130	nC
Gate-Source Charge	Q_{gs}		–	12	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	42	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	13	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	52	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 13A, V_{GS} = 0V	–	–	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 13A, dI_F/dt = 100A/µs	280	600	1200	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 13A, dI_F/dt = 100A/µs	3.2	7.5	14	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 9.2mH, R_{GS} = 25Ω, I_{PEAK} = 13A (See Figure 15)

Performance Curves

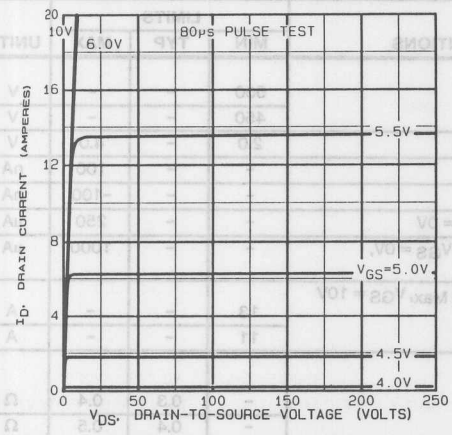


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

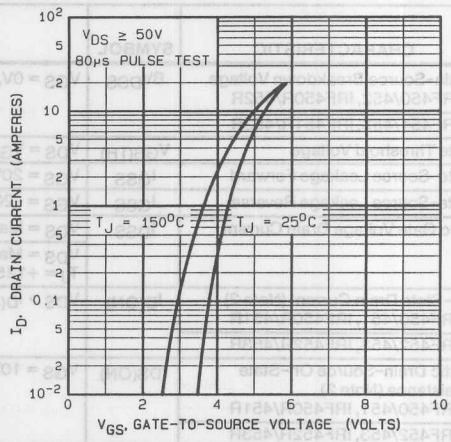


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

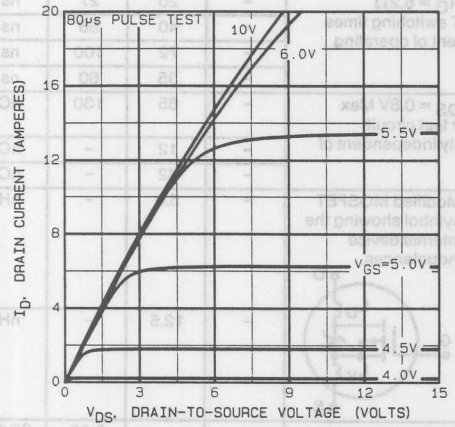


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

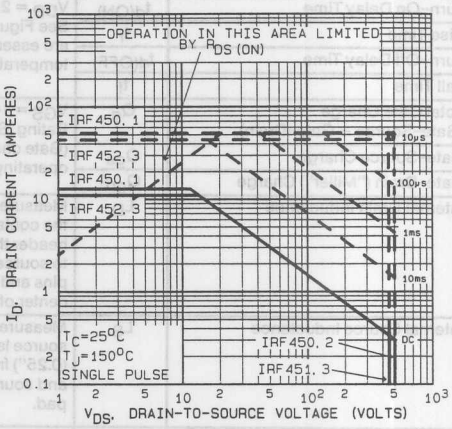


FIGURE 4. MAXIMUM SAFE OPERATING AREA

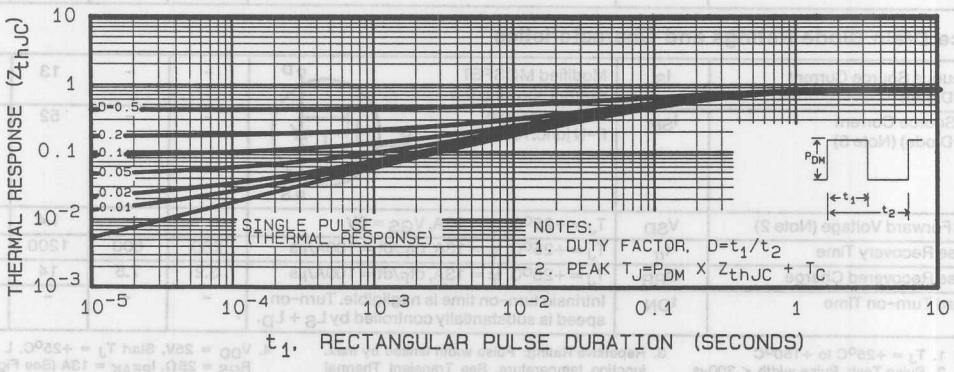


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

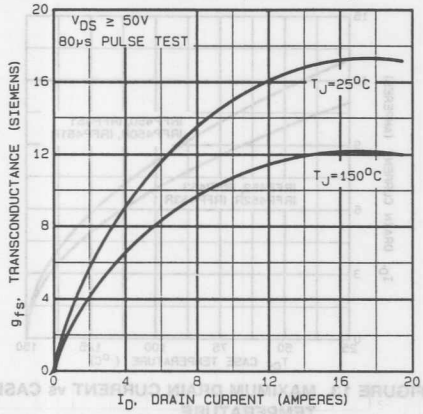


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

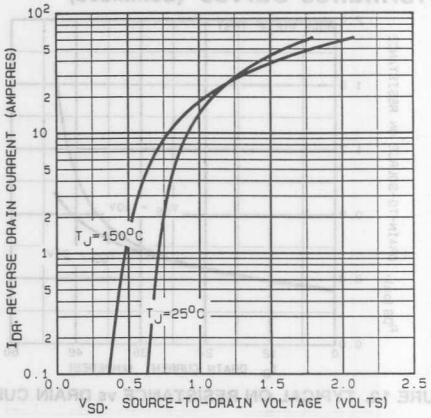


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

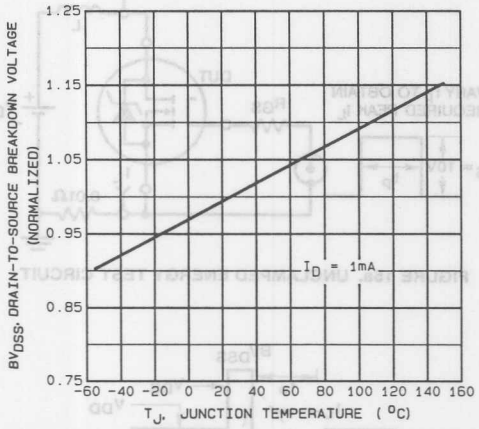


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

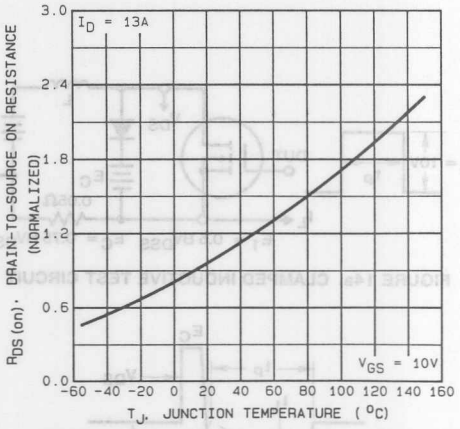


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

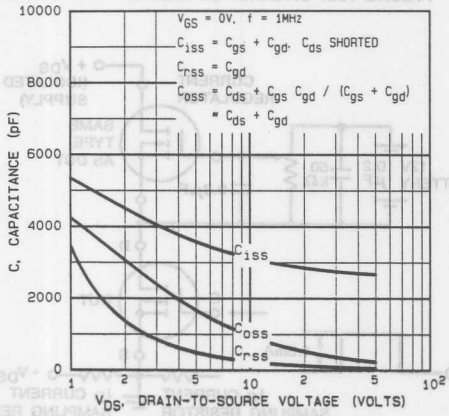


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

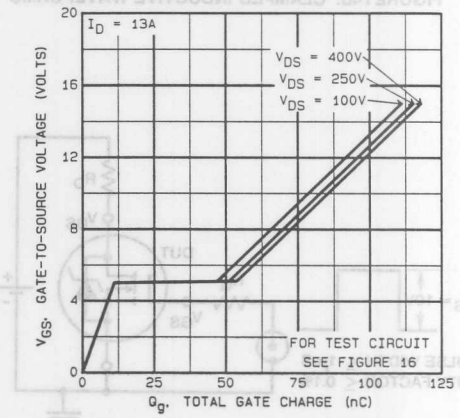


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

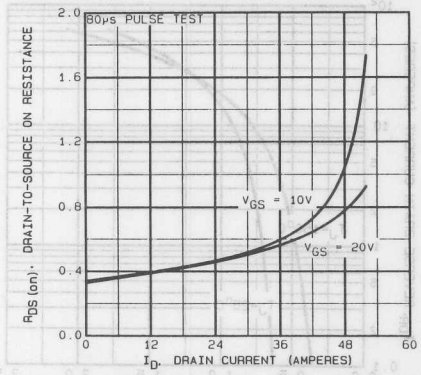


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

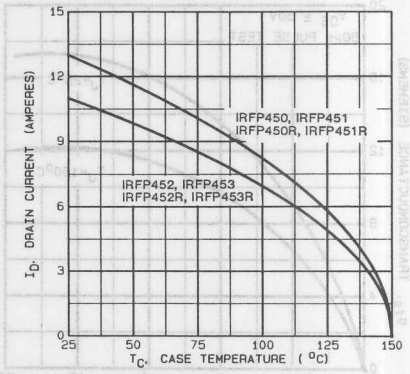


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

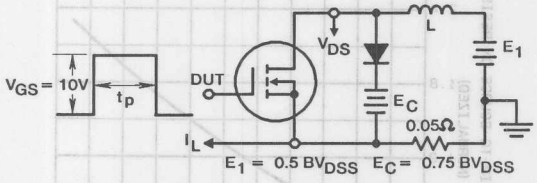


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

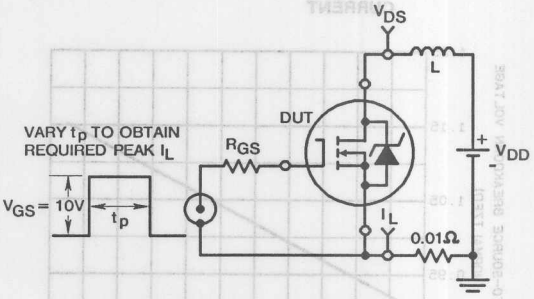


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

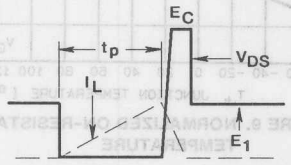


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

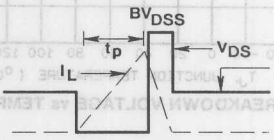


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

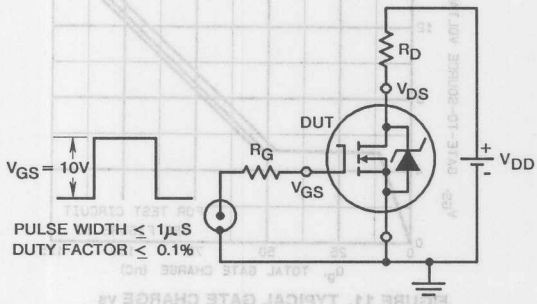


FIGURE 16. SWITCHING TIME TEST CIRCUIT

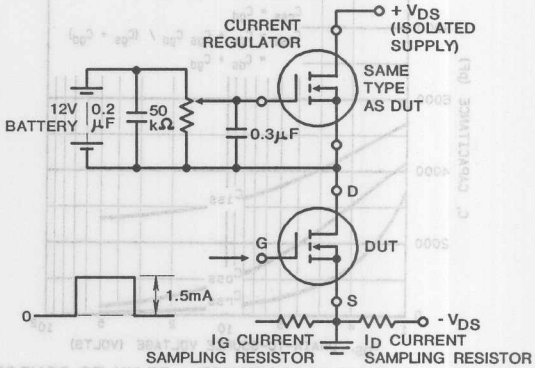


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF460
IRF462

N-Channel Power MOSFETs
Avalanche-Energy Rated

August 1991

Features

- 21A and 19A, 500V
- $r_{DS}(on)$ = 0.27Ω and 0.35Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

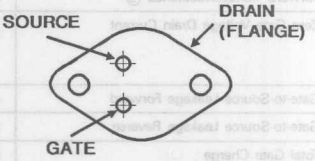
Description

The IRF460 and IRF462 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

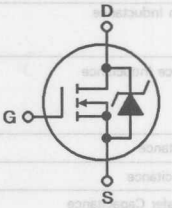
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4

N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF460	IRF462	UNITS
Continuous Drain Current			
T_C = +25°C ..... I_D	21	19	A
T_C = +100°C ..... I_D	14	12	A
Pulsed Drain Current (1) ..... I_{DM}	84	76	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = +25°C ..... P_D	300	300	W
Linear Derating Factor	2.4	2.4	W/°C
Single Pulse Avalanche Energy Rating (2) ..... E_{AS}* See Figure 14	1200	1200	mj
Avalanche Current, Repetitive or Non-repetitive (1) ..... I_{AR}	21	21	A
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	°C

NOTES:

1. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
2. V_{DD} = 50V, starting T_J = +25°C, L = 4.9mH, R_{GS} = 25Ω, Peak I_L = 21A.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

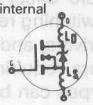
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2277.1

BV_{DSS}	Drain-to-Source Breakdown Voltage	ALL	500	–	–	V	V_{GS} = 0V, I_D = 250 μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRF460	–	0.24	0.27	Ω	V_{GS} = 10V, I_D = 12A
		IRF462	–	0.27	0.35		
$I_{D(on)}$	On-State Drain Current ③	IRF460	21	–	–	A	V_{DS} > $I_{D(on)}$ X $R_{DS(on)}$ Max.
		IRF462	19	–	–		V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance ③	ALL	13	20	–	S (℧)	V_{DS} ≥ 50V, I_{DS} = 12A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	–	–	–100	nA	V_{GS} = –20V
Q_g	Total Gate Charge	ALL	–	120	190	nC	V_{GS} = 10V, I_D = 21A
Q_{gs}	Gate-to-Source Charge	ALL	–	18	—	nC	V_{DS} = 0.8 x Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	–	62	—	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	–	23	35	ns	V_{DD} = 250V, I_D ≈ 21A, R_G = 4.3Ω
t_r	Rise Time	ALL	–	81	120	ns	R_D = 12Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	85	130	ns	See Fig. 15
t_f	Fall Time	ALL	–	65	98	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	13	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	–	4100	–	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	–	480	–	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	–	84	–	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	–	–	0.42	°C/W	
R_{thJS}	Case-to-Sink	ALL	–	0.10	–	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Typical socket mount

Modified MOSFET symbol showing the internal inductances.



① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 4.9 μH, R_G = 25Ω, Peak I_L = 21A.

③ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	–	–	21	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	–	–	84	A	
V_{SD}	Diode Forward Voltage ③	ALL	–	–	1.8	V	T_J = 25°C, I_S = 21A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	280	580	1200	ns	T_J = 25°C, I_F = 21A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	3.8	8.1	18	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



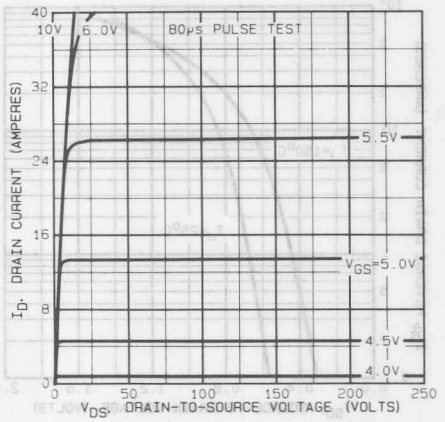


Fig. 1 - Typical output characteristics.

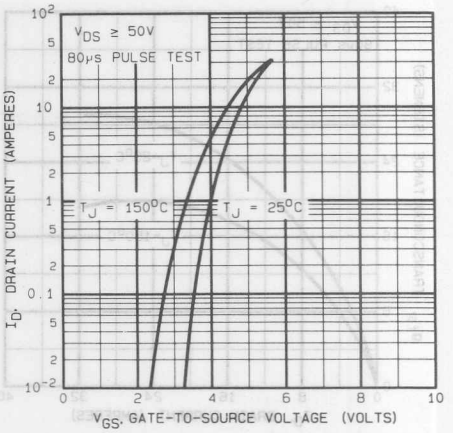


Fig. 2 - Typical transfer characteristics.

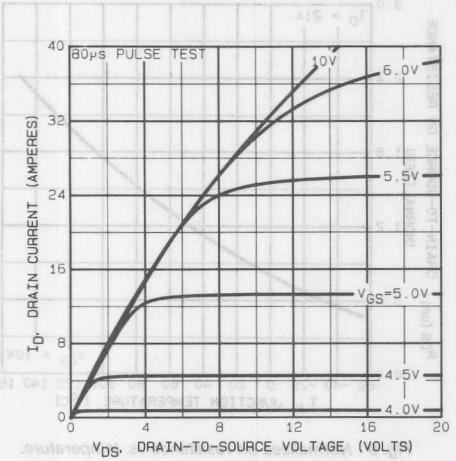


Fig. 3 - Typical saturation characteristics.

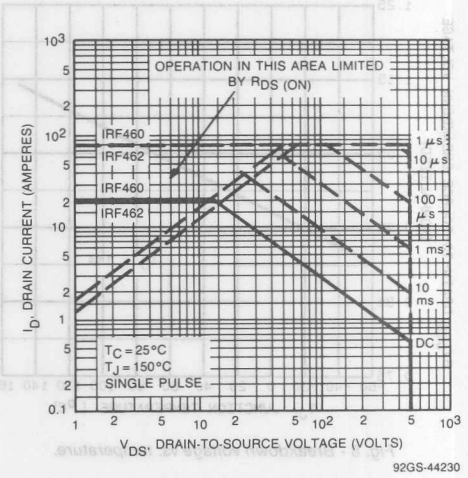


Fig. 4 - Maximum safe operating area.

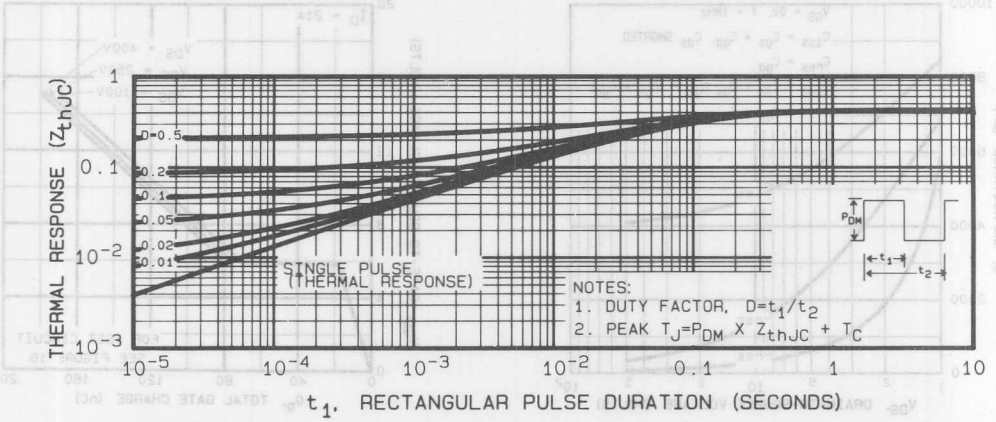


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

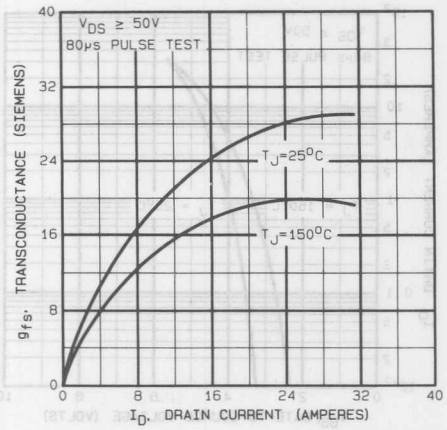


Fig. 6 - Typical transconductance vs. drain current.

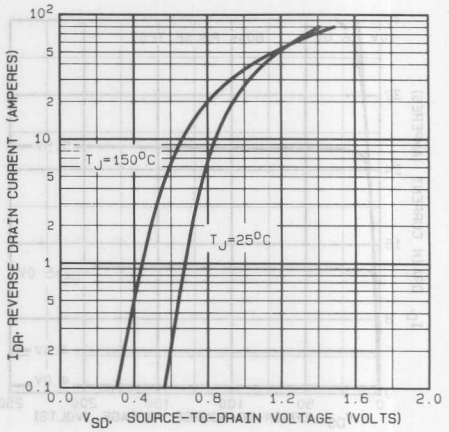


Fig. 7 - Typical source-drain diode forward voltage.

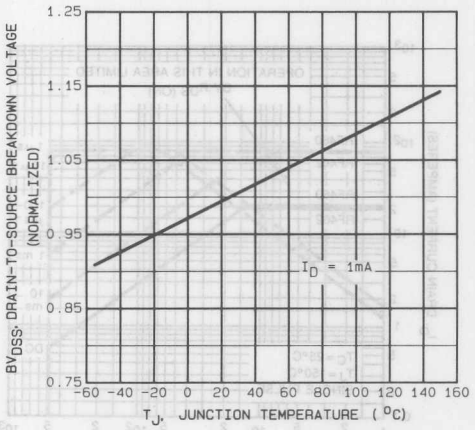


Fig. 8 - Breakdown voltage vs. temperature.

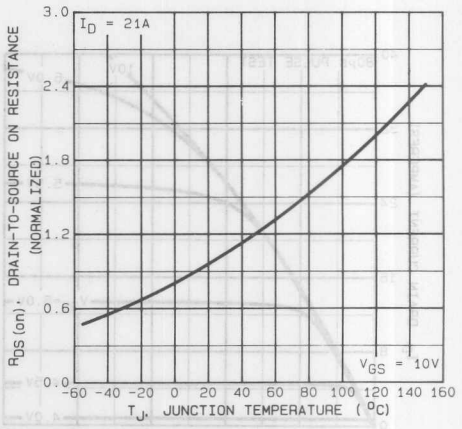


Fig. 9 - Normalized on-resistance vs. temperature.

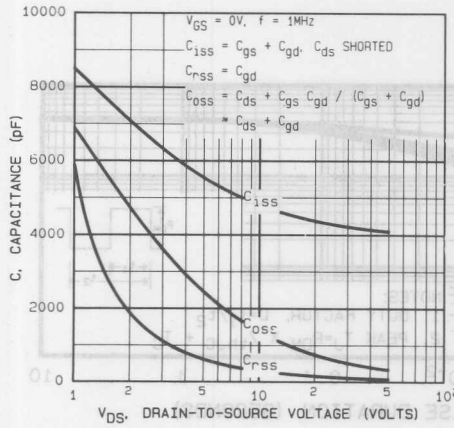


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

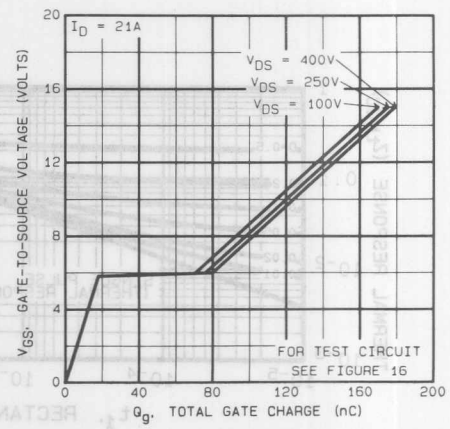


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

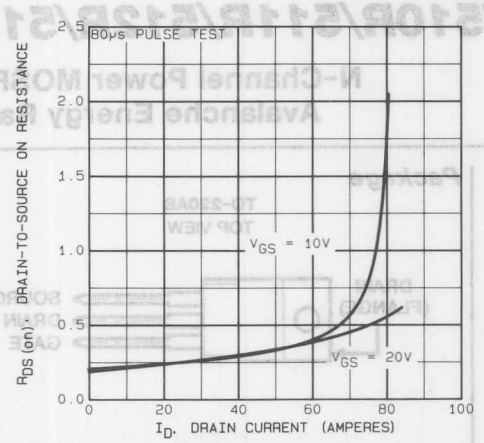


Fig. 12 - Typical on-resistance vs. drain current.

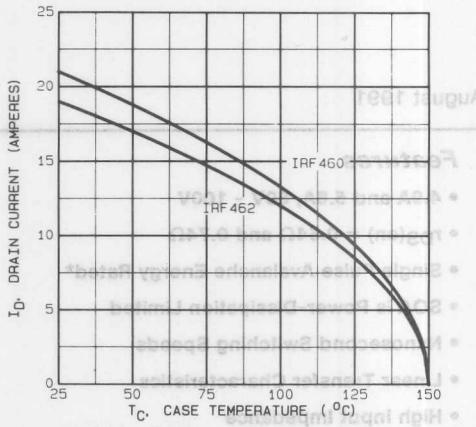


Fig. 13 - Maximum drain current vs. case temperature.

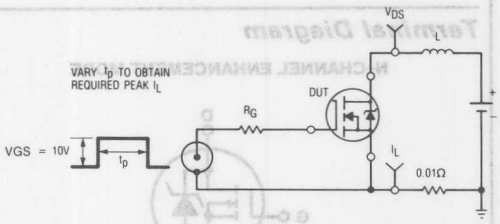


Fig. 14a - Unclamped inductive test circuit.

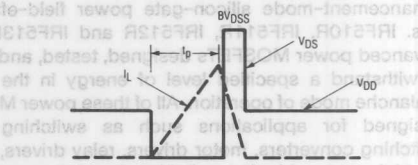


Fig. 14b - Unclamped inductive waveforms.

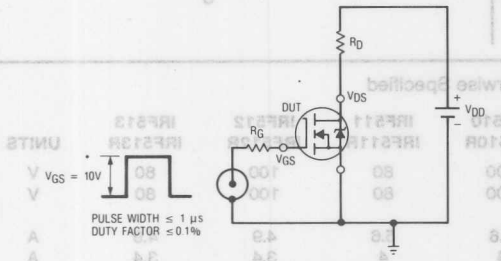


Fig. 15a - Switching time test circuit.

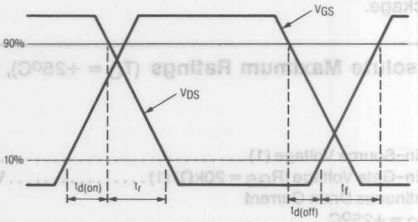


Fig. 15b - Switching time waveforms.

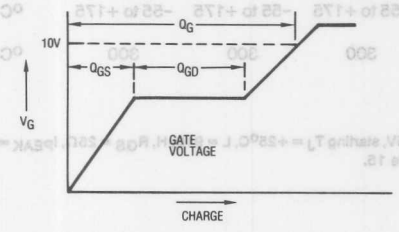


Fig. 16a - Basic gate charge waveform.

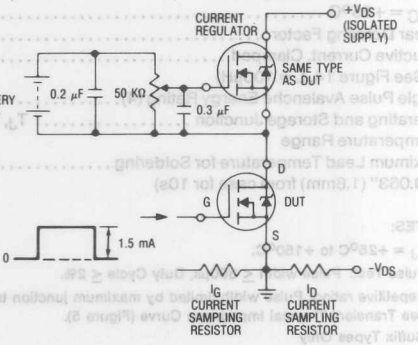


Fig. 16b - Gate charge test circuit.

HARRIS

IRF510/511/512/513
IRF510R/511R/512R/513R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 4.9A and 5.6A, 80V - 100V
- $r_{DS}(on)$ = 0.54Ω and 0.74Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

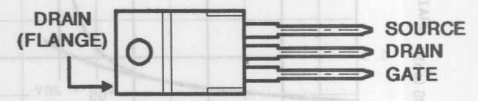
Description

The IRF510, IRF511, IRF512, and IRF513 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF510R, IRF511R, IRF512R and IRF513R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

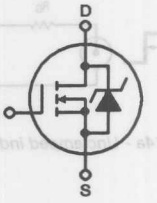
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF510 IRF510R	IRF511 IRF511R	IRF512 IRF512R	IRF513 IRF513R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	5.6	5.6	4.9	4.9	A
T_C = +100°C ..... I_D	4	4	3.4	3.4	A
Pulsed Drain Current (3) ..... I_{DM}	20	20	18	18	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	43	43	43	43	W
Linear Derating Factor	0.29	0.29	0.29	0.29	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	16	16	14	14	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	19	19	19	19	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 910μH, R_{GS} = 25Ω, I_{PEAK} = 5.6A. See Figure 15.

*R Suffix Types Only

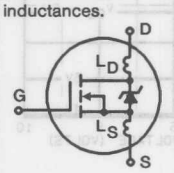
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1573.1

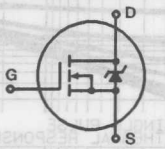
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF510/512, IRF510R/512R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	–	–	V
IRF511/513, IRF511R/513R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +150°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF510/511, IRF510R/511R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	5.6	–	–	A
IRF512/513, IRF512R/513R			4.9	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF510/511, IRF510R/511R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.4A	–	0.4	0.54	Ω
IRF512/513, IRF512R/513R			–	0.5	0.74	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 3.4A	1.3	2.0	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	135	–	pF
Output Capacitance	C_{OSS}		–	80	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, $I_D \simeq$ 5.6A, R_G = 24Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	8	11	ns
Rise Time	t_r		–	25	36	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	15	21	ns
Fall Time	t_f		–	12	21	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 5.6A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	5.0	7.7	nC
Gate-Source Charge	Q_{gs}		–	2.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	3.0	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	3.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	5.6	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	20	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 5.6A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 5.6A, dI_F/dt = 100A/µs	4.6	96	200	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 5.6A, dI_F/dt = 100A/µs	0.17	0.4	0.83	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 910µH, R_{GS} = 25Ω, I_{PEAK} = 5.6A (See Figure 15)

Performance Curves

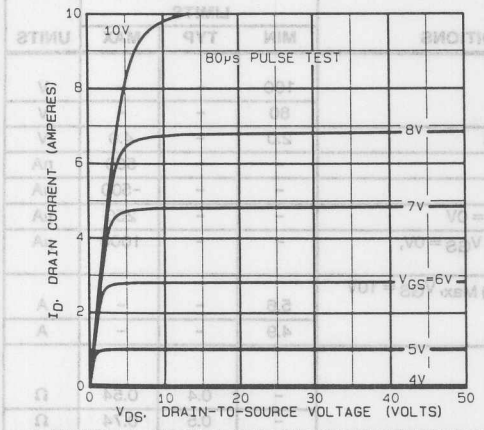


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

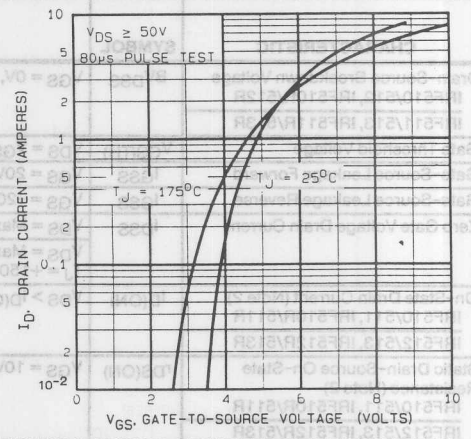


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

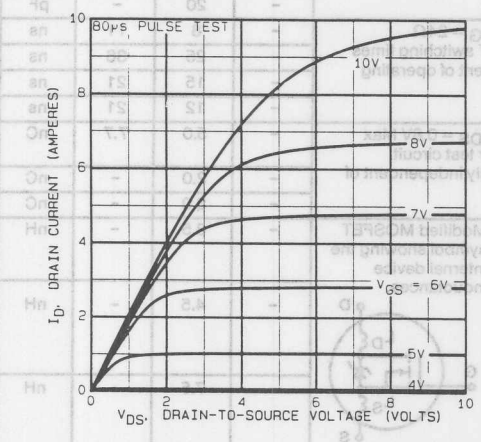


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

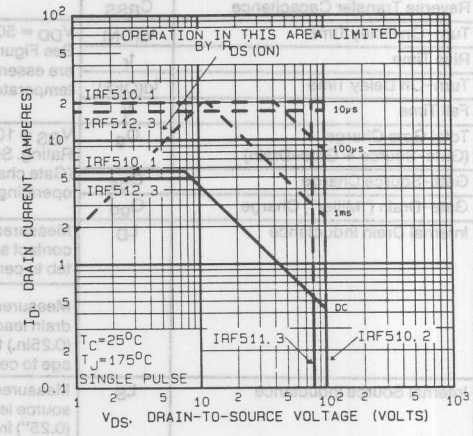


FIGURE 4. MAXIMUM SAFE OPERATING AREA

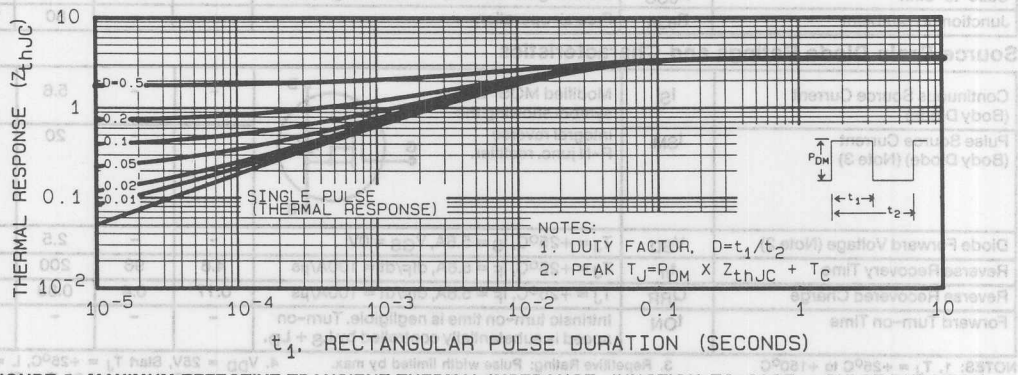


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

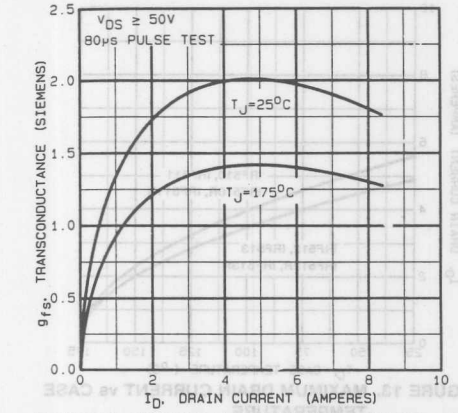


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

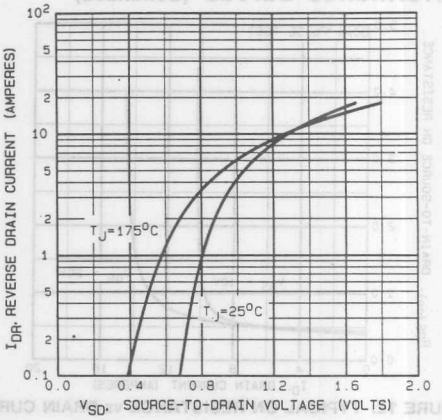


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

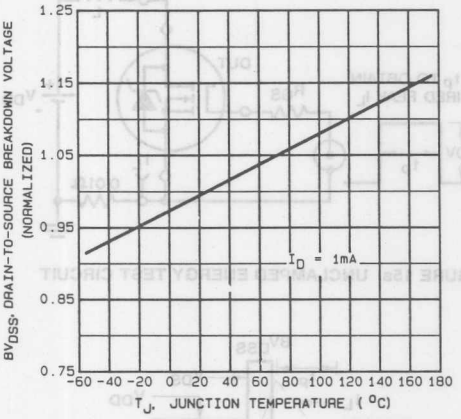


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

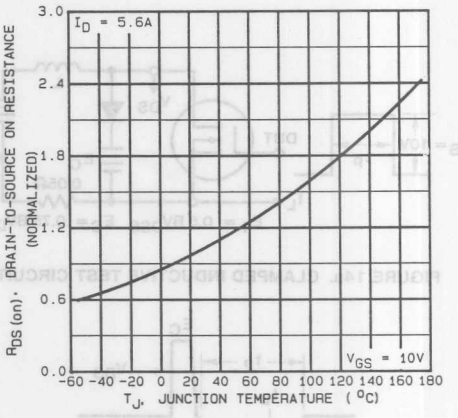


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

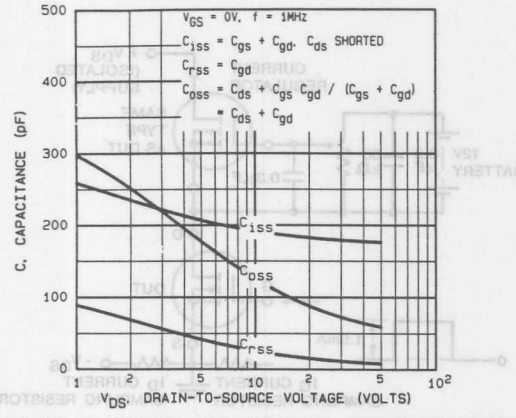


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

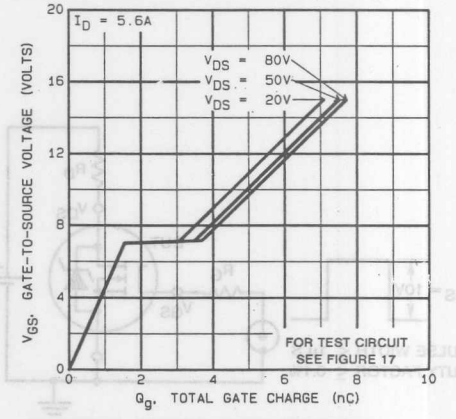


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

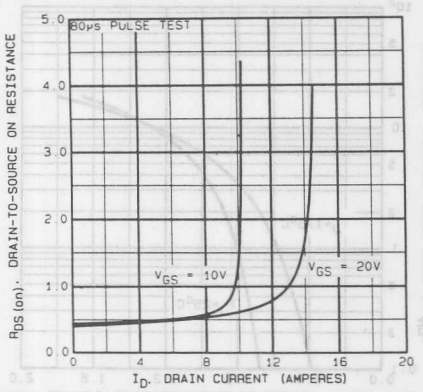


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

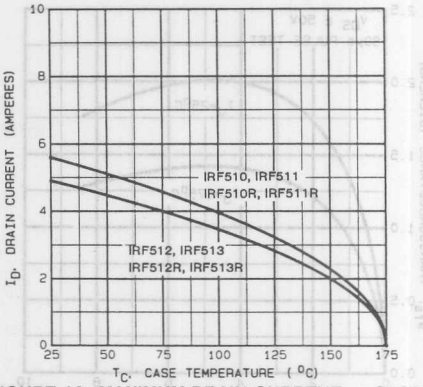


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

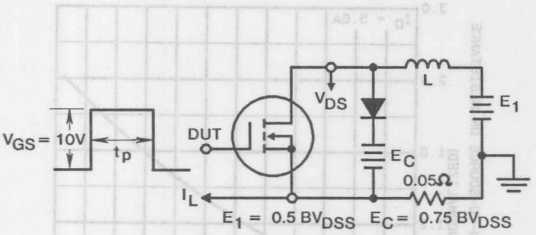


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

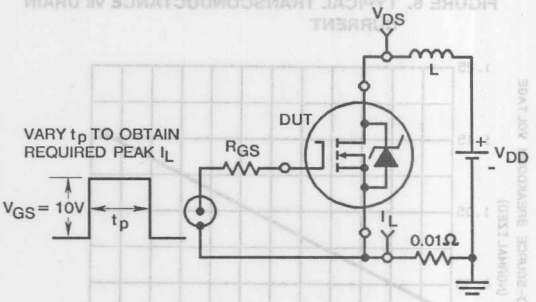


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

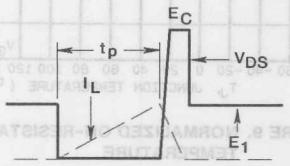


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

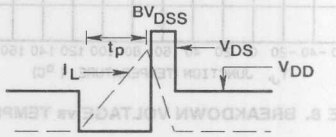


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

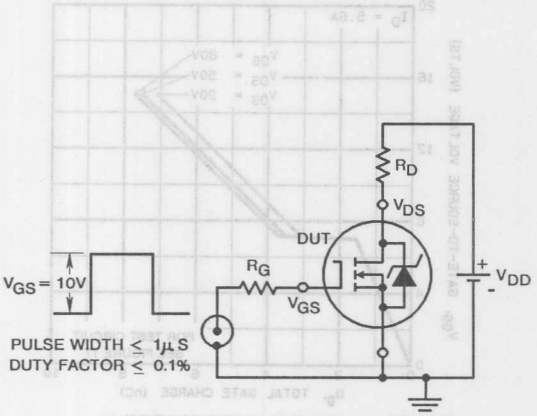


FIGURE 16. SWITCHING TIME TEST CIRCUIT

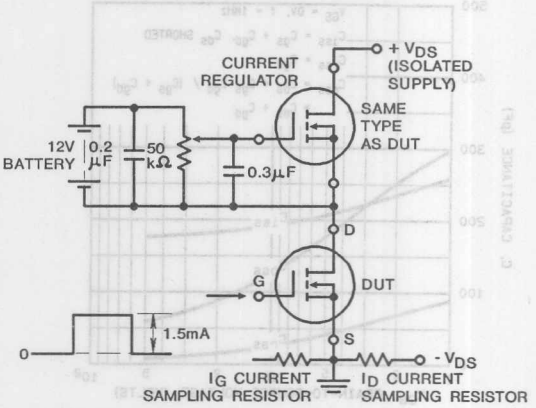


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRF520/521/522/523
IRF520R/521R/522R/523R

N-Channel Power MOSFETs
Avalanche Energy Rated*

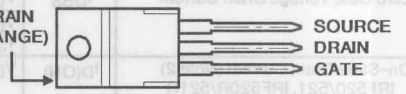
August 1991

Features

- 8A and 9.2A, 80V - 100V
- $r_{DS}(on)$ = 0.27Ω and 0.36Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-220AB
TOP VIEW



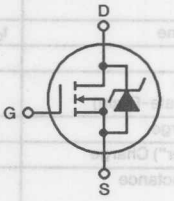
Description

The IRF520, IRF521, IRF522, and IRF523 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF520R, IRF521R, IRF522R and IRF523R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF520 IRF520R	IRF521 IRF521R	IRF522 IRF522R	IRF523 IRF523R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	9.2	9.2	8	8	A
T_C = +100°C ..... I_D	6.5	6.5	5.6	5.6	A
Pulsed Drain Current (3) ..... I_{DM}	37	37	32	32	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	60	60	60	60	W
Linear Derating Factor	0.4	0.4	0.4	0.4	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	32	32	28	28	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	36	36	36	36	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 640μH, R_{GS} = 25Ω, I_{PEAK} = 9.2A. See Figures 15 & 16.

*R Suffix Types Only

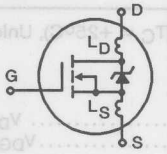
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1574.1

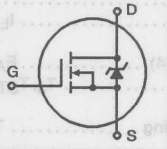
Drain-Source Breakdown Voltage IRF520/522, IRF520R/522R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	–	–	V
IRF521/523, IRF521R/523R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +150°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF520/521, IRF520R/521R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, V_{GS} = 10V	9.2	–	–	A
IRF522/523, IRF522R/523R			8.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF520/521, IRF520R/521R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.6A	–	0.25	0.27	Ω
IRF522/523, IRF522R/523R			–	0.27	0.36	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 5.6A	2.7	4.1	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	350	–	pF
Output Capacitance	C_{OSS}		–	130	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	25	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D ≃ 9.2A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	9	13	ns
Rise Time	t_r		–	30	45	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	18	29	ns
Fall Time	t_f		–	20	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 9.2A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	10	15	nC
Gate-Source Charge	Q_{gs}		–	2.5	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	2.5	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	2.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Modified MOSFET symbol showing the internal device inductances.



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	9.2	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	37	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 9.2A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 9.2A, dI_F/dt = 100A/μs	5.5	100	240	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 9.2A, dI_F/dt = 100A/μs	0.25	0.5	1.1	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 640μH, R_{GS} = 25Ω, I_{PEAK} = 9.2A (See Figures 15 & 16)

Performance Curves

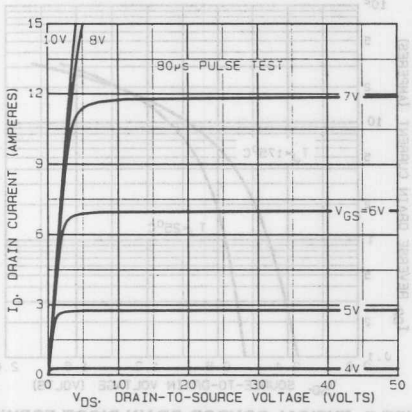


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

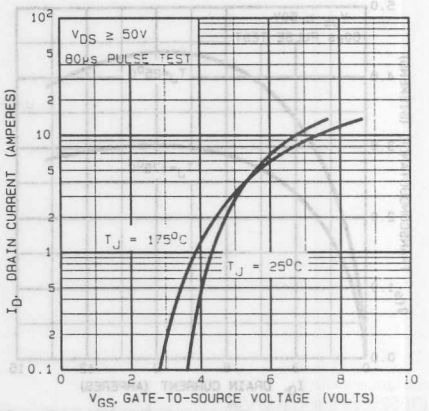


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

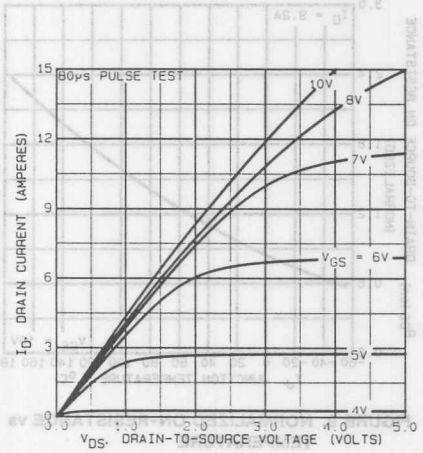


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

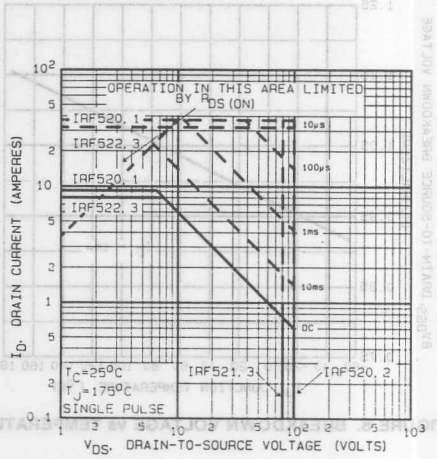


FIGURE 4. MAXIMUM SAFE OPERATING AREA

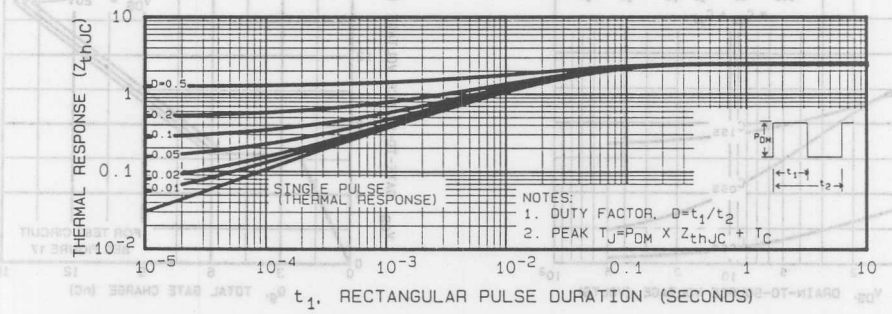


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

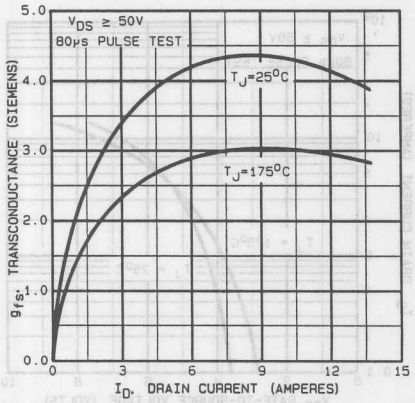


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

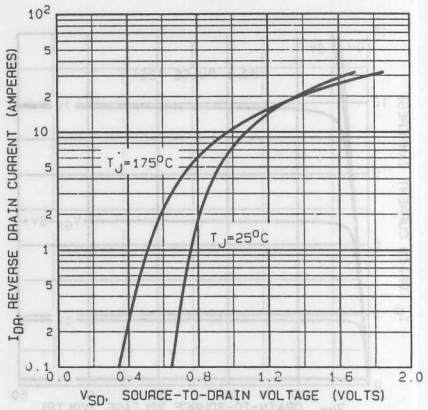


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

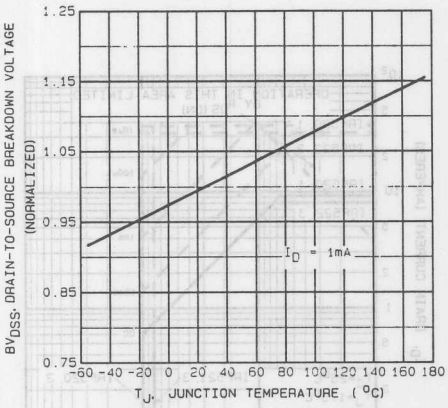


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

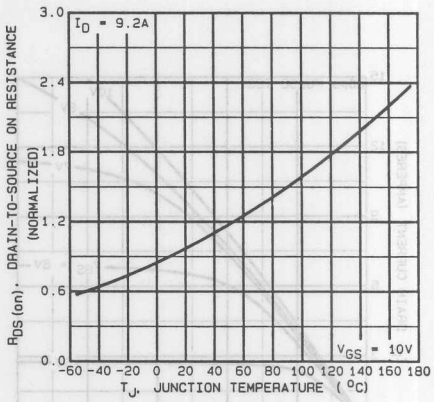


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

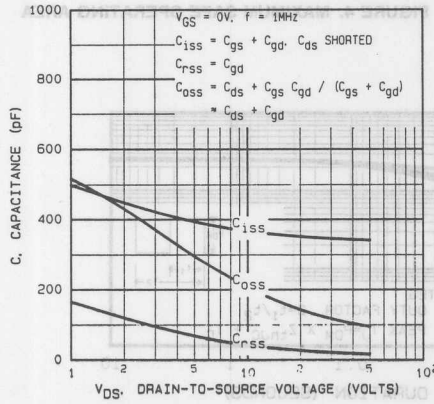


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

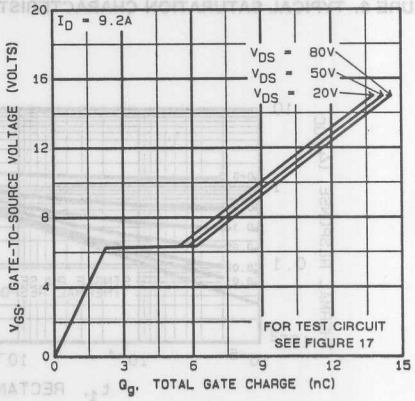


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

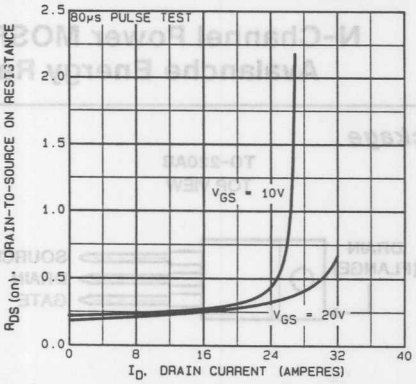


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

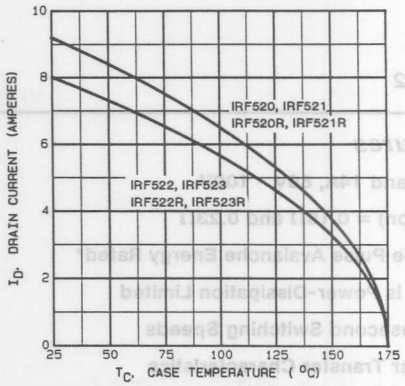


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

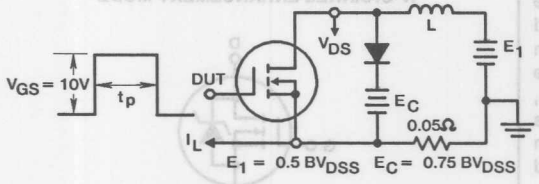


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

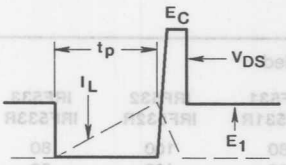


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

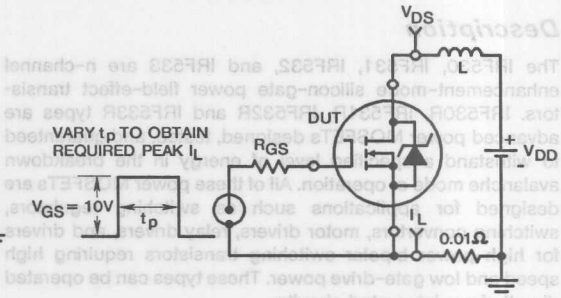


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

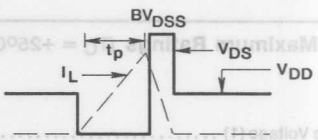


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

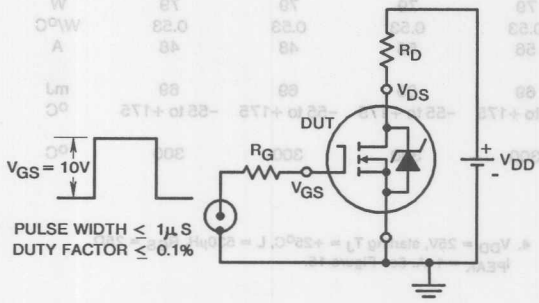


FIGURE 16. SWITCHING TIME TEST CIRCUIT

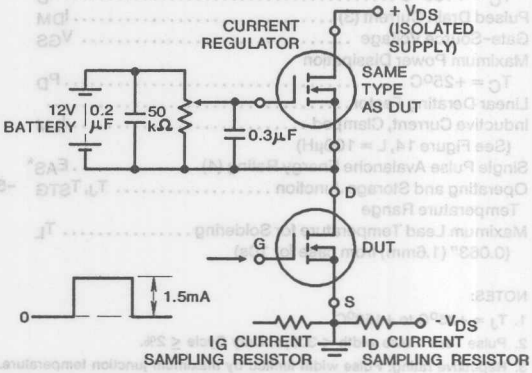


FIGURE 17. GATE CHARGE TEST CIRCUIT

4 N-CHANNEL POWER MOSFETs

HARRIS

IRF530/531/532/533
IRF530R/531R/532R/533R

N-Channel Power MOSFETs
Avalanche Energy Rated*

May 1992

Features

- 12A and 14A, 80V - 100V
- $r_{DS}(on)$ = 0.16Ω and 0.23Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

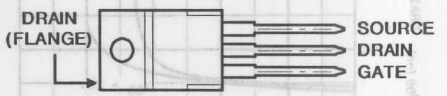
Description

The IRF530, IRF531, IRF532, and IRF533 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF530R, IRF531R, IRF532R and IRF533R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF530 IRF530R	IRF531 IRF531R	IRF532 IRF532R	IRF533 IRF533R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	14	14	12	12	A
T_C = +100°C ..... I_D	10	10	8.3	8.3	A
Pulsed Drain Current (3) ..... I_{DM}	56	56	48	48	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	79	79	79	79	W
Linear Derating Factor	0.53	0.53	0.53	0.53	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	56	56	48	48	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	69	69	69	69	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 530μH, R_{GS} = 25Ω, I_{PEAK} = 14A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

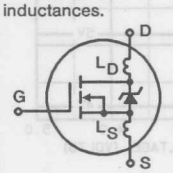
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File Number 1575.2

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

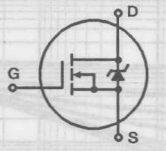
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF530/532, IRF530R/532R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	–	–	V
IRF531/533, IRF531R/533R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF530/531, IRF530R/531R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	14	–	–	A
IRF532/533, IRF532R/533R			12	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF530/531, IRF530R/531R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8.3A	–	0.14	0.16	Ω
IRF532/533, IRF532R/533R			–	0.20	0.23	Ω
Forward Transconductance (Note 2)	g_{ts}	V_{DS} ≥ 50V, I_D = 8.3A	5.1	7.6	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	250	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	50	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D ≃ 14A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	12	15	ns
Rise Time	t_r		–	35	51	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	25	35	ns
Fall Time	t_f		–	25	36	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	18	26	nC
Gate-Source Charge	Q_{gs}		–	4	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	7	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.9	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Modified MOSFET symbol showing the internal device inductances.



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	14	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	56	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 14A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/µs	5.5	120	250	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/µs	0.26	0.6	1.3	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 350µH, R_{GS} = 25Ω, I_{PEAK} = 14A (See Figure 15)

Performance Curves

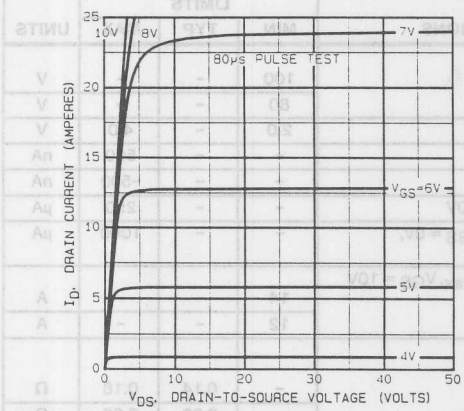


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

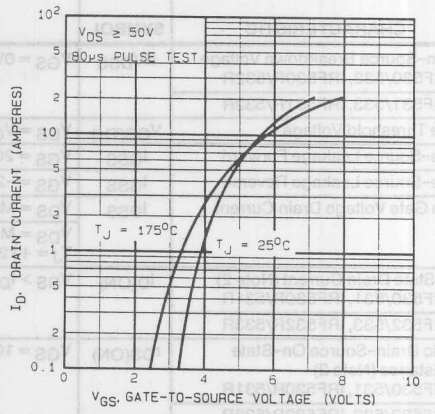


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

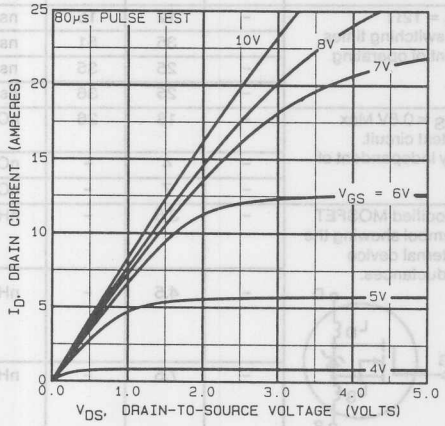


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

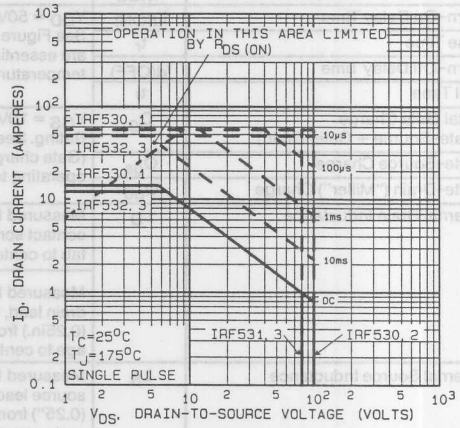


FIGURE 4. MAXIMUM SAFE OPERATING AREA

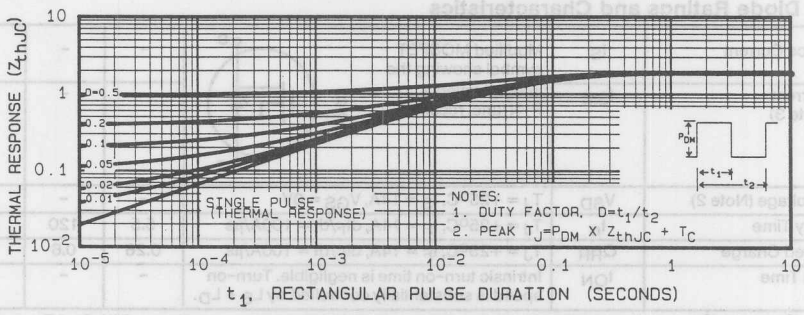


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

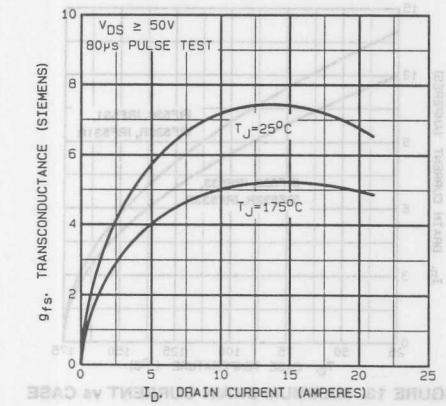


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

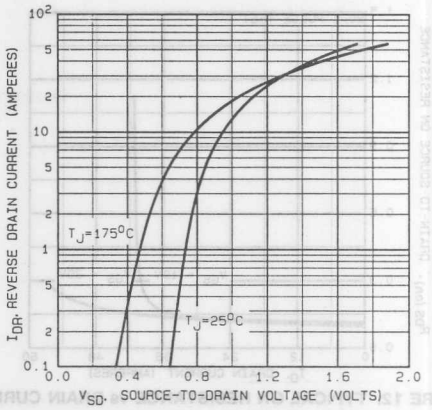


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

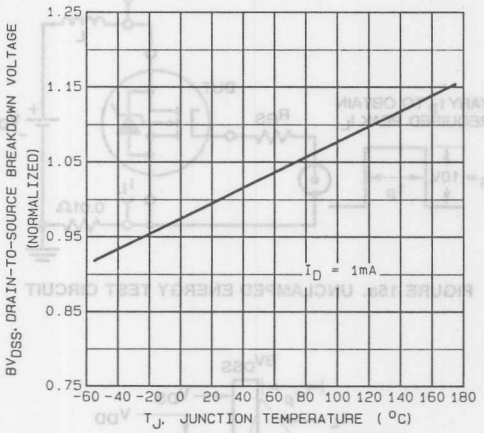


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

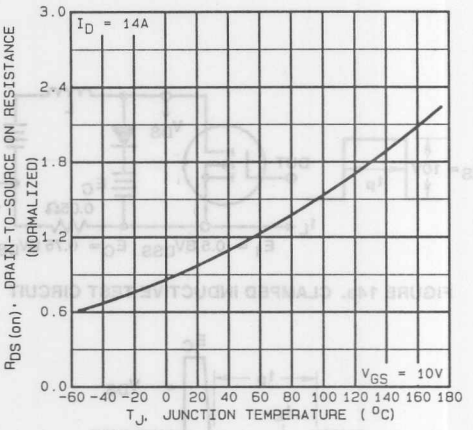


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

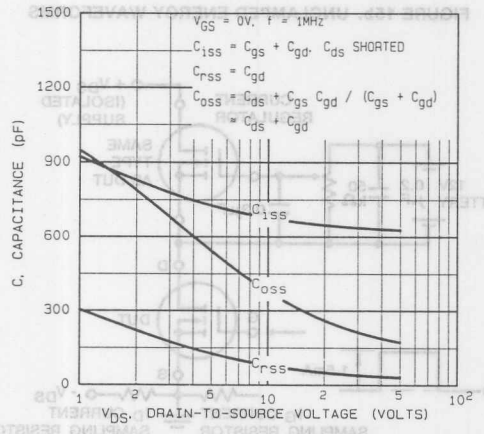


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

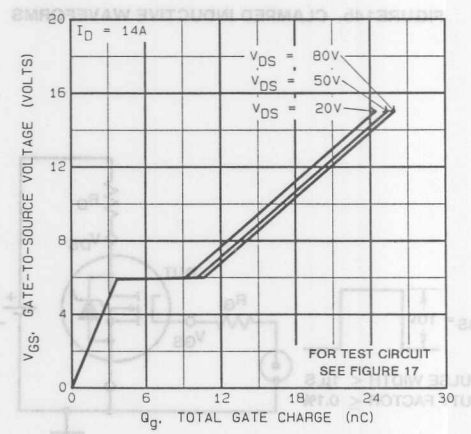


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

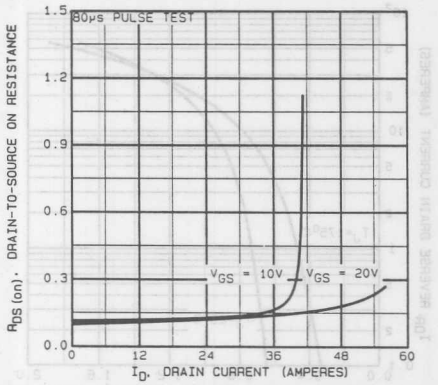


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

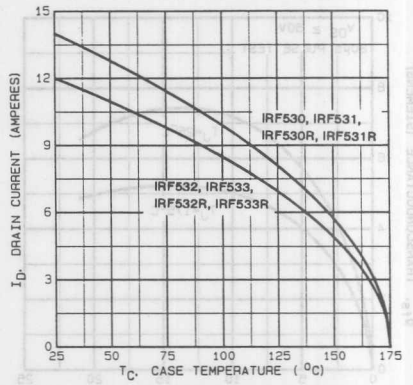


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

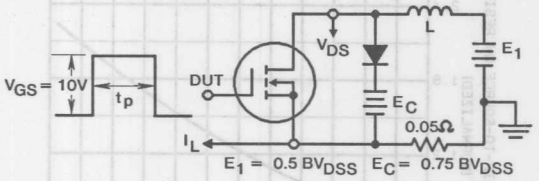


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

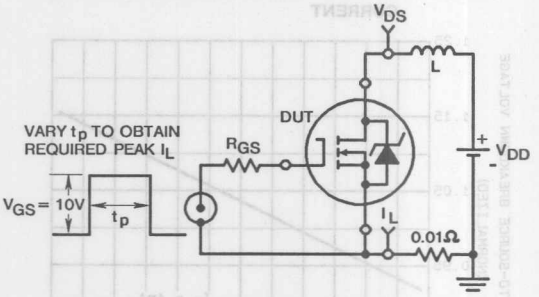


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

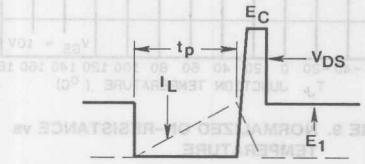


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

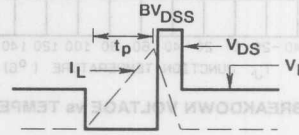


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

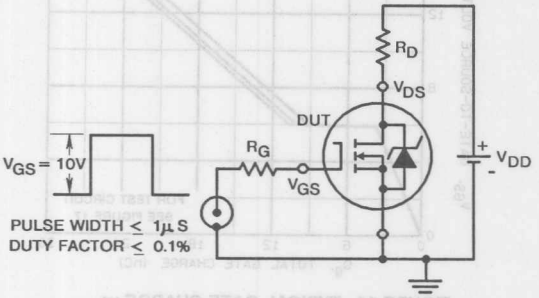


FIGURE 16. SWITCHING TIME TEST CIRCUIT

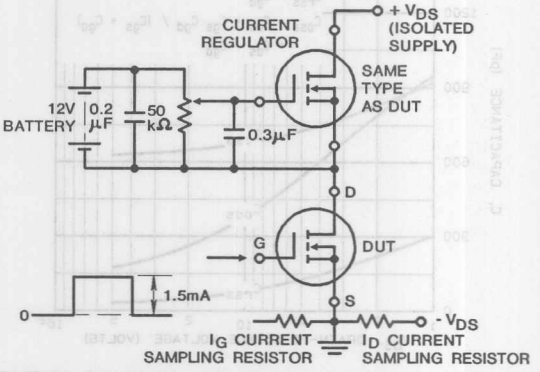


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS IRF540/541/542/543 IRF540R/541R/542R/543R

N-Channel Power MOSFETs Avalanche Energy Rated*

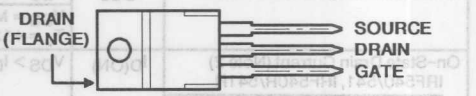
August 1991

Features

- 25A and 28A, 80V - 100V
- $r_{DS}(on)$ = 0.077Ω and 0.10Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-220AB
TOP VIEW



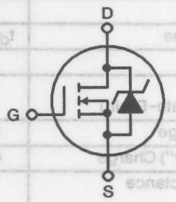
Description

The IRF540, IRF541, IRF542, and IRF543 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF540R, IRF541R, IRF542R and IRF543R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF540 IRF540R	IRF541 IRF541R	IRF542 IRF542R	IRF543 IRF543R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	28	28	25	25	A
T_C = +100°C ..... I_D	20	20	17	17	A
Pulsed Drain Current (3) ..... I_{DM}	110	110	100	100	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	150	150	150	150	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	108	108	96	96	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	230	230	230	230	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 440μH, R_{GS} = 25Ω, I_{PEAK} = 28A. See Figure 15.

*R Suffix Types Only

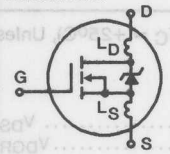
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2309.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

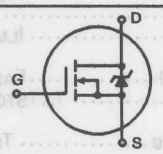
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF540/542, IRF540R/542R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	–	–	V
IRF541/543, IRF541R/543R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF540/541, IRF540R/541R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	28	–	–	A
IRF542/543, IRF542R/543R			25	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF540/541, IRF540R/541R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 17A	–	0.06	0.077	Ω
IRF542/543, IRF542R/543R			–	0.08	0.10	Ω
Forward Transconductance (Note 2)	g_{ts}	V_{DS} ≥ 50V, I_D = 17A	8.7	13	–	S( )
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1450	–	pF
Output Capacitance	C_{OSS}		–	550	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	100	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D ≃ 28A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	15	23	ns
Rise Time	t_r		–	70	110	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	40	60	ns
Fall Time	t_f		–	50	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 28A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	38	59	nC
Gate-Source Charge	Q_{gs}		–	8	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	21	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Modified MOSFET symbol showing the internal device inductances.



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	28	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	110	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 27A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 28A, dI_F/dt = 100A/µs	70	150	300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 28A, dI_F/dt = 100A/µs	0.44	1.0	1.9	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 440µH, R_{GS} = 25Ω, I_{PEAK} = 28A (See Figure 15)

Performance Curves

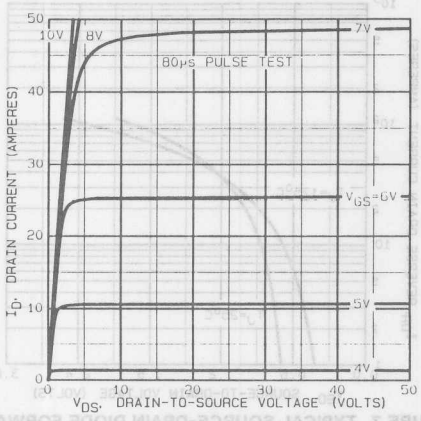


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

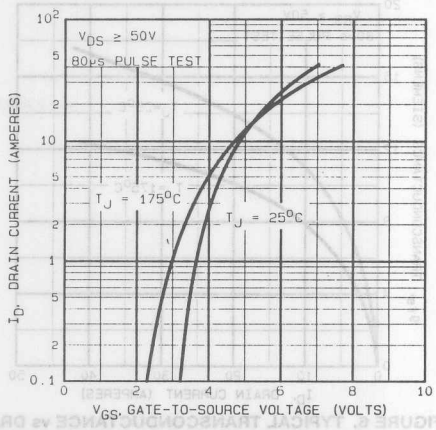


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

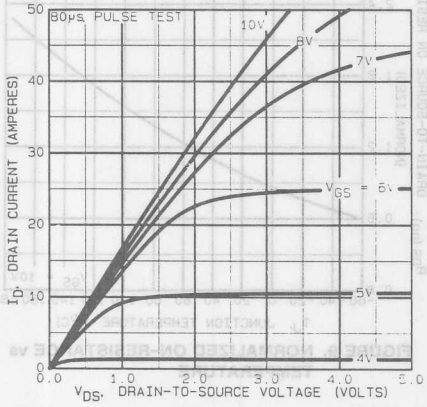


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

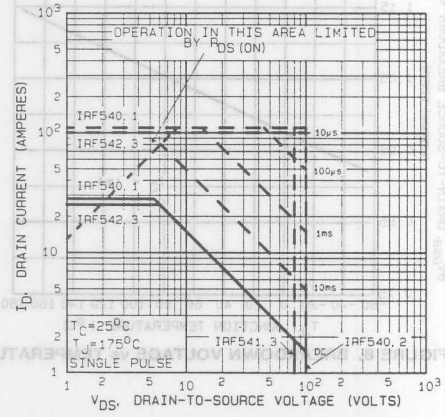


FIGURE 4. MAXIMUM SAFE OPERATING AREA

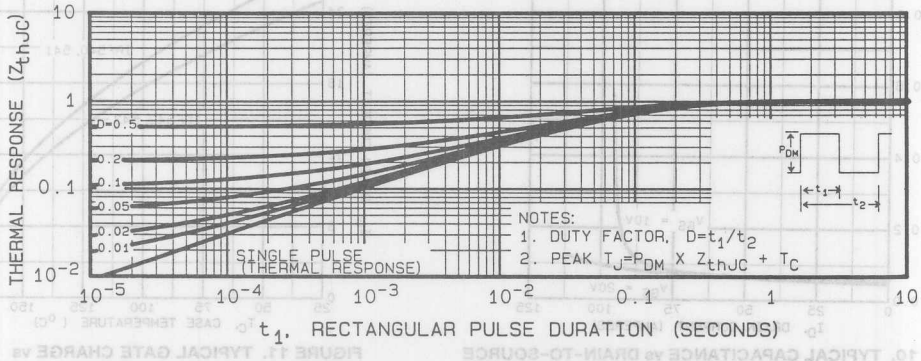


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

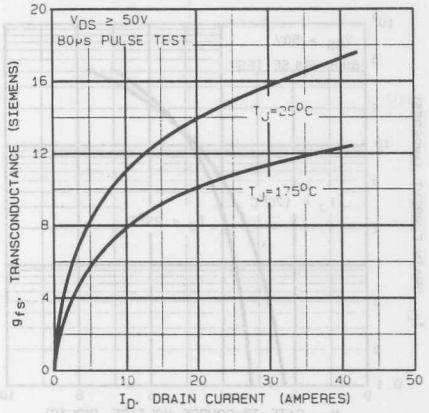


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

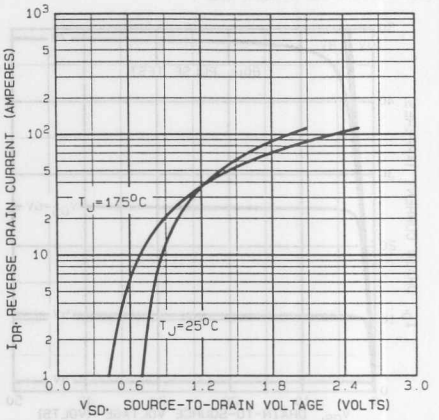


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

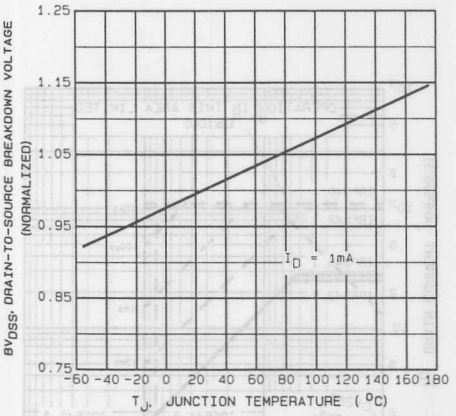


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

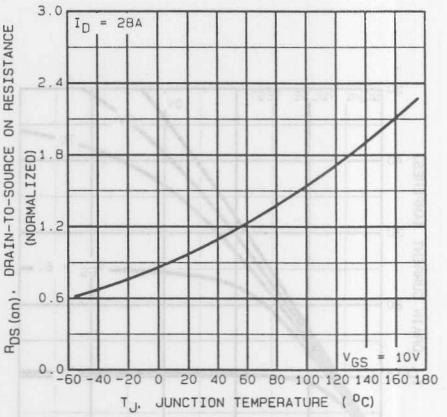


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

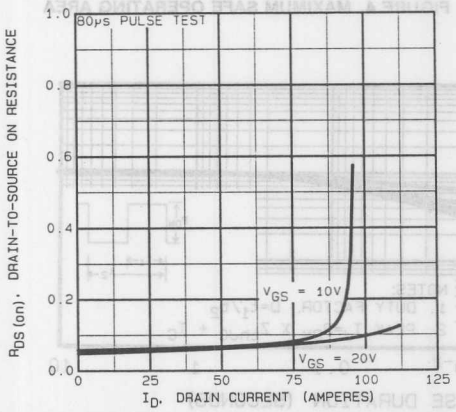


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

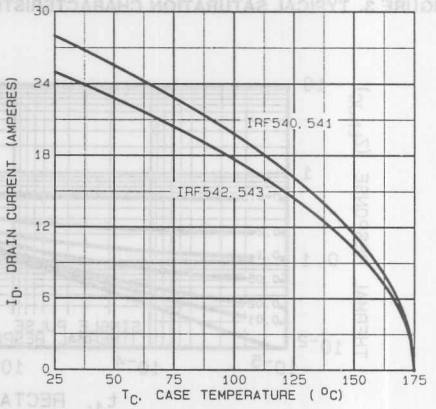


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

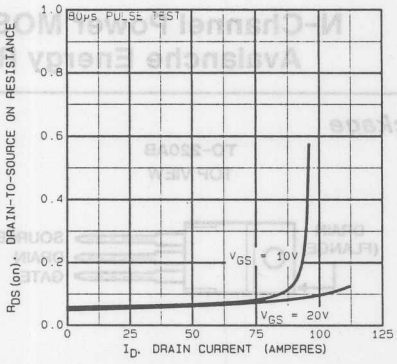


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

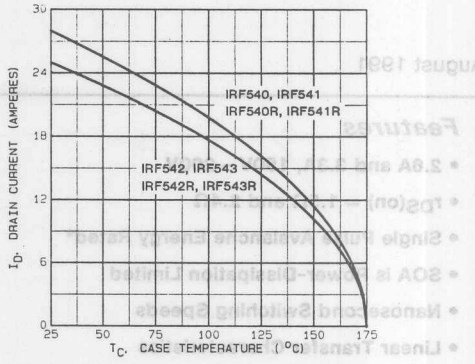


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

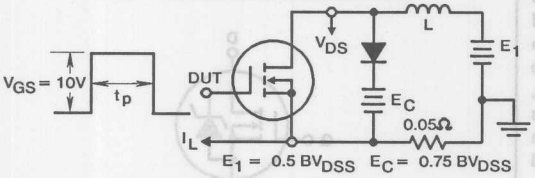


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

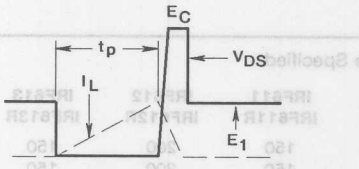


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

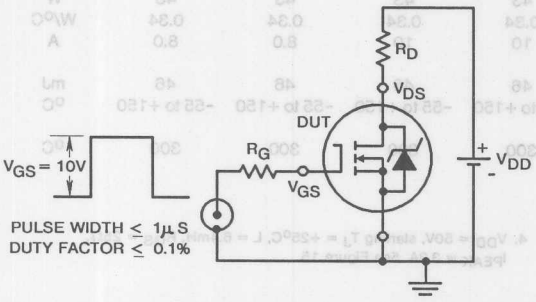


FIGURE 16. SWITCHING TIME TEST CIRCUIT

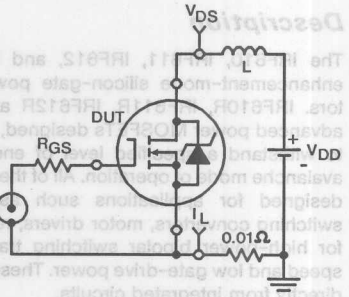


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

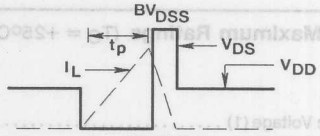


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

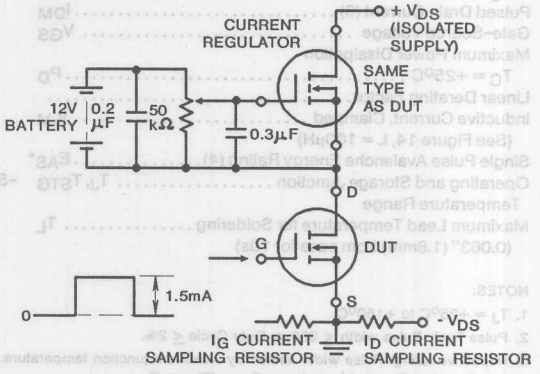


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRF610/611/612/613
IRF610R/611R/612R/613R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 2.6A and 3.3A, 150V - 200V
- $r_{DS}(on)$ = 1.5Ω and 2.4Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

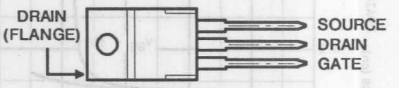
Description

The IRF610, IRF611, IRF612, and IRF613 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF610R, IRF611R, IRF612R and IRF613R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF610 IRF610R	IRF611 IRF611R	IRF612 IRF612R	IRF613 IRF613R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	3.3	3.3	2.6	2.6	A
T_C = +100°C ..... I_D	2.1	2.1	1.6	1.6	A
Pulsed Drain Current (3) ..... I_{DM}	8	8	6.5	6.5	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	43	43	43	43	W
Linear Derating Factor	0.34	0.34	0.34	0.34	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	10	10	8.0	8.0	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	46	46	46	46	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 6.4mH, R_{GS} = 25Ω, I_{PEAK} = 3.3A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

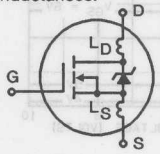
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File Number **1576.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

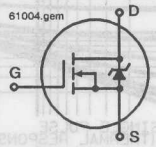
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF610/612, IRF610R/612R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRF611/613, IRF611R/613R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF610/611, IRF610R/611R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	3.3	–	–	A
IRF612/613, IRF612R/613R			2.6	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF610/611, IRF610R/611R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.6A	–	1.0	1.5	Ω
IRF612/613, IRF612R/613R			–	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 1.6A	0.8	1.3	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	135	–	pF
Output Capacitance	C_{OSS}		–	60	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	16	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, $I_D \simeq$ 3.3A, R_G = 24Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	8	12	ns
Rise Time	t_r		–	17	26	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	13	21	ns
Fall Time	t_f		–	9	13	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.3A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	5.3	8.2	nC
Gate-Source Charge	Q_{gs}		–	1.2	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	3.0	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	2.9	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Modified MOSFET symbol showing the internal device inductances.



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	3.3	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	8	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.3A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 3.3A, dI_F/dt = 100A/µs	75	160	310	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 3.3A, dI_F/dt = 100A/µs	0.33	0.9	1.4	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 6.4mH, R_{GS} = 25Ω, I_{PEAK} = 3.3A (See Figure 15)

Performance Curves

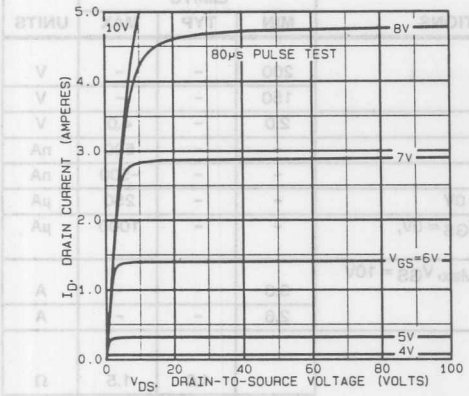


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

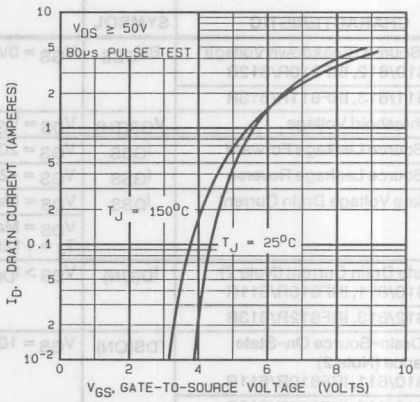


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

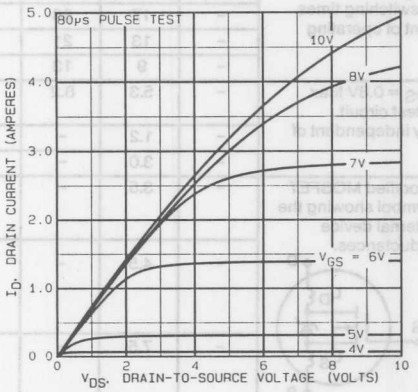


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

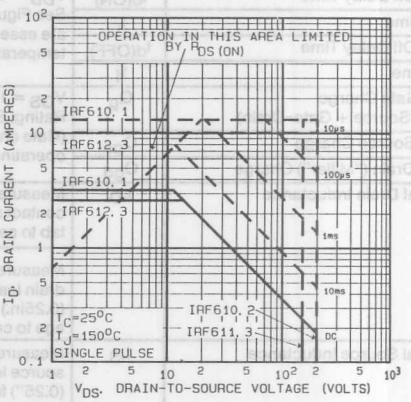


FIGURE 4. MAXIMUM SAFE OPERATING AREA

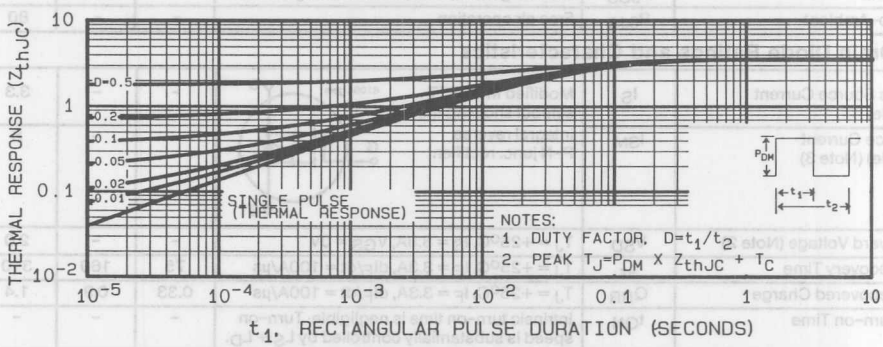


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

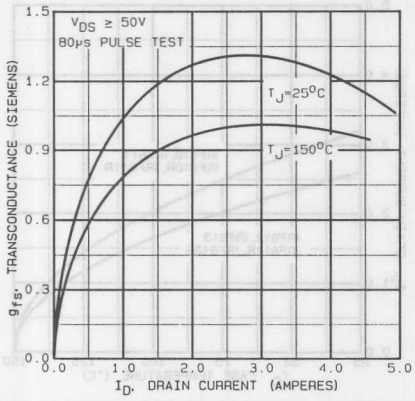


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

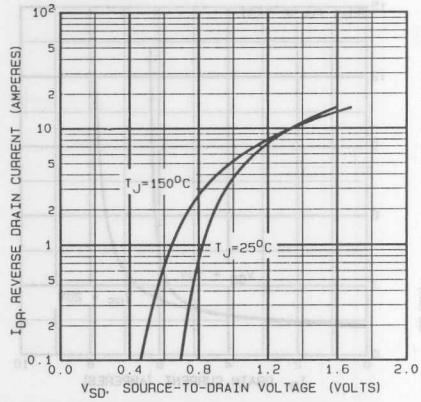


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

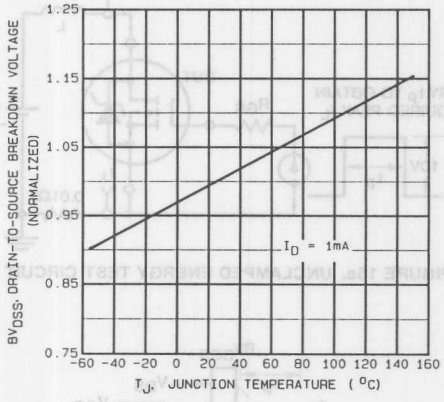


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

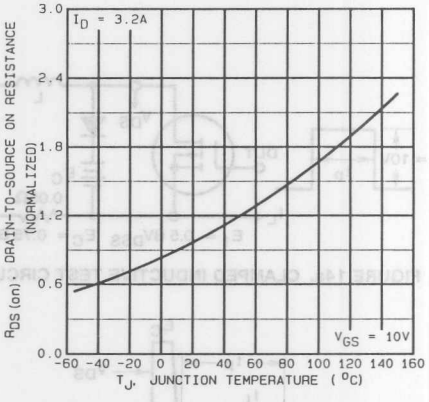


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

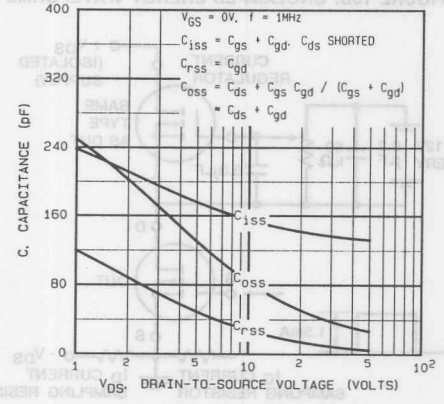


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

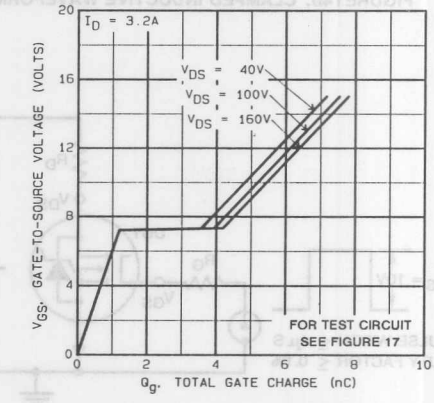


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

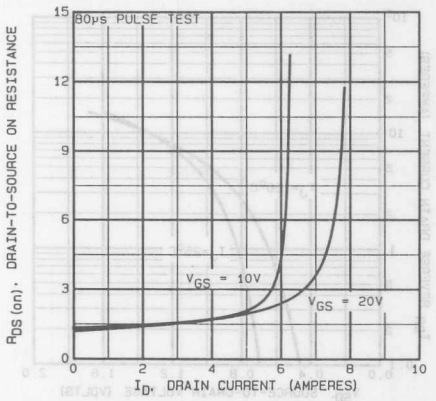


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

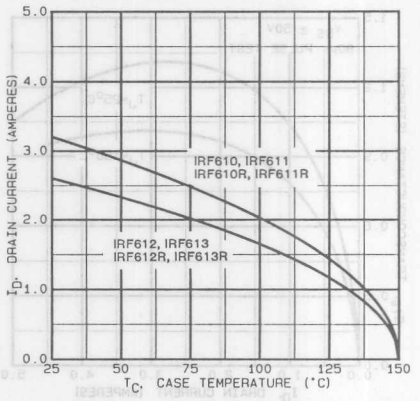


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

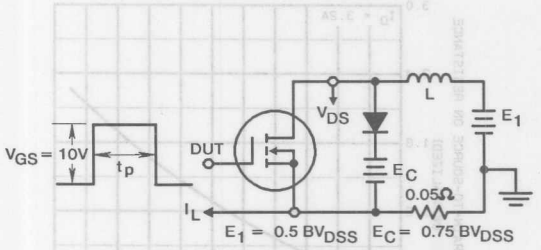


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

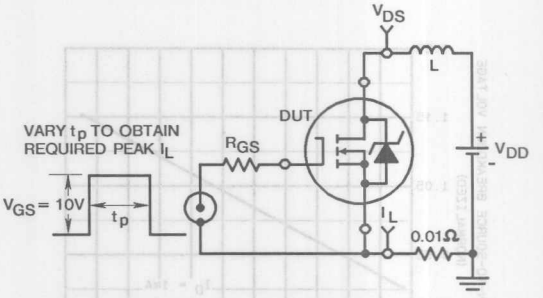


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

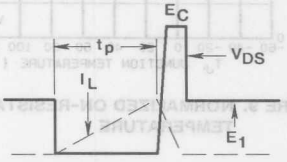


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

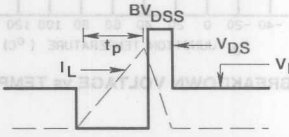


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

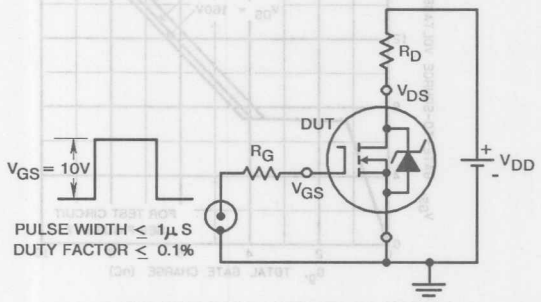


FIGURE 16. SWITCHING TIME TEST CIRCUIT

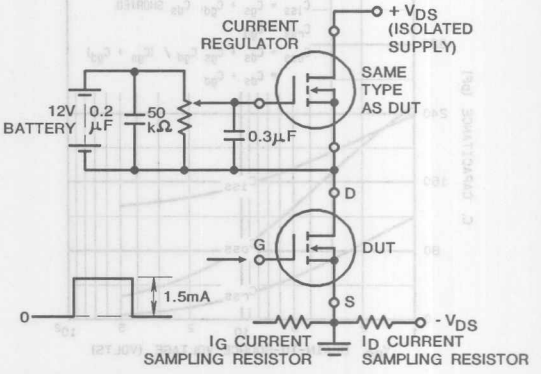


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRF620/621/622/623
IRF620R/621R/622R/623R

N-Channel Power MOSFETs
Avalanche Energy Rated*

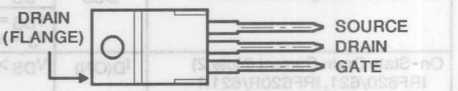
August 1991

Features

- 4.0A and 5.0A, 150V - 200V
- $r_{DS}(on)$ = 0.8Ω and 1.2Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-220AB
TOP VIEW



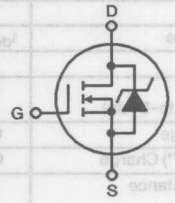
Description

The IRF620, IRF621, IRF622, and IRF623 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF620R, IRF621R, IRF622R and IRF623R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF620 IRF620R	IRF621 IRF621R	IRF622 IRF622R	IRF623 IRF623R	UNITS
Drain-Source Voltage (1)	V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	200	150	200	150	V
Continuous Drain Current						
T_C = +25°C	I_D	5.0	5.0	4.0	4.0	A
T_C = +100°C	I_D	3.0	3.0	2.5	2.5	A
Pulsed Drain Current (3)	I_{DM}	20	20	16	16	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	40	40	40	40	W
Linear Derating Factor		0.32	0.32	0.32	0.32	W/°C
Inductive Current, Clamped (See Figure 14, L = 100μH)	I_{LM}	20	20	16	16	A
Single Pulse Avalanche Energy Rating (4)	E_{AS}*	85	85	85	85	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 10V, starting T_J = +25°C, L = 6.18mH, R_{GS} = 50Ω, I_{PEAK} = 5A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

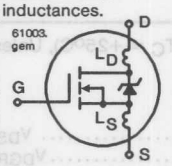
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File Number 1577.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

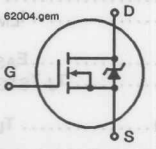
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF620/622, IRF620R/622R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRF621/623, IRF621R/623R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF620/621, IRF620R/621R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	5.0	–	–	A
IRF622/623, IRF622R/623R			4.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF620/621, IRF620R/621R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 2.5A	–	0.5	0.8	Ω
IRF622/623, IRF622R/623R			–	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$Max, I_D = 2.5A	1.3	2.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	450	–	pF
Output Capacitance	C_{OSS}		–	150	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	40	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 2.5BVDSS, I_D = 5.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	20	40	ns
Rise Time	t_r		–	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	100	ns
Fall Time	t_f		–	30	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 5.0A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	11	15	nC
Gate-Source Charge	Q_{gs}		–	5.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	6.0	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	3.12	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Modified MOSFET symbol showing the internal device inductances.



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	5.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	20	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 5.0A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 5.0A, dI_F/dt = 100A/µs	–	350	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 5.0A, dI_F/dt = 100A/µs	–	2.3	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 10V, Start T_J = +25°C, L = 6.18mH, R_{GS} = 50Ω, I_{PEAK} = 5A (See Figure 15)

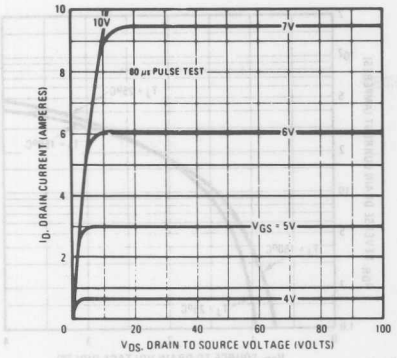


Fig. 1 – Typical Output Characteristics

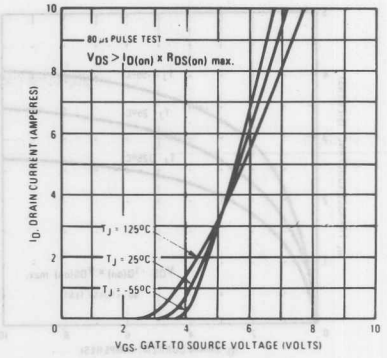


Fig. 2 – Typical Transfer Characteristics

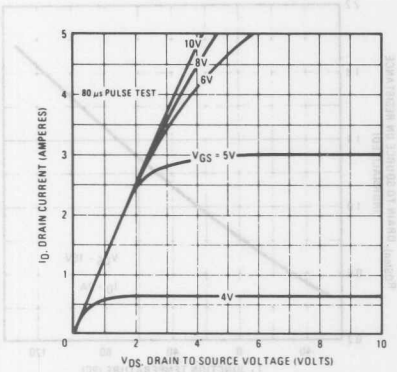


Fig. 3 – Typical Saturation Characteristics

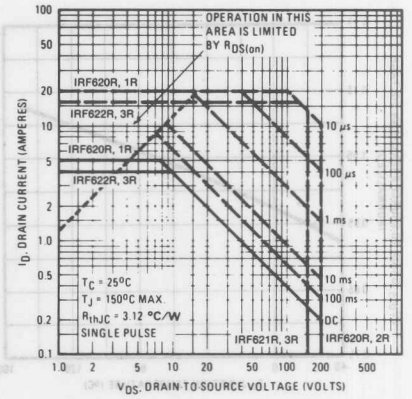


Fig. 4 – Maximum Safe Operating Area

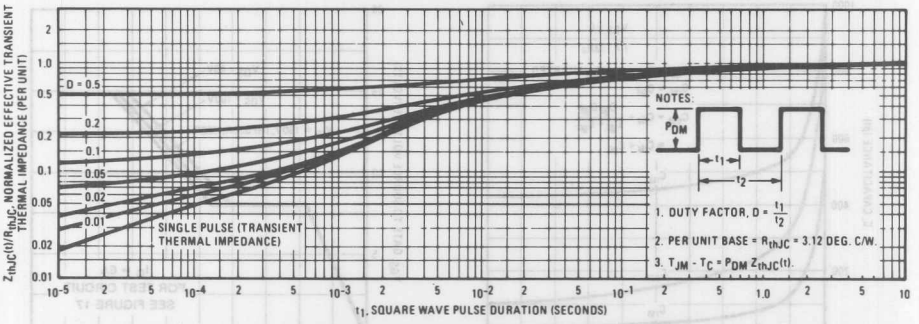


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

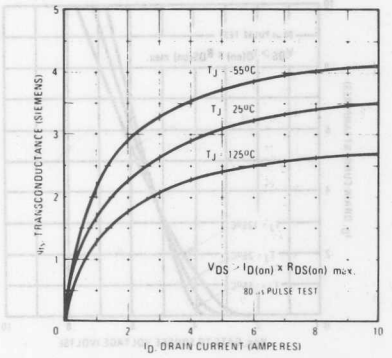


Fig. 6 – Typical Transconductance Vs. Drain Current

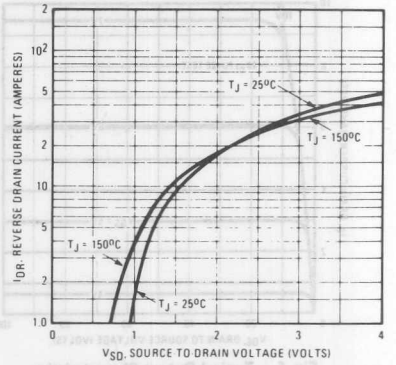


Fig. 7 – Typical Source-Drain Diode Forward Voltage

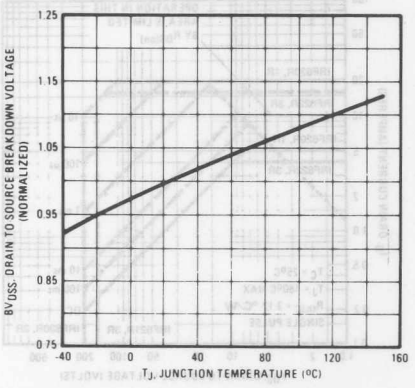


Fig. 8 – Breakdown Voltage Vs. Temperature

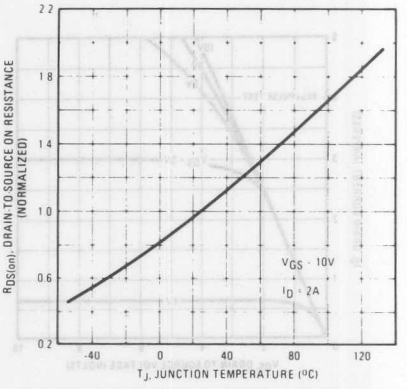


Fig. 9 – Normalized On-Resistance Vs. Temperature

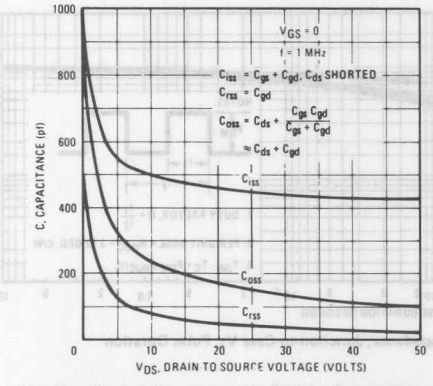


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

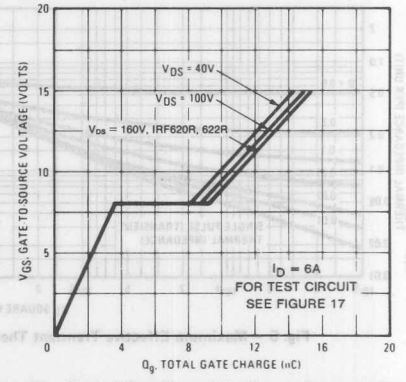


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

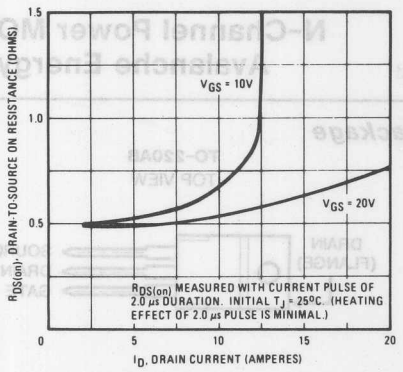


Fig. 12 — Typical On-Resistance Vs. Drain Current

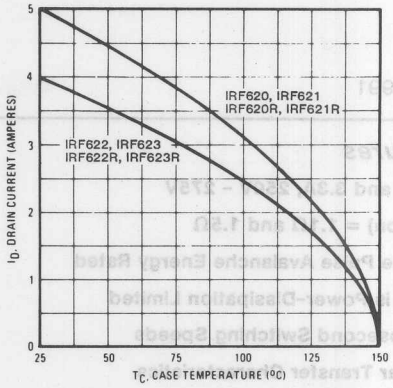


Fig. 13 — Maximum Drain Current Vs. Case Temperature

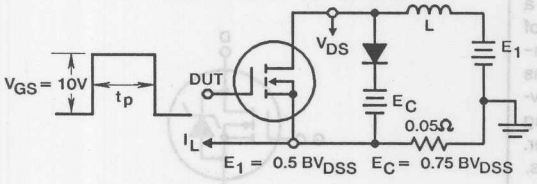


Fig. 14a — Clamped Inductive Test Circuit

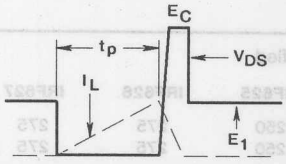


Fig. 14b — Clamped Inductive Waveforms

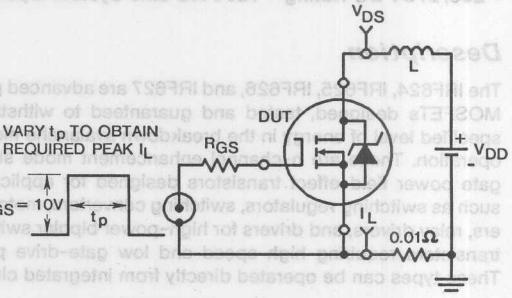


Fig. 15a — Unclamped Energy Test Circuit

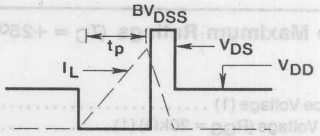


Fig. 15b — Unclamped Energy Waveforms

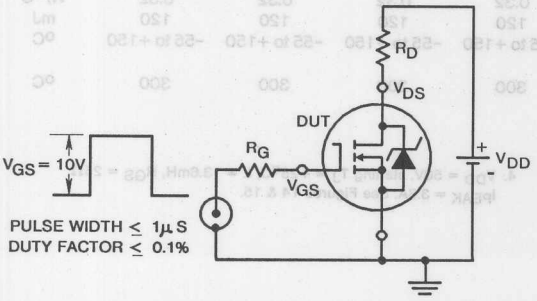


Fig. 16 — Switching Time Test Circuit

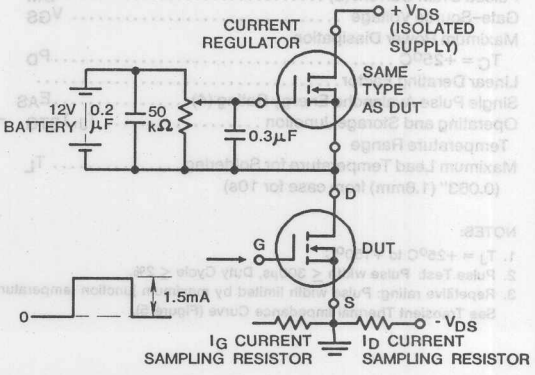


Fig. 17 — Gate Charge Test Circuit

HARRIS

IRF624, IRF625 IRF626, IRF627

N-Channel Power MOSFETs Avalanche Energy Rated

August 1991

Features

- 3.8A and 3.3A, 250V - 275V
- $r_{DS}(on)$ = 1.1Ω and 1.5Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 250/275V DC Rating - 120V AC Line System Operation

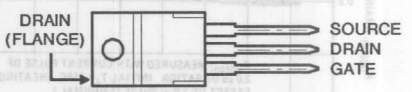
Description

The IRF624, IRF625, IRF626, and IRF627 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF624	IRF625	IRF626	IRF627	UNITS
Drain-Source Voltage (1) ..... V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	250	250	275	275	V
Continuous Drain Current					
T_C = +25°C ..... I_D	3.8	3.3	3.8	3.3	A
T_C = +100°C ..... I_D	2.4	2.1	2.4	2.1	A
Pulsed Drain Current (3) ..... I_{DM}	15	13	15	13	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	40	40	40	40	W
Linear Derating Factor	0.32	0.32	0.32	0.32	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}	120	120	120	120	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

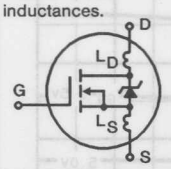
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 13.6mH, R_{GS} = 25Ω, I_{PEAK} = 3.8A. See Figures 14 & 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

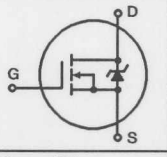
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Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF624, IRF626	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	275	–	–	V
IRF625, IRF627			250	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF624, IRF626	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	3.8	–	–	A
IRF625, IRF627			3.3	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF624, IRF626	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.4A	–	0.8	1.1	Ω
IRF625, IRF627			–	1.05	1.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 2 x V_{GS}, I_{DS} = 1.9A	1.4	2.1	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	340	–	pF
Output Capacitance	C_{OSS}		–	110	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	32	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 3.8A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	11	17	ns
Rise Time	t_r		–	24	36	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	21	32	ns
Fall Time	t_f		–	13	20	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.8A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	15	22	nC
Gate-Source Charge	Q_{gs}		–	4.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	7.2	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	3.12	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	3.8	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	15	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.8A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 3.8A, dI_F/dt = 100A/µs	81	180	370	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 3.8A, dI_F/dt = 100A/µs	0.44	0.93	2.0	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 20V, starting T_J = +25°C, L = 3.37mH, R_{GS} = 50Ω, I_{PEAK} = 9A. See Figure 15.

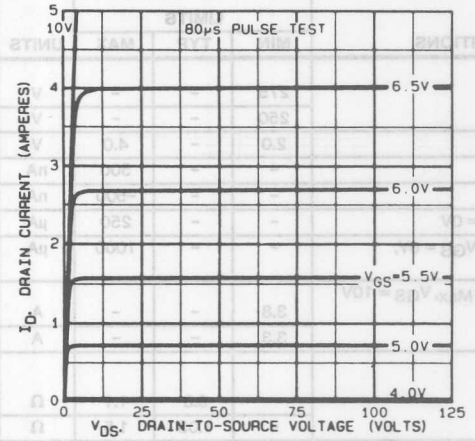


Fig. 1 — Typical Output Characteristics

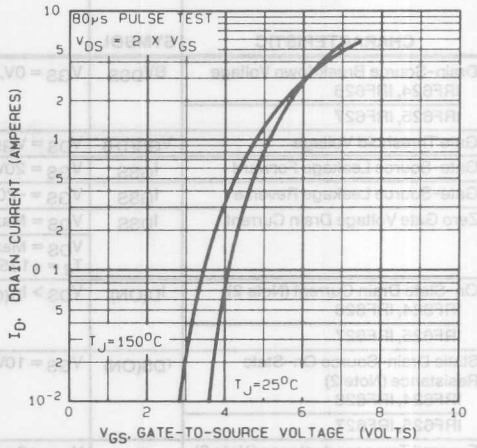


Fig. 2 — Typical Transfer Characteristics

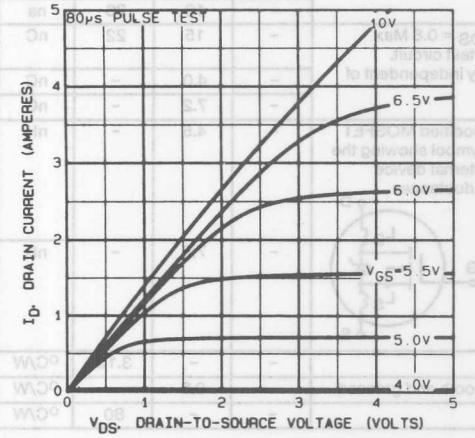


Fig. 3 — Typical Saturation Characteristics

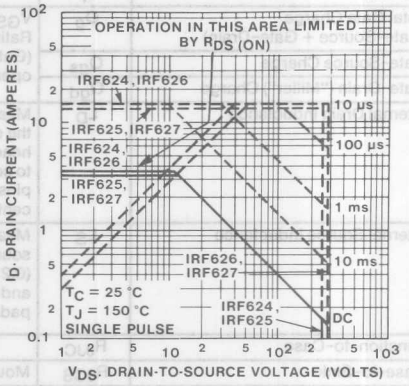


Fig. 4 — Maximum Safe Operating Area

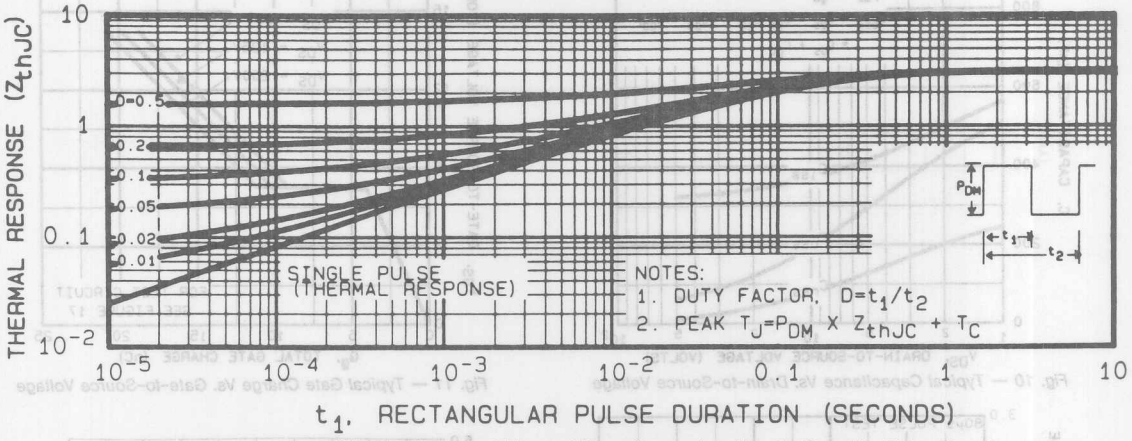


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

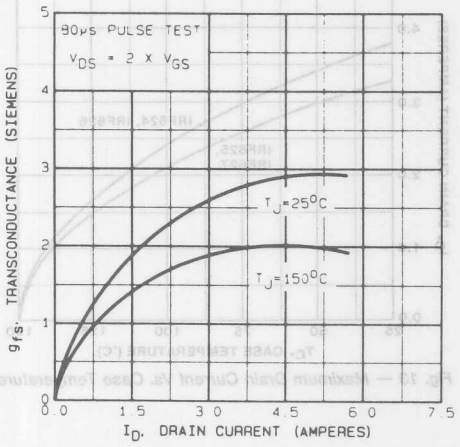


Fig. 6 — Typical Transconductance Vs. Drain Current

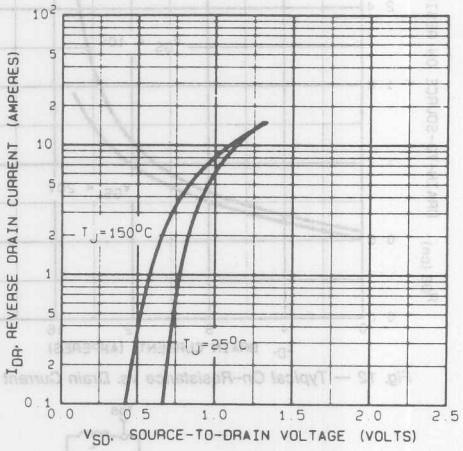


Fig. 7 — Typical Source-Drain Diode Forward Voltage

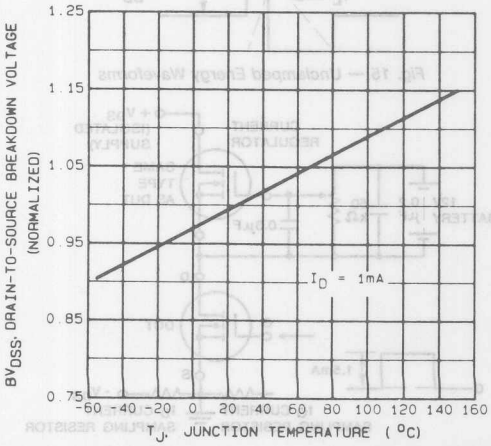


Fig. 8 — Breakdown Voltage Vs. Temperature

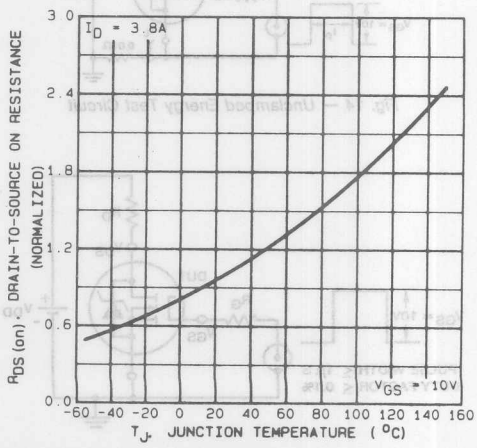


Fig. 9 — Normalized On-Resistance Vs. Temperature

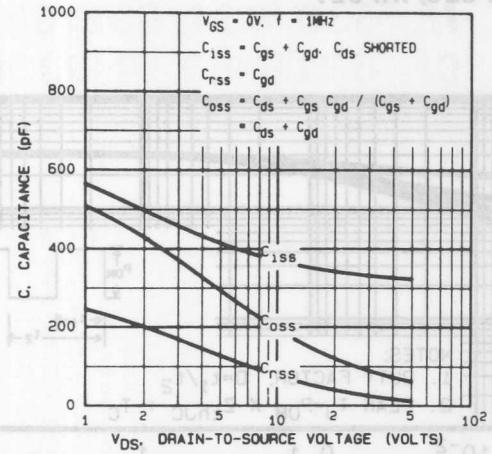


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

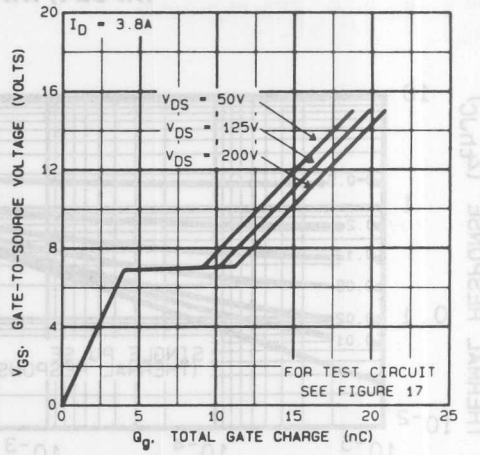


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

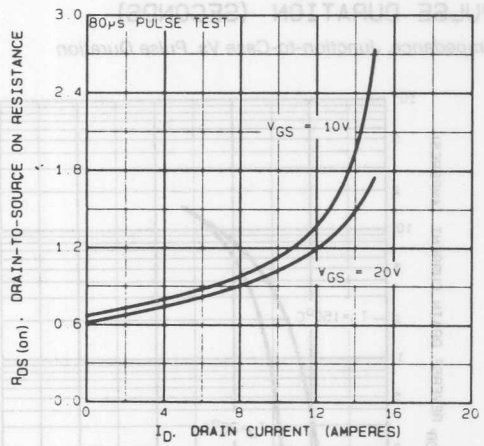


Fig. 12 — Typical On-Resistance Vs. Drain Current

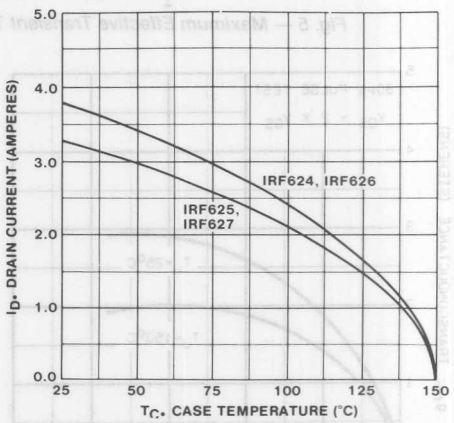


Fig. 13 — Maximum Drain Current Vs. Case Temperature

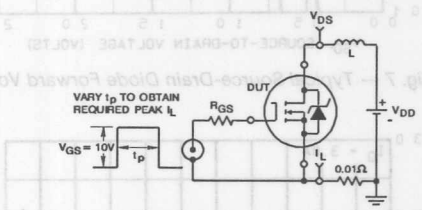


Fig. 14 — Unclamped Energy Test Circuit

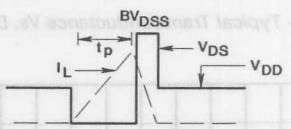


Fig. 15 — Unclamped Energy Waveforms

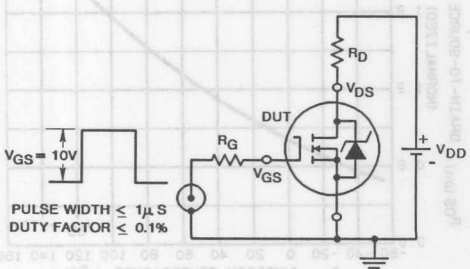


Fig. 16 — Switching Time Test Circuit

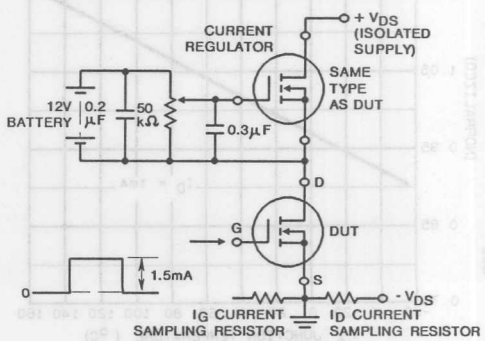


Fig. 17 — Gate Charge Test Circuit

IRF630/631/632/633
IRF630R/631R/632R/633R

N-Channel Power MOSFETs
Avalanche Energy Rated*

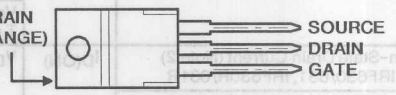
August 1991

Features

- 8.0A and 9.0A, 150V - 200V
- $r_{DS}(on)$ = 0.4Ω and 0.6Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-220AB
TOP VIEW



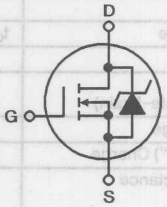
Description

The IRF630, IRF631, IRF632, and IRF633 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF630R, IRF631R, IRF632R and IRF633R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF630 IRF630R	IRF631 IRF631R	IRF632 IRF632R	IRF633 IRF633R	UNITS
Drain-Source Voltage (1)	V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	200	150	200	150	V
Continuous Drain Current						
T_C = +25°C	I_D	9.0	9.0	8.0	8.0	A
T_C = +100°C	I_D	6.0	6.0	5.0	5.0	A
Pulsed Drain Current (3)	I_{DM}	36	36	32	32	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	75	75	75	75	W
Linear Derating Factor		0.6	0.6	0.6	0.6	W/°C
Inductive Current, Clamped (See Figure 14, L = 100μH)	I_{LM}	36	36	32	32	A
Single Pulse Avalanche Energy Rating (4)	E_{AS}*	150	150	150	150	mj
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 20V, starting T_J = +25°C, L = 3.37mH, R_{GS} = 50Ω, I_{PEAK} = 9A. See Figure 15.

*R Suffix Types Only

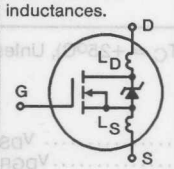
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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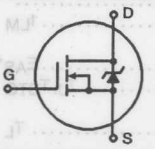
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF630/632, IRF630R/632R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	200	-	-	V
IRF631/633, IRF631R/633R			150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF630/631, IRF630R/631R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	9.0	-	-	A
IRF632/633, IRF632R/633R			8.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF630/631, IRF630R/631R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.0A	-	0.25	0.4	Ω
IRF632/633, IRF632R/633R			-	0.4	0.6	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$Max, I_D = 5.0A	3.0	4.8	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	250	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	80	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 90V, I_D = 9.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	-	30	ns
Rise Time	t_r		-	-	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	50	ns
Fall Time	t_f		-	-	40	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 9.0A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	19	30	nC
Gate-Source Charge	Q_{gs}		-	10	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	9.0	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	9.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	36	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 9.0A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 9.0A, dI_F/dt = 100A/μs	-	450	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 9.0A, dI_F/dt = 100A/μs	-	3.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 20V, Start T_J = +25°C, L = 3.37mH, R_{GS} = 50Ω, I_{PEAK} = 9A (See Figure 15)

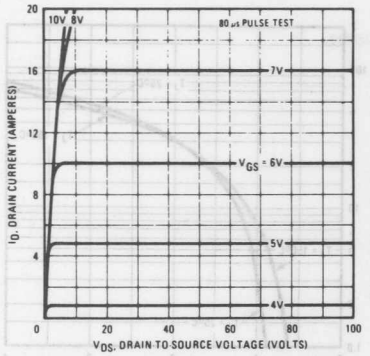


Fig. 1 – Typical Output Characteristics

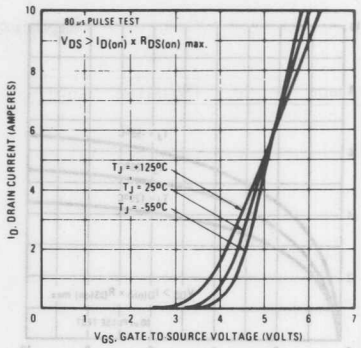


Fig. 2 – Typical Transfer Characteristics

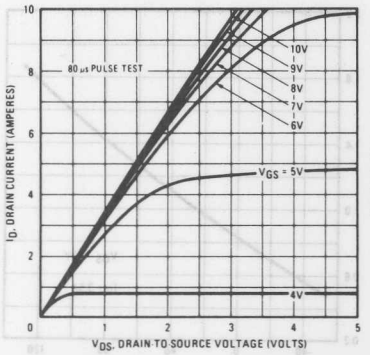


Fig. 3 – Typical Saturation Characteristics

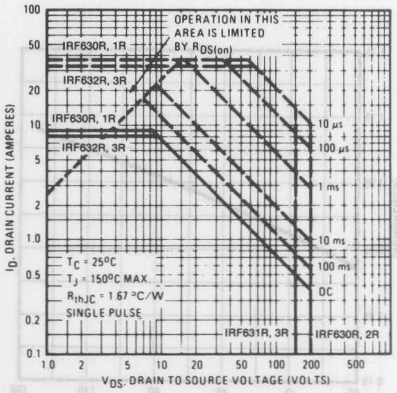


Fig. 4 – Maximum Safe Operating Area

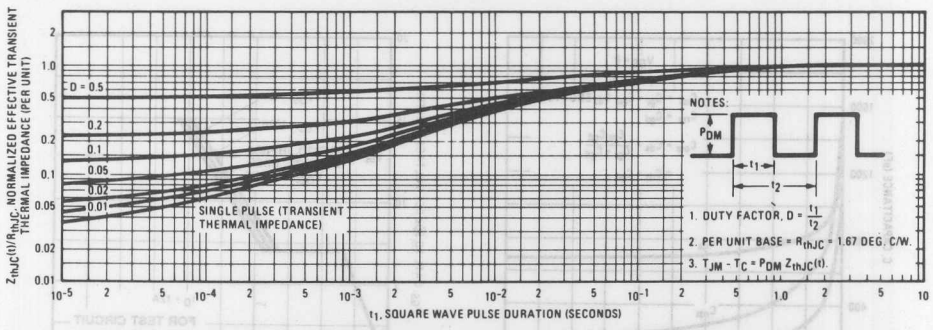


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

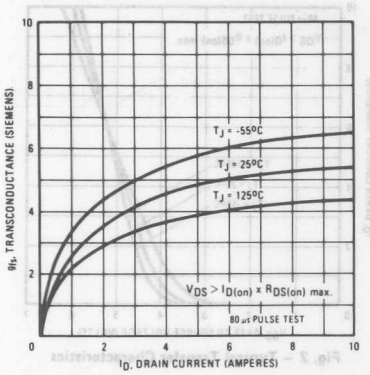


Fig. 6 – Typical Transconductance Vs. Drain Current

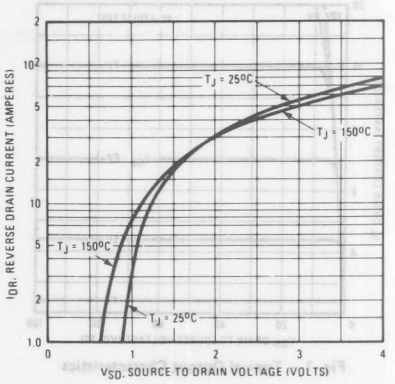


Fig. 7 – Typical Source-Drain Diode Forward Voltage

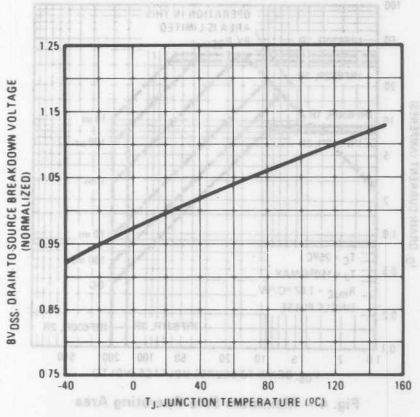


Fig. 8 – Breakdown Voltage Vs. Temperature

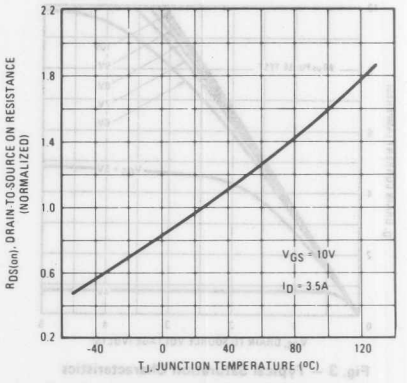


Fig. 9 – Normalized On-Resistance Vs. Temperature

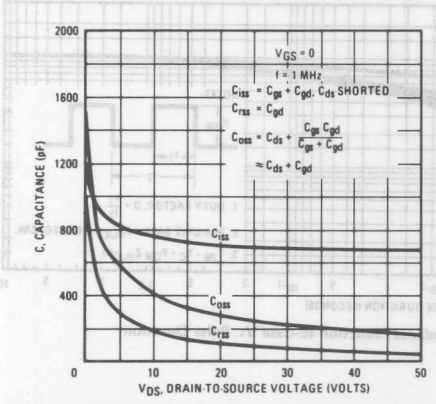


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

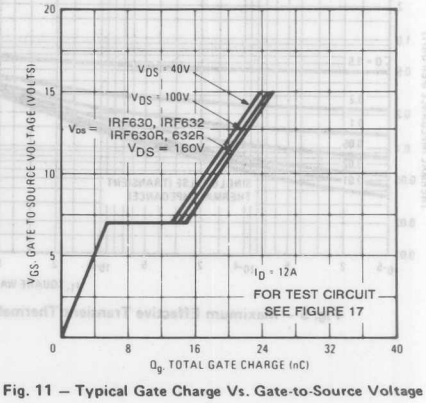


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

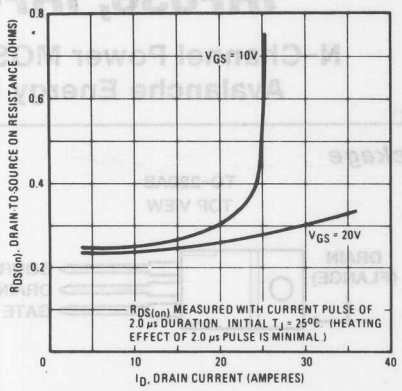


Fig. 12 — Typical On-Resistance Vs. Drain Current

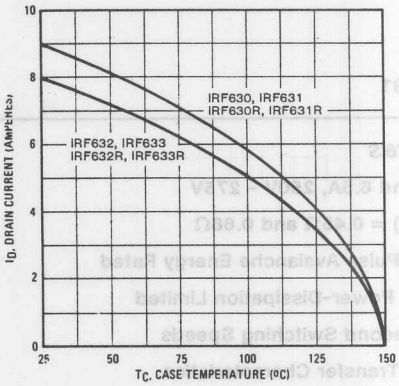


Fig. 13 — Maximum Drain Current Vs. Case Temperature

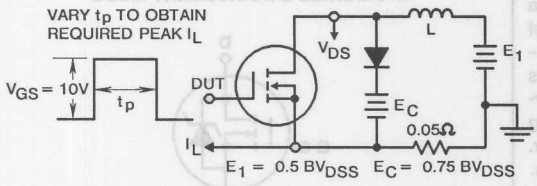


Fig. 14a — Clamped Inductive Test Circuit

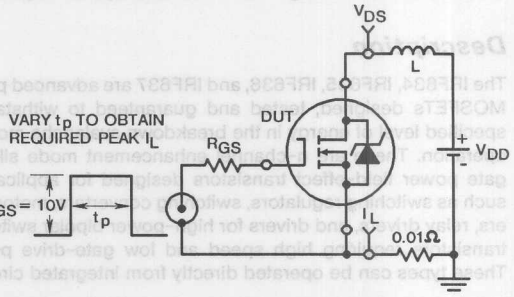


Fig. 15a — Unclamped Energy Test Circuit

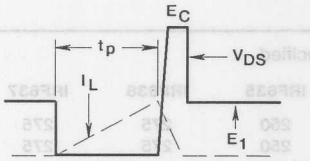


Fig. 14b — Clamped Inductive Waveforms

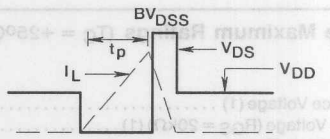


Fig. 15b — Unclamped Energy Waveforms

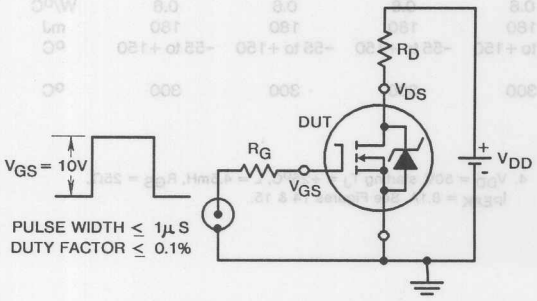


Fig. 16 — Switching Time Test Circuit

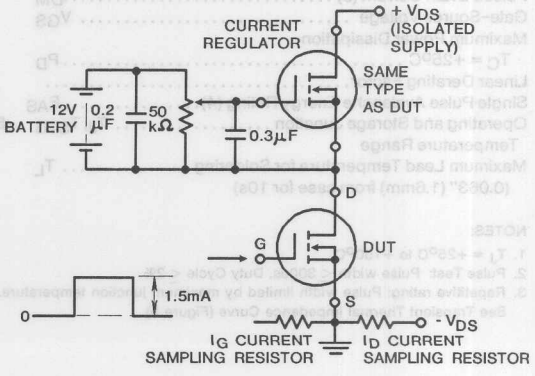


Fig. 17 — Gate Charge Test Circuit

Avalanche Energy Rated

Features

- 8.1A and 6.5A, 250V - 275V
- $r_{DS}(on)$ = 0.45Ω and 0.68Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275/250V DC Rating - 120V AC Line System Operation

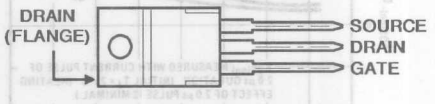
Description

The IRF634, IRF635, IRF636, and IRF637 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

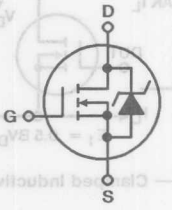
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF634	IRF635	IRF636	IRF637	UNITS
Drain-Source Voltage (1)	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current						
T_C = +25°C	I_D	8.1	6.5	8.1	6.5	A
T_C = +100°C	I_D	5.1	4.1	5.1	4.1	A
Pulsed Drain Current (3)	I_{DM}	32	26	32	26	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	75	75	75	75	W
Linear Derating Factor		0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{AS}	180	180	180	180	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

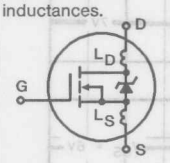
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 8.1A. See Figures 14 & 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

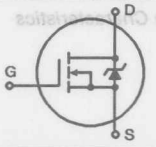
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File Number **2168.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF636, IRF637	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	275	-	-	V
IRF634, IRF635			250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF634, IRF636	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	8.1	-	-	A
IRF635, IRF637			6.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF634, IRF636	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.1A	-	0.32	0.45	Ω
IRF635, IRF637			-	0.48	0.68	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 2 x V_{GS} 0V, I_D = 4.1A	2.9	4.3	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	180	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	52	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D ≃ 8.1A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	9.1	14	ns
Rise Time	t_r		-	23	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	31	47	ns
Fall Time	t_f		-	19	29	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8.1A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	24	35	nC
Gate-Source Charge	Q_{gs}		-	5.1	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	8.1	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.1A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 8.1A, dI_F/dt = 100A/μs	92	180	390	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 8.1A, dI_F/dt = 100A/μs	0.63	1.3	2.7	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 8.1A (See Figures 14 & 15)

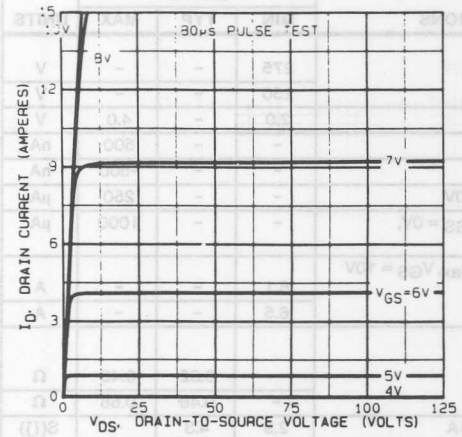


Fig. 1 — Typical Output Characteristics

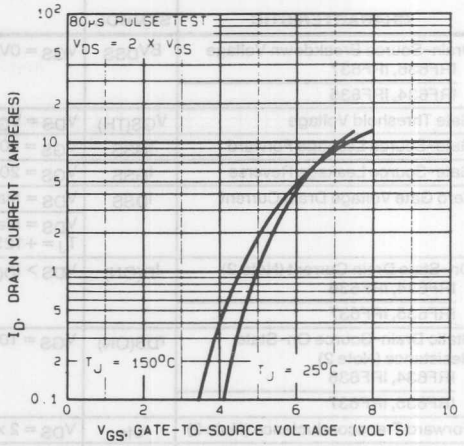


Fig. 2 — Typical Transfer Characteristics

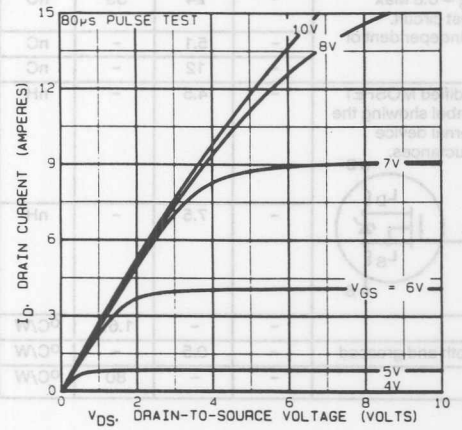


Fig. 3 — Typical Saturation Characteristics

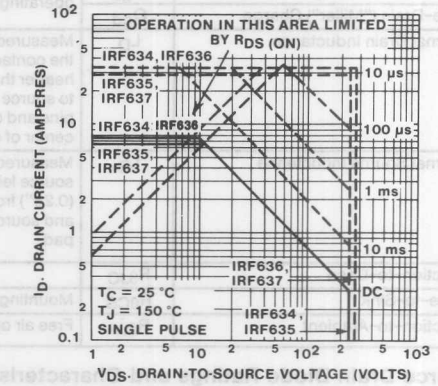


Fig. 4 — Maximum Safe Operating Area

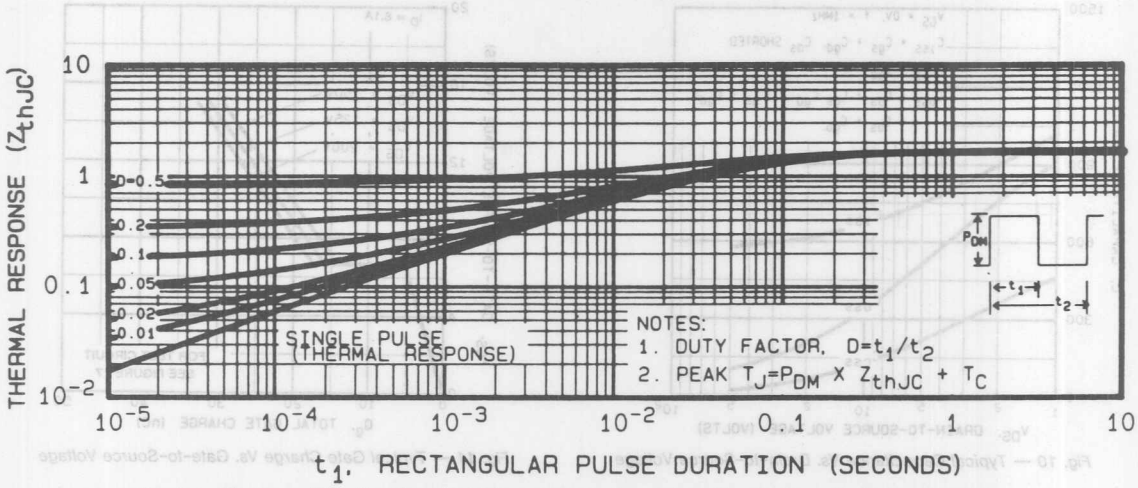


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

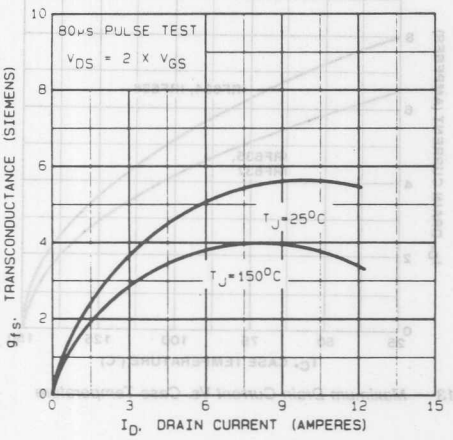


Fig. 6 — Typical Transconductance Vs. Drain Current

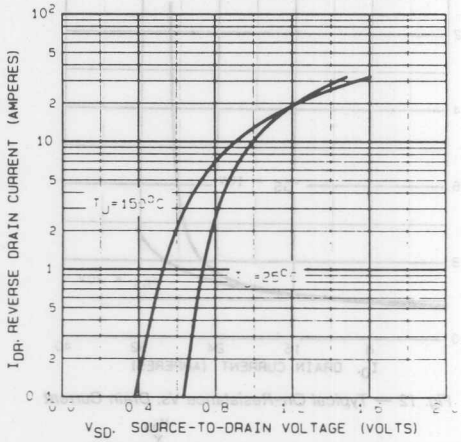


Fig. 7 — Typical Source-Drain Diode Forward Voltage

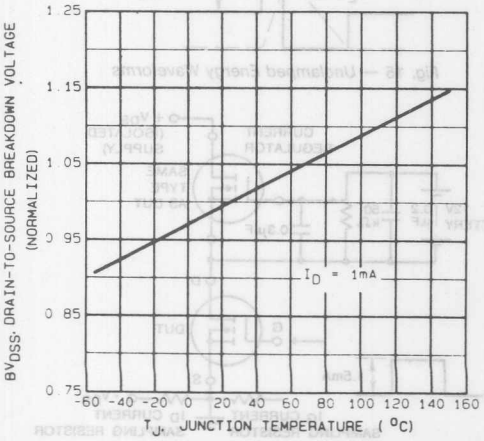


Fig. 8 — Breakdown Voltage Vs. Temperature

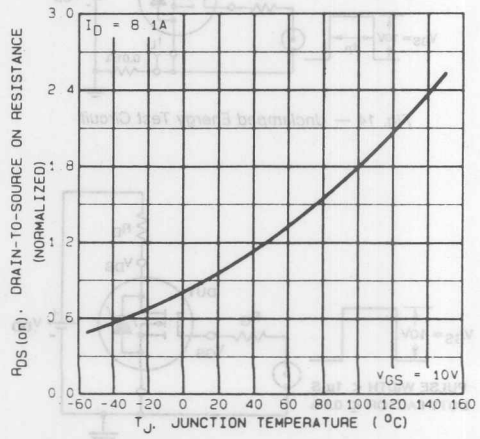


Fig. 9 — Normalized On-Resistance Vs. Temperature

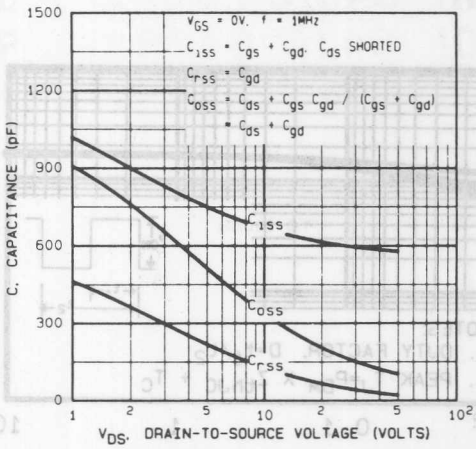


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

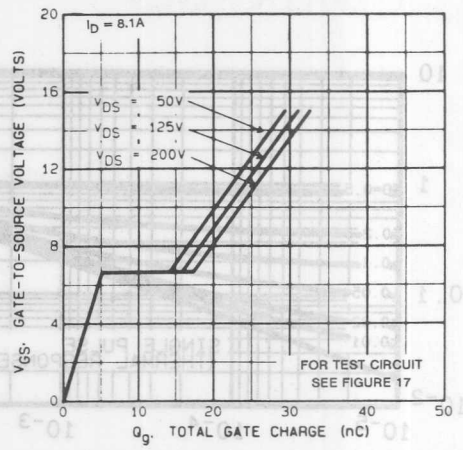


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

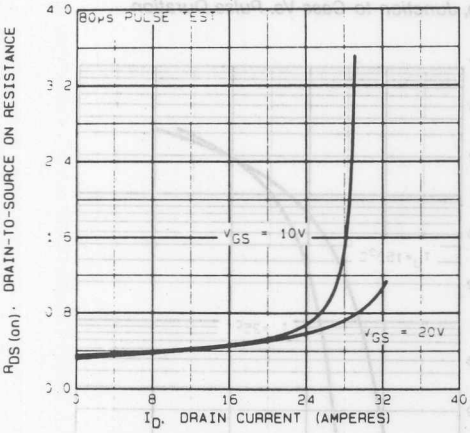


Fig. 12 — Typical On-Resistance Vs. Drain Current

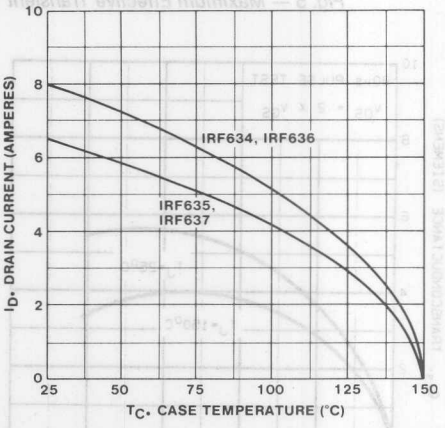


Fig. 13 — Maximum Drain Current Vs. Case Temperature

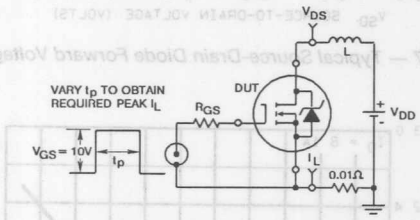


Fig. 14 — Unclamped Energy Test Circuit

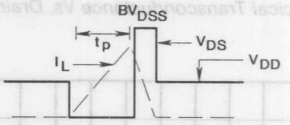


Fig. 15 — Unclamped Energy Waveforms

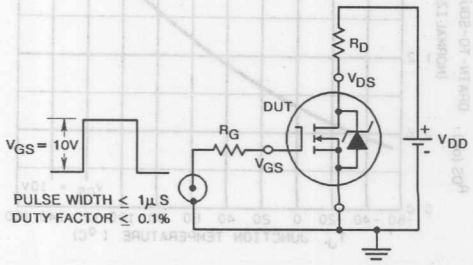


Fig. 16 — Switching Time Test Circuit

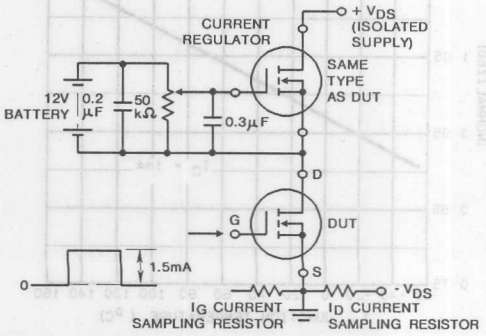


Fig. 17 — Gate Charge Test Circuit

HARRIS

IRF640/641/642/643
IRF640R/641R/642R/643R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 16A and 18A, 150V - 200V
- $r_{DS}(on)$ = 0.18Ω and 0.22Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

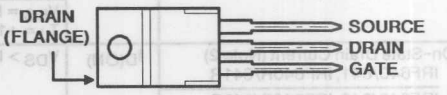
Description

The IRF640, IRF641, IRF642, and IRF643 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF640R, IRF641R, IRF642R and IRF643R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

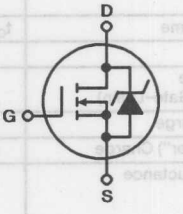
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF640 IRF640R	IRF641 IRF641R	IRF642 IRF642R	IRF643 IRF643R	UNITS
Drain-Source Voltage (1)	V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	200	150	200	150	V
Continuous Drain Current						
T_C = +25°C	I_D	18	18	16	16	A
T_C = +100°C	I_D	11	11	10	10	A
Pulsed Drain Current (3)	I_{DM}	72	72	64	64	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	125	125	125	125	W
Linear Derating Factor		1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped (See Figure 14, L = 100μH)	I_{LM}	72	72	64	64	A
Single Pulse Avalanche Energy Rating (4)	E_{AS}*	580	580	580	580	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 2.7mH, R_{GS} = 25Ω, I_{PEAK} = 18A. See Figure 15.

*R Suffix Types Only

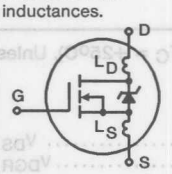
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1585.1**

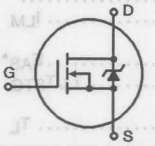
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF640/642, IRF640R/642R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	-	-	V
IRF641/643, IRF641R/643R			150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRF640/641, IRF640R/641R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	18	-	-	A
IRF642/643, IRF642R/643R			16	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF640/641, IRF640R/641R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 10A	-	0.14	0.18	Ω
IRF642/643, IRF642R/643R			-	0.20	0.22	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 10A	6.7	10	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	1275	-	pF
Output Capacitance	C_{OSS}		-	400	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, I_D = 18A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	13	21	ns
Rise Time	t_r		-	50	77	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	46	68	ns
Fall Time	t_f		-	35	54	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	43	64	nC
Gate-Source Charge	Q_{gs}		-	8	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	22	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	18	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	72	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 18A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 18A, dI_F/dt = 100A/µs	120	240	530	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 18A, dI_F/dt = 100A/µs	1.3	2.8	5.6	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 20V, Start T_J = +25°C, L = 3.37mH, R_{GS} = 25Ω, I_{PEAK} = 18A (See Figure 15)

Performance Curves

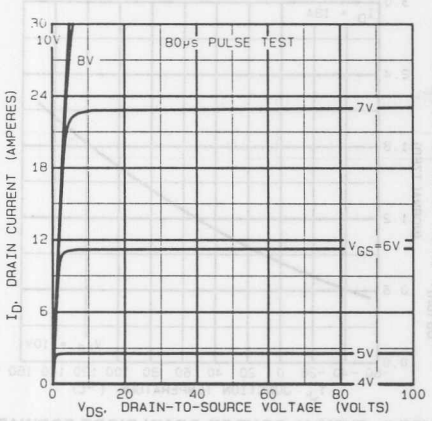


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

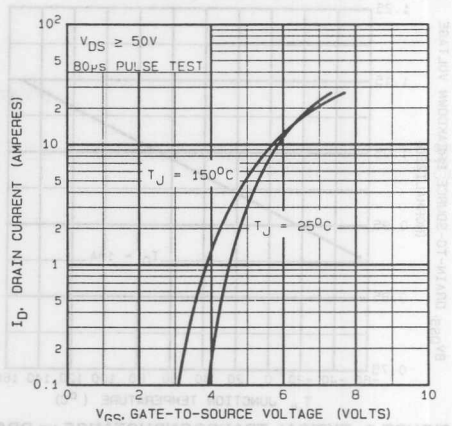


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

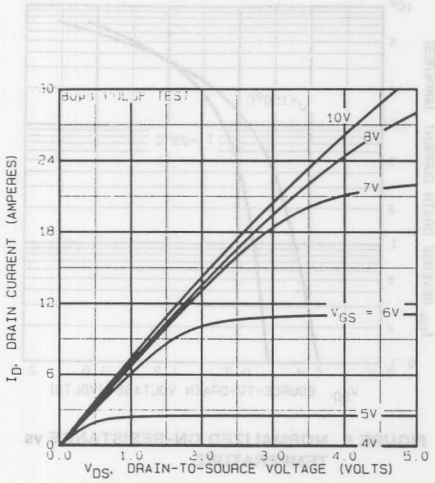


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

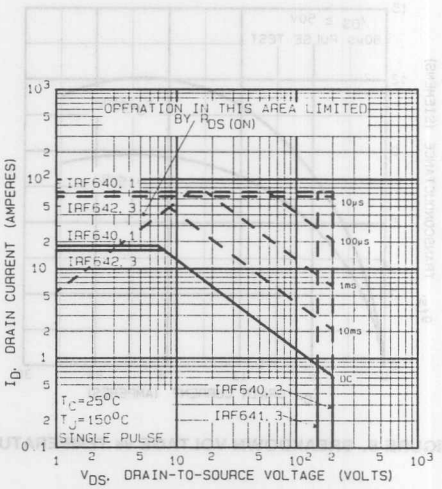


FIGURE 4. MAXIMUM SAFE OPERATING AREA

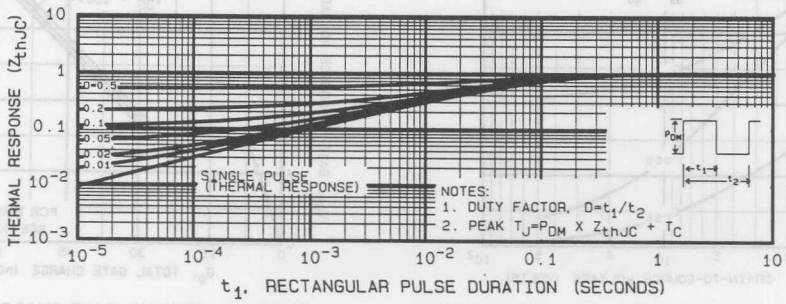


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

4 N-CHANNEL POWER MOSFETs

Performance Curves (Continued)

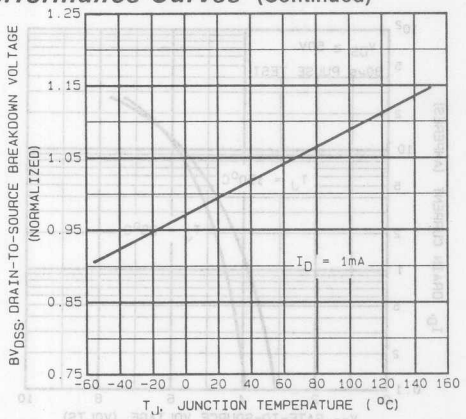


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

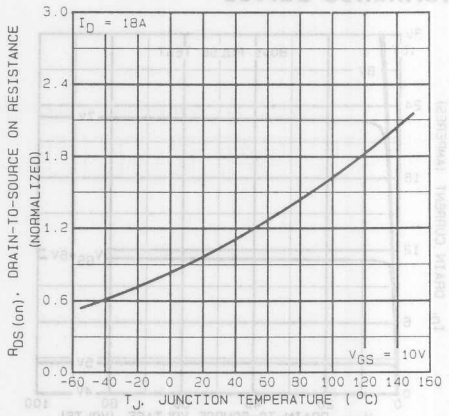


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

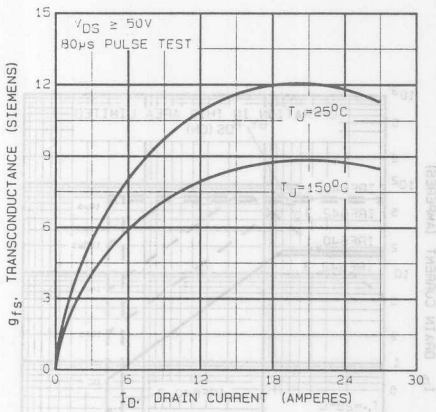


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

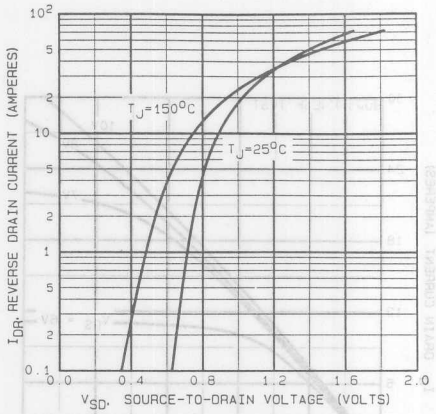


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

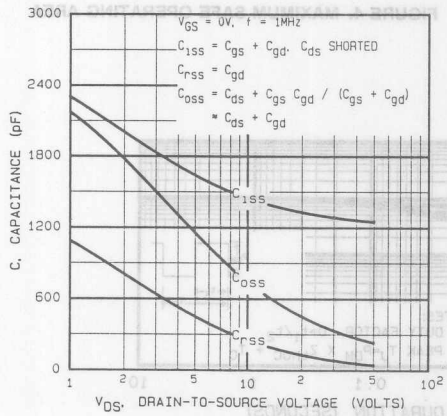


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

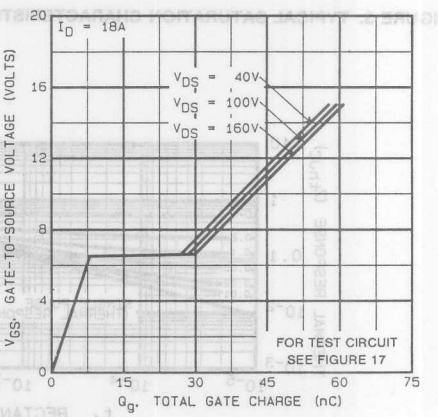


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

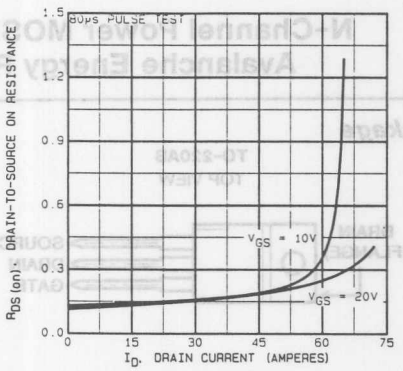


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

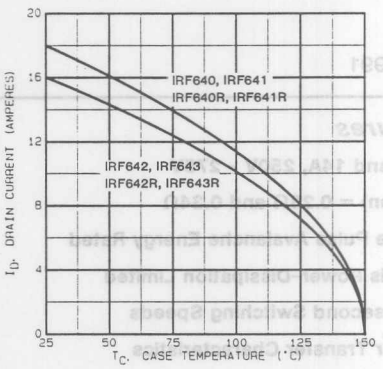


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

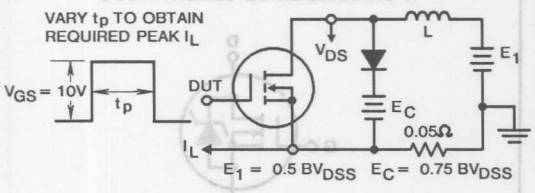


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

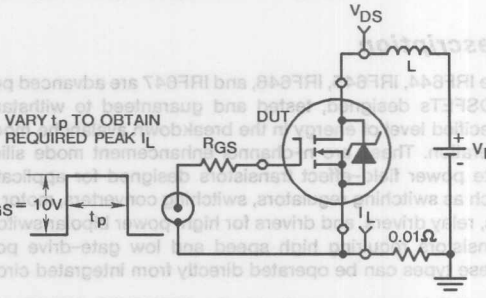


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

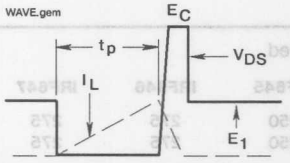


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

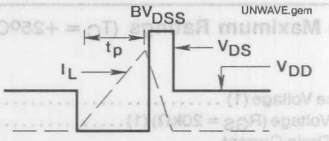


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

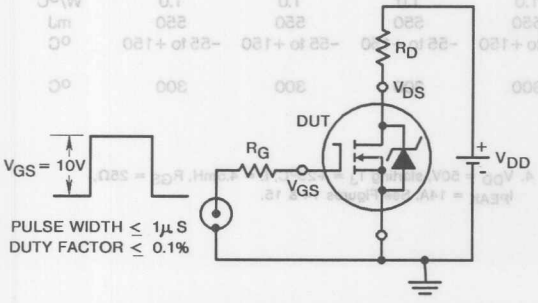


FIGURE 16. SWITCHING TIME TEST CIRCUIT

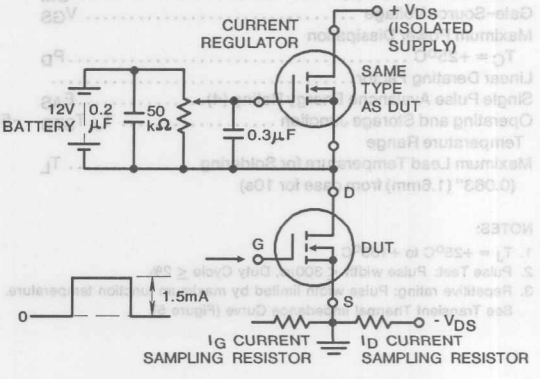


FIGURE 17. GATE CHARGE TEST CIRCUIT

Features

- 13A and 14A, 250V - 275V
- $r_{DS}(on)$ = 0.28Ω and 0.34Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275/250V DC Rating - 120V AC Line System Operation

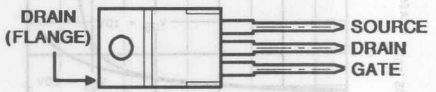
Description

The IRF644, IRF645, IRF646, and IRF647 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

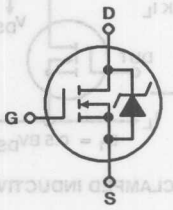
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF644	IRF645	IRF646	IRF647	UNITS
Drain-Source Voltage (1) ..... V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	250	250	275	275	V
Continuous Drain Current					
T_C = +25°C ..... I_D	14	13	14	13	A
T_C = +100°C ..... I_D	8.8	8.0	8.8	8.0	A
Pulsed Drain Current (3) ..... I_{DM}	56	52	56	52	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}	550	550	550	550	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

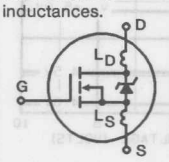
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 14A. See Figures 14 & 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

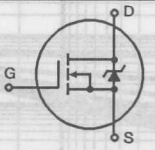
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File Number **2169.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF646, IRF647	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	275	-	-	V
IRF644, IRF645			250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF644, IRF646	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	14	-	-	A
IRF645, IRF647			13	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF644, IRF646	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8A	-	0.20	0.28	Ω
IRF645, IRF647			-	0.28	0.34	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 8A	6.7	10	-	S( )
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	1300	-	pF
Output Capacitance	C_{OSS}		-	320	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	69	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 14A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	16	24	ns
Rise Time	t_r		-	67	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	53	80	ns
Fall Time	t_f		-	49	74	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	39	59	nC
Gate-Source Charge	Q_{gs}		-	6.6	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	20	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	14	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	56	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 14A, V_{GS} = 0V	-	-	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/μs	150	300	640	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/μs	1.6	3.4	7.2	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 14A (See Figures 14 & 15)

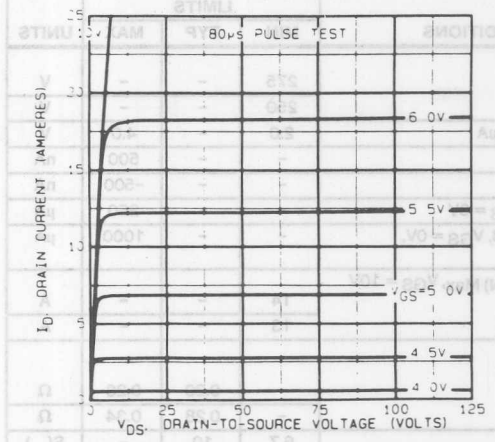


Fig. 1 — Typical Output Characteristics

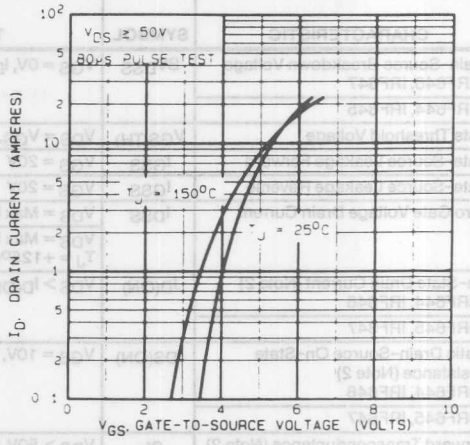


Fig. 2 — Typical Transfer Characteristics

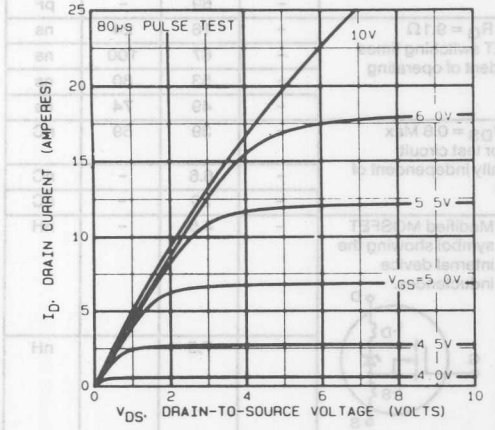


Fig. 3 — Typical Saturation Characteristics

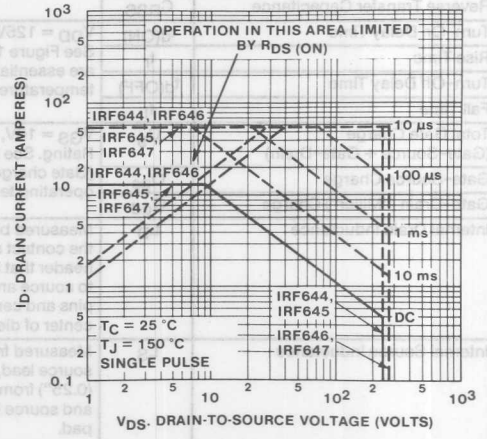


Fig. 4 — Maximum Safe Operating Area

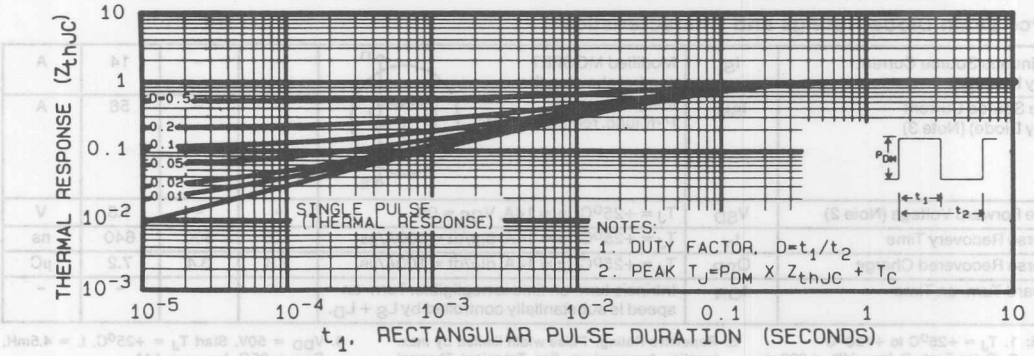


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

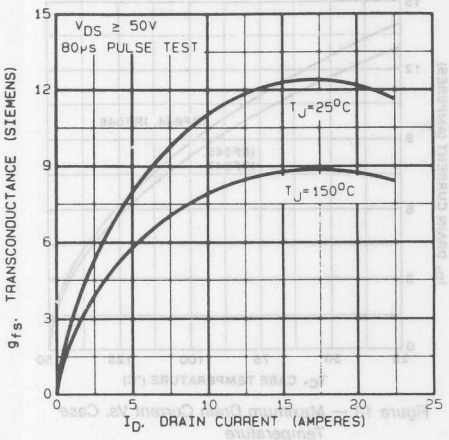


Fig. 6 — Typical Transconductance Vs. Drain Current

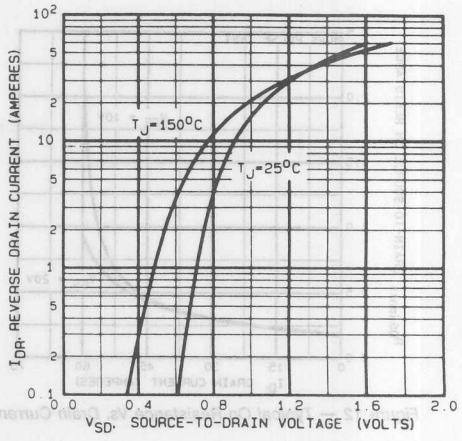


Fig. 7 — Typical Source-Drain Diode Forward Voltage

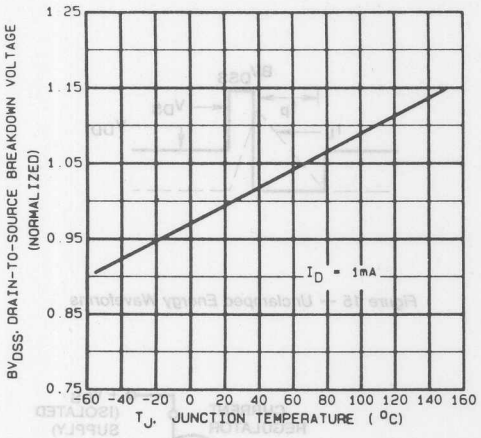


Fig. 8 — Breakdown Voltage Vs. Temperature

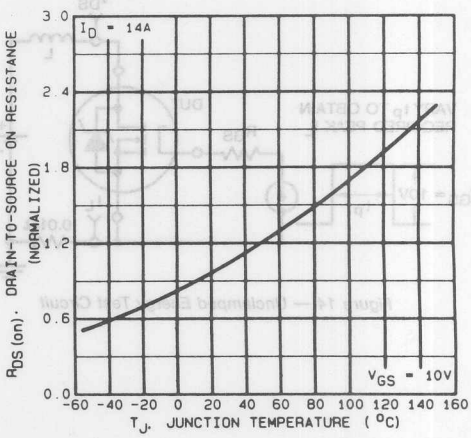


Fig. 9 — Normalized On-Resistance Vs. Temperature

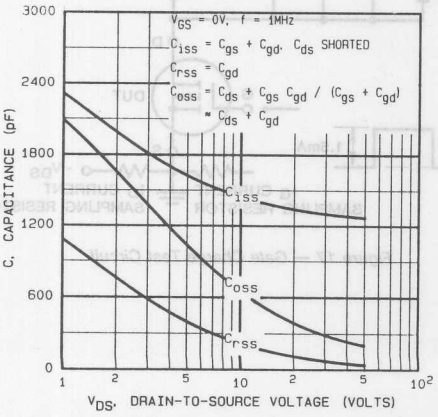


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

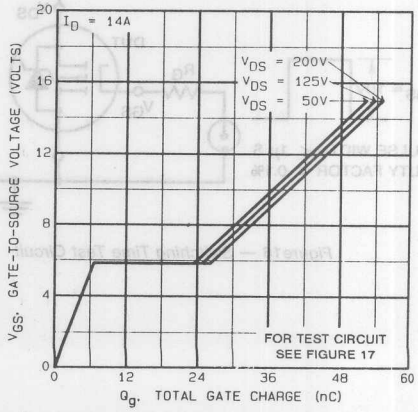


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

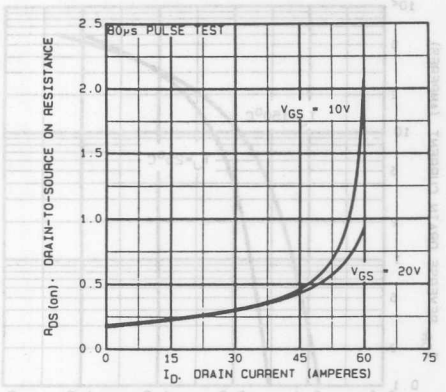


Figure 12 — Typical On Resistance Vs. Drain Current

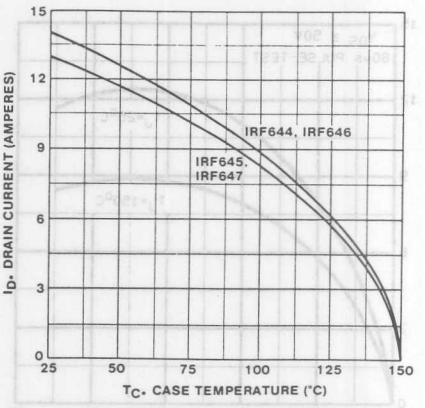


Figure 13 — Maximum Drain Current Vs. Case Temperature

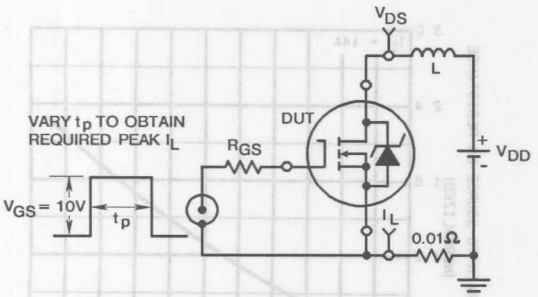


Figure 14 — Unclamped Energy Test Circuit

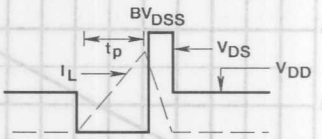


Figure 15 — Unclamped Energy Waveforms

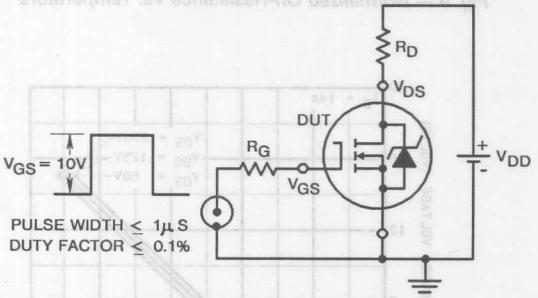


Figure16 — Switching Time Test Circuit

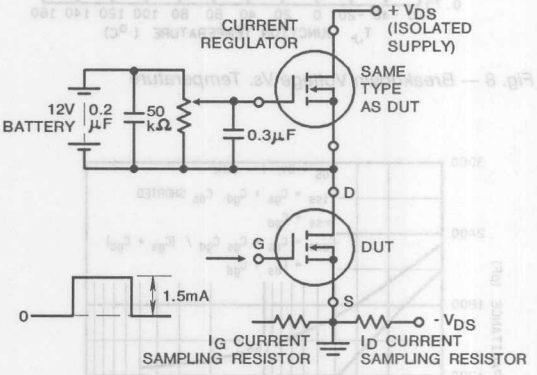


Figure 17 — Gate Charge Test Circuit

HARRIS

IRF710/711/712/713
IRF710R/711R/712R/713R

N-Channel Power MOSFETs
Avalanche Energy Rated*

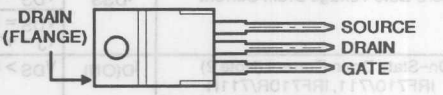
August 1991

Features

- 1.7A and 2.0A, 350V - 400V
- $r_{DS}(on)$ = 3.6Ω and 5.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-220AB
TOP VIEW



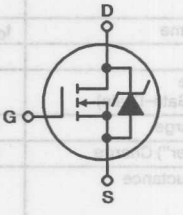
Description

The IRF710, IRF711, IRF712, and IRF713 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF710R, IRF711R, IRF712R and IRF713R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4

N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF710 IRF710R	IRF711 IRF711R	IRF712 IRF712R	IRF713 IRF713R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	2	2	1.7	1.7	A
T_C = +100°C ..... I_D	1.2	1.2	1.1	1.1	A
Pulsed Drain Current (3) ..... I_{DM}	5	5	4.3	4.3	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	36	36	36	36	W
Linear Derating Factor	0.29	0.29	0.29	0.29	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	6.0	6.0	5.0	5.0	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	120	120	120	120	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

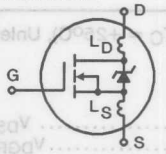
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 53mH, R_{GS} = 25Ω, I_{PEAK} = 2A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number **2310.1**

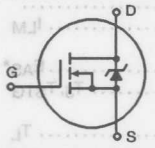
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF710/712, IRF710R/712R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	–	–	V
IRF711/713, IRF711R/713R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF710/711, IRF710R/711R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V	2.0	–	–	A
IRF712/713, IRF712R/713R			1.7	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF710/711, IRF710R/711R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.1A	–	3.3	3.6	Ω
IRF712/713, IRF712R/713R			–	3.6	5.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 1.1A	1.0	1.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	135	–	pF
Output Capacitance	C_{OSS}		–	35	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	8.0	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D ≃ 5.6A, R_G = 24Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	8.0	12	ns
Rise Time	t_r		–	10	15	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	21	32	ns
Fall Time	t_f		–	11	17	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 2.0A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	7.0	12	nC
Gate-Source Charge	Q_{gs}		–	1.2	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	4.0	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	3.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	2.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	5.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.0A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 2.0A, dI_F/dt = 100A/µs	110	–	520	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 2.0A, dI_F/dt = 100A/µs	0.40	–	1.4	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 53mH, R_{GS} = 25Ω, I_{PEAK} = 2A (See Figure 15)

Performance Curves

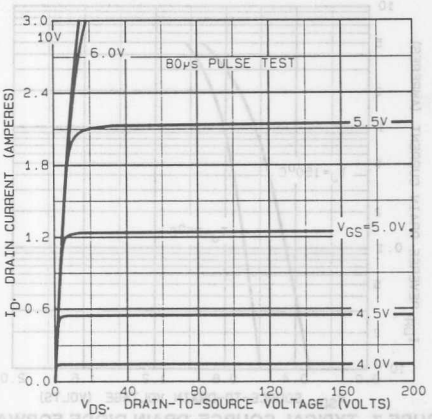


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

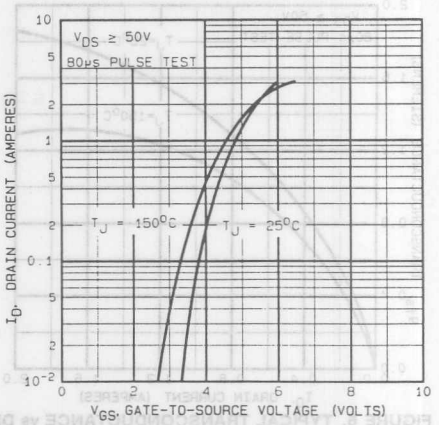


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

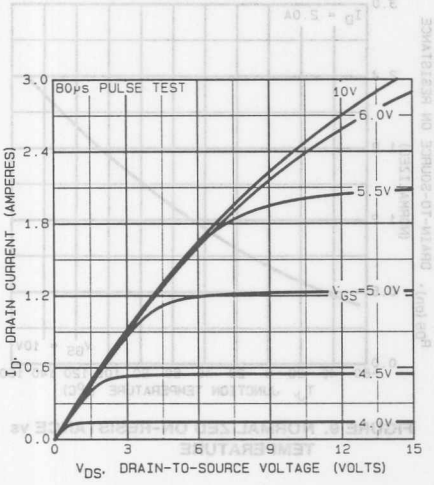


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

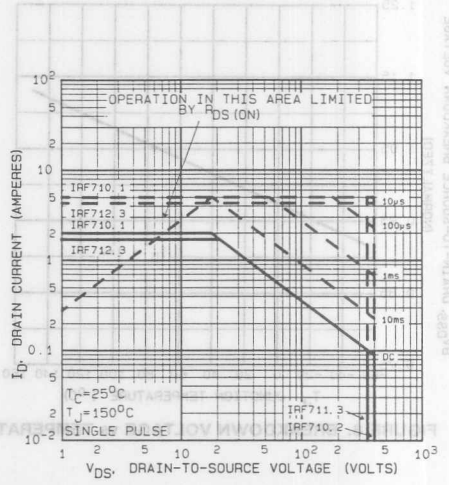


FIGURE 4. MAXIMUM SAFE OPERATING AREA

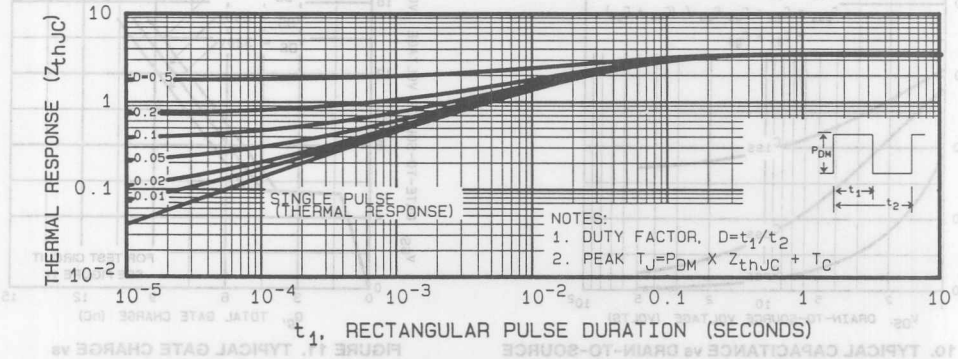


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

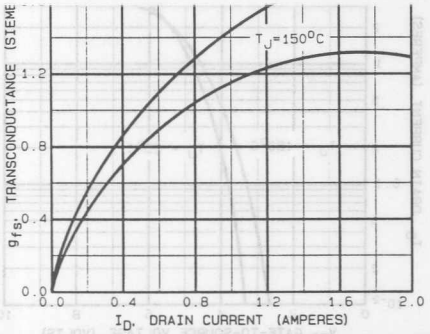


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

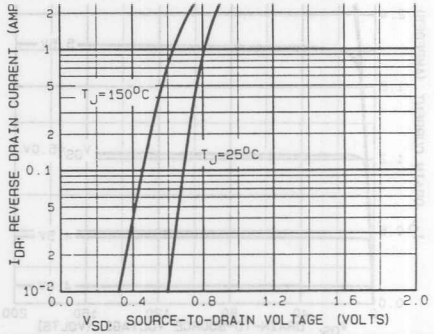


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

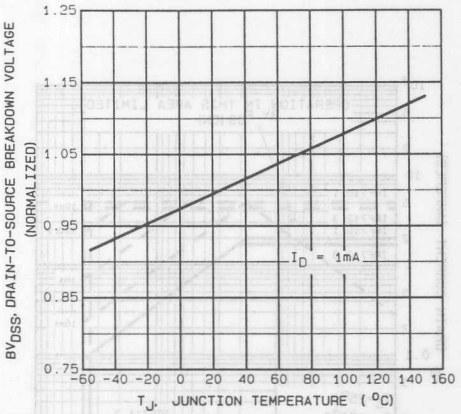


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

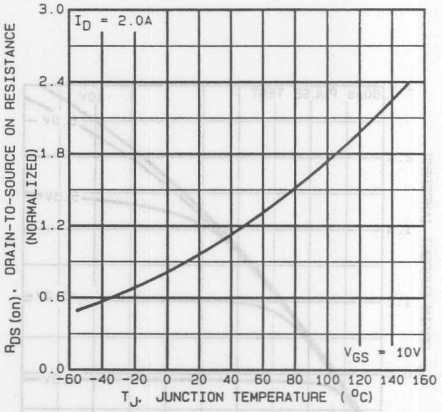


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

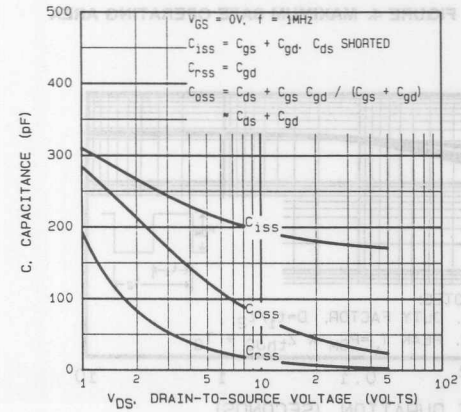


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

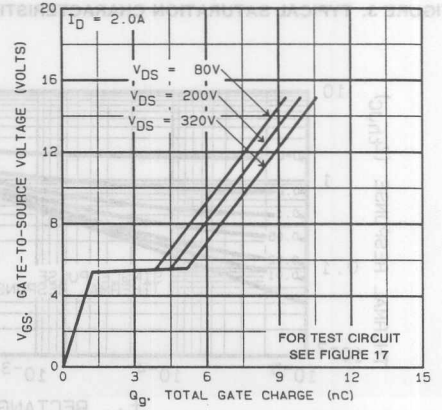


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

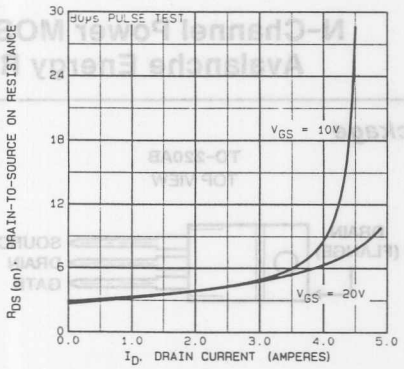


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

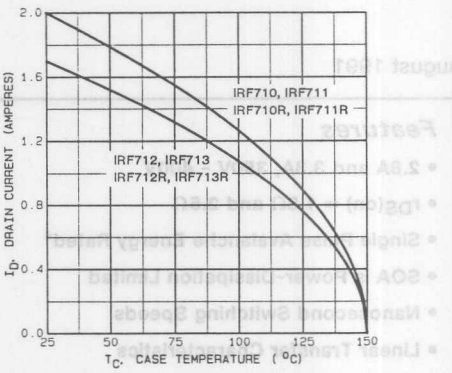


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

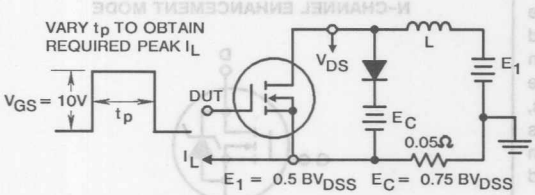


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

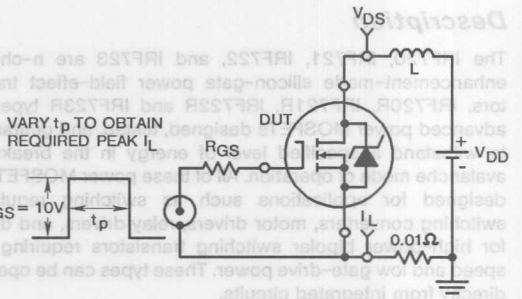


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

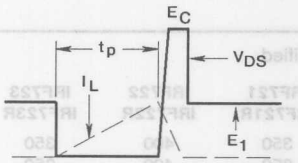


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

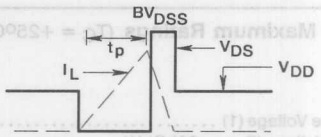


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

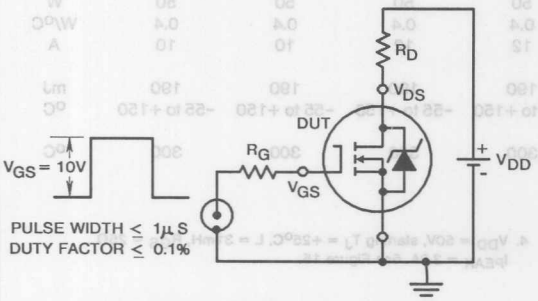


FIGURE 16. SWITCHING TIME TEST CIRCUIT

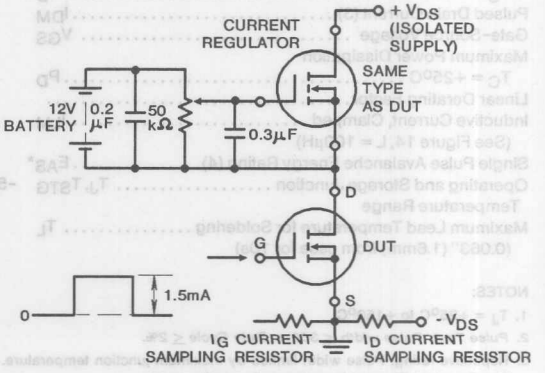


FIGURE 17. GATE CHARGE TEST CIRCUIT

4 N-CHANNEL POWER MOSFETs

HARRIS

IRF720/721/722/723
IRF720R/721R/722R/723R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 2.8A and 3.3A, 350V - 400V
- $r_{DS}(on)$ = 1.8Ω and 2.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

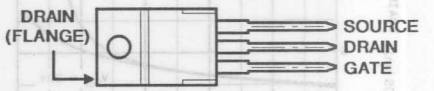
Description

The IRF720, IRF721, IRF722, and IRF723 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF720R, IRF721R, IRF722R and IRF723R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF720 IRF720R	IRF721 IRF721R	IRF722 IRF722R	IRF723 IRF723R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	3.3	3.3	2.8	2.8	A
T_C = +100°C ..... I_D	2.1	2.1	1.8	1.8	A
Pulsed Drain Current (3) ..... I_{DM}	13	13	11	11	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	50	50	50	50	W
Linear Derating Factor	0.4	0.4	0.4	0.4	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	12	12	10	10	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	190	190	190	190	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 31mH, R_{GS} = 25Ω, I_{PEAK} = 3.3A. See Figure 15.

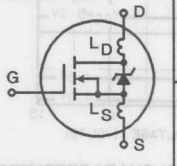
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1579.1

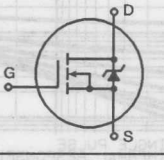
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF720/722, IRF720R/722R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	–	–	V
IRF721/723, IRF721R/723R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF720/721, IRF720R/721R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V	3.3	–	–	A
IRF722/723, IRF722R/723R			2.8	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF720/721, IRF720R/721R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.8A	–	1.5	1.8	Ω
IRF722/723, IRF722R/723R			–	1.8	2.5	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 1.8A	1.8	2.7	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	360	–	pF
Output Capacitance	C_{OSS}		–	55	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, $I_D \simeq$ 3.3A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	10	15	ns
Rise Time	t_r		–	14	21	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	30	45	ns
Fall Time	t_f		–	13	20	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.3A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	12	20	nC
Gate-Source Charge	Q_{gs}		–	2.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	6.0	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	2.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	3.3	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	13	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.3A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 3.3A, dI_F/dt = 100A/µs	120	–	600	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 3.3A, dI_F/dt = 100A/µs	0.64	–	3.0	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 31mH, R_{GS} = 25Ω, I_{PEAK} = 3.3A (See Figure 15)

Performance Curves

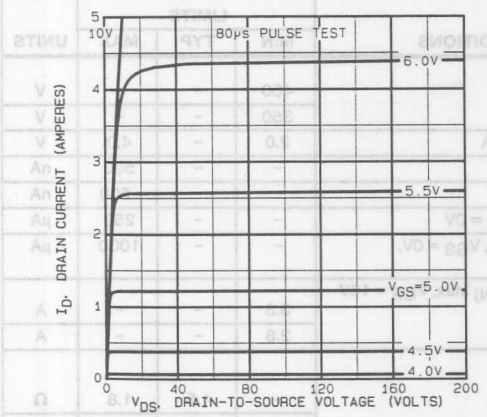


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

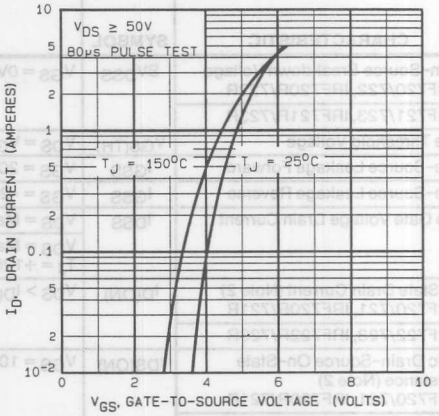


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

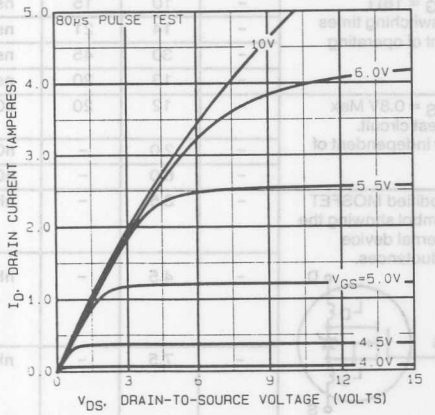


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

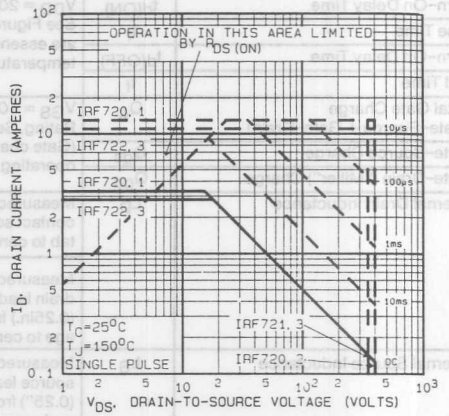


FIGURE 4. MAXIMUM SAFE OPERATING AREA

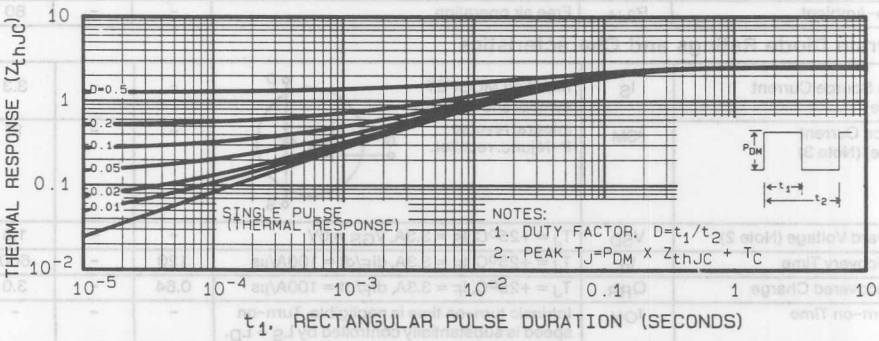


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

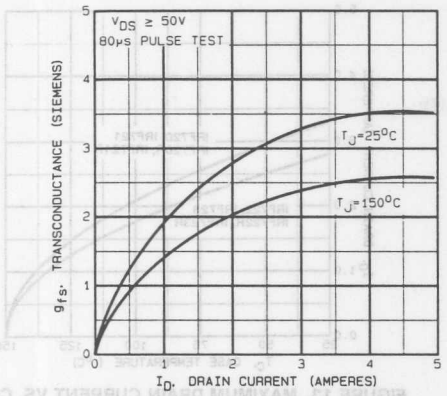


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

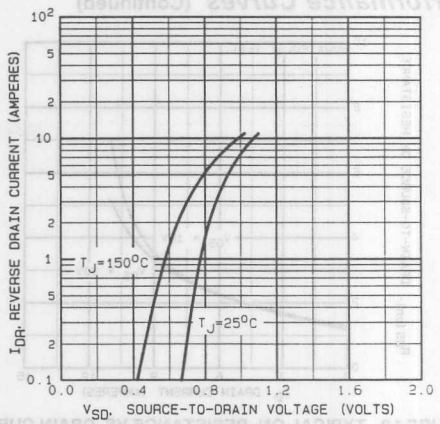


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

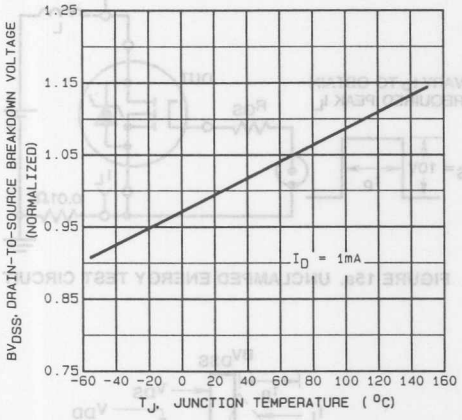


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

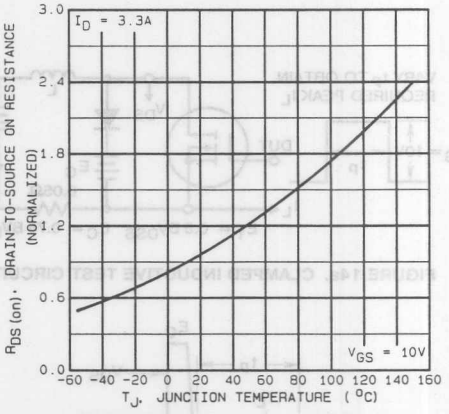


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

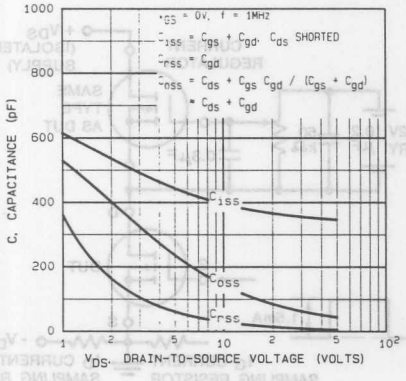


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

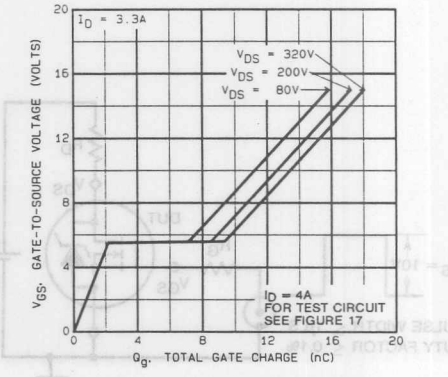


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

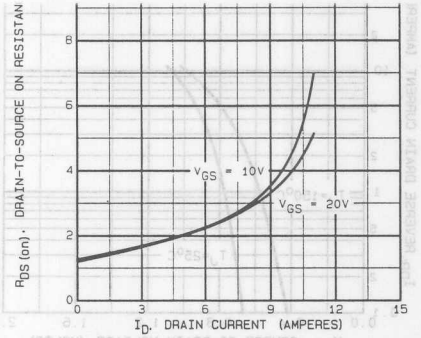


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

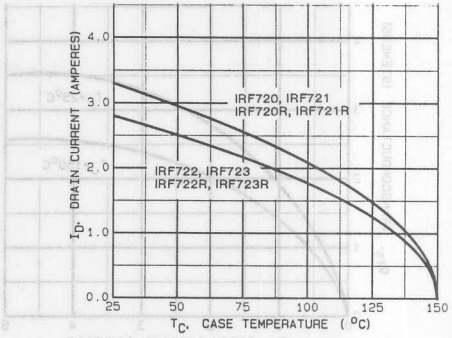


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

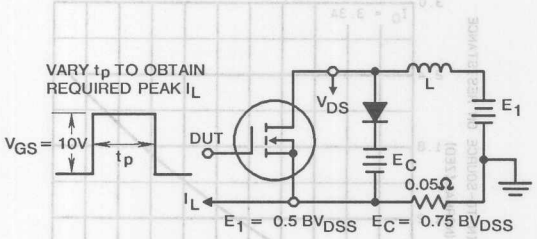


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

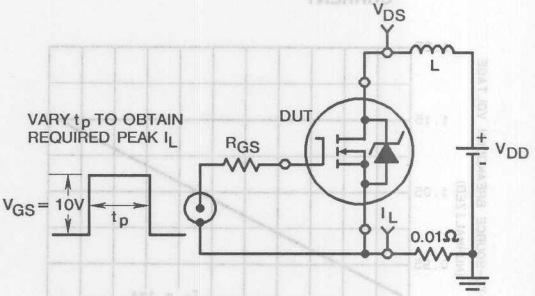


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

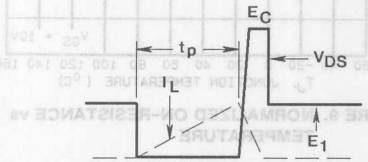


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

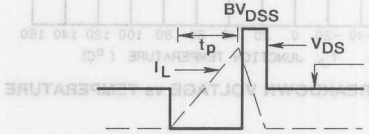


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

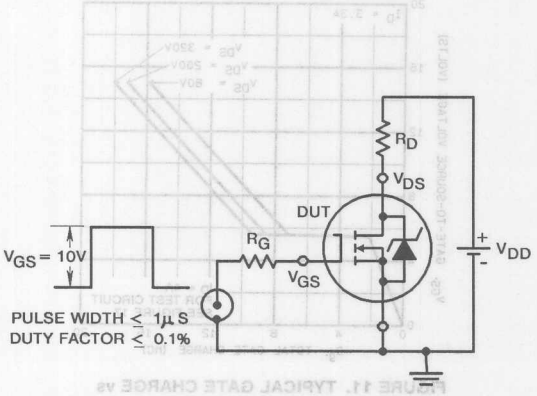


FIGURE 16. SWITCHING TIME TEST CIRCUIT

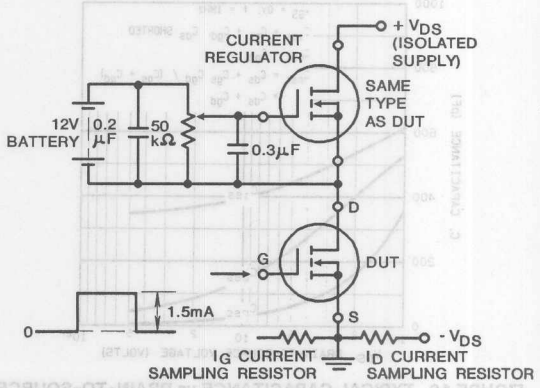


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF730/731/732/733
IRF730R/731R/732R/733R

N-Channel Power MOSFETs
Avalanche Energy Rated*

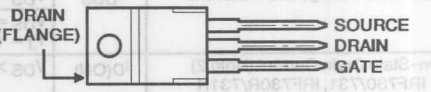
August 1991

Features

- 4.5A and 5.5A, 350V - 400V
- $r_{DS}(on)$ = 1.0Ω and 1.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-220AB
TOP VIEW



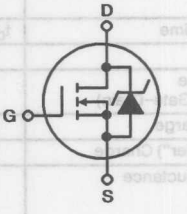
Description

The IRF730, IRF731, IRF732, and IRF733 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF730R, IRF731R, IRF732R and IRF733R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF730 IRF730R	IRF731 IRF731R	IRF732 IRF732R	IRF733 IRF733R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	5.5	5.5	4.5	4.5	A
T_C = +100°C ..... I_D	3.5	3.5	3.0	3.0	A
Pulsed Drain Current (3) ..... I_{DM}	22	22	18	18	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	22	22	18	18	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	300	300	300	300	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 17mH, R_{GS} = 25Ω, I_{PEAK} = 5.5A. See Figure 15.

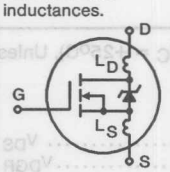
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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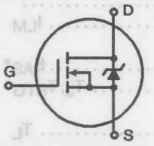
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF730/732, IRF730R/732R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	-	-	V
IRF731/733, IRF731R/733R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRF730/731, IRF730R/731R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V	5.5	-	-	A
IRF732/733, IRF732R/733R			4.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF730/731, IRF730R/731R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.0A	-	0.8	1.0	Ω
IRF732/733, IRF732R/733R			-	1.0	1.5	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 3.0A	2.9	4.4	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	150	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	40	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, $I_D \simeq$ 5.5A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	10	17	ns
Rise Time	t_r		-	20	29	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	35	56	ns
Fall Time	t_f		-	15	24	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 5.5A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	20	35	nC
Gate-Source Charge	Q_{gs}		-	3.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	10	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	5.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	22	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 5.5A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/µs	140	300	660	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/µs	0.93	2.1	4.3	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 17mH, R_{GS} = 25Ω, I_{PEAK} = 5.5A (See Figure 15)

Performance Curves

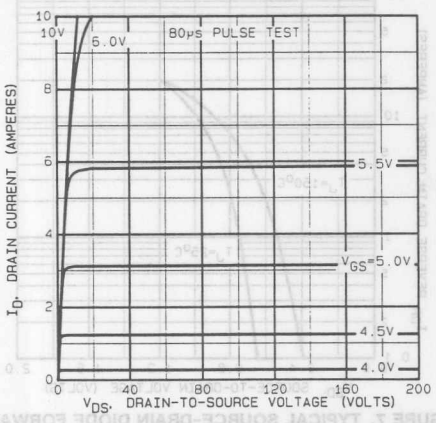


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

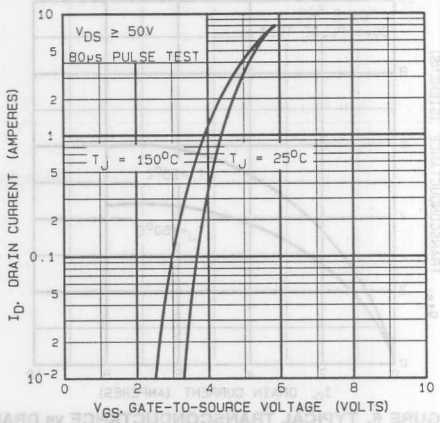


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

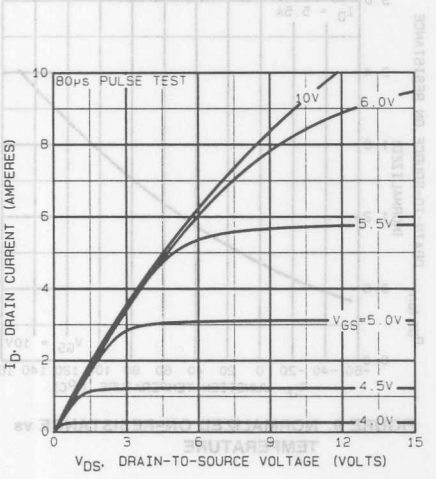


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

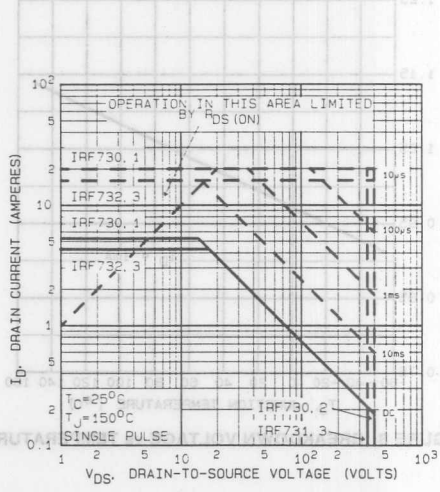


FIGURE 4. MAXIMUM SAFE OPERATING AREA

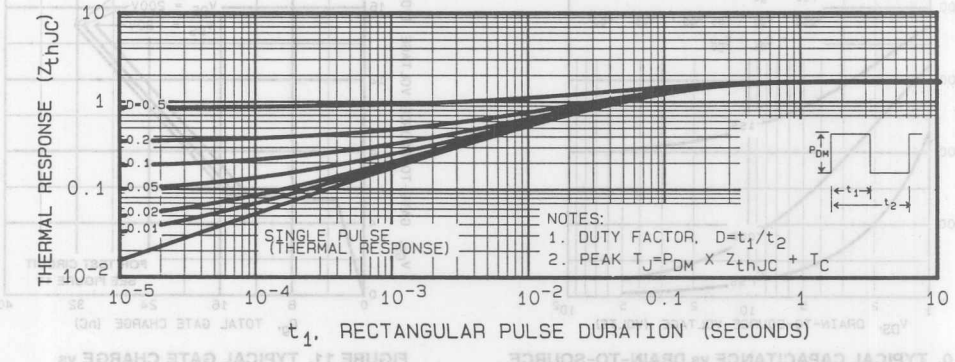


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

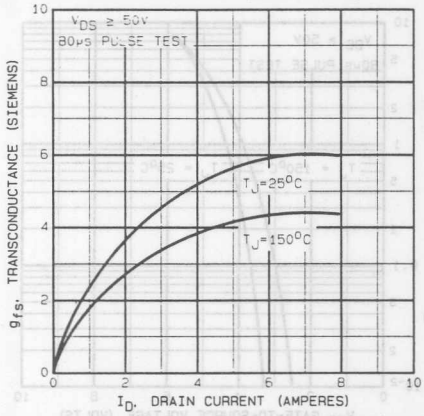


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

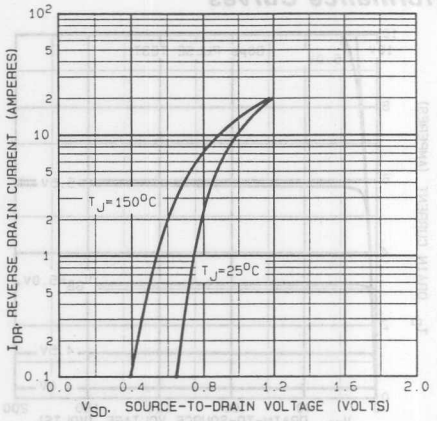


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

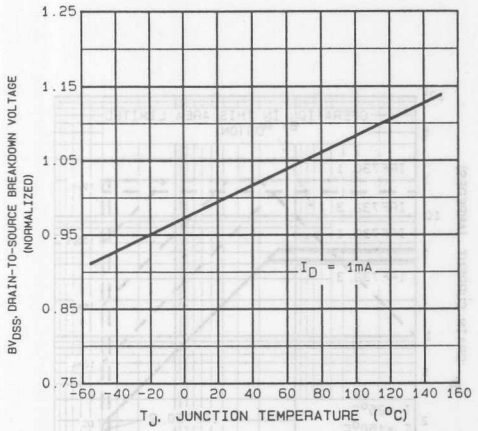


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

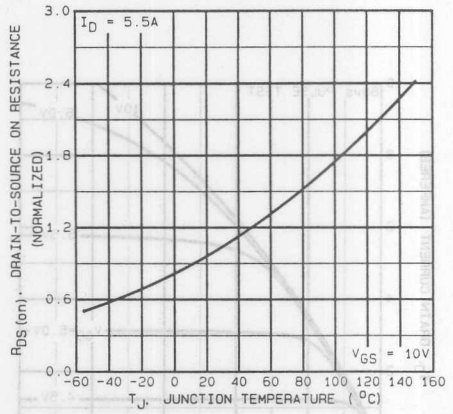


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

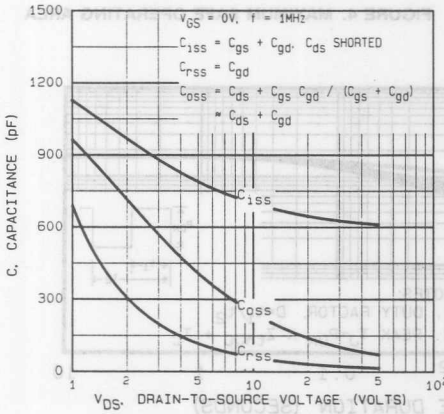


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

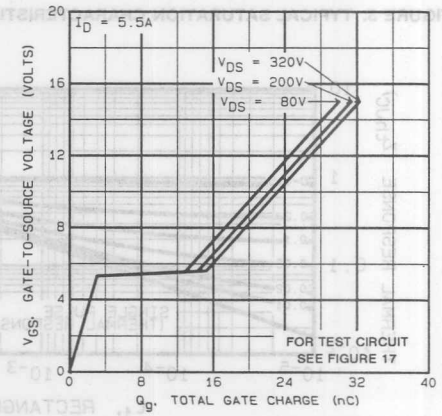


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

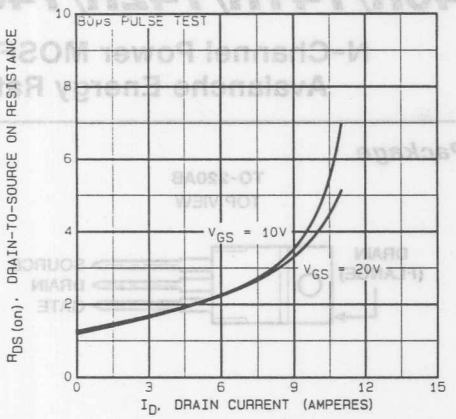


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

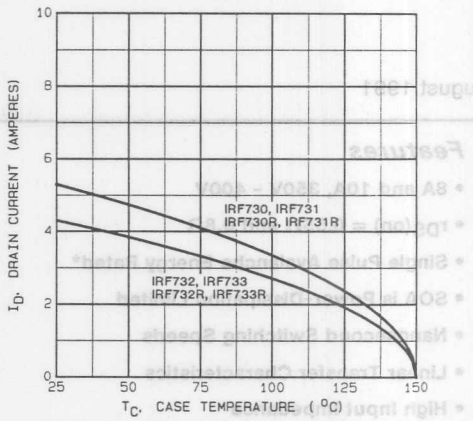


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

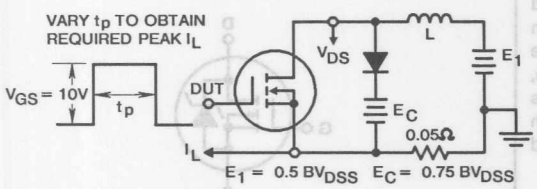


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

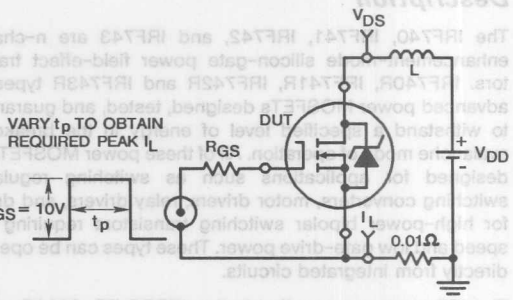


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

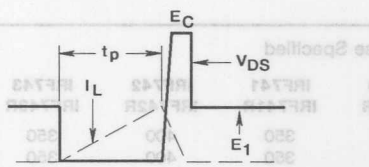


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

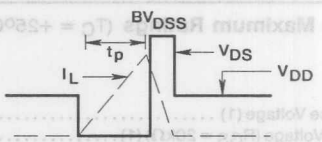


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

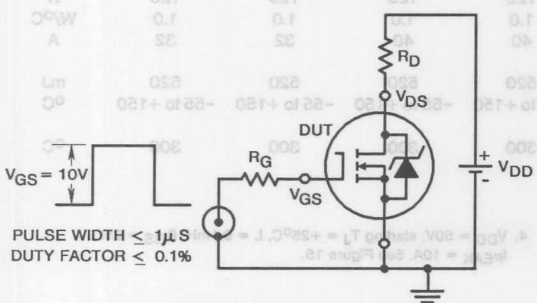


FIGURE 16. SWITCHING TIME TEST CIRCUIT

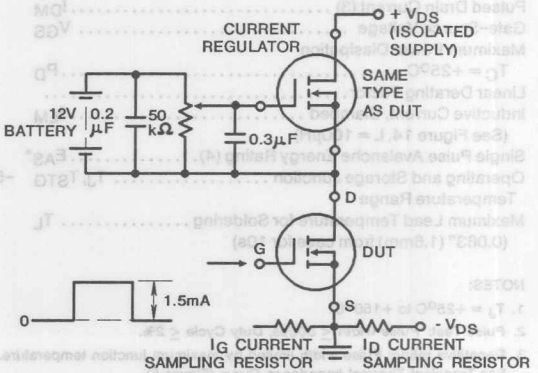


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF740/741/742/743
IRF740R/741R/742R/743R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 8A and 10A, 350V - 400V
- $r_{DS}(on)$ = 0.55Ω and 0.8Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

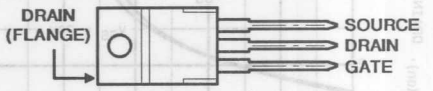
Description

The IRF740, IRF741, IRF742, and IRF743 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF740R, IRF741R, IRF742R and IRF743R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

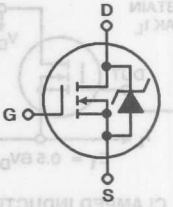
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF740 IRF740R	IRF741 IRF741R	IRF742 IRF742R	IRF743 IRF743R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	10	10	8.0	8.0	A
T_C = +100°C ..... I_D	6.3	6.3	5.2	5.2	A
Pulsed Drain Current (3) ..... I_{DM}	40	40	33	33	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	40	40	32	32	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	520	520	520	520	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 9.1mH, R_{GS} = 25Ω, I_{PEAK} = 10A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

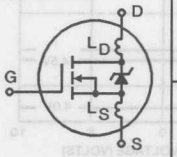
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File Number 2311.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

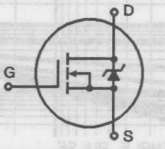
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF740/742, IRF740R/742R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	-	-	V
IRF741/743, IRF741R/743R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF740/741, IRF740R/741R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V	10	-	-	A
IRF742/743, IRF742R/743R			8.3	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF740/741, IRF740R/741R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.2A	-	0.47	0.55	Ω
IRF742/743, IRF742R/743R			-	0.68	0.80	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 5.2A	5.8	8.9	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	1250	-	pF
Output Capacitance	C_{OSS}		-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	80	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 10A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	15	21	ns
Rise Time	t_r		-	25	41	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	52	75	ns
Fall Time	t_f		-	25	36	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	41	63	nC
Gate-Source Charge	Q_{gs}		-	6.5	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	23	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W

Modified MOSFET symbol showing the internal device inductances.



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	10	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	40	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 10A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 10A, dI_F/dt = 100A/μs	170	390	790	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 10A, dI_F/dt = 100A/μs	1.6	4.5	8.2	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 9.1mH, R_{GS} = 25Ω, I_{PEAK} = 10A (See Figure 15)

Performance Curves

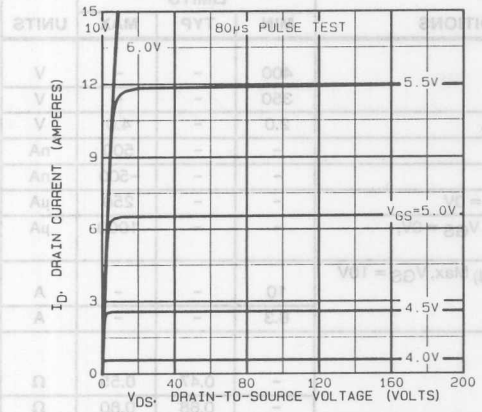


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

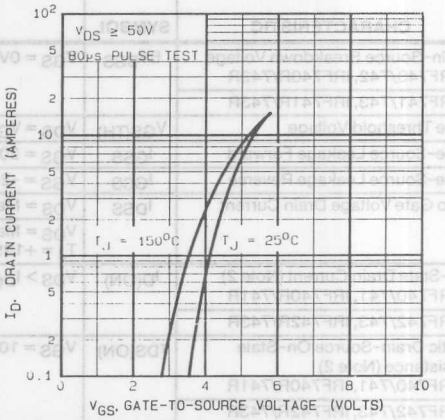


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

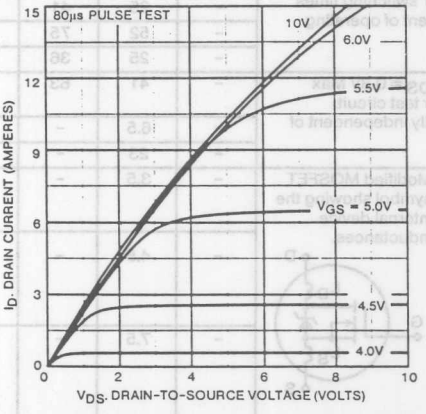


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

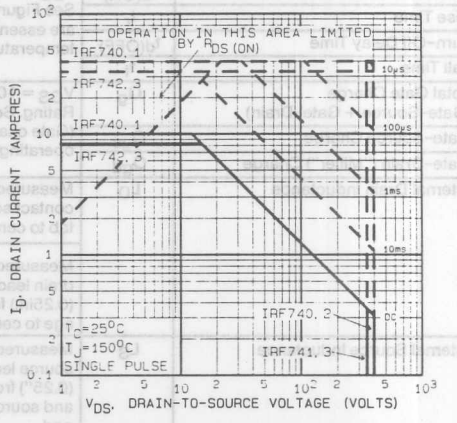


FIGURE 4. MAXIMUM SAFE OPERATING AREA

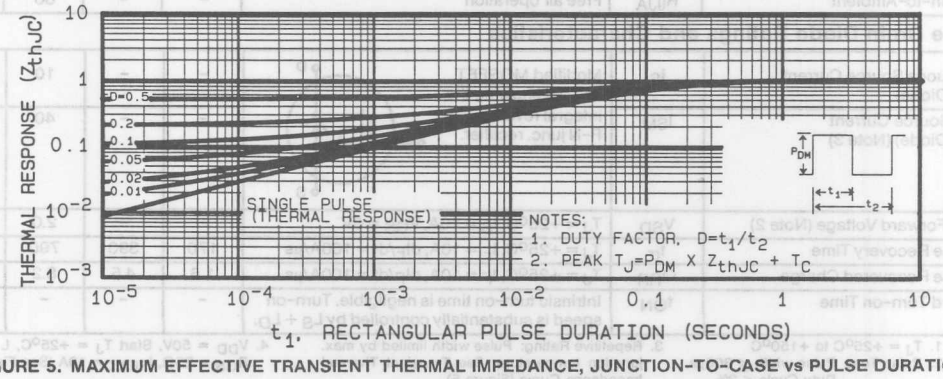


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

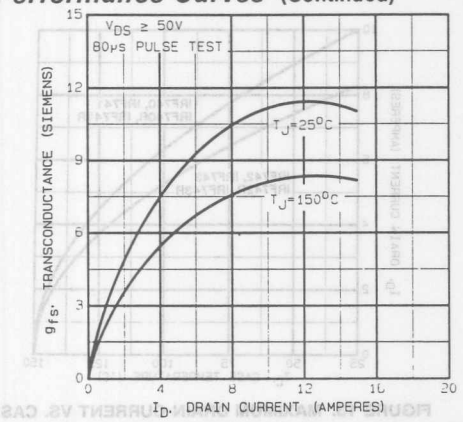


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

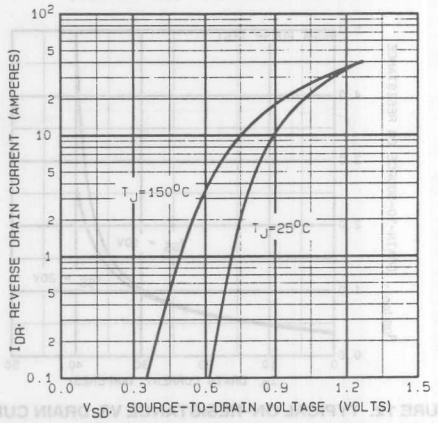


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

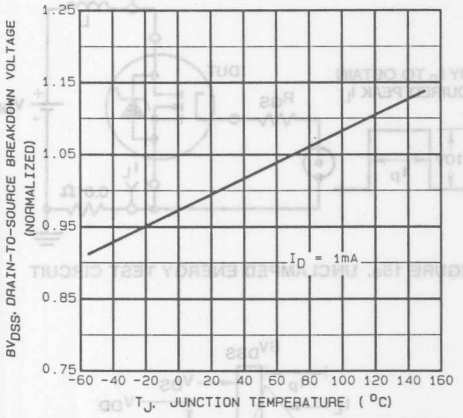


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

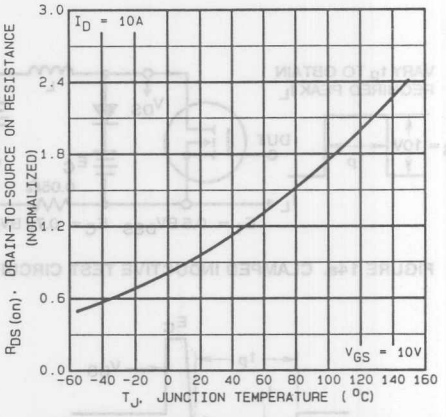


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

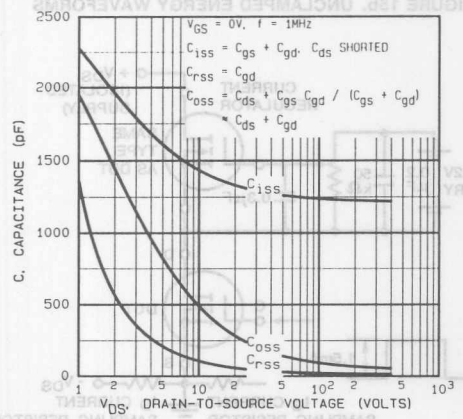


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

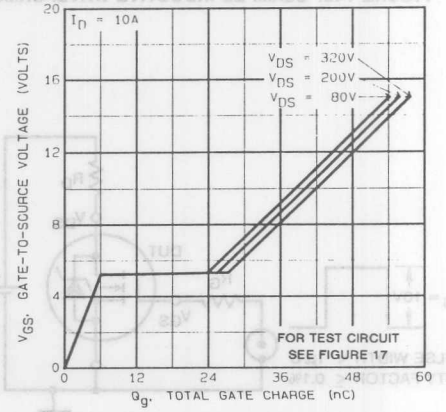


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

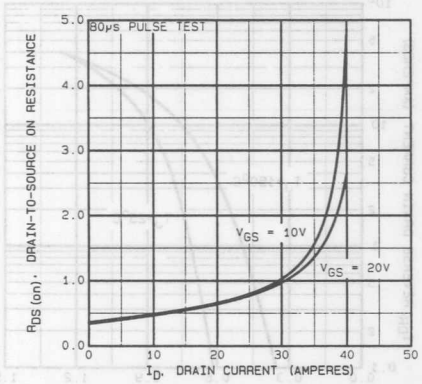


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

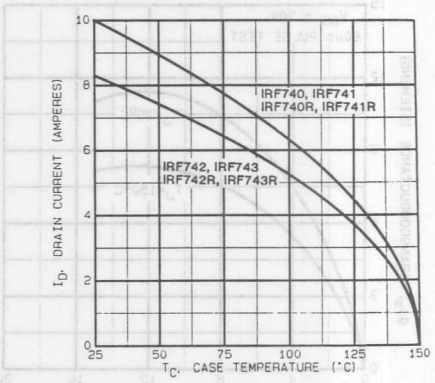


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

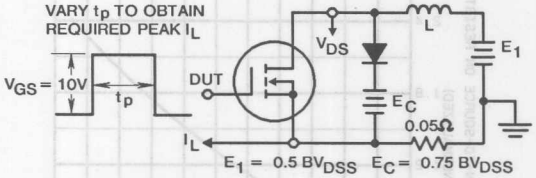


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

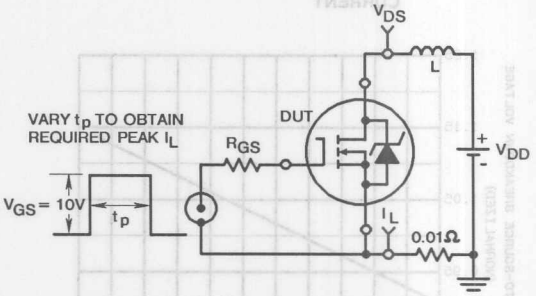


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

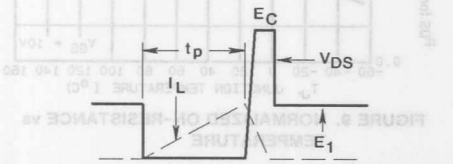


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

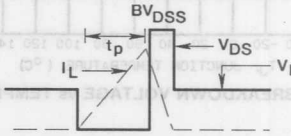


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

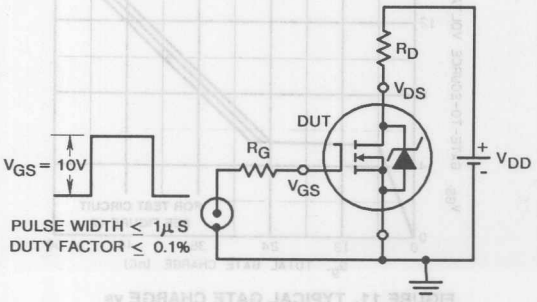


FIGURE 16. SWITCHING TIME TEST CIRCUIT

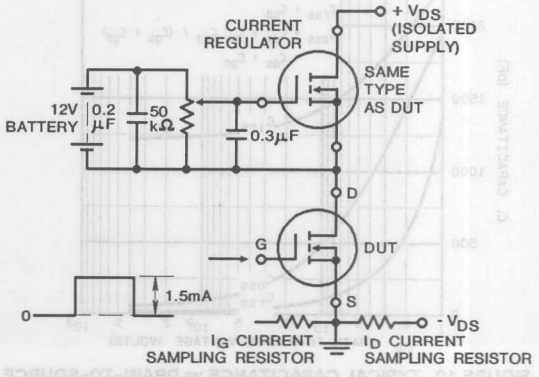


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF820/821/822/823
IRF820R/821R/822R/823R

N-Channel Power MOSFETs
Avalanche Energy Rated*

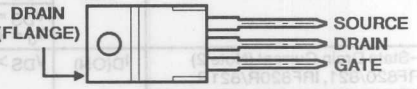
August 1991

Features

- 2.2 and 2.5A, 450V - 500V
- $r_{DS}(on)$ = 3.0Ω and 4.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-220AB
TOP VIEW



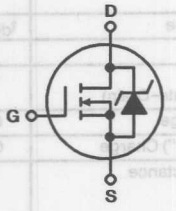
Description

The IRF820, IRF821, IRF822, and IRF823 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF820R, IRF821R, IRF822R and IRF823R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4

N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF820 IRF820R	IRF821 IRF821R	IRF822 IRF822R	IRF823 IRF823R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	2.5	2.5	2.0	2.0	A
T_C = +100°C ..... I_D	1.6	1.6	1.4	1.4	A
Pulsed Drain Current (3) ..... I_{DM}	8.0	8.0	7.0	7.0	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	50	50	50	50	W
Linear Derating Factor	0.40	0.40	0.40	0.40	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	10	10	8.0	8.0	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	210	210	210	210	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 60mH, R_{GS} = 25Ω, I_{PEAK} = 2.5A. See Figure 15.

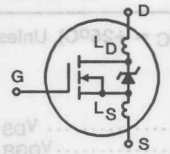
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1581.1

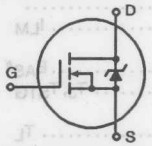
Drain-Source Breakdown Voltage IRF820/822, IRF820R/822R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500	–	–	V
IRF821/823, IRF821R/823R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF820/821, IRF820R/821R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V	2.5	–	–	A
IRF822/823, IRF822R/823R			2.2	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF820/821, IRF820R/821R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.4A	–	2.5	3.0	Ω
IRF822/823, IRF822R/823R			–	3.0	4.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 1.4A	1.5	2.3	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	360	–	pF
Output Capacitance	C_{OSS}		–	60	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	10	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 2.5A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	11	15	ns
Rise Time	t_r		–	11	18	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	29	42	ns
Fall Time	t_f		–	12	18	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 2.5A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	12	19	nC
Gate-Source Charge	Q_{gs}		–	2.5	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	6.0	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	2.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Modified MOSFET symbol showing the internal device inductances.



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	2.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	8.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.5A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 2.5A, dI_F/dt = 100A/μs	130	300	540	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 2.5A, dI_F/dt = 100A/μs	0.57	1.4	2.3	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES:
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 60mH, R_{GS} = 25Ω, I_{PEAK} = 2.5A (See Figure 15)

Performance Curves

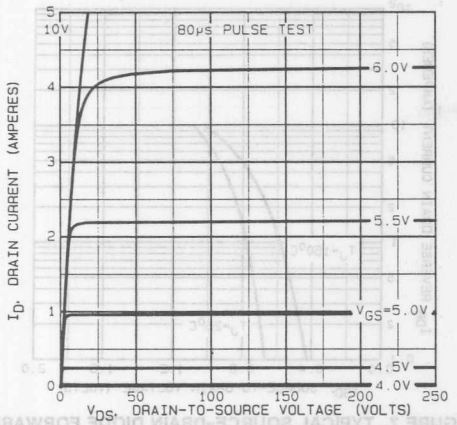


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

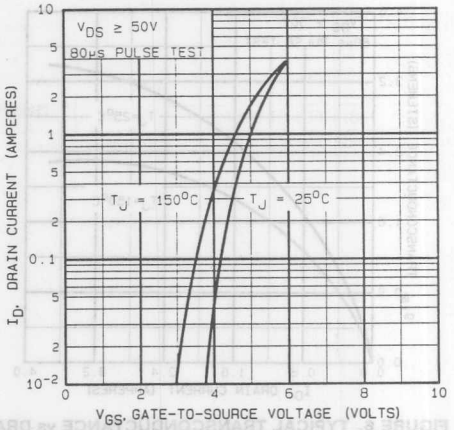


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

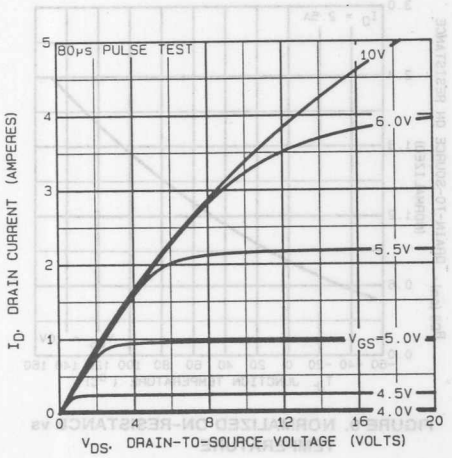


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

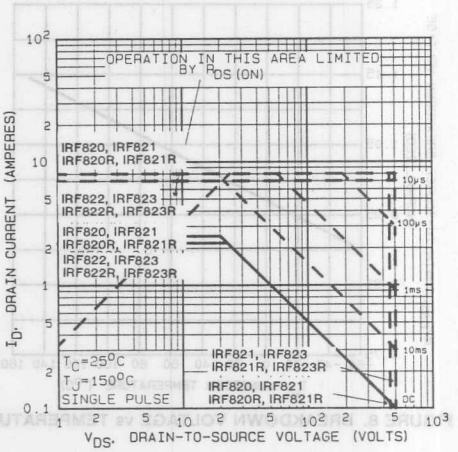


FIGURE 4. MAXIMUM SAFE OPERATING AREA

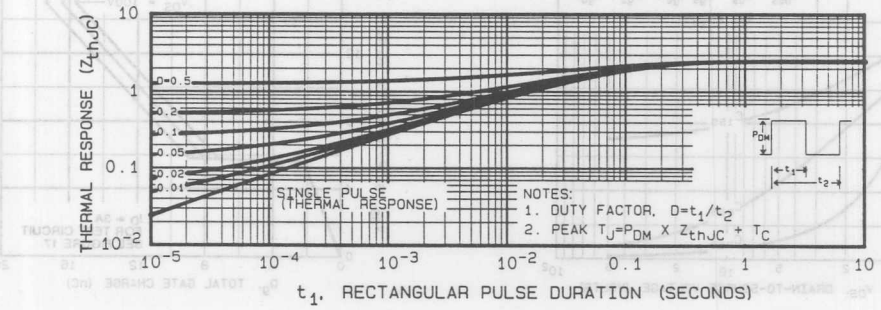


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

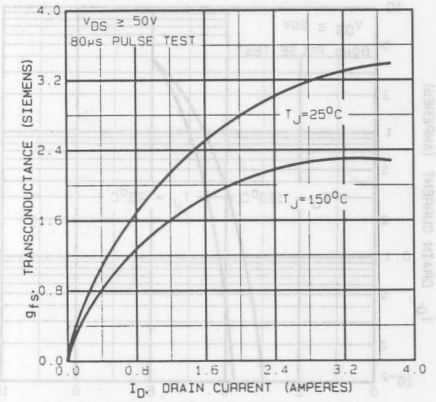


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

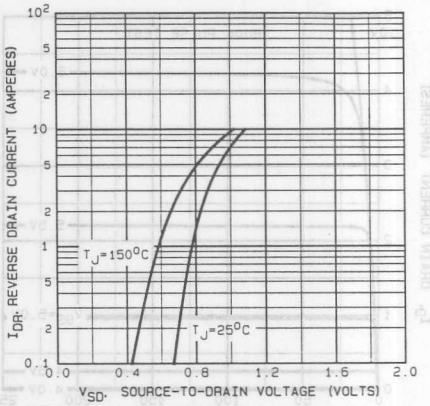


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

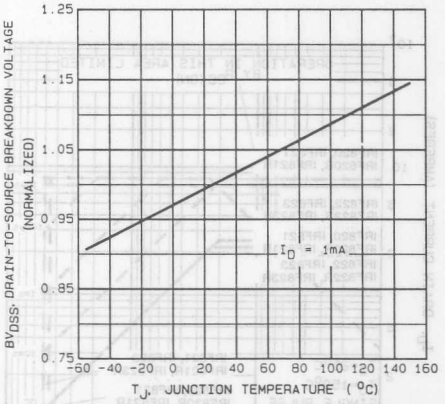


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

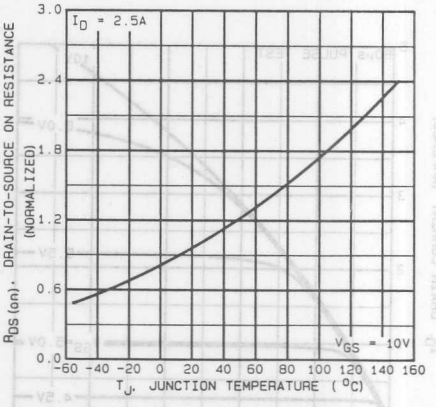


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

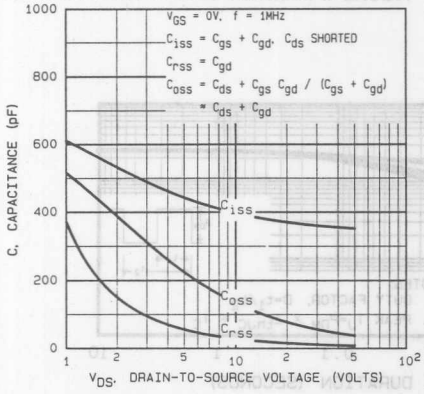


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

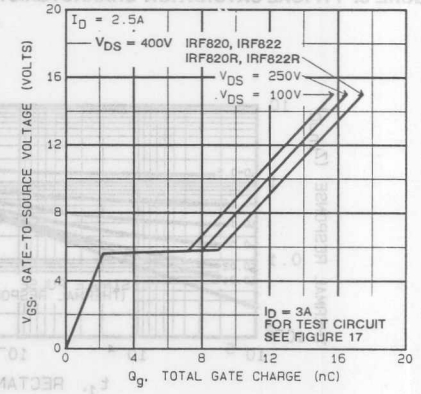


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

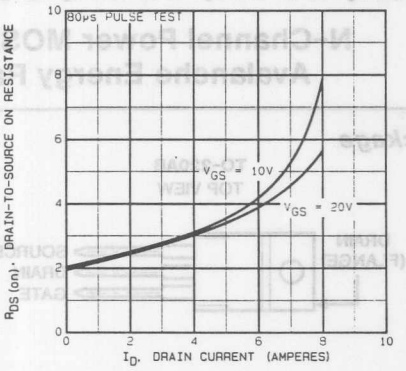


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

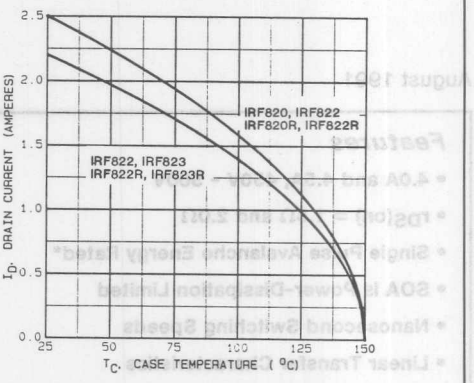


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

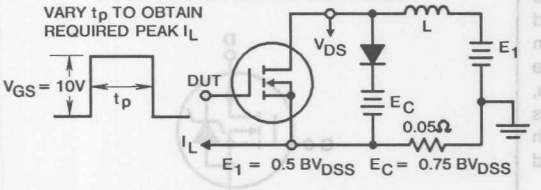


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

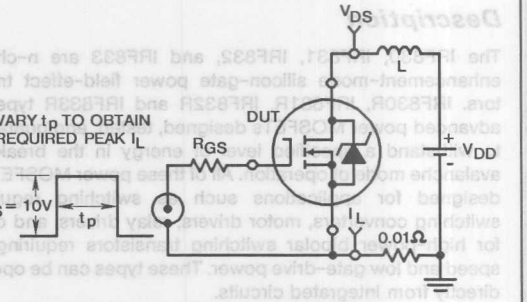


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

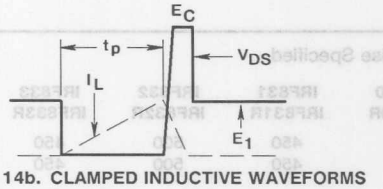


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

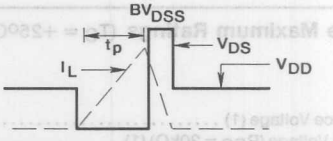


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

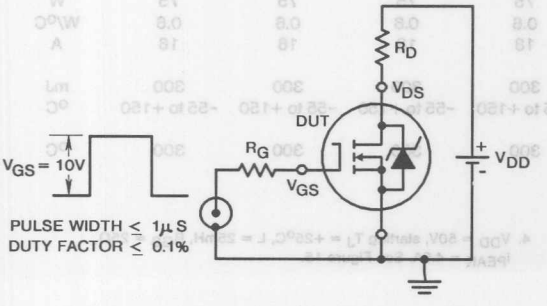


FIGURE 16. SWITCHING TIME TEST CIRCUIT

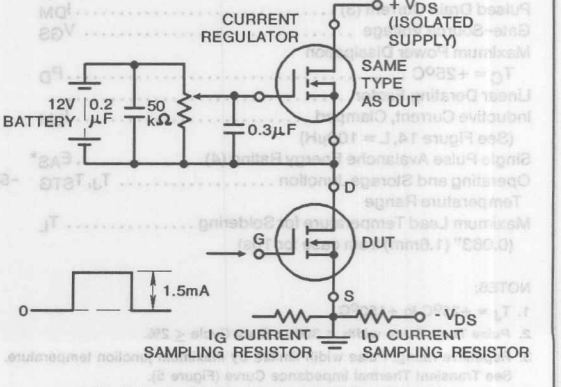


FIGURE 17. GATE CHARGE TEST CIRCUIT

4 N-CHANNEL POWER MOSFETs

HARRIS

IRF830/831/832/833
IRF830R/831R/832R/833R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 4.0A and 4.5A, 450V - 500V
- $r_{DS}(on)$ = 1.5Ω and 2.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

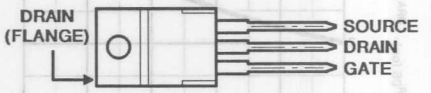
Description

The IRF830, IRF831, IRF832, and IRF833 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF830R, IRF831R, IRF832R and IRF833R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF830 IRF830R	IRF831 IRF831R	IRF832 IRF832R	IRF833 IRF833R	UNITS
Drain-Source Voltage (1)	V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	500	450	500	450	V
Continuous Drain Current						
T_C = +25°C	I_D	4.5	4.5	4.0	4.0	A
T_C = +100°C	I_D	3.0	3.0	2.5	2.5	A
Pulsed Drain Current (3)	I_{DM}	18	18	16	16	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	75	75	75	75	W
Linear Derating Factor		0.6	0.6	0.6	0.6	W/°C
Inductive Current, Clamped (See Figure 14, L = 100μH)	I_{LM}	18	18	16	16	A
Single Pulse Avalanche Energy Rating (4)	E_{AS}*	300	300	300	300	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 25mH, R_{GS} = 25Ω, I_{PEAK} = 4.5A. See Figure 15.

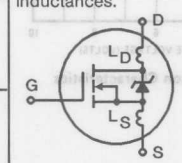
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1582.1

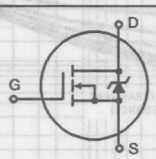
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF830/832, IRF830R/832R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500	-	-	V
IRF831/833, IRF831R/833R			450	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF830/831, IRF830R/831R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V	4.5	-	-	A
IRF832/833, IRF832R/833R			4.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF830/831, IRF830R/831R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 2.5A	-	1.3	1.5	Ω
IRF832/833, IRF832R/833R			-	1.5	2.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 2.5A	2.7	4.2	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	20	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 4.5A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	10	17	ns
Rise Time	t_r		-	15	23	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	33	53	ns
Fall Time	t_f		-	16	23	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 4.5A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	22	32	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	11	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	4.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	18	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 4.5A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 4.5A, dI_F/dt = 100A/μs	180	350	760	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 4.5A, dI_F/dt = 100A/μs	0.96	2.2	4.3	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 25mH, R_{GS} = 25Ω, I_{PEAK} = 4.5A (See Figure 15)

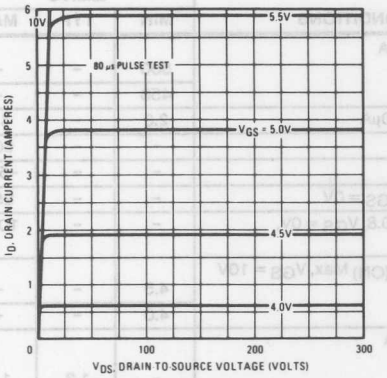


Fig. 1 – Typical Output Characteristics

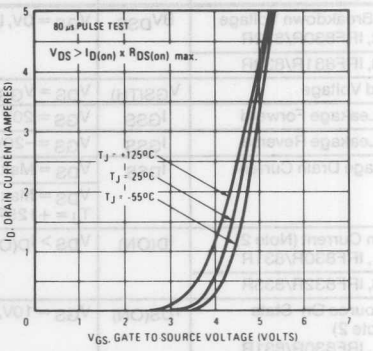


Fig. 2 – Typical Transfer Characteristics

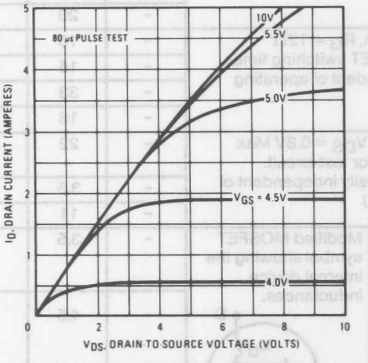


Fig. 3 – Typical Saturation Characteristics

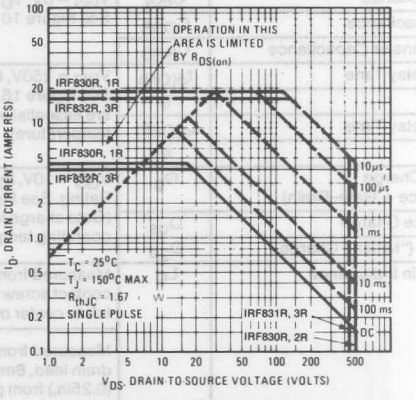


Fig. 4 – Maximum Safe Operating Area

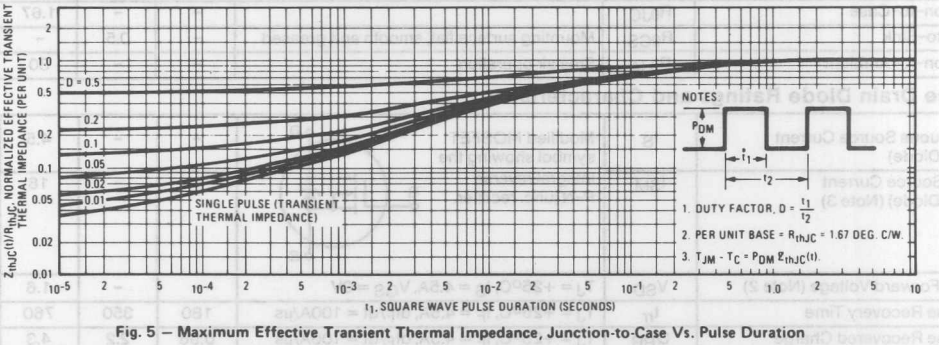


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

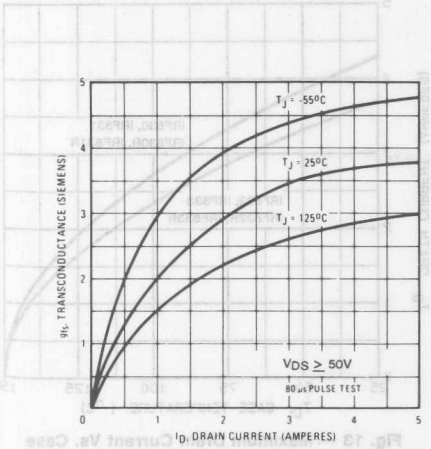


Fig. 6 – Typical Transconductance Vs. Drain Current

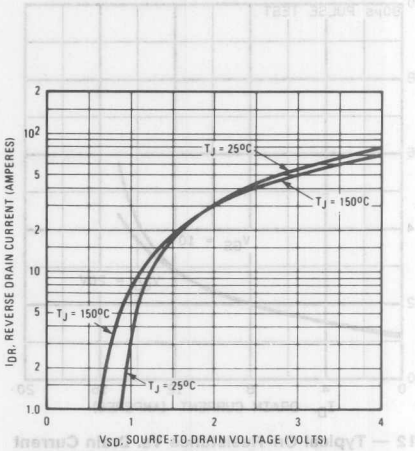


Fig. 7 – Typical Source-Drain Diode Forward Voltage

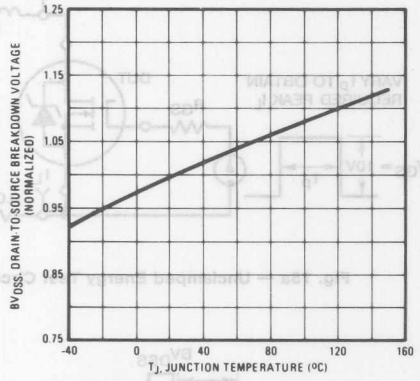


Fig. 8 – Breakdown Voltage Vs. Temperature

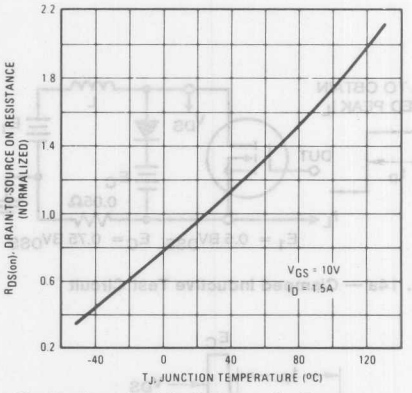


Fig. 9 – Normalized On-Resistance Vs. Temperature

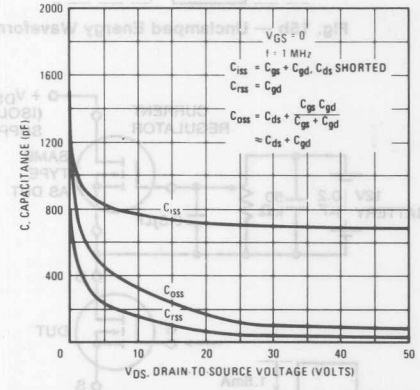


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

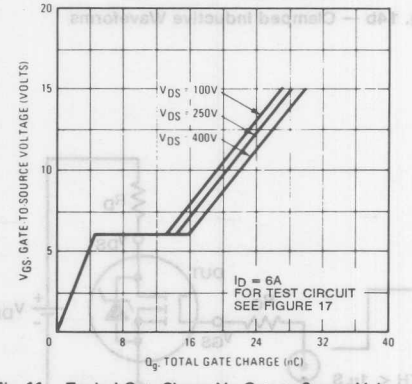


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

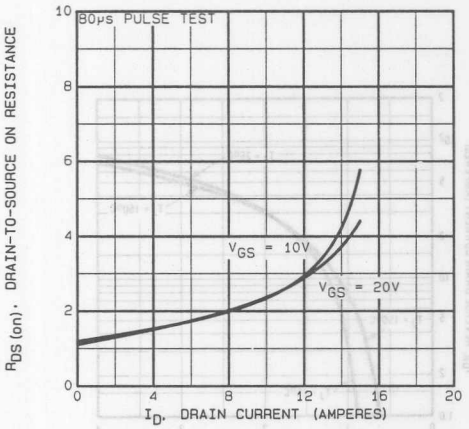


Fig. 12 — Typical On-Resistance Vs. Drain Current

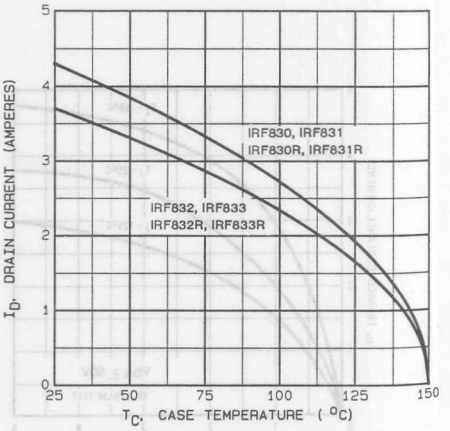


Fig. 13 — Maximum Drain Current Vs. Case Temperature

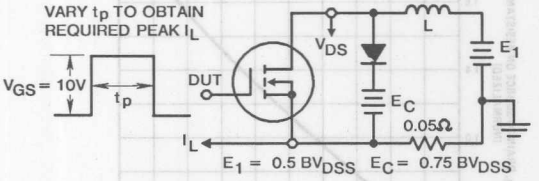


Fig. 14a — Clamped Inductive Test Circuit

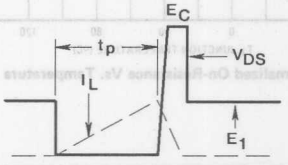


Fig. 14b — Clamped Inductive Waveforms

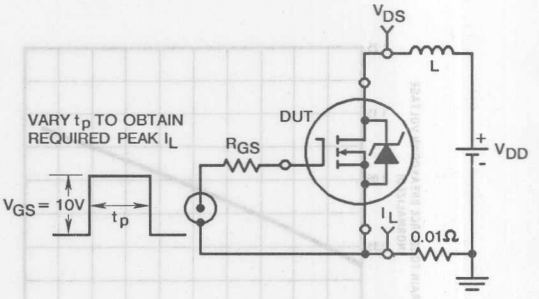


Fig. 15a — Unclamped Energy Test Circuit

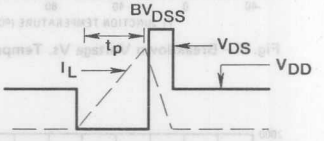


Fig. 15b — Unclamped Energy Waveforms

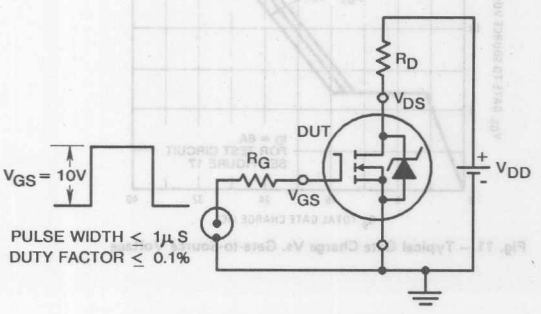


Fig. 16 — Switching Time Test Circuit

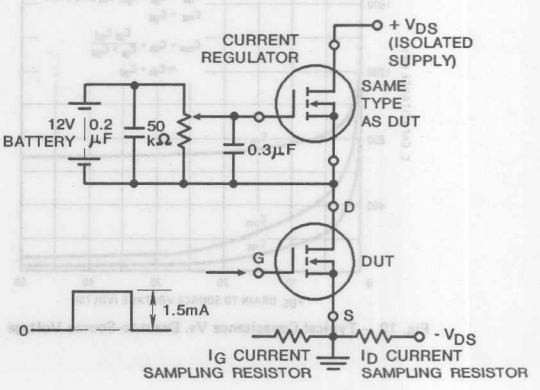


Fig. 17 — Gate Charge Test Circuit

IRF840/841/842/843
IRF840R/841R/842R/843R

N-Channel Power MOSFETs
Avalanche Energy Rated*

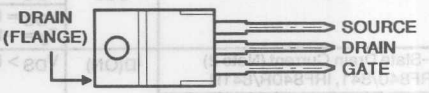
August 1991

Features

- 7A and 8A, 450V - 500V
- $r_{DS}(on)$ = 0.85Ω and 1.1Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-220AB
TOP VIEW



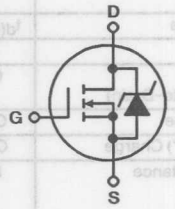
Description

The IRF840, IRF841, IRF842, and IRF843 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF840R, IRF841R, IRF842R and IRF843R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF840 IRF840R	IRF841 IRF841R	IRF842 IRF842R	IRF843 IRF843R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	8.0	8.0	7.0	7.0	A
T_C = +100°C ..... I_D	5.1	5.1	4.4	4.4	A
Pulsed Drain Current (3) ..... I_{DM}	32	32	28	28	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	32	32	28	28	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	510	510	510	510	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 14mH, R_{GS} = 25Ω, I_{PEAK} = 8A. See Figure 15.

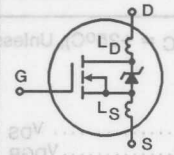
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2312.1

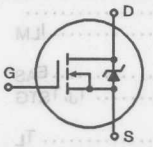
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF840/842, IRF840R/842R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	-	-	V
IRF841/843, IRF841R/843R			450	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRF840/841, IRF840R/841R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V	8.0	-	-	A
IRF842/843, IRF842R/843R			7.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF840/841, IRF840R/841R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.4A	-	0.8	0.85	Ω
IRF842/843, IRF842R/843R			-	1.0	1.1	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 4.4A	4.9	7.4	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	1225	-	pF
Output Capacitance	C_{OSS}		-	200	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	85	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D ≃ 8A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	15	21	ns
Rise Time	t_r		-	21	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	74	ns
Fall Time	t_f		-	20	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	42	63	nC
Gate-Source Charge	Q_{gs}		-	7.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	22	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	8.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.0A, V_{GS} = 100A/µs	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 8.0A, dI_F/dt = 100A/µs	210	475	970	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 8.0A, dI_F/dt = 100A/µs	2.0	4.6	8.2	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width < 300µs, Duty Cycle < 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 14mH, R_{GS} = 25Ω, I_{PEAK} = 8A (See Figure 15)

Performance Curves

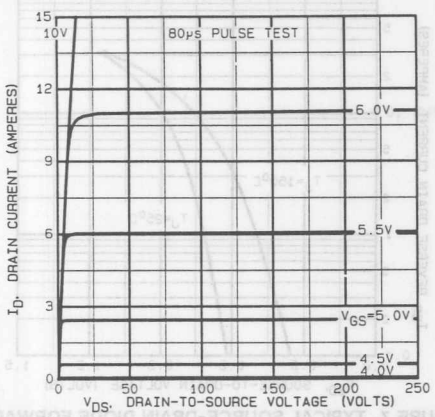


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

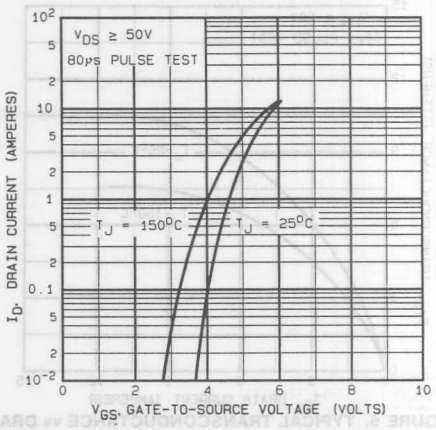


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

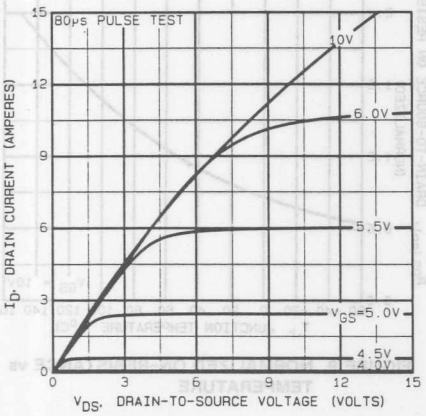


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

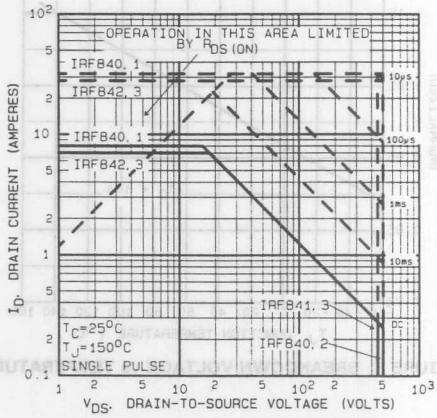


FIGURE 4. MAXIMUM SAFE OPERATING AREA

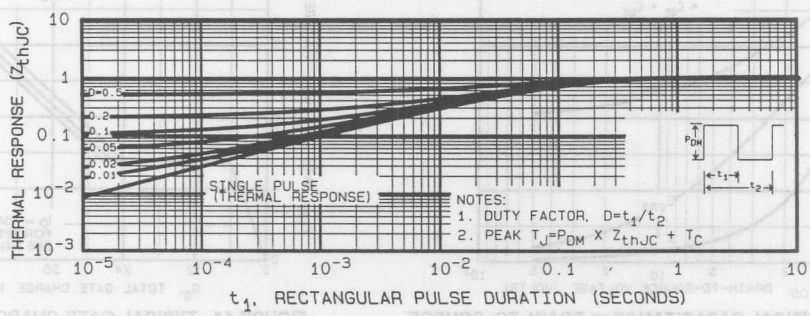


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

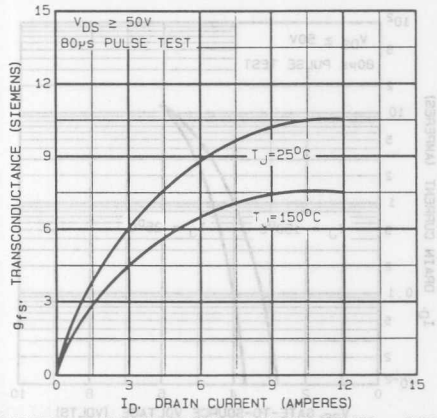


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

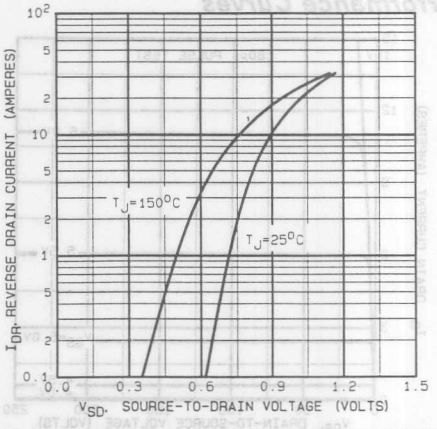


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

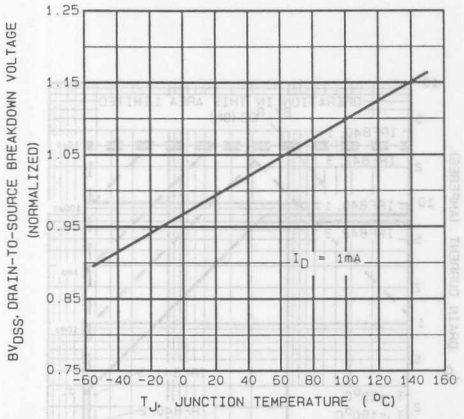


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

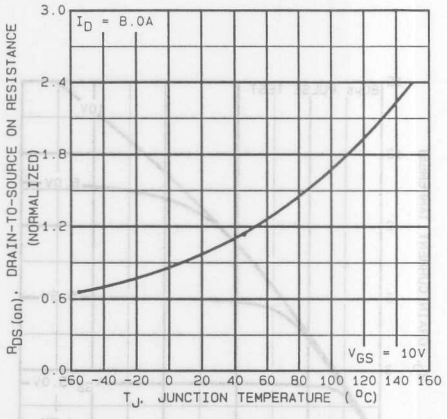


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

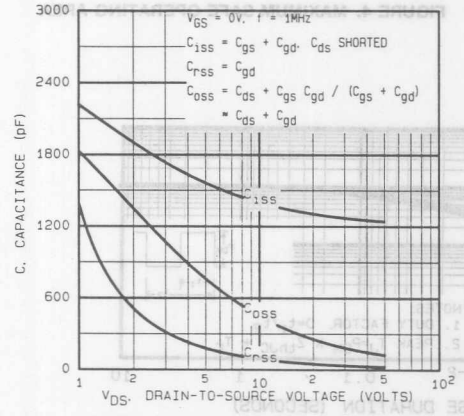


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

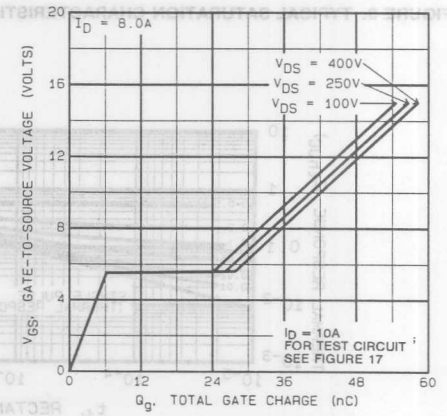


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

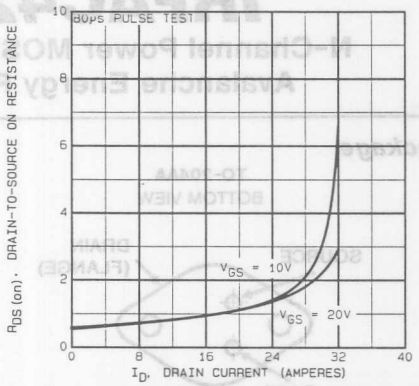


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

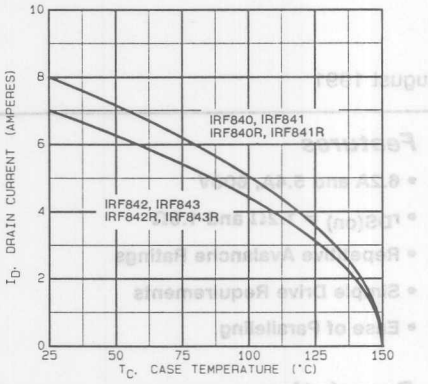


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

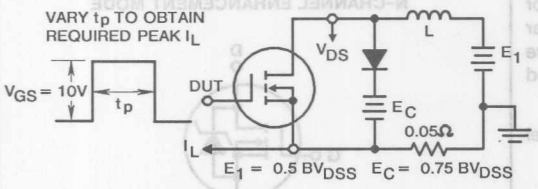


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

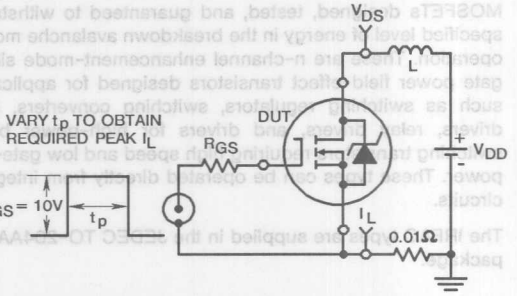


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

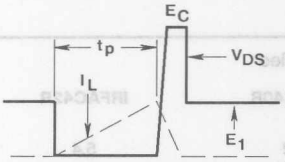


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

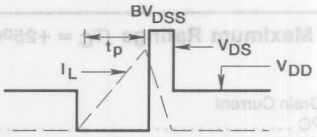


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

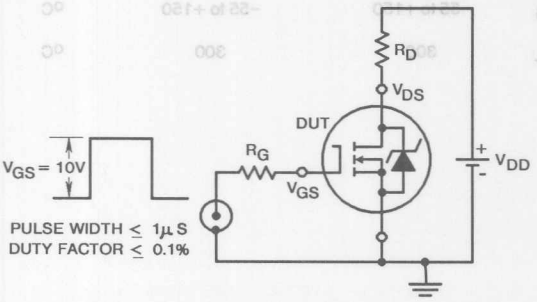


FIGURE 16. SWITCHING TIME TEST CIRCUIT

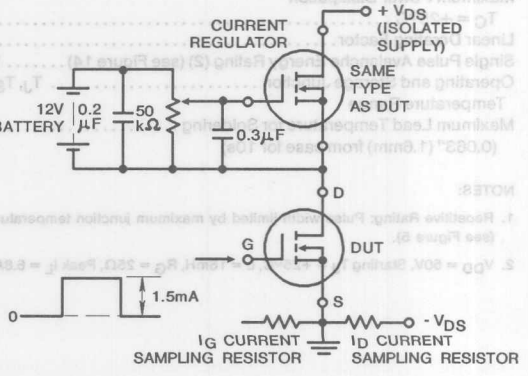


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRFAC40R
IRFAC42R

N-Channel Power MOSFETs
Avalanche Energy Rated

August 1991

Features

- 6.2A and 5.4A, 600V
- $r_{DS(on)}$ = 1.2Ω and 1.6Ω
- Repetitive Avalanche Ratings
- Simple Drive Requirements
- Ease of Paralleling

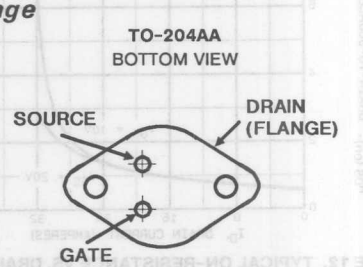
Description

The IRFAC40R and IRFAC42R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFAC types are supplied in the JEDEC TO-204AA steel package.

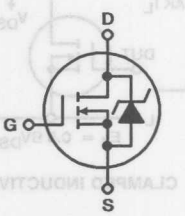
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFAC40R	IRFAC42R	UNITS
Continuous Drain Current			
T_C = +25°C ..... I_D	6.2	5.4	A
T_C = +100°C ..... I_D	3.9	3.4	A
Pulsed Drain Current (1) ..... I_{DM}	25	22	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = +25°C ..... P_D	125	125	W
Linear Derating Factor	1.0	1.0	W/°C
Single Pulse Avalanche Energy Rating (2) (see Figure 14) ..... E_{as}	570	570	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	°C

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature (see Figure 5).
2. V_{DD} = 50V, Starting T_J = +25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFAC40R IRFAC42R	600	—	—	V	V_{GS} = 0V, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFAC40R IRFAC42R	— —	0.97 1.2	1.2 1.6	Ω	V_{GS} = 10V, I_D = 3.4A
$I_{D(on)}$	On-State Drain Current ③	IRFAC40R IRFAC42R	6.2 5.4	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance ③	ALL	4.7	70	—	S(℧)	$V_{DS} \geq$ 50V, I_{DS} = 3.4A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	— —	— —	250 1000	μA	V_{DS} = Max. Rating, V_{GS} = 0V V_{DS} = 0.8 x Max. Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
Q_g	Total Gate Charge	ALL	—	40	60	nC	V_{GS} = 10V, I_D = 6.2A
Q_{gs}	Gate-to-Source Charge	ALL	—	5.5	—	nC	V_{DS} = 0.8 x Max. Rating
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	—	20	—	nC	See Fig. 16 (Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	—	13	20	ns	V_{DD} = 300V, I_D = 6.2A, R_G = 9.1Ω
t_r	Rise Time	ALL	—	18	27	ns	R_D = 47Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	55	83	ns	See Fig. 15
t_f	Fall Time	ALL	—	20	30	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	13	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	1300	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	—	160	—	pF	f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	30	—	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.12	—	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Typical-socket mount

Modified MOSFET symbol showing the internal inductances.



Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	—	—	6.2	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifer.
I_{SM}	Pulse Source Current (Body Diode) ①	ALL	—	—	25	A	
V_{SD}	Diode Forward Voltage ③	ALL	—	—	1.5	V	T_J = 25°C, I_S = 6.2A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	200	450	940	ns	T_J = 25°C, I_F = 6.2A, di/dt = 100A/μs
Q_{RR}	Reverse Recovery Charge	ALL	1.8	3.8	7.9	μC	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 5).

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A

③ Pulse width ≤ 300μs; Duty Cycle ≤ 2%

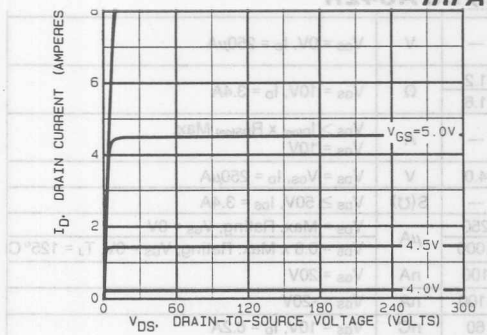


Fig. 1 - Typical Output Characteristics

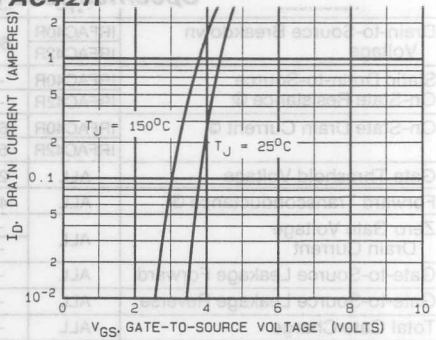


Fig. 2 - Typical Transfer Characteristics

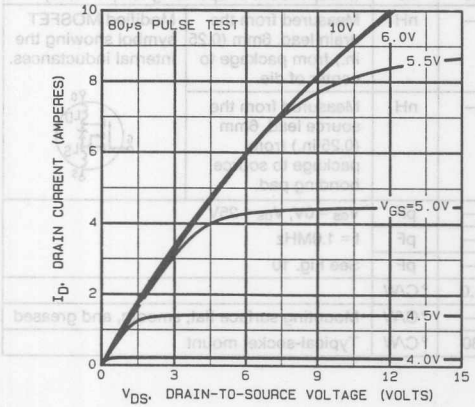


Fig. 3 - Typical Saturation Characteristics

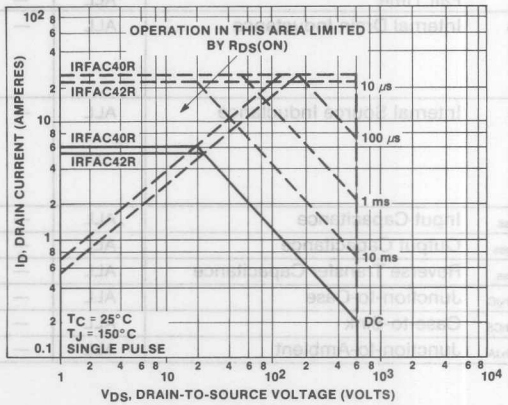


Fig. 4 - Maximum Safe Operating Area

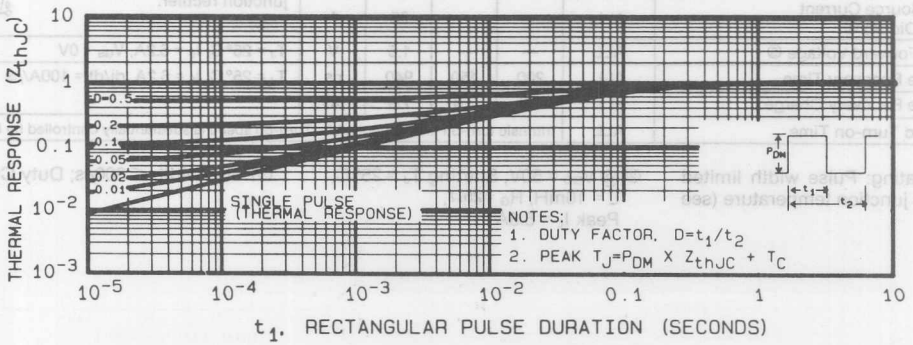


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

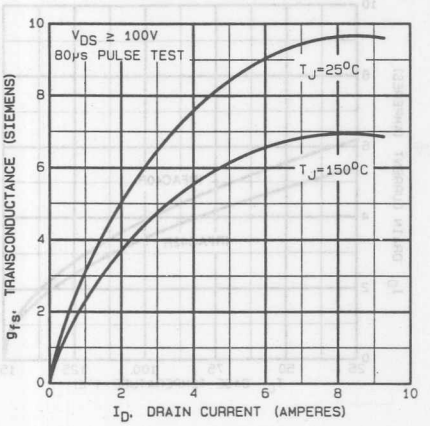


Fig. 6 - Typical Transconductance Vs. Drain Current

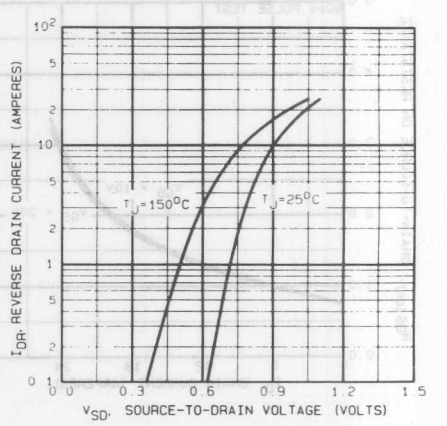


Fig. 7 - Typical Source-Drain Diode Forward Voltage

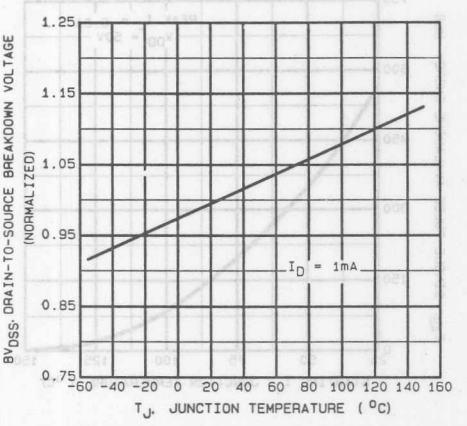


Fig. 8 - Breakdown Voltage Vs. Temperature

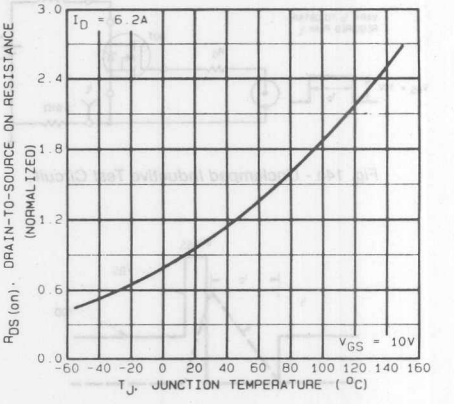


Fig. 9 - Normalized On-Resistance Vs. Temperature

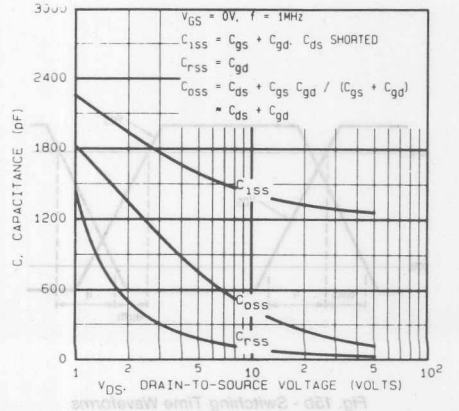


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

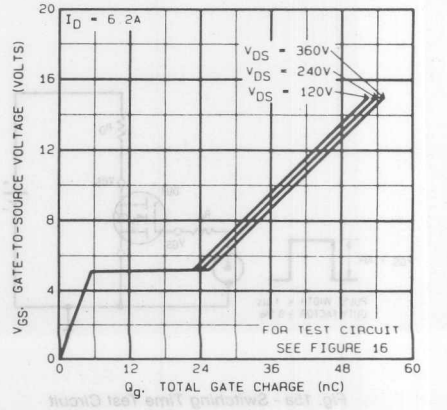


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

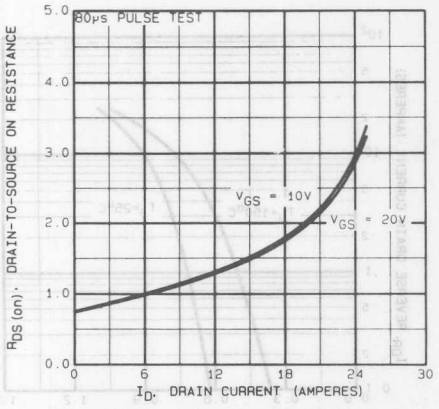


Fig. 12 - Typical On-Resistance Vs. Drain Current

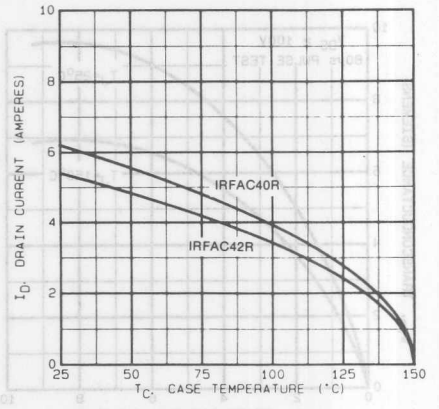


Fig. 13 - Maximum Drain Current Vs. Case Temperature

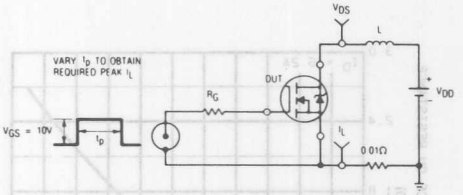


Fig. 14a - Unclamped Inductive Test Circuit

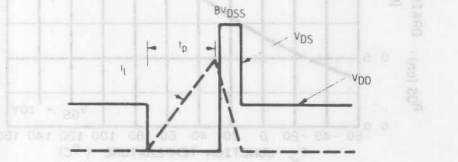


Fig. 14b - Unclamped Inductive Waveforms

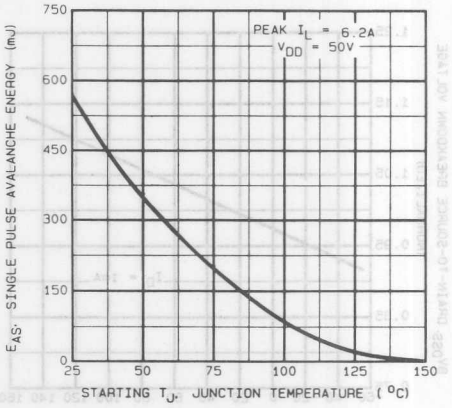


Fig. 14c - Maximum Avalanche Energy Vs. Starting Junction Temperature

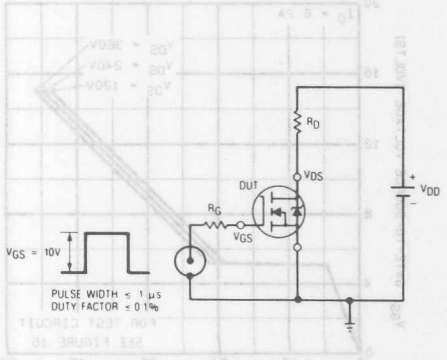


Fig. 15a - Switching Time Test Circuit

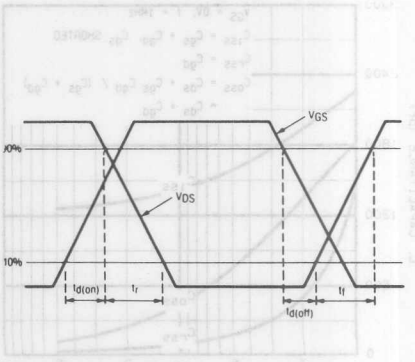


Fig. 15b - Switching Time Waveforms

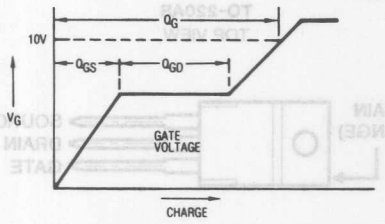
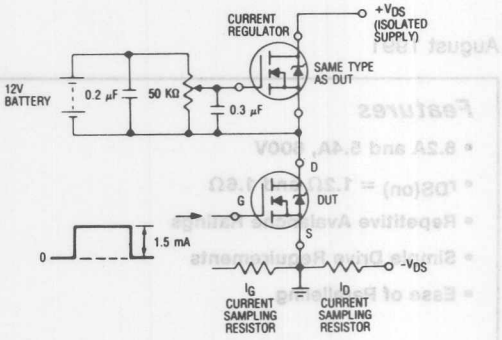


Fig. 16a - Basic Gate Charge Waveform



Fib. 16b - Gate Charge Test Circuit

HARRIS

IRFBC40R
IRFBC42R

N-Channel Power MOSFETs
Avalanche Energy Rated

August 1991

Features

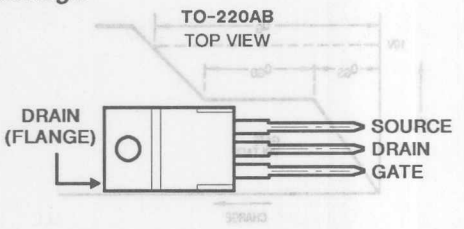
- 6.2A and 5.4A, 600V
- $r_{DS(on)}$ = 1.2Ω and 1.6Ω
- Repetitive Avalanche Ratings
- Simple Drive Requirements
- Ease of Paralleling

Description

The IRFBC40R and IRFBC42R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

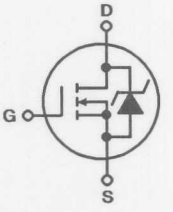
The IRFAC types are supplied in the JEDEC TO-220AB steel package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFBC40R	IRFBC42R	UNITS
Continuous Drain Current			
T_C = +25°C ..... I_D	6.2	5.4	A
T_C = +100°C ..... I_D	3.9	3.4	A
Pulsed Drain Current (1) ..... I_{DM}	25	22	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = +25°C ..... P_D	125	125	W
Linear Derating Factor	1.0	1.0	W/°C
Single Pulse Avalanche Energy Rating (2) (see Figure 14) ..... E_{as}	570	570	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	°C

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature (see Figure 5).
2. V_{DD} = 50V, Starting T_J = +25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

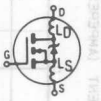
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File Number 2157.1

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFBC40R	600	—	—	V	V_{GS} = 0V, I_D = 250μA
		IRFBC42R					
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFBC40R	—	0.97	1.2	Ω	V_{GS} = 10V, I_D = 3.4A
		IRFBC42R	—	1.2	1.6		
$I_{D(on)}$	On-State Drain Current ③	IRFBC40R	6.2	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. V_{GS} = 10V
		IRFBC42R	5.4				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance ③	ALL	4.7	70	—	S(℧)	$V_{DS} \geq$ 100V, I_{DS} = 3.4A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000		V_{DS} = 0.8 x Max. Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
Q_g	Total Gate Charge	ALL	—	40	60	nC	V_{GS} = 10V, I_D = 6.2A
Q_{gs}	Gate-to-Source Charge	ALL	—	5.5	—	nC	V_{DS} = 0.7 x Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	—	20	—	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	—	13	20	ns	V_{DD} = 300V, I_D = 6.2A, R_G = 9.1Ω
t_r	Rise Time	ALL	—	18	27	ns	R_D = 47Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	55	83	ns	See Fig. 15
t_f	Fall Time	ALL	—	20	30	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	1300	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	—	160	—	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	45	—	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.50	—	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Typical-socket mount

Modified MOSFET symbol showing the internal inductances.



Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	—	—	6.2	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ①	ALL	—	—	25	A	
V_{SD}	Diode Forward Voltage ③	ALL	—	—	1.5	V	T_J = 25°C, I_S = 6.2A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	200	450	940	ns	T_J = 25°C, I_F = 6.2A, di/dt = 100A/μs
Q_{RR}	Reverse Recovery Charge	ALL	1.8	3.8	8.0	μC	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 5).

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A

③ Pulse width ≤ 300μs; Duty Cycle ≤ 2%

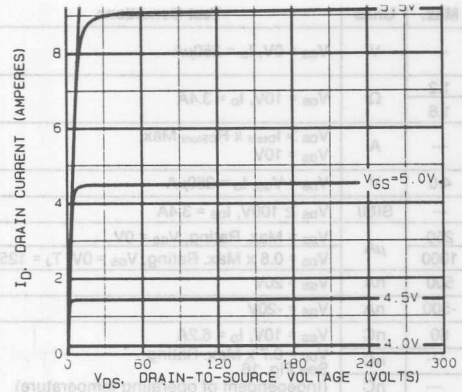


Fig. 1 - Typical Output Characteristics

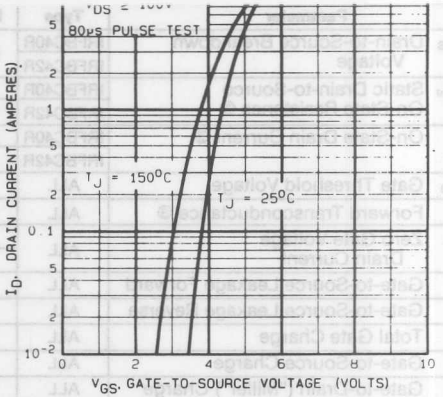


Fig. 2 - Typical Transfer Characteristics

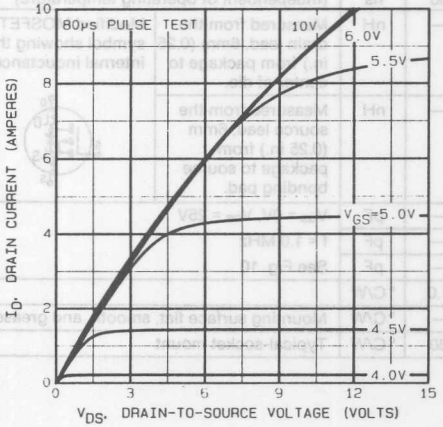


Fig. 3 - Typical Saturation Characteristics

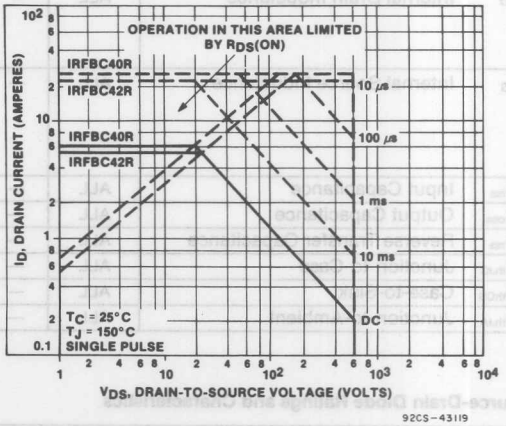


Fig. 4 - Maximum Safe Operating Area

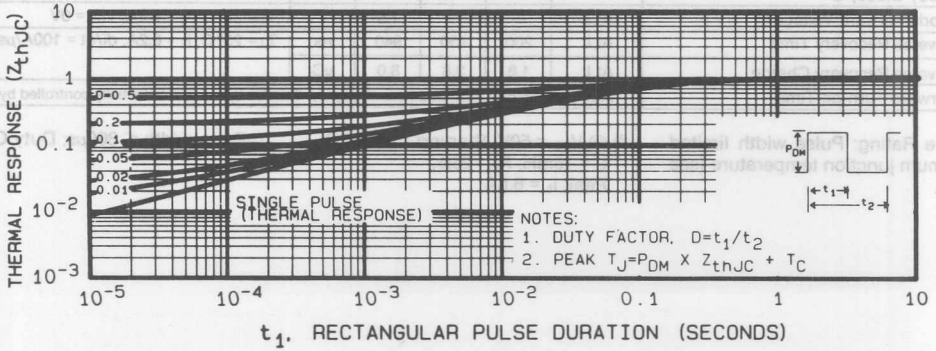


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

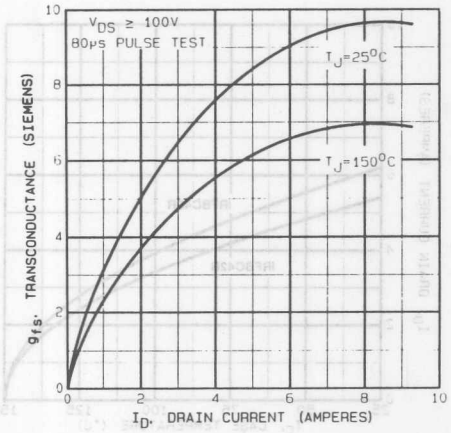


Fig. 6 - Typical Transconductance Vs. Drain Current

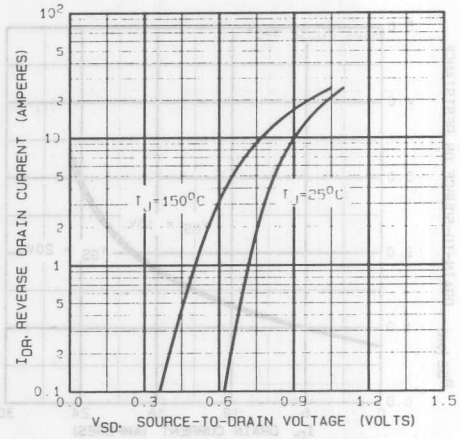


Fig. 7 - Typical Source-Drain Diode Forward Voltage

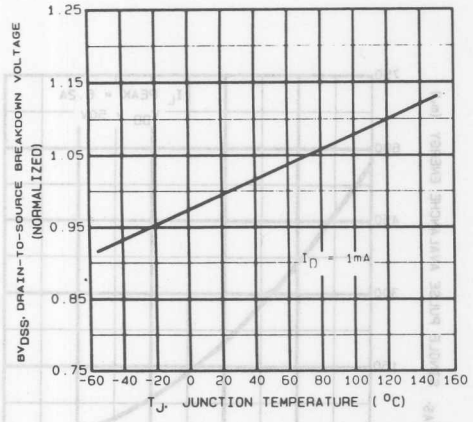


Fig. 8 - Breakdown Voltage Vs. Temperature

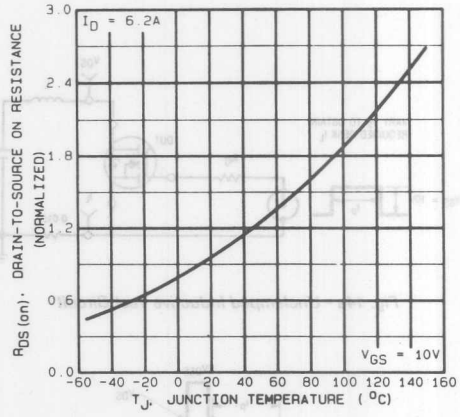


Fig. 9 - Normalized On-Resistance Vs. Temperature

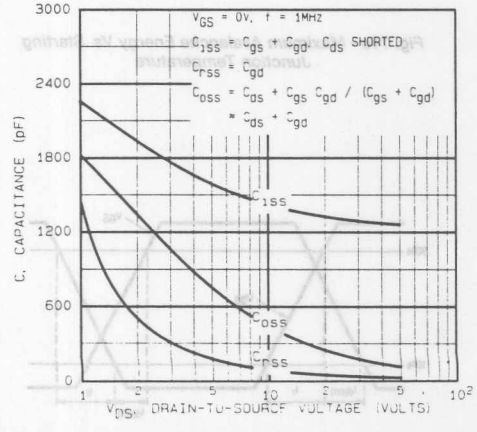


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

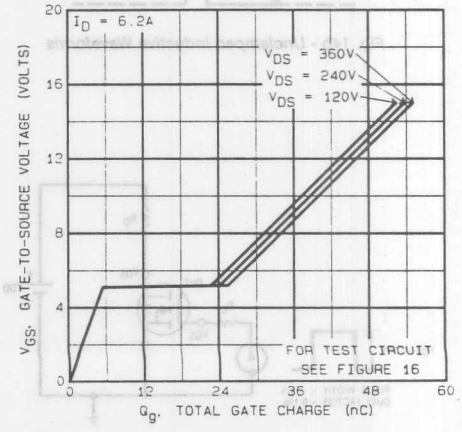


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

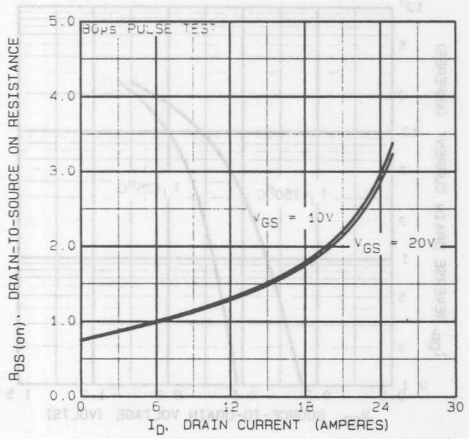


Fig. 12 - Typical On-Resistance Vs. Drain Current

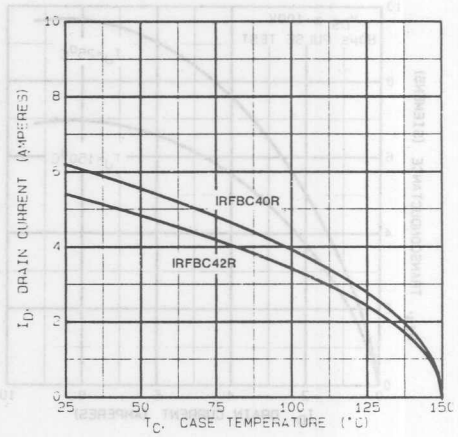


Fig. 13 - Maximum Drain Current Vs. Case Temperature

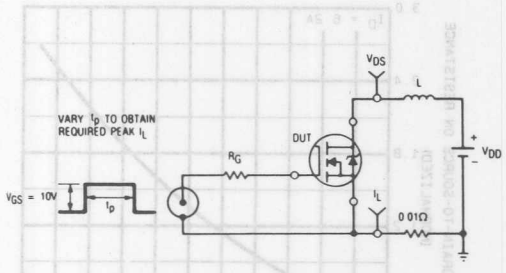


Fig. 14a - Unclamped Inductive Test Circuit

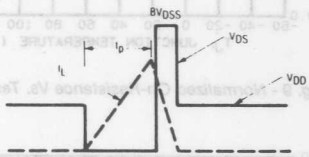


Fig. 14b - Unclamped Inductive Waveforms

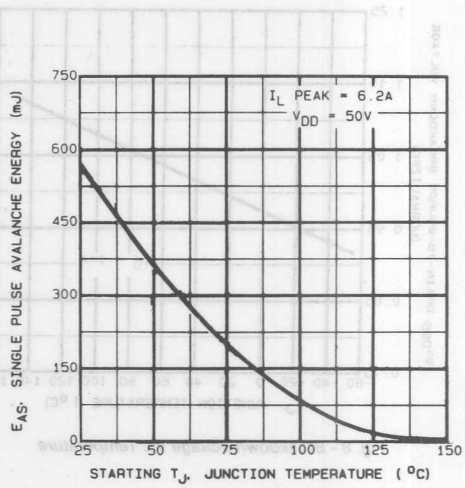


Fig. 14c - Maximum Avalanche Energy Vs. Starting Junction Temperature

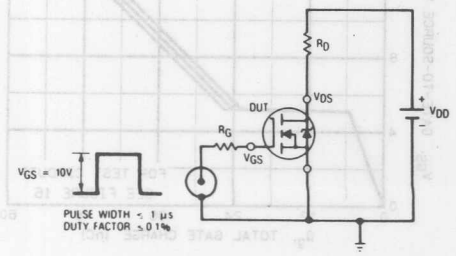


Fig. 15a - Switching Time Test Circuit

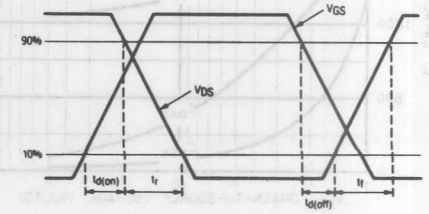


Fig. 15b - Switching Time Waveforms

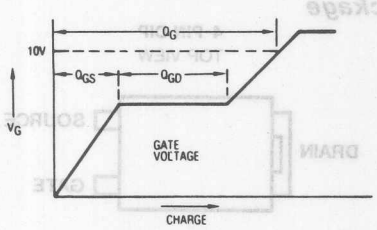


Fig. 16a - Basic Gate Charge Waveform

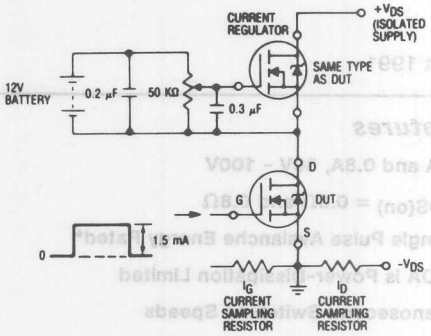


Fig. 16b - Gate Charge Test Circuit

IRFD110/111/112/113
IRFD110R/111R/112R/113R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

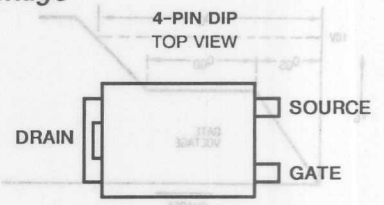
- 1A and 0.8A, 80V - 100V
- $r_{DS(on)}$ = 0.6Ω and 0.8Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFD110, IRFD111, IRFD112, and IRFD113 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD110R, IRFD111R, IRFD112R, and IRFD113R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

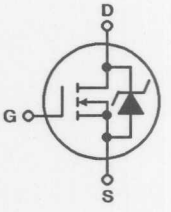
The IRFD types are supplied in the 4-pin dual-in-line plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD110 IRFD110R	IRFD111 IRFD111R	IRFD112 IRFD112R	IRFD113 IRFD113R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current T_C = +25°C ..... I_D	1.0	1.0	0.8	0.8	A
Pulsed Drain Current ..... I_{DM}	8.0	8.0	6.4	6.4	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	8.0	8.0	6.4	6.4	A
Single Pulse Avalanche Energy Rating (3) ..... E_{as}*	19	19	19	19	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. V_{DD} = 25V, starting T_J = +25°C, L = 28.5mH, R_{GS} = 25Ω, I_{PEAK} = 1.0A. See Figure 15.

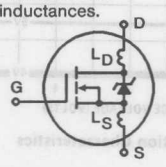
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

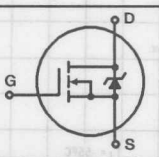
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File Number **2314.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD110/112, IRFD110R/112R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	–	–	V
IRFD111/113, IRFD111R/113R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFD110/111, IRFD110R/111R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	1.0	–	–	A
IRFD112/113, IRFD112R/113R			0.8	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFD110/111, IRFD110R/111R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.8A	–	0.5	0.6	Ω
IRFD112/113, IRFD112R/113R			–	0.6	0.8	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, I_D = 0.8A	0.8	1.2	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	135	–	pF
Output Capacitance	C_{OSS}		–	80	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 1.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	10	20	ns
Rise Time	t_r		–	15	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	15	25	ns
Fall Time	t_f		–	10	20	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 1.0A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	5.0	7.0	nC
Gate-Source Charge	Q_{gs}		–	2.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	7.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	4.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	–	6.0	–	nH
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	1.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	8.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 1.0A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 1.0A, dI_F/dt = 100A/μs	–	100	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 1.0A, dI_F/dt = 100A/μs	–	0.2	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	–	–	–	–

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. V_{DD} = 25V, starting T_J = +25°C, L = 28.5mH, R_{GS} = 25Ω, I_{PEAK} = 1.0A. (See Figure 15.)

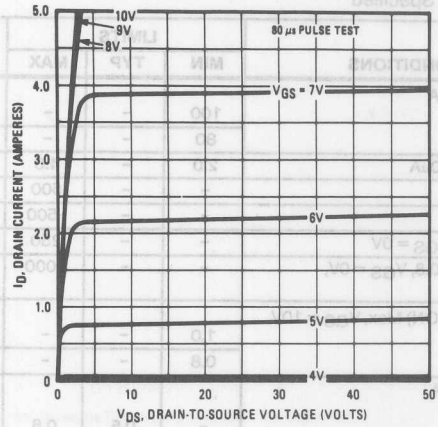


Fig. 1 — Typical Output Characteristics

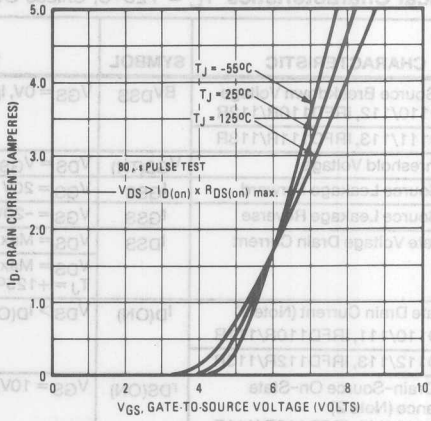


Fig. 2 — Typical Transfer Characteristics

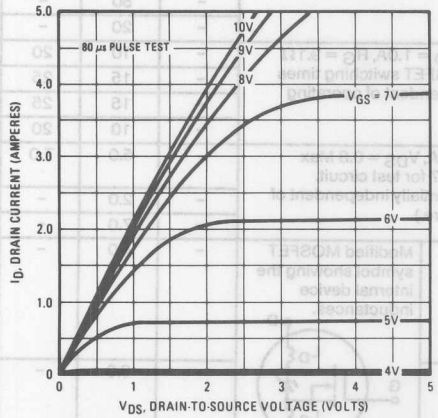


Fig. 3 — Typical Saturation Characteristics

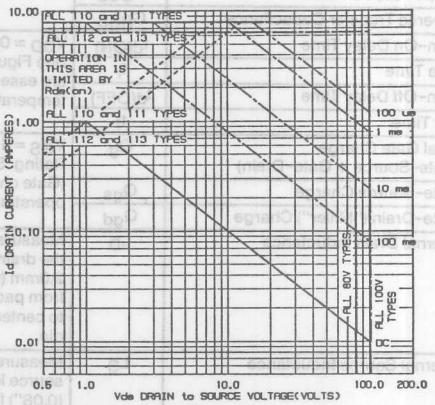


Fig. 4 — Maximum Safe Operating Area

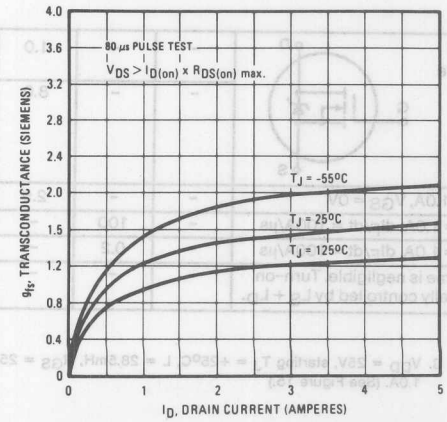


Fig. 5 — Typical Transconductance Vs. Drain Current

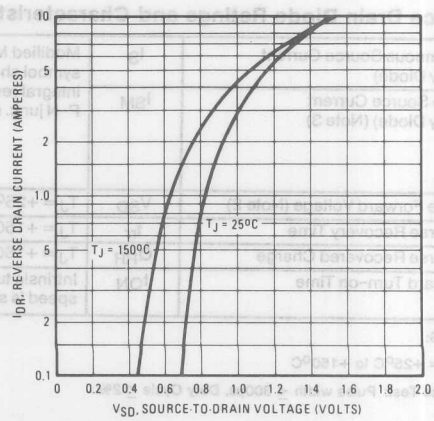


Fig. 6 — Typical Source-Drain Diode Forward Voltage

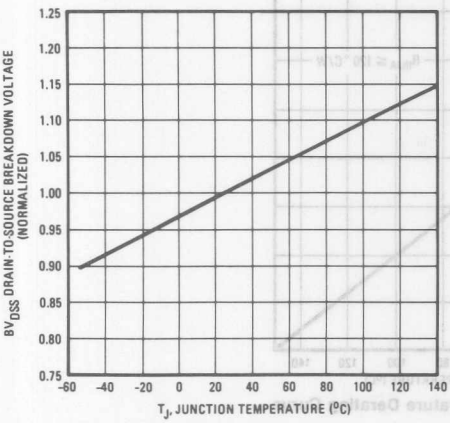


Fig. 7 — Breakdown Voltage Vs. Temperature

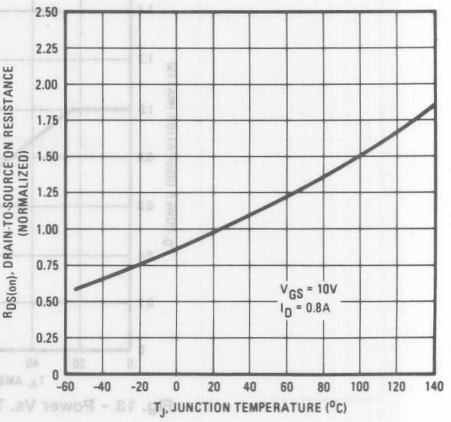


Fig. 8 — Normalized On-Resistance Vs. Temperature

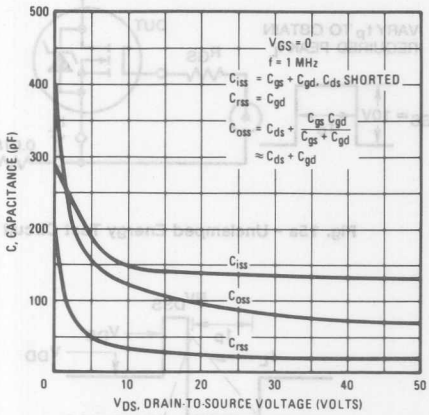


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

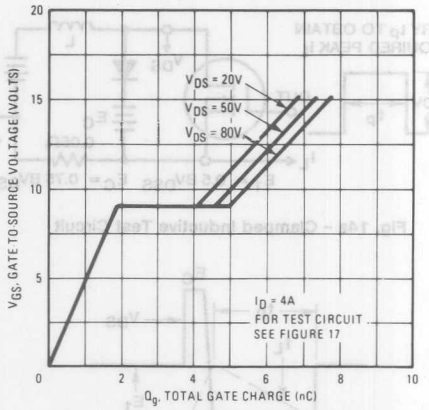


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

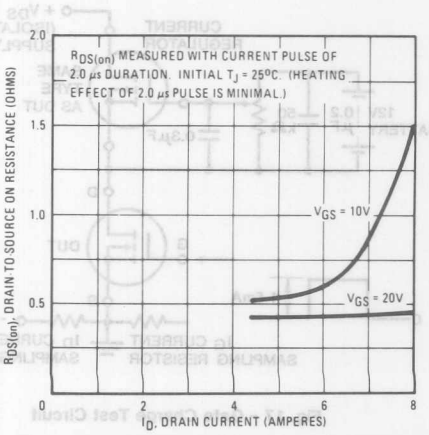


Fig. 11 — Typical On-Resistance Vs. Drain Current

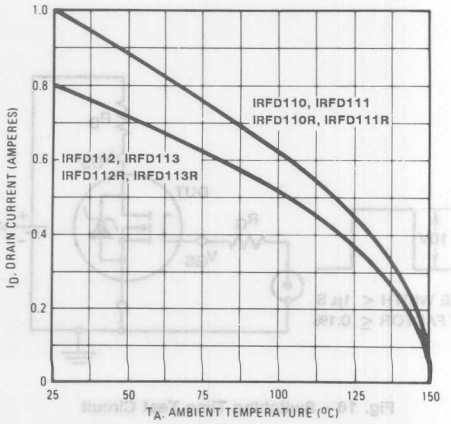


Fig. 12 — Maximum Drain Current Vs. Case Temperature

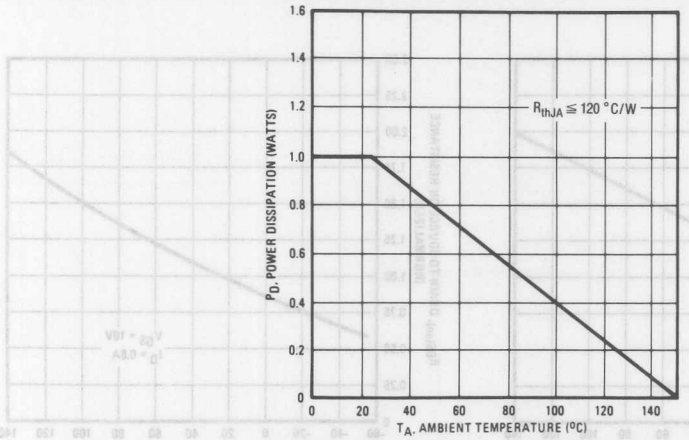


Fig. 13 – Power Vs. Temperature Derating Curve

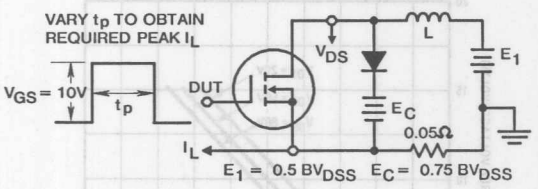


Fig. 14a – Clamped Inductive Test Circuit

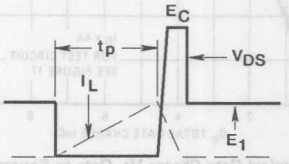


Fig. 14b – Clamped Inductive Waveforms

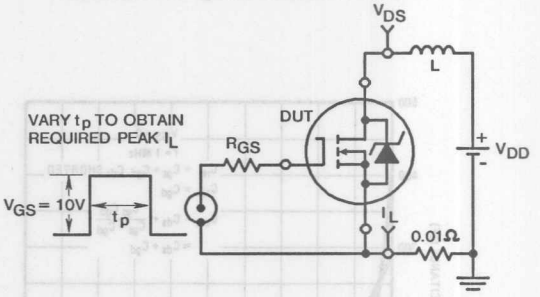


Fig. 15a – Unclamped Energy Test Circuit

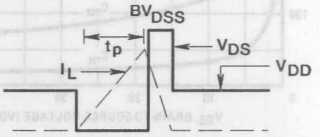


Fig. 15b – Unclamped Energy Waveforms

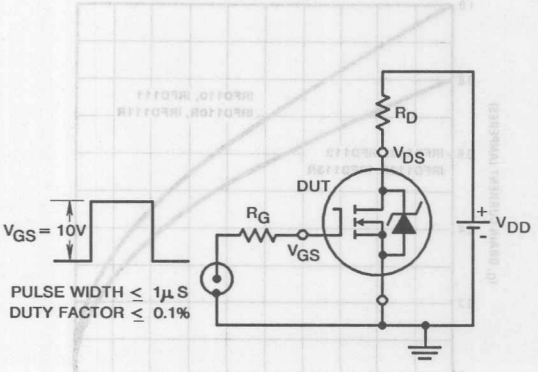


Fig. 16 – Switching Time Test Circuit

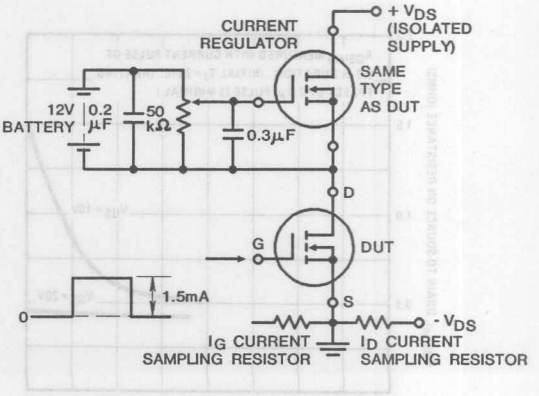


Fig. 17 – Gate Charge Test Circuit

IRFD120/121/122/123
IRFD120R/121R/122R/123R

N-Channel Power MOSFETs
Avalanche Energy Rated*

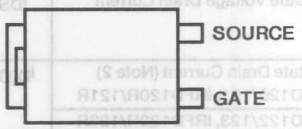
August 1991

Features

- 1.3A and 1.1A, 80V - 100V
- $r_{DS(on)}$ = 0.30Ω and 0.40Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

4-PIN DIP
TOP VIEW



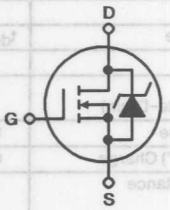
Description

The IRFD120, IRFD121, IRFD122, and IRFD123 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD120R, IRFD121R, IRFD122R, and IRFD123R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin dual-in-line plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD120 IRFD120R	IRFD121 IRFD121R	IRFD122 IRFD122R	IRFD123 IRFD123R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current T_C = +25°C ..... I_D	1.3	1.3	1.1	1.1	A
Pulsed Drain Current ..... I_{DM}	5.2	5.2	4.4	4.4	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	5.2	5.2	4.4	4.4	A
Single Pulse Avalanche Energy Rating (3) ..... E_{as}*	36	36	36	36	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

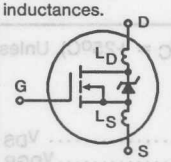
NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. V_{DD} = 25V, starting T_J = +25°C, L = 32mH, R_{GS} = 25Ω, I_{PEAK} = 1.3A. See Figure 15.

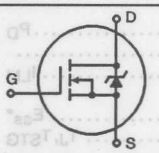
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number **2315.1**

Drain-Source Breakdown Voltage IRFD120/122, IRFD120R/122R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	–	–	V
IRFD121/123, IRFD121R/123R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFD120/121, IRFD120R/121R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	1.3	–	–	A
IRFD122/123, IRFD122R/123R			1.1	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFD120/121, IRFD120R/121R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.6A	–	0.25	0.30	Ω
IRFD122/123, IRFD122R/123R			–	0.30	0.40	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, I_D = 0.6A	0.9	1.0	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 9	–	450	–	pF
Output Capacitance	C_{OSS}		–	200	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	50	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 1.3A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	20	40	ns
Rise Time	t_r		–	35	70	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	100	ns
Fall Time	t_f		–	35	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 1.3A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	11	15	nC
Gate-Source Charge	Q_{gs}		–	6.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	5.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	4.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	–	6.0	–	nH
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	1.3	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	5.2	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 1.3A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 1.3A, dI_F/dt = 100A/μs	–	280	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 1.3A, dI_F/dt = 100A/μs	–	1.6	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	–	–	–	–

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. V_{DD} = 25V, starting T_J = +25°C, L = 32mH, R_{GS} = 25Ω, I_{PEAK} = 1.3A. (See Figure 15.)

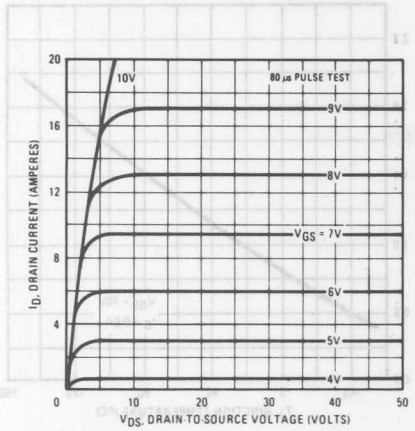


Fig. 1 – Typical Output Characteristics

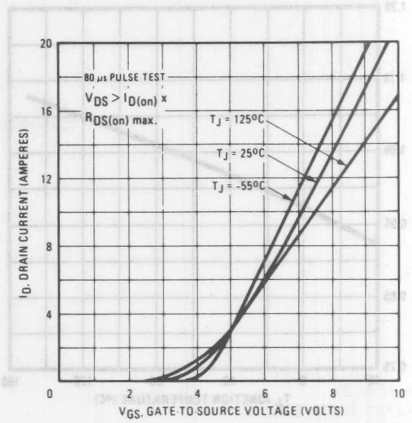


Fig. 2 – Typical Transfer Characteristics

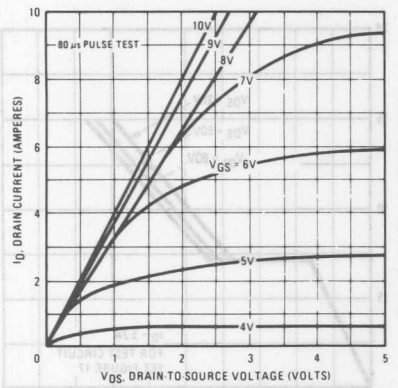


Fig. 3 – Typical Saturation Characteristics

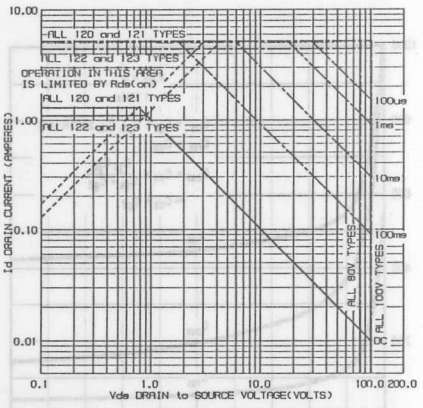


Fig. 4 – Maximum Safe Operating Area

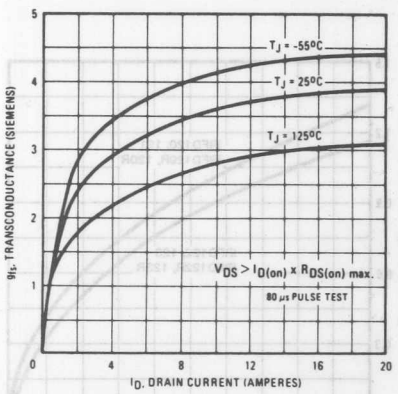


Fig. 5 – Typical Transconductance Vs. Drain Current

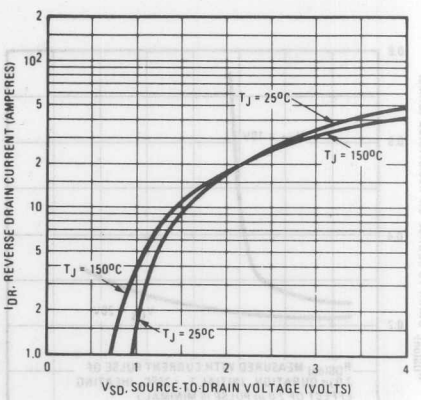


Fig. 6 – Typical Source-Drain Diode Forward Voltage

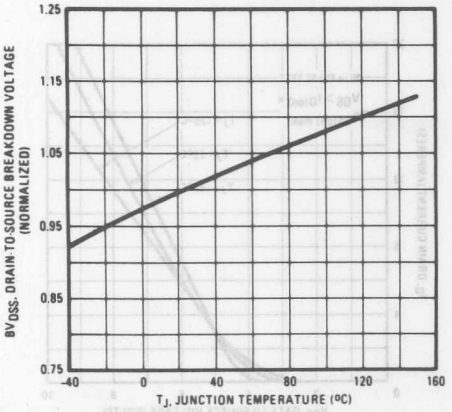


Fig. 7 – Breakdown Voltage Vs. Temperature

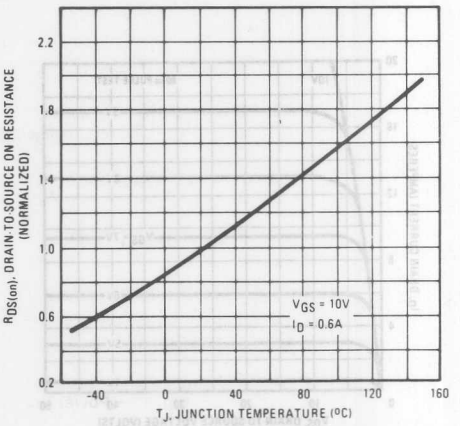


Fig. 8 – Normalized On-Resistance Vs. Temperature

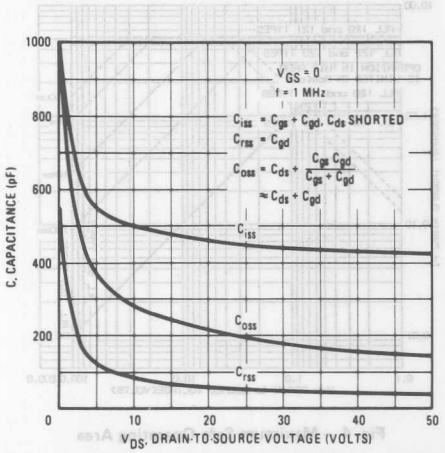


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

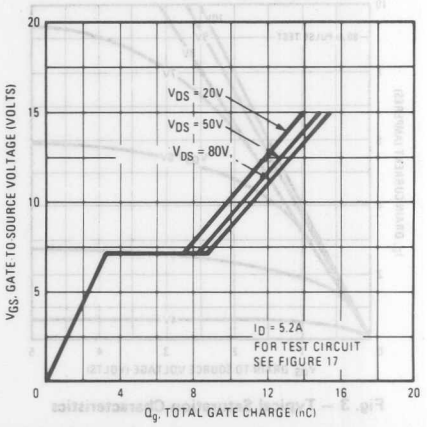


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

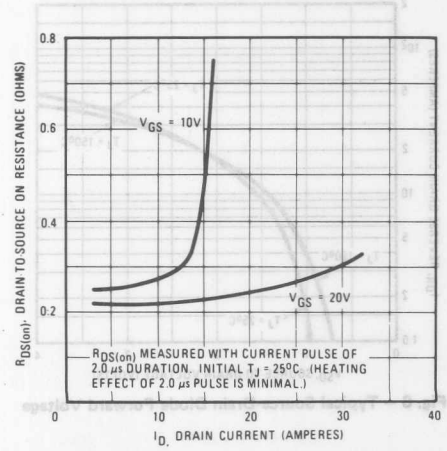


Fig. 11 – Typical On-Resistance Vs. Drain Current

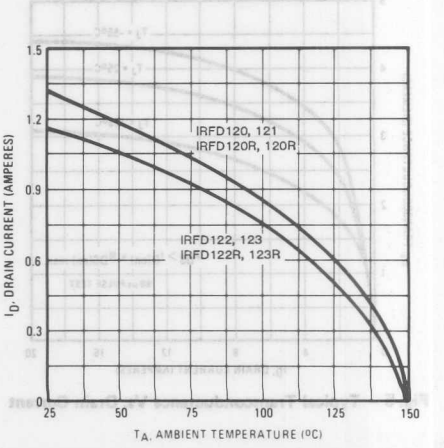


Fig. 12 – Maximum Drain Current Vs. Case Temperature

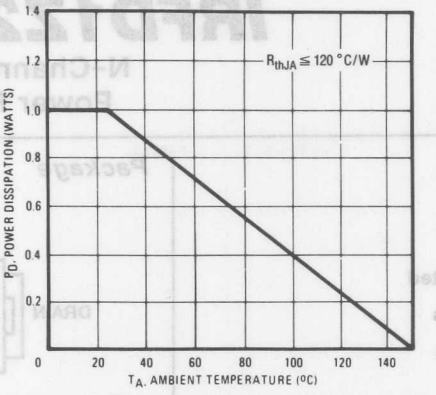


Fig. 13 – Power Vs. Temperature Derating Curve

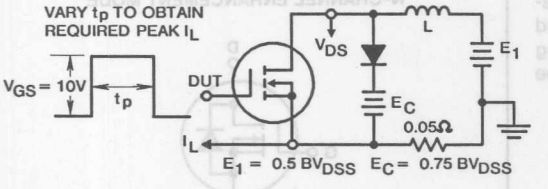


Fig. 14a – Clamped Inductive Test Circuit

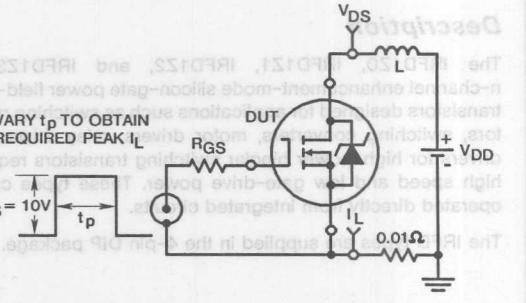


Fig. 15a – Unclamped Energy Test Circuit

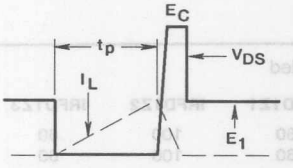


Fig. 14b – Clamped Inductive Waveforms

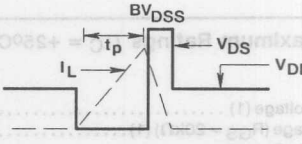


Fig. 15b – Unclamped Energy Waveforms

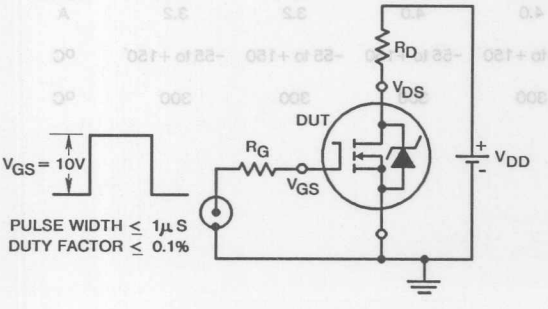


Fig. 16 – Switching Time Test Circuit

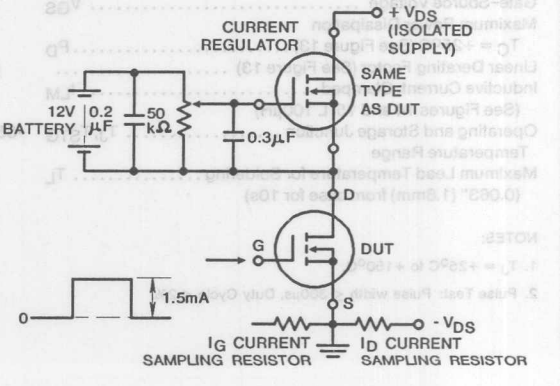


Fig. 17 – Gate Charge Test Circuit

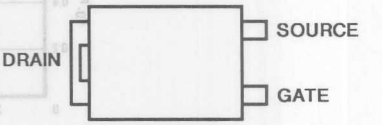
HARRIS IRFD1Z0, IRFD1Z1

Features

- 0.4A and 0.5A, 60V - 100V
- $r_{DS(on)}$ = 2.4Ω and 3.2Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

4-PIN DIP
TOP VIEW



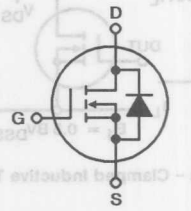
Description

The IRFD1Z0, IRFD1Z1, IRFD1Z2, and IRFD1Z3 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin DIP package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFD1Z0	IRFD1Z1	IRFD1Z2	IRFD1Z3	UNITS
Drain-Source Voltage (1)	V_{DS}	100	60	100	60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	100	60	100	60	V
Continuous Drain Current T_C = +25°C	I_D	0.5	0.5	0.4	0.4	A
Pulsed Drain Current	I_{DM}	4.0	4.0	3.2	3.2	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13)	P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped (See Figures 14 and 15, L 100μH)	I_{LM}	4.0	4.0	3.2	3.2	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2313

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD1Z0, 2	100	–	–	V	V_{GS} = 0V
		IRFD1Z1, 3	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate - Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate - Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD1Z0, 1	0.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFD1Z2, 3	0.4	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD1Z0, 1	–	2.2	2.4	Ω	V_{GS} = 10V, I_D = 0.25A
		IRFD1Z2, 3	–	2.8	3.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.25	0.35	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.25A
C_{iss}	Input Capacitance	ALL	–	50	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	20	–	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	5.0	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 0.25A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	2.0	3.0	nC	V_{GS} = 10V, I_D = 1.2A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	1.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	1.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measure from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	–	–	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD1Z0, 1	–	–	0.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD1Z2, 3	–	–	0.4	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD1Z0, 1	–	–	4.0	A	
		IRFD1Z2, 3	–	–	3.2	A	
V_{SD}	Diode Forward Voltage ②	IRFD1Z0, 1	–	–	1.4	V	T_A = 25°C, I_S = 0.5A, V_{GS} = 0V
		IRFD1Z2, 3	–	–	1.3	V	T_A = 25°C, I_S = 0.4A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	100	–	ns	T_J = 150°C, I_F = 0.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	0.2	–	μC	T_J = 150°C, I_F = 0.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

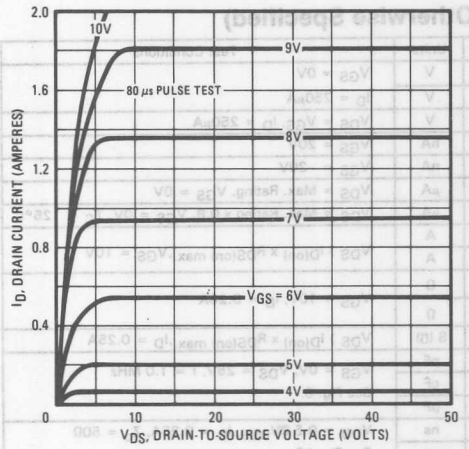


Fig. 1 — Typical Output Characteristics

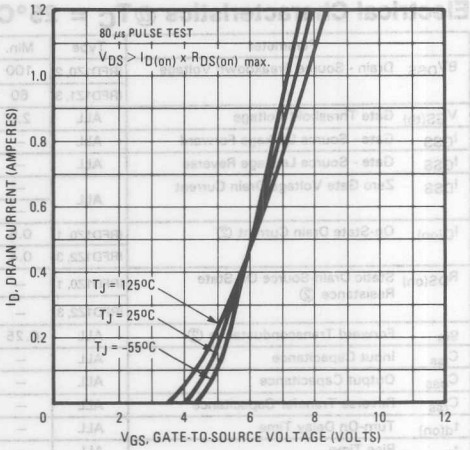


Fig. 2 — Typical Transfer Characteristics

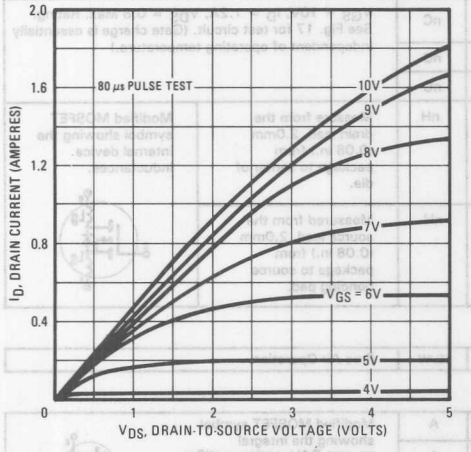


Fig. 3 — Typical Saturation Characteristics

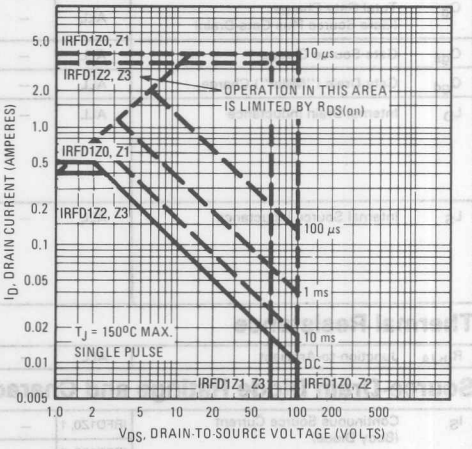


Fig. 4 — Maximum Safe Operating Area

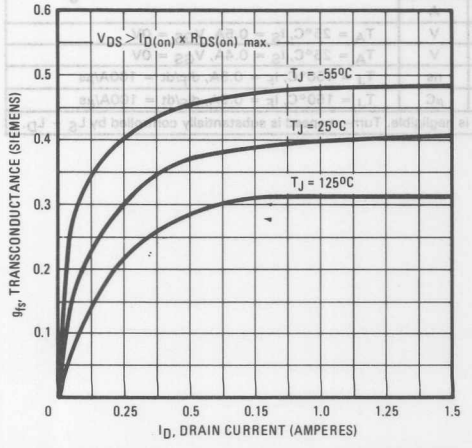


Fig. 5 — Typical Transconductance Vs. Drain Current

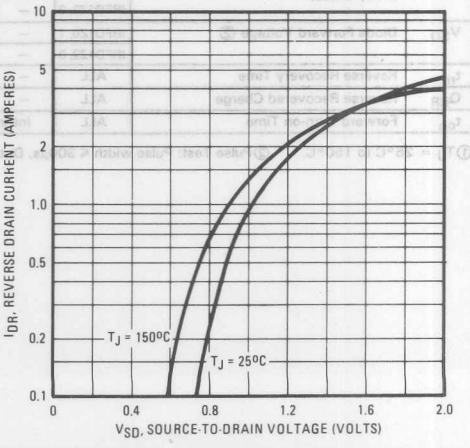


Fig. 6 — Typical Source-Drain Diode Forward Voltage

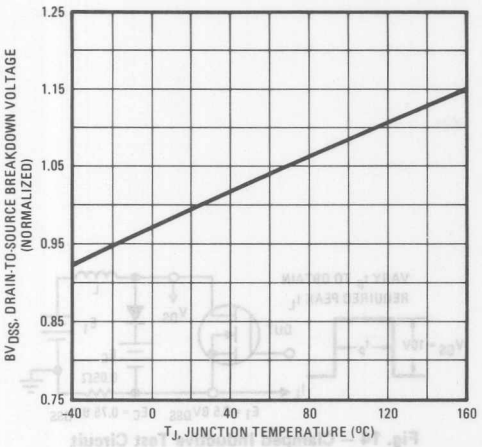


Fig. 7 — Breakdown Voltage Vs. Temperature

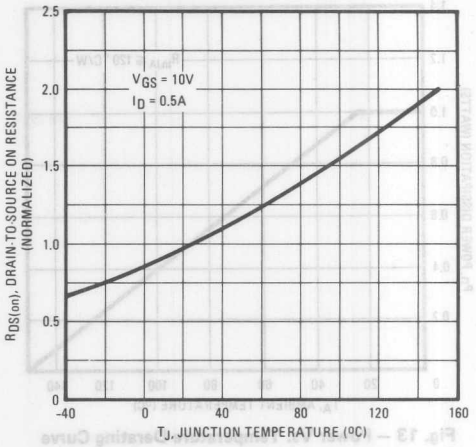


Fig. 8 — Normalized On-Resistance Vs. Temperature

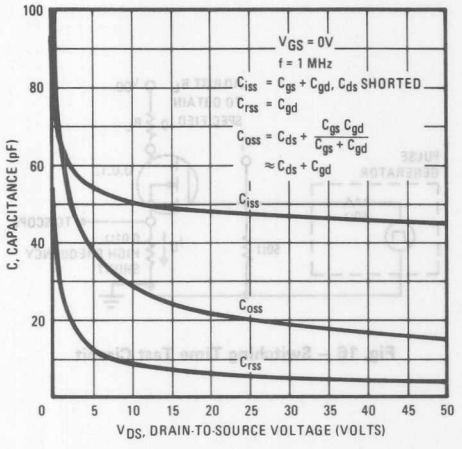


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

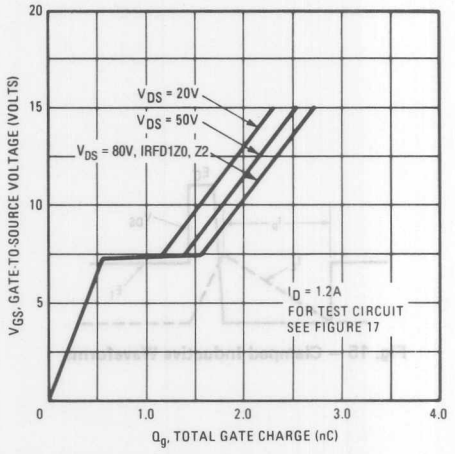


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

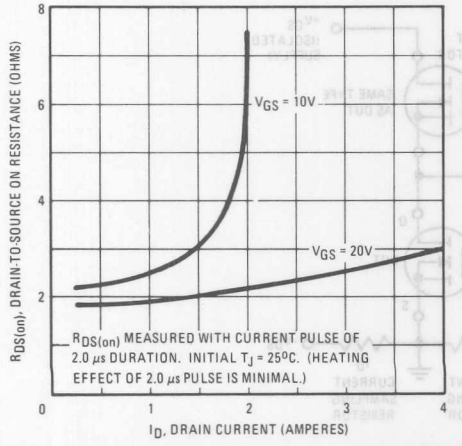


Fig. 11 — Typical On-Resistance Vs. Drain Current

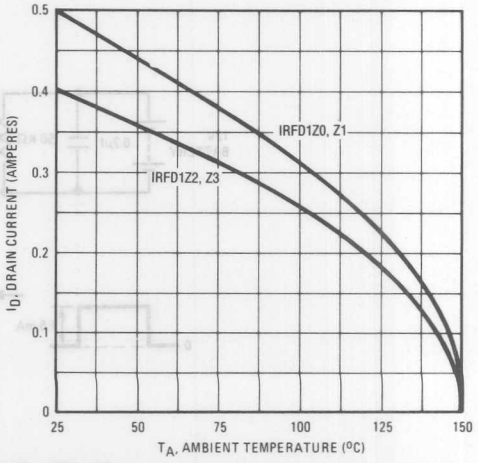


Fig. 12 — Maximum Drain Current Vs. Case Temperature

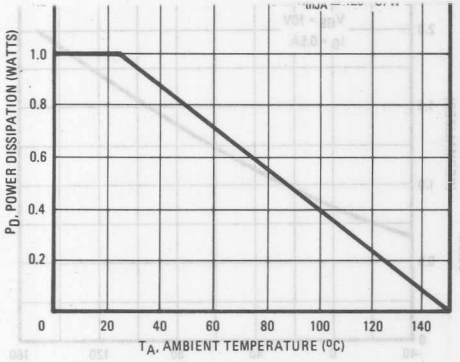


Fig. 13 – Power Vs. Temperature Derating Curve

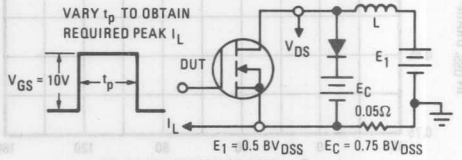


Fig. 14 – Clamped Inductive Test Circuit

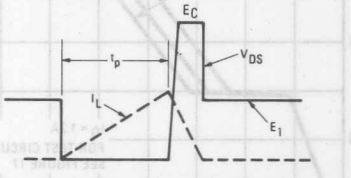


Fig. 15 – Clamped Inductive Waveforms

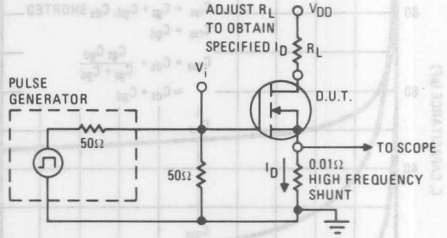


Fig. 16 – Switching Time Test Circuit

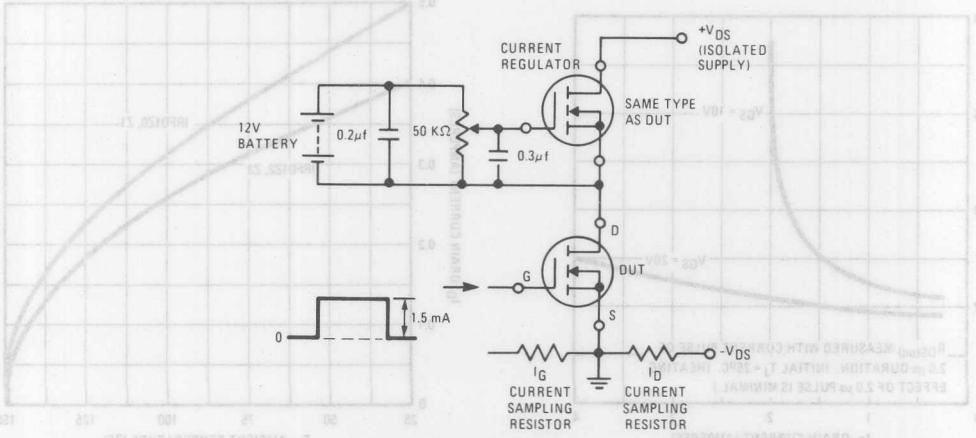


Fig. 17 – Gate Charge Test Circuit

IRFD210/211/212/213
IRFD210R/211R/212R/213R

N-Channel Power MOSFETs
Avalanche Energy Rated*

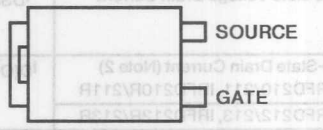
August 1991

Features

- 0.6A and 0.45A, 150V - 200V
- $r_{DS(on)}$ = 1.5Ω and 2.4Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

4-PIN DIP
TOP VIEW



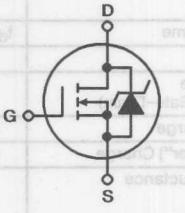
Description

The IRFD210, IRFD211, IRFD212, and IRFD213 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD210R, IRFD211R, IRFD212R, and IRFD213R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin dual-in-line plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD210 IRFD210R	IRFD211 IRFD211R	IRFD212 IRFD212R	IRFD213 IRFD213R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C ..... I_D	0.6	0.6	0.45	0.45	A
Pulsed Drain Current ..... I_{DM}	2.5	2.5	1.8	1.8	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	2.5	2.5	1.8	1.8	A
Single Pulse Avalanche Energy Rating (3) ..... E_{as}*	30	30	30	30	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

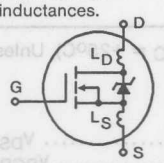
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. V_{DD} = 20V, starting T_J = +25°C, L = 112.7mH, R_{GS} = 50Ω, I_{PEAK} = 2.2A. See Figure 15.

* R Suffix Types Only

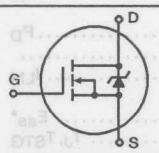
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
Copyright © Harris Corporation 1991

File Number **2316.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD210/212, IRFD210R/212R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRFD211/213, IRFD211R/213R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFD210/211, IRFD210R/211R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	0.6	–	–	A
IRFD212/213, IRFD212R/213R			0.45	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFD210/211, IRFD210R/211R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.3A	–	1.0	1.5	Ω
IRFD212/213, IRFD212R/213R			–	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 0.3A	0.5	0.8	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 9	–	135	–	pF
Output Capacitance	C_{OSS}		–	60	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	16	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 0.6A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	8.0	15	ns
Rise Time	t_r		–	15	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	10	15	ns
Fall Time	t_f		–	8.0	15	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 0.6A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	5.0	7.5	nC
Gate-Source Charge	Q_{gs}		–	2.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	3.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	4.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	–	6.0	–	nH
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	0.6	A
Pulse Source Current (Body Diode)	I_{SM}		–	–	2.5	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 0.6A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 0.6A, dI_F/dt = 100A/µs	–	290	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 0.6A, dI_F/dt = 100A/µs	–	2.0	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. V_{DD} = 20V, starting T_J = +25°C, L = 112.7mH, R_{GS} = 50Ω, I_{PEAK} = 2.2A. (See Figure 15.)

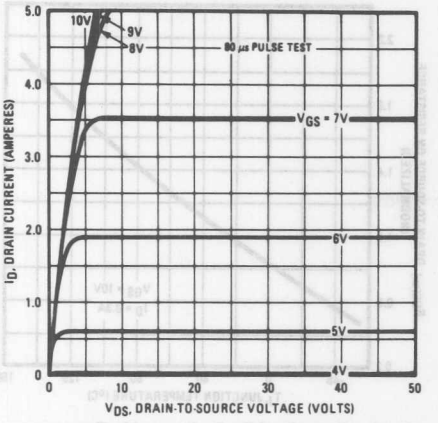


Fig. 1 – Typical Output Characteristics

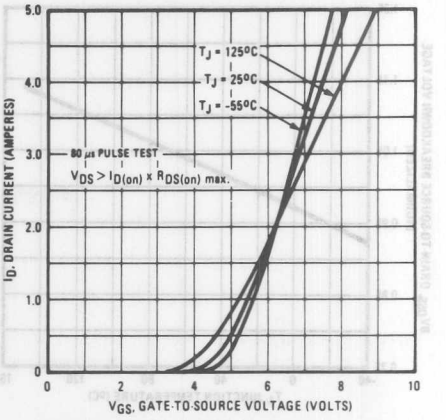


Fig. 2 – Typical Transfer Characteristics

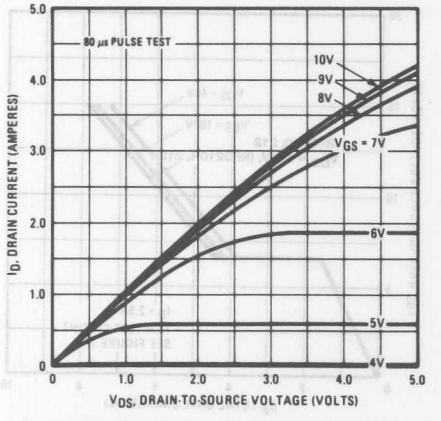


Fig. 3 – Typical Saturation Characteristics

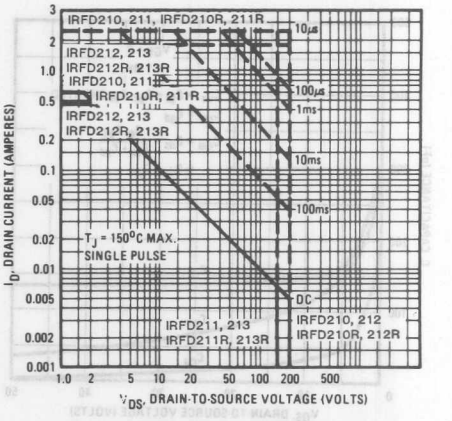


Fig. 4 – Maximum Safe Operating Area

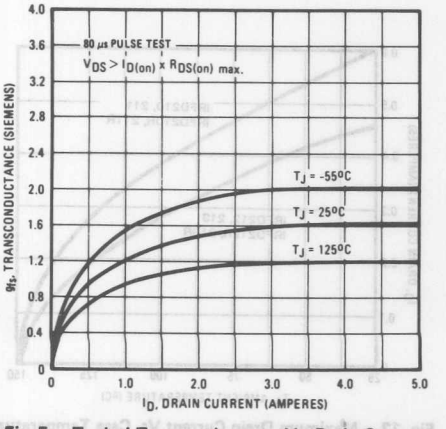


Fig. 5 – Typical Transconductance Vs. Drain Current

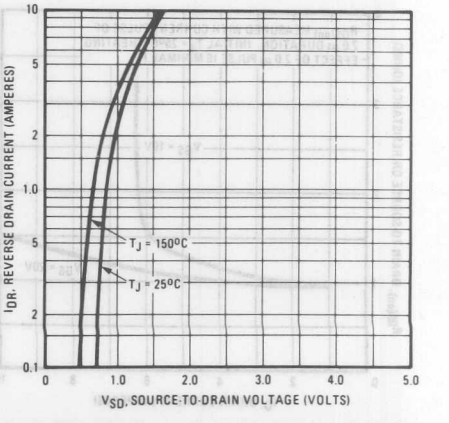


Fig. 6 – Typical Source-Drain Diode Forward Voltage

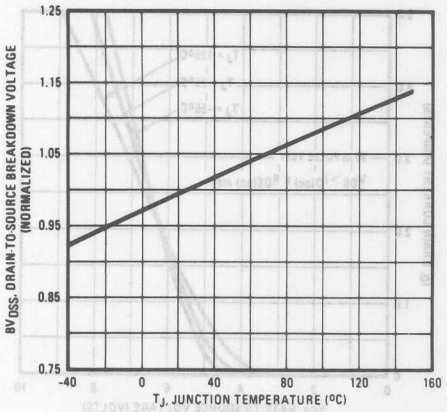


Fig. 7 — Breakdown Voltage Vs. Temperature

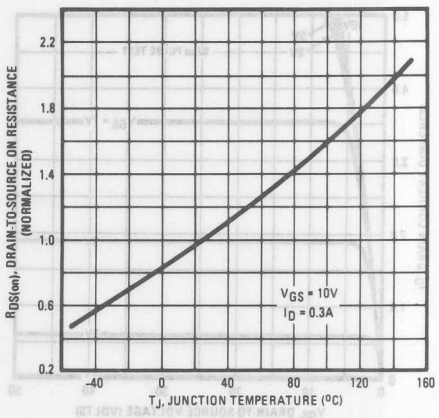


Fig. 8 — Normalized On-Resistance Vs. Temperature

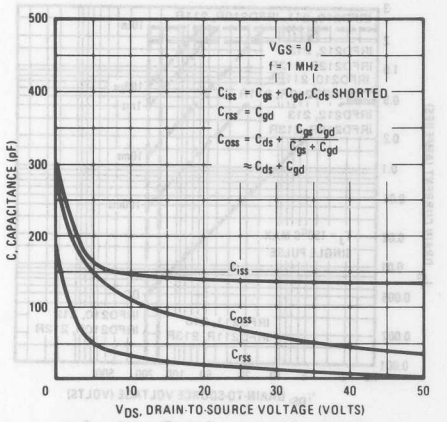


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

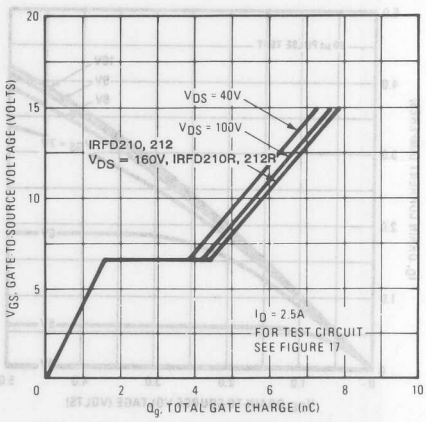


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

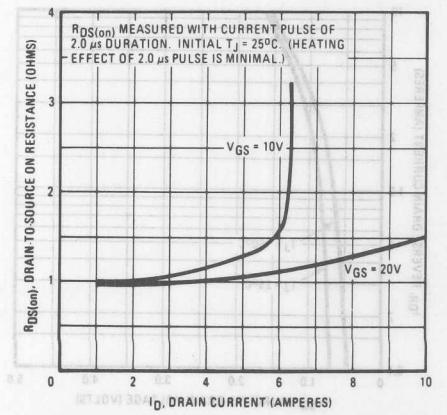


Fig. 11 — Typical On-Resistance Vs. Drain Current

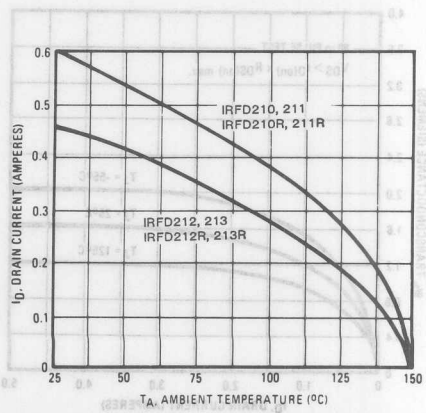


Fig. 12 — Maximum Drain Current Vs. Case Temperature

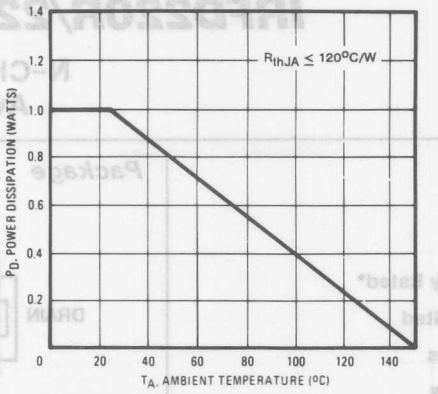


Fig. 13 - Power Vs. Temperature Derating Curve

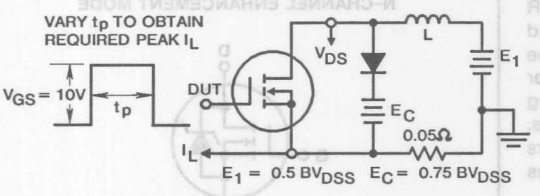


Fig. 14a - Clamped Inductive Test Circuit

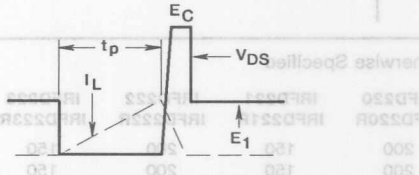


Fig. 14b - Clamped Inductive Waveforms

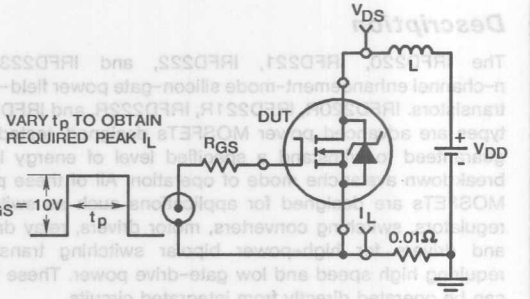


Fig. 15a - Unclamped Energy Test Circuit

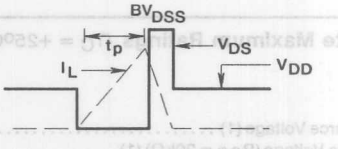


Fig. 15b - Unclamped Energy Waveforms

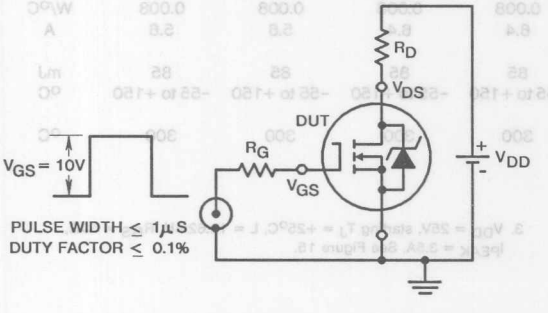


Fig. 16 - Switching Time Test Circuit

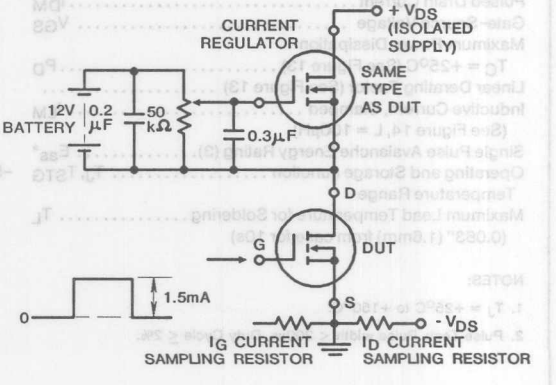


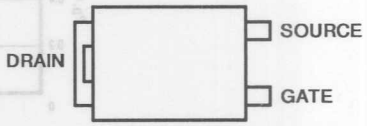
Fig. 17 - Gate Charge Test Circuit

Features

- 0.7A and 0.8A, 150V - 200V
- $r_{DS(on)}$ = 0.8Ω and 1.2Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

4-PIN DIP
TOP VIEW



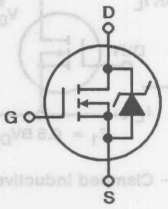
Description

The IRFD220, IRFD221, IRFD222, and IRFD223 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD220R, IRFD221R, IRFD222R, and IRFD223R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin dual-in-line plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD220 IRFD220R	IRFD221 IRFD221R	IRFD222 IRFD222R	IRFD223 IRFD223R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C ..... I_D	0.8	0.8	0.7	0.7	A
Pulsed Drain Current ..... I_{DM}	6.4	6.4	5.6	5.6	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	6.4	6.4	5.6	5.6	A
Single Pulse Avalanche Energy Rating (3) ..... E_{as}*	85	85	85	85	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

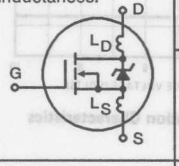
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. V_{DD} = 25V, starting T_J = +25°C, L = 12.62mH, R_{GS} = 50Ω, I_{PEAK} = 3.5A. See Figure 15.

* R Suffix Types Only

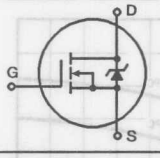
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number **2317.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD220/222, IRFD220R/222R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRFD221/223, IRFD221R/223R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFD220/221, IRFD220R/221R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	0.8	–	–	A
IRFD222/223, IRFD222R/223R			0.7	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFD220/221, IRFD220R/221R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.4A	–	0.5	0.8	Ω
IRFD222/223, IRFD222R/223R			–	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 0.4A	0.5	1.1	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 9	–	450	–	pF
Output Capacitance	C_{OSS}		–	150	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	40	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 0.5BV_{DSS}, I_D = 0.8A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	20	40	ns
Rise Time	t_r		–	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	100	ns
Fall Time	t_f		–	30	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 0.8A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	11	15	nC
Gate-Source Charge	Q_{gs}		–	6.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	5.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	4.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	–	6.0	–	nH
Junction-to-Case	$R_{\theta JC}$	Free air operation	–	–	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	0.8	A
Pulse Source Current (Body Diode)	I_{SM}		–	–	6.4	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 0.8A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 0.8A, dI_F/dt = 100A/µs	–	150	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 0.8A, dI_F/dt = 100A/µs	–	0.6	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. V_{DD} = 25V, starting T_J = +25°C, L = 12.62mH, R_{GS} = 50Ω, I_{PEAK} = 3.5A. (See Figure 15.)

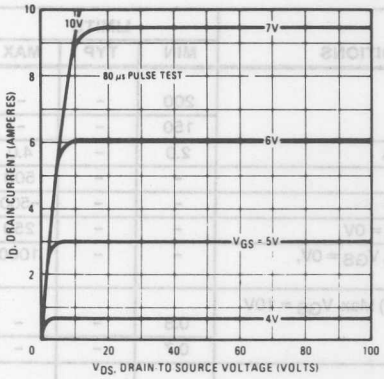


Fig. 1 — Typical Output Characteristics

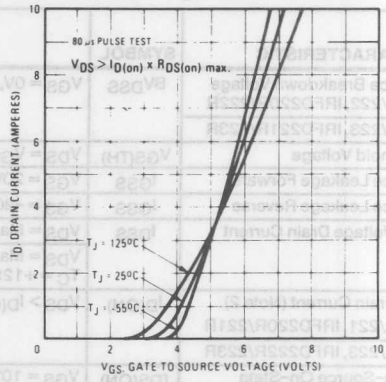


Fig. 2 — Typical Transfer Characteristics

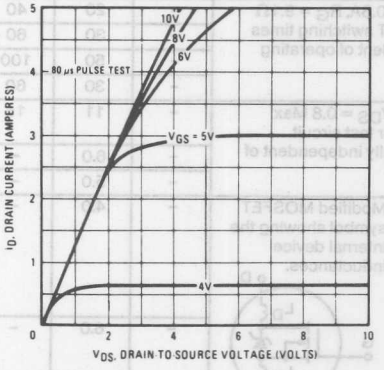


Fig. 3 — Typical Saturation Characteristics

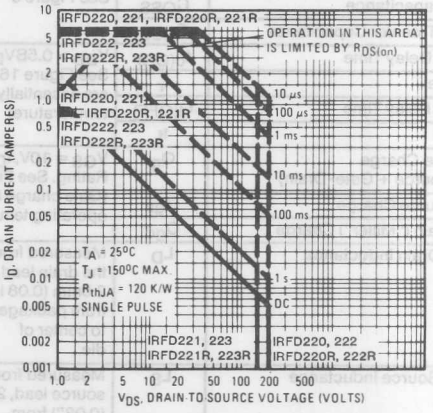


Fig. 4 — Maximum Safe Operating Area

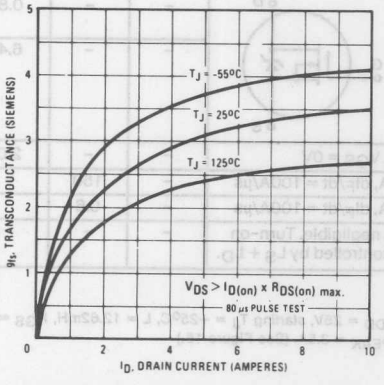


Fig. 5 — Typical Transconductance Vs. Drain Current

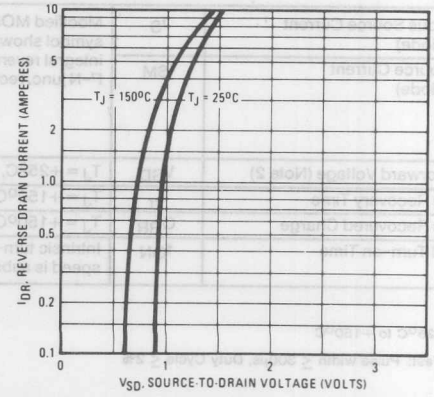


Fig. 6 — Typical Source-Drain Diode Forward Voltage

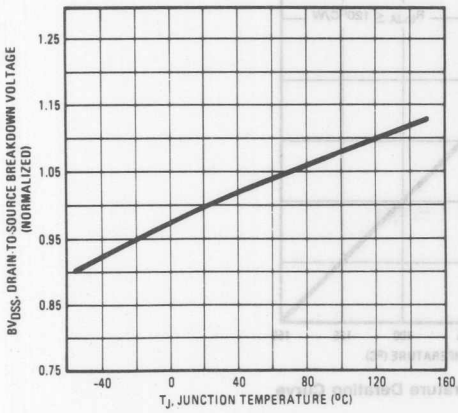


Fig. 7 – Breakdown Voltage Vs. Temperature

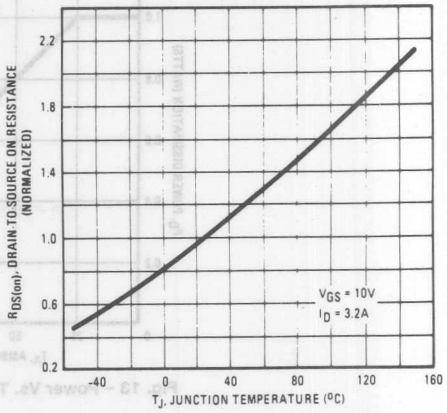


Fig. 8 – Normalized On-Resistance Vs. Temperature

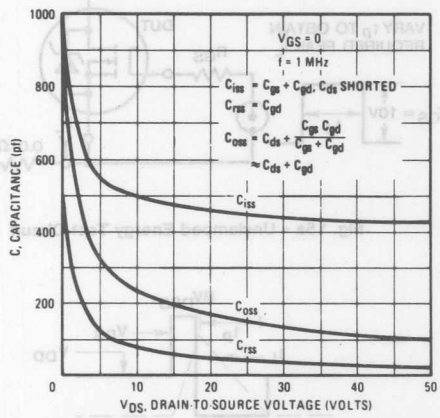


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

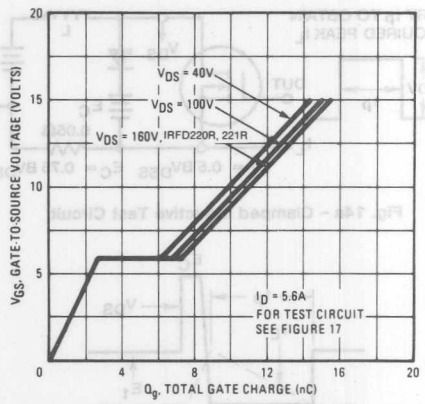


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

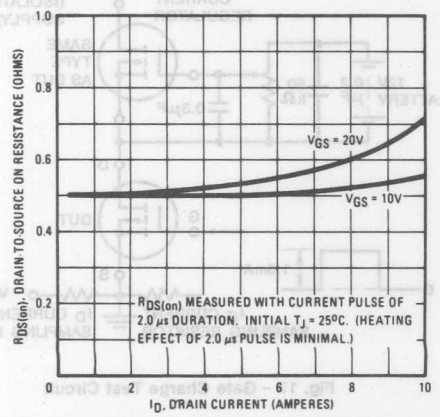


Fig. 11 – Typical On-Resistance Vs. Drain Current

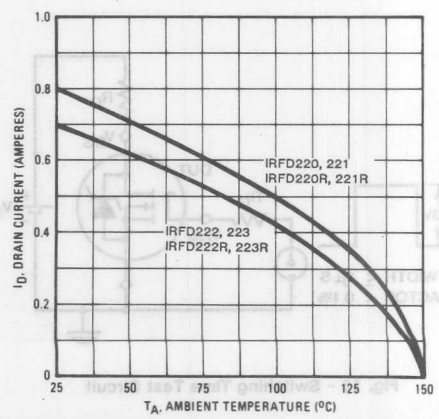


Fig. 12 – Maximum Drain Current Vs. Case Temperature

4 N-CHANNEL POWER MOSFETs

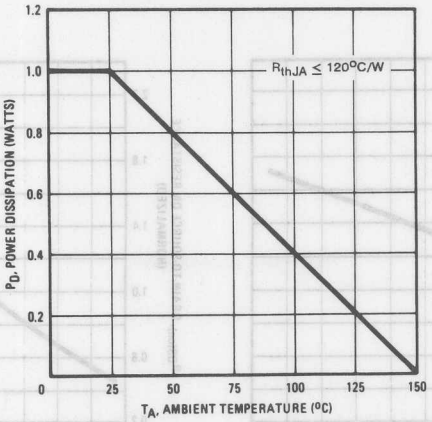


Fig. 13 - Power Vs. Temperature Derating Curve

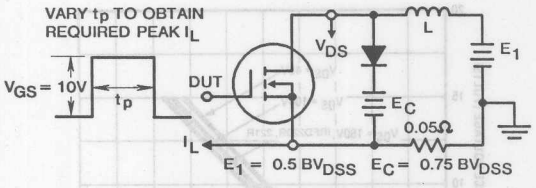


Fig. 14a - Clamped Inductive Test Circuit

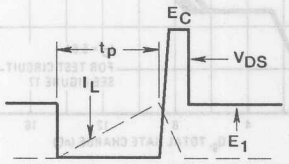


Fig. 14b - Clamped Inductive Waveforms

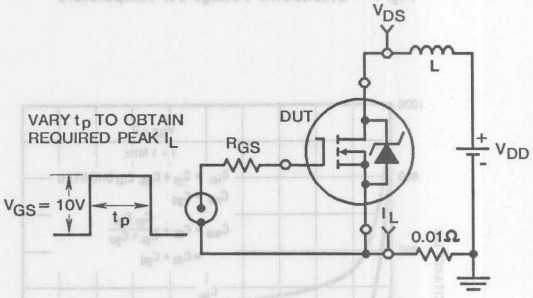


Fig. 15a - Unclamped Energy Test Circuit

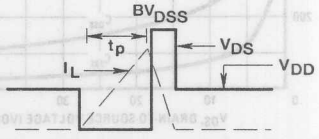


Fig. 15b - Unclamped Energy Waveforms

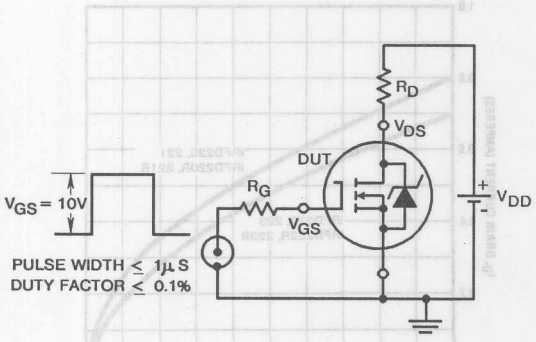


Fig. 16 - Switching Time Test Circuit

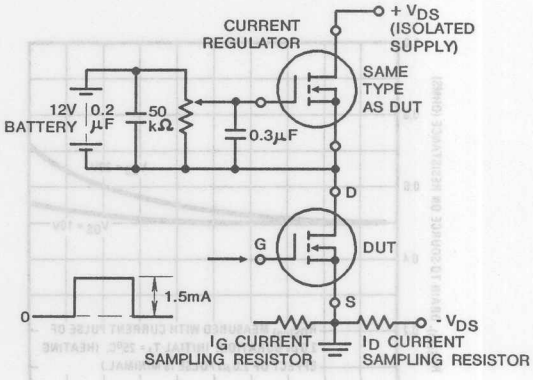


Fig. 17 - Gate Charge Test Circuit

IRFD2Z0, IRFD2Z1 IRFD2Z2, IRFD2Z3

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 0.30A and 0.32A, 150V - 200V
- $r_{DS(on)}$ = 5.0Ω and 6.5Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

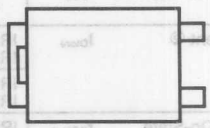
Description

The IRFD2Z0, IRFD2Z1, IRFD2Z2, and IRFD2Z3 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin DIP package.

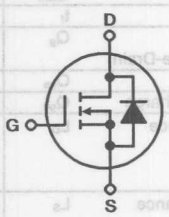
Package

4-PIN DIP
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFD2Z0	IRFD2Z1	IRFD2Z2	IRFD2Z3	UNITS
Drain-Source Voltage (1)	V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C	I_D	0.32	0.32	0.30	0.30	A
Pulsed Drain Current	I_{DM}	1.5	1.5	1.4	1.4	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13)	P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped (3)	I_{LM}	1.5	1.5	1.4	1.4	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. See Figures 14 and 15. L = 100μH

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

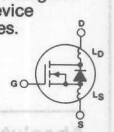
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File Number 2329.1

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFD2Z0 IRFD2Z2	200	—	—	V	V_{GS} = 0 V
		IRFD2Z1 IRFD2Z3	150	—	—	V	I_D = 250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = -20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRFD2Z0 IRFD2Z1	0.32	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = -10 V
		IRFD2Z2 IRFD2Z3	0.30	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFD2Z0 IRFD2Z1	—	4.6	5.0	Ω	V_{GS} = 10 V, I_D = 0.15 A
		IRFD2Z2 IRFD2Z3	—	5.7	6.5	Ω	
Forward Transconductance ②	g_{fs}	ALL	0.06	0.11	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = 0.15 A
Input Capacitance	C_{iss}	ALL	—	37	—	pF	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz See Fig. 9
Output Capacitance	C_{oss}	ALL	—	15	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	4.0	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	15	—	ns	$V_{DD} \simeq 0.5\ BV_{DSS}$, I_D = 0.15 A, Z_O = 50 Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	10	—	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	22	—	ns	
Fall Time	t_f	ALL	—	28	—	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	2.5	4.0	nC	V_{GS} = 10 V, I_D = 1.5 A, V_{DS} = 0.8 V Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	1.5	—	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	1.5	--	nC	
Internal Drain Inductance	L_D	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



THERMAL RESISTANCE

Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	120	°C/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFD2Z0 IRFD2Z1	—	—	0.32	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD2Z2 IRFD2Z3	—	—	0.30	A	
Pulse Source Current (Body Diode)	I_{SM}	IRFD2Z0 IRFD2Z1	—	—	1.5	A	
		IRFD2Z2 IRFD2Z3	—	—	1.4	A	
Diode Forward Voltage ②	V_{SD}	IRFD2Z0 IRFD2Z1	—	—	1.3	V	T_C = 25°C, I_S = 0.32 A, V_{GS} = 0 V
		IRFD2Z2 IRFD2Z3	—	—	1.3	V	T_C = 25°C, I_S = 0.30 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	125	—	ns	T_J = 150°C, I_F = 0.30 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	0.2	—	μC	T_J = 150°C, I_F = 0.30 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ (See Fig. 14 and 15) L = 100 μH

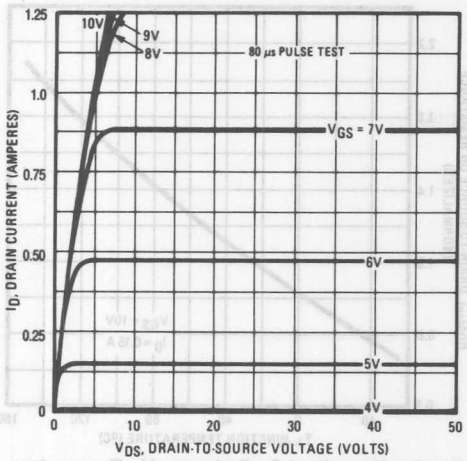


Fig. 1 – Typical Output Characteristics

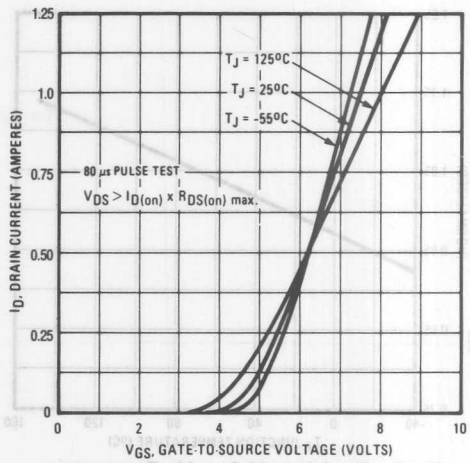


Fig. 2 – Typical Transfer Characteristics

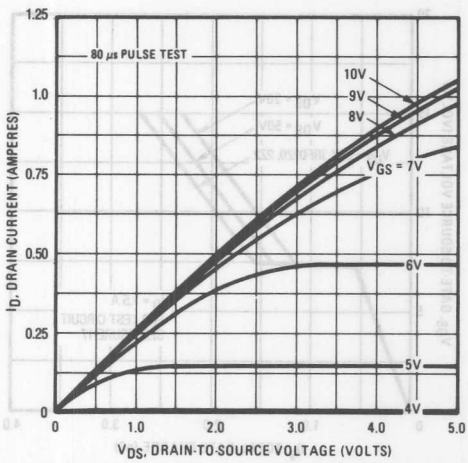


Fig. 3 – Typical Saturation Characteristics

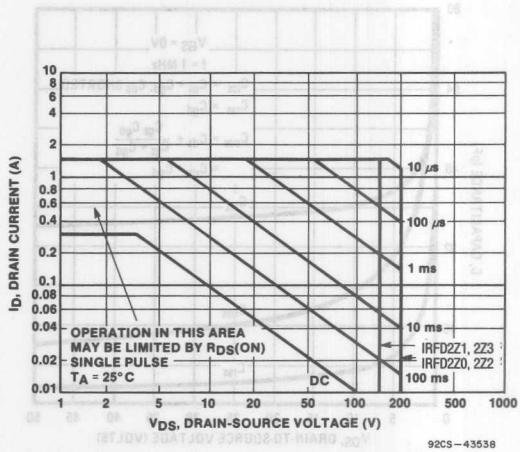


Fig. 4 – Maximum Safe Operating Area

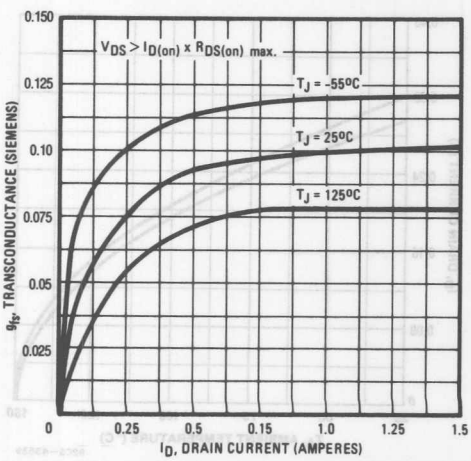


Fig. 5 – Typical Transconductance Vs. Drain Current

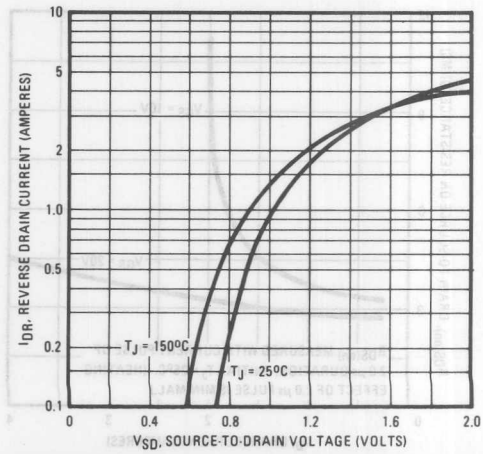


Fig. 6 – Typical Source-Drain Diode Forward Voltage

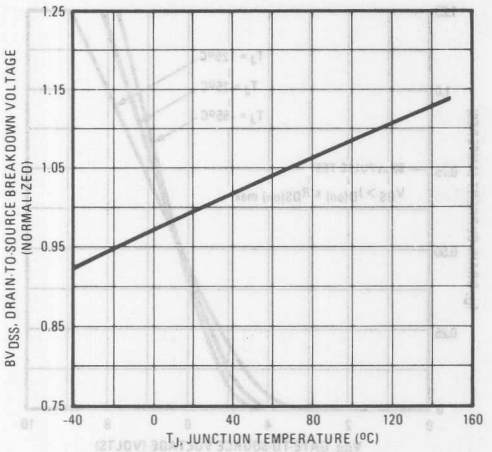


Fig. 7 — Breakdown Voltage Vs. Temperature

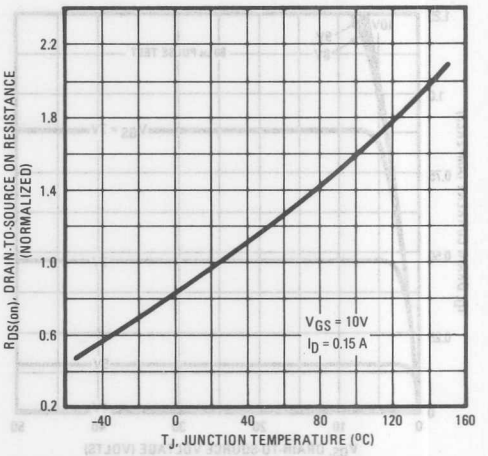


Fig. 8 — Normalized On-Resistance Vs. Temperature

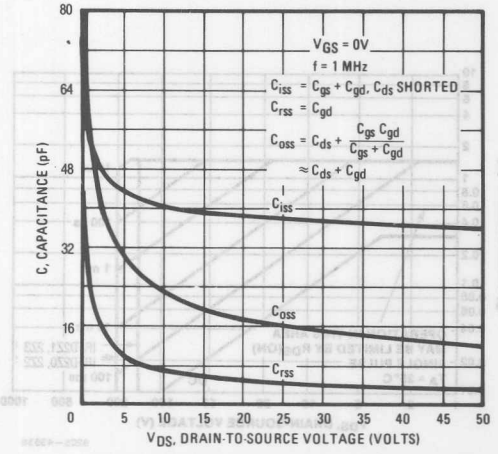


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

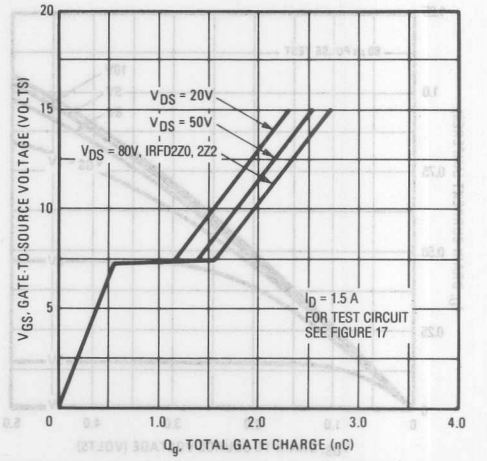


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

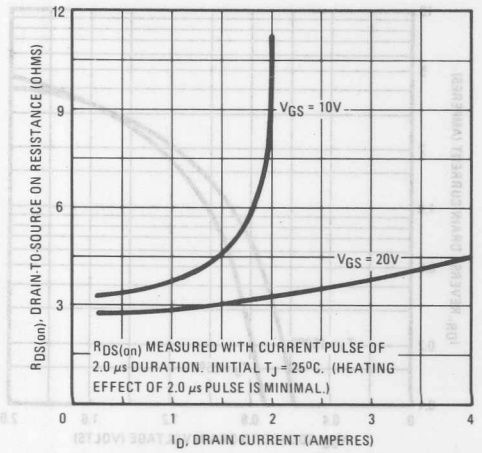


Fig. 11 — Typical On-Resistance Vs. Drain Current

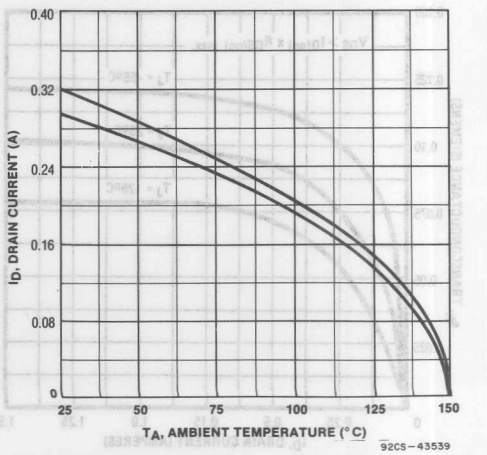


Fig. 12 — Maximum Drain Current Vs. Case Temperature

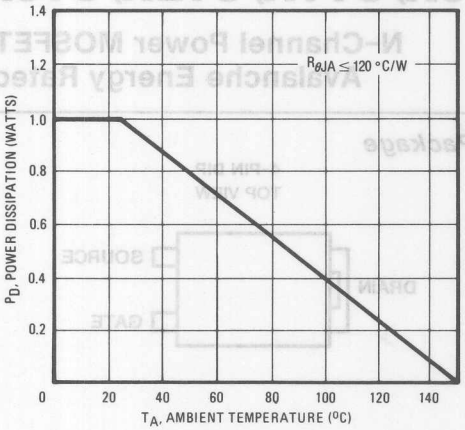


Fig. 13 — Power Vs. Temperature Derating Curve

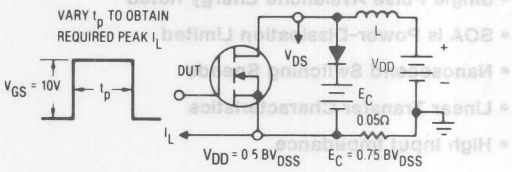


Fig. 14 — Clamped Inductive Test Circuit

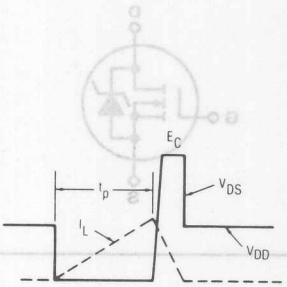


Fig. 15 — Clamped Inductive Waveforms

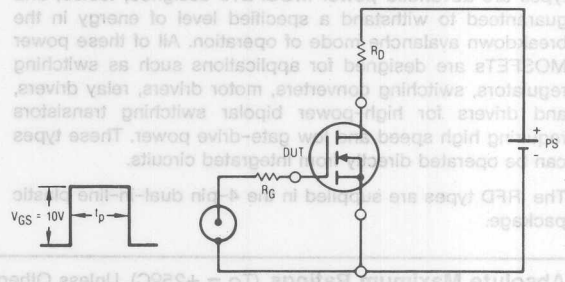


Fig. 16 — Switching Time Test Circuit

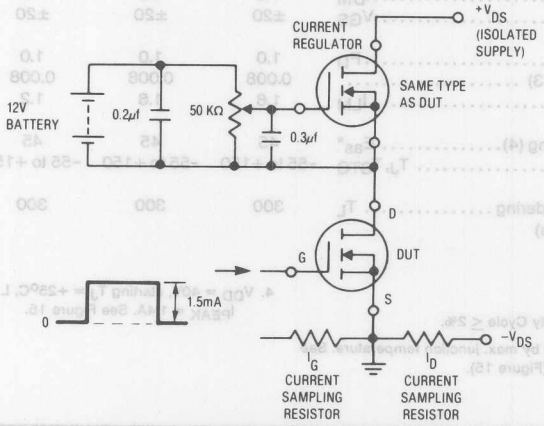


Fig. 17 — Gate Charge Test Circuit

Features

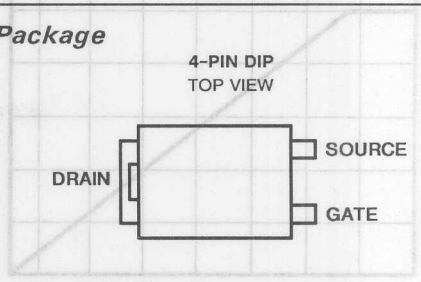
- 0.3A and 0.4A, 350V - 400V
- $r_{DS(on)}$ = 3.6Ω and 5.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFD310, IRFD311, IRFD312, and IRFD313 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD310R, IRFD311R, IRFD312R, and IRFD313R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

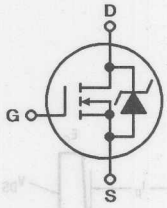
The IRFD types are supplied in the 4-pin dual-in-line plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD310 IRFD310R	IRFD311 IRFD311R	IRFD312 IRFD312R	IRFD313 IRFD313R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current T_C = +25°C ..... I_D	0.4	0.4	0.3	0.3	A
Pulsed Drain Current (3) ..... I_{DM}	1.6	1.6	1.2	1.2	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 14) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	1.6	1.6	1.2	1.2	A
Single Pulse Avalanche Energy Rating (4)..... E_{as}*	45	45	45	45	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 15).
4. V_{DD} = 40V, starting T_J = +25°C, L = 44.89mH, R_{GS} = 50Ω, I_{PEAK} = 1.4A. See Figure 15.

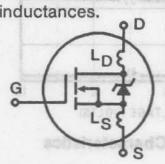
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

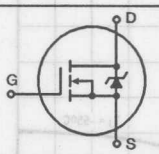
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File Number 2324.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD310/312, IRFD310R/312R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	-	-	V
IRFD311/313, IRFD311R/313R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRFD310/311, IRFD310R/311R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	0.4	-	-	A
IRFD312/313, IRFD312R/313R			0.3	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD310/311, IRFD310R/311R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.2A	-	3.3	3.6	Ω
IRFD312/313, IRFD312R/313R			-	3.6	5.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 0.2A	0.5	1.2	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	135	-	pF
Output Capacitance	C_{OSS}		-	35	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	8.0	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 0.4A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature)	-	3.0	10	ns
Rise Time	t_r		-	10	20	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	5.0	10	ns
Fall Time	t_f		-	8.0	15	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 0.4A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	6.0	7.5	nC
Gate-Source Charge	Q_{gs}		-	3.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	3.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	0.4	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	1.6	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 1.6A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 1.6A, dI_F/dt = 100A/µs	-	380	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 1.6A, dI_F/dt = 100A/µs	-	2.7	-	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 44.89mH, R_{GS} = 50Ω, I_{PEAK} = 1.4A. (See Figure 15.)

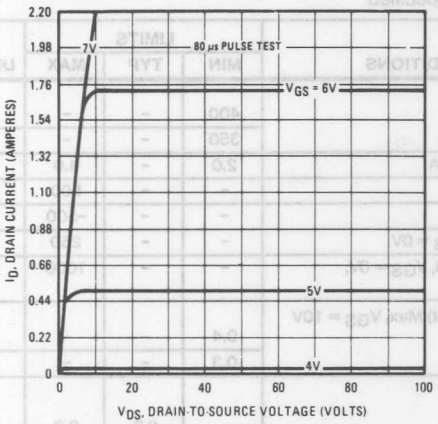


Fig. 1 — Typical Output Characteristics

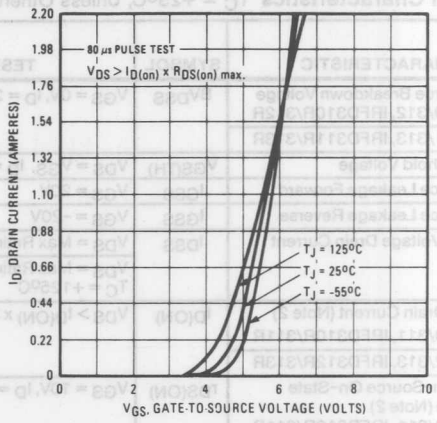


Fig. 2 — Typical Transfer Characteristics

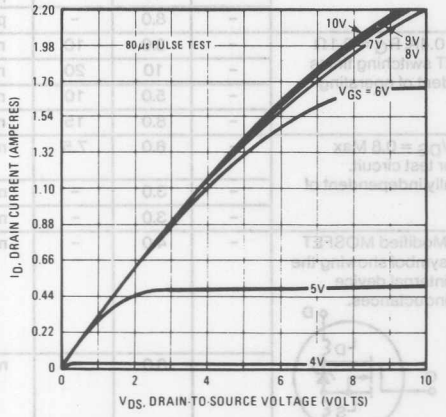


Fig. 3 — Typical Saturation Characteristics

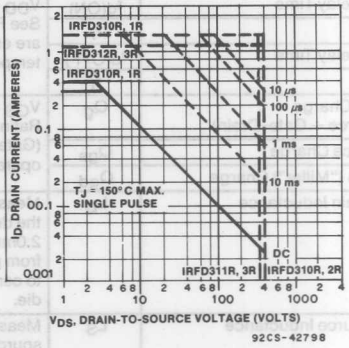


Fig. 4 — Maximum Safe Operating Area

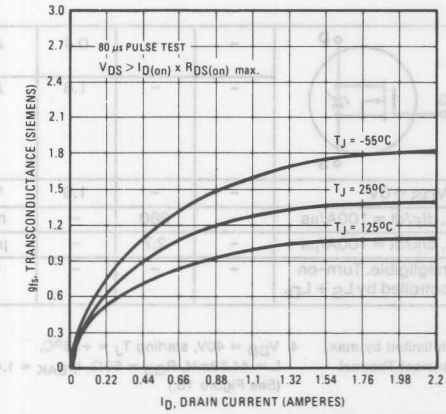


Fig. 5 — Typical Transconductance Vs. Drain Current

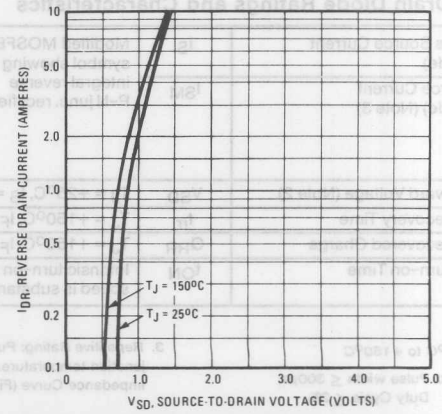


Fig. 6 — Typical Source-Drain Diode Forward Voltage

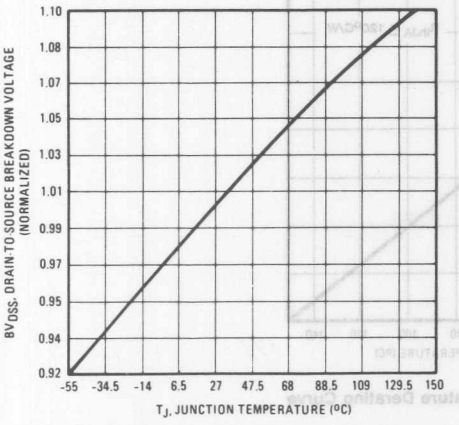


Fig. 7 — Breakdown Voltage Vs. Temperature

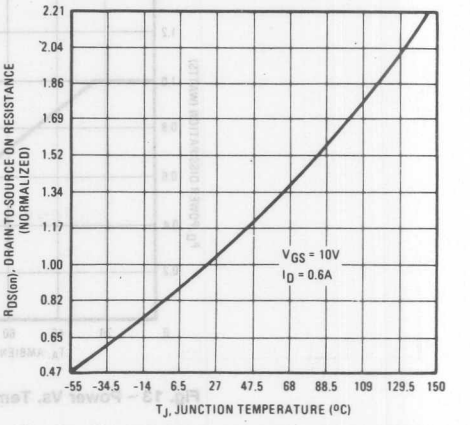


Fig. 8 — Normalized On-Resistance Vs. Temperature

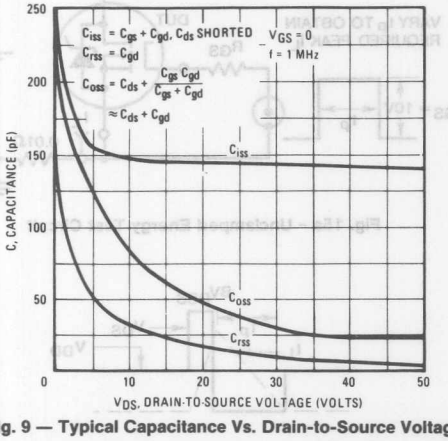


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

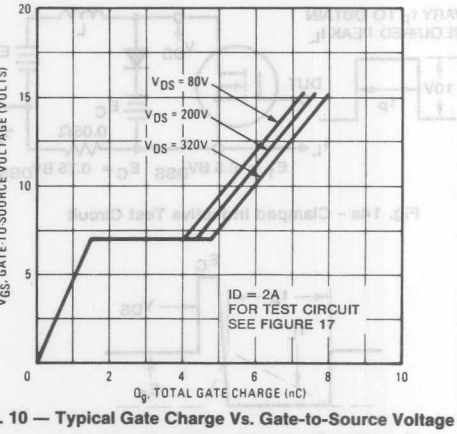


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

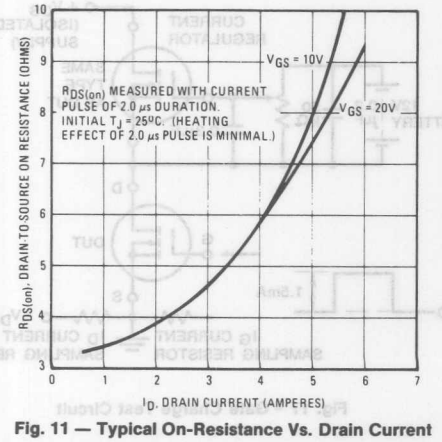


Fig. 11 — Typical On-Resistance Vs. Drain Current

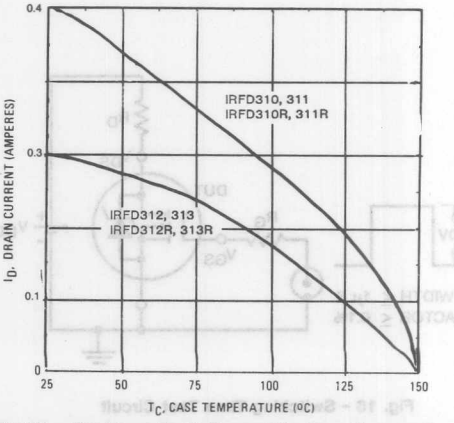


Fig. 12 — Maximum Drain Current Vs. Case Temperature

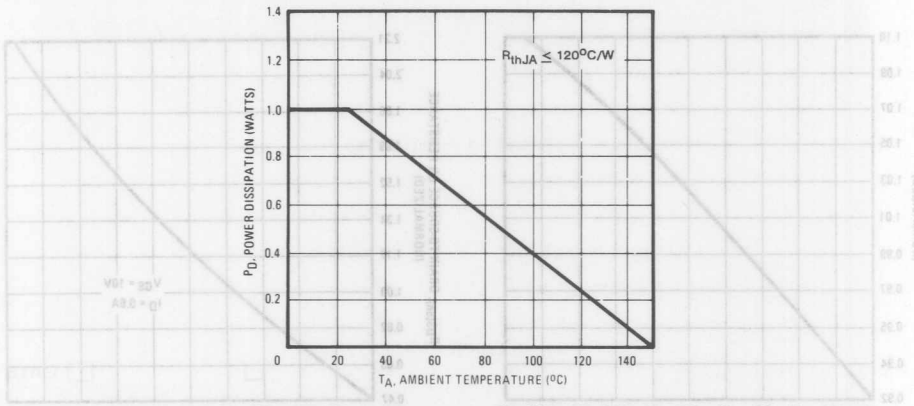


Fig. 13 - Power Vs. Temperature Derating Curve

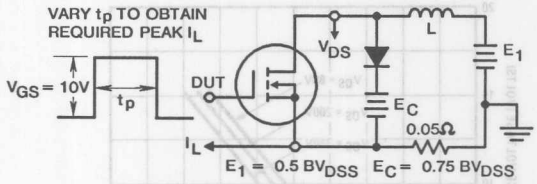


Fig. 14a - Clamped Inductive Test Circuit

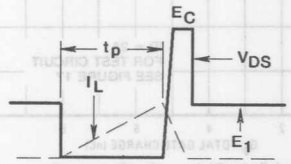


Fig. 14b - Clamped Inductive Waveforms

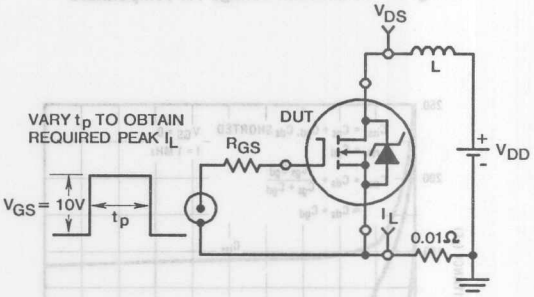


Fig. 15a - Unclamped Energy Test Circuit

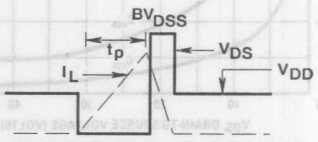


Fig. 15b - Unclamped Energy Waveforms

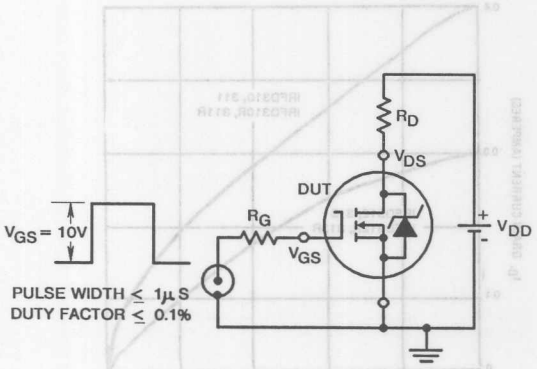


Fig. 16 - Switching Time Test Circuit

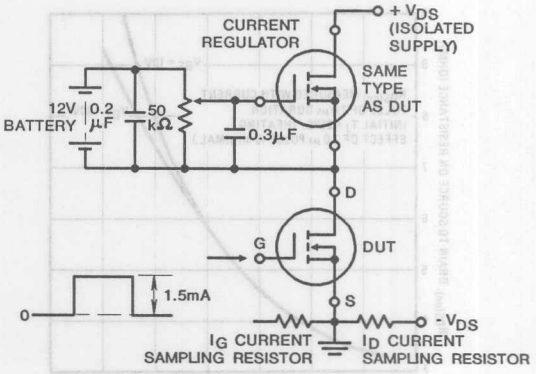


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFD320/321/322/323
IRFD320R/321R/322R/323R

N-Channel Power MOSFETs
Avalanche Energy Rated*

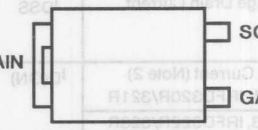
August 1991

Features

- 0.5A and 0.4A, 350V - 400V
- $r_{DS(on)}$ = 1.8Ω and 2.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

4-PIN DIP
TOP VIEW



Description

The IRFD320, IRFD332, IRFD322, and IRFD323 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD320R, IRFD332R, IRFD322R, and IRFD323R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin dual-in-line plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD320 IRFD320R	IRFD332 IRFD332R	IRFD322 IRFD322R	IRFD323 IRFD323R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current T_C = +25°C ..... I_D	0.5	0.5	0.4	0.4	A
Pulsed Drain Current (3) ..... I_{DM}	2.0	2.0	1.6	1.6	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	2.0	2.0	1.6	1.6	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	100	100	100	100	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 29.09mH, R_{GS} = 50Ω, I_{PEAK} = 2.5A. See Figure 15.

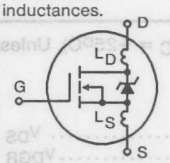
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

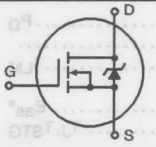
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File Number **2325.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD320/322, IRFD320R/322R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	-	-	V
IRFD321/323, IRFD321R/323R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFD320/321, IRFD320R/321R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	0.5	-	-	A
IRFD322/323, IRFD322R/323R			0.4	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD320/321, IRFD320R/321R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.25A	-	1.5	1.8	Ω
IRFD322/323, IRFD322R/323R			-	1.8	2.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 0.25A	1.0	2.0	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	455	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	20	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 0.5BV_{DSS}, I_D = 0.5A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	20	40	ns
Rise Time	t_r		-	25	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	25	50	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 0.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	12	15	nC
Gate-Source Charge	Q_{gs}		-	6.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	6.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	0.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	2.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.0A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 2.0A, dI_F/dt = 100A/μs	-	450	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 2.0A, dI_F/dt = 100A/μs	-	3.1	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 29.09mH, R_{GS} = 50Ω, I_{PEAK} = 2.5A (See Figure 15.)

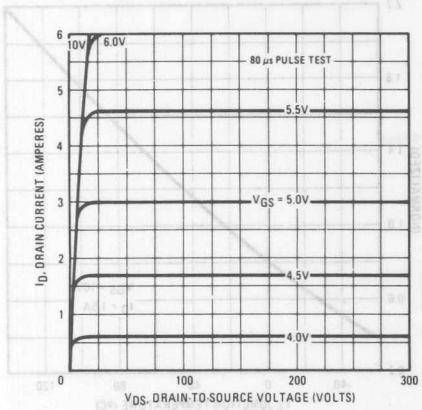


Fig. 1 — Typical Output Characteristics

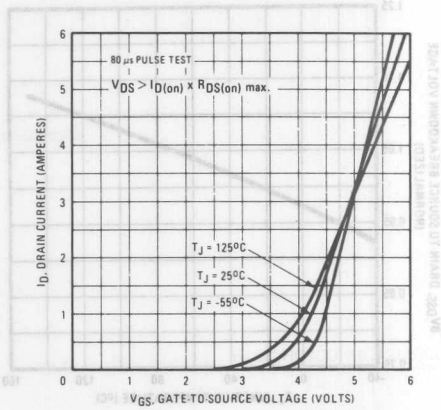


Fig. 2 — Typical Transfer Characteristics

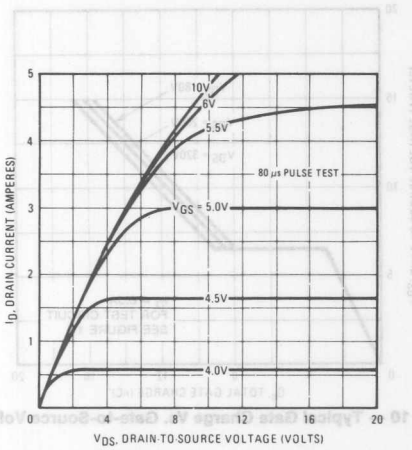


Fig. 3 — Typical Saturation Characteristics

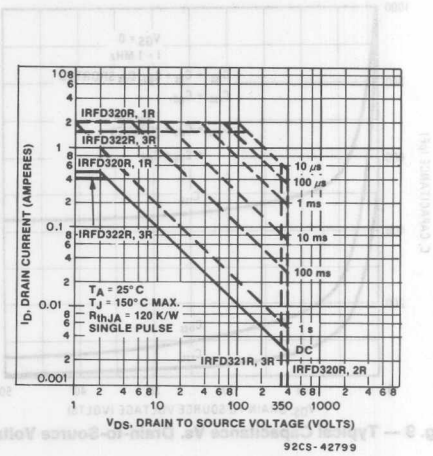


Fig. 4 — Maximum Safe Operating Area

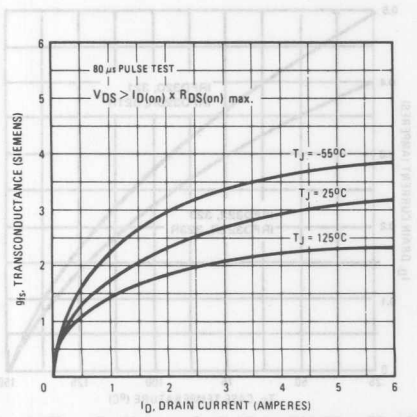


Fig. 5 — Typical Transconductance Vs. Drain Current

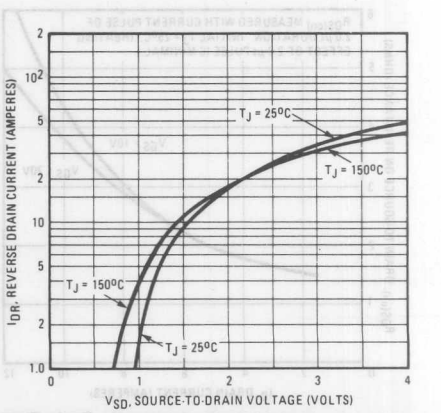


Fig. 6 — Typical Source-Drain Diode Forward Voltage

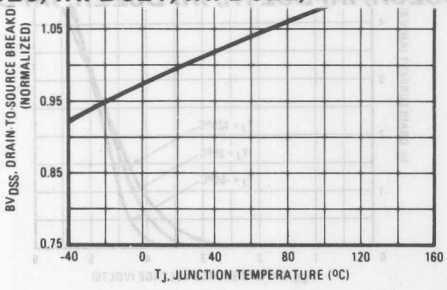


Fig. 7 — Breakdown Voltage Vs. Temperature

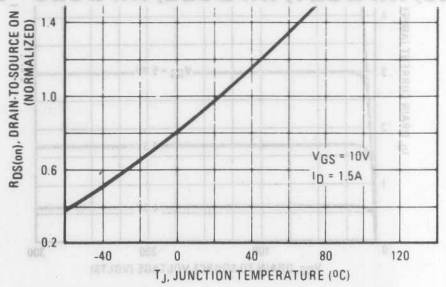


Fig. 8 — Normalized On-Resistance Vs. Temperature

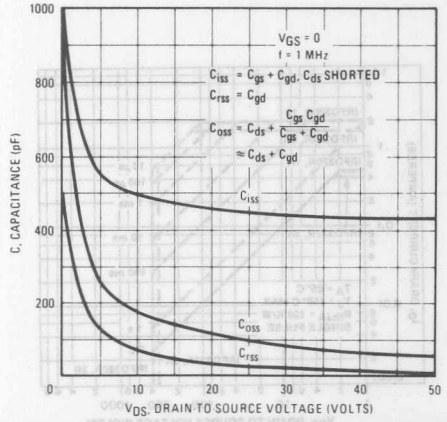


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

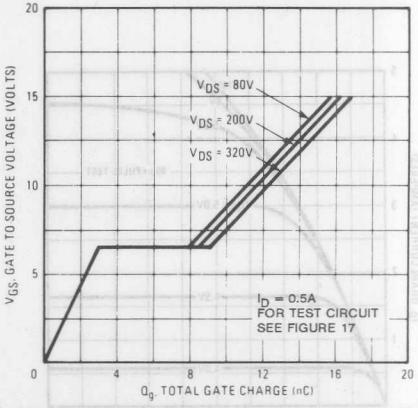


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

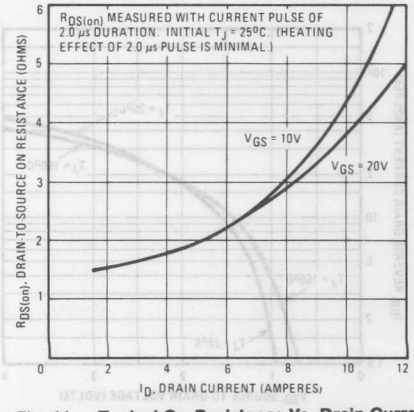


Fig. 11 — Typical On-Resistance Vs. Drain Current

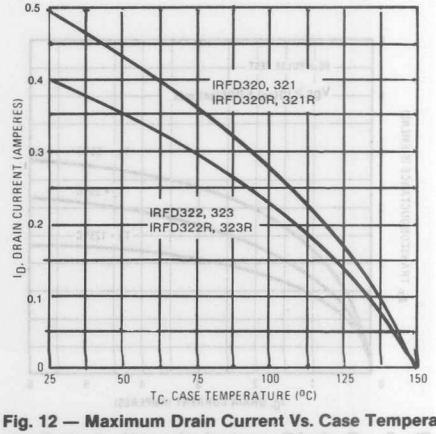


Fig. 12 — Maximum Drain Current Vs. Case Temperature

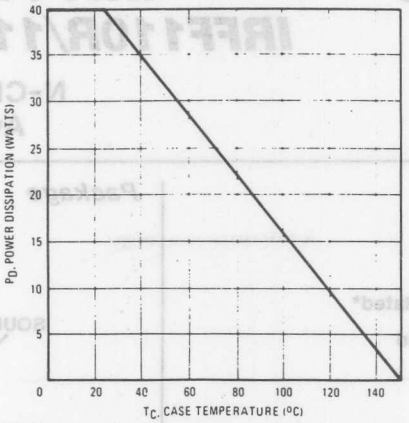


Fig. 13 - Power Vs. Temperature Derating Curve

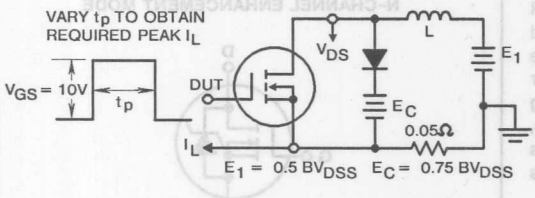


Fig. 14a - Clamped Inductive Test Circuit

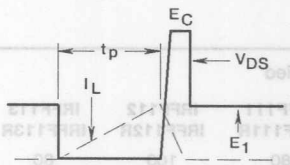


Fig. 14b - Clamped Inductive Waveforms

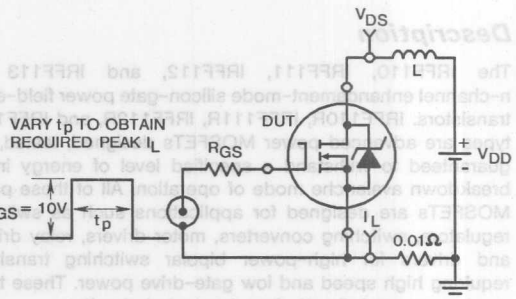


Fig. 15a - Unclamped Energy Test Circuit

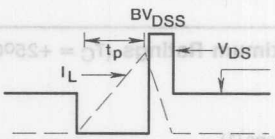


Fig. 15b - Unclamped Energy Waveforms

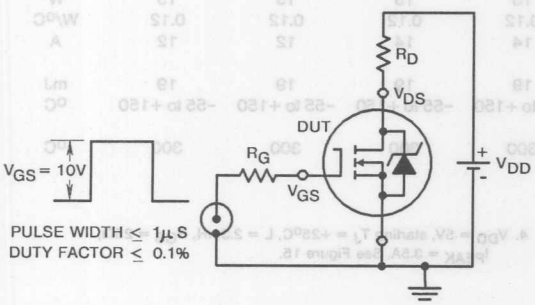


Fig. 16 - Switching Time Test Circuit

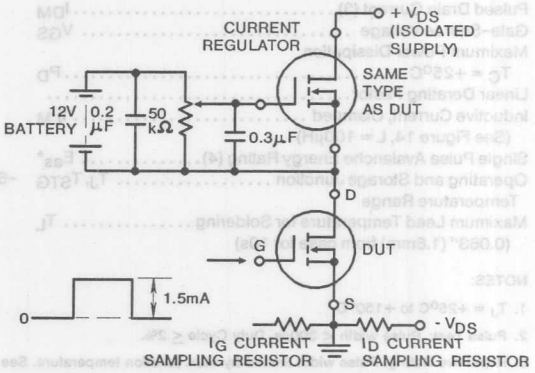


Fig. 17 - Gate Charge Test Circuit

IRFF110/111/112/113
IRFF110R/111R/112R/113R

N-Channel Power MOSFETs
Avalanche Energy Rated*

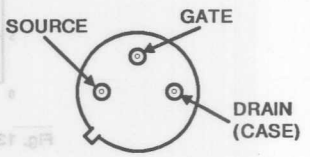
August 1991

Features

- 3.0A and 3.5A, 80V - 100V
- $r_{DS(on)}$ = 0.6Ω and 0.8Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-205AF
BOTTOM VIEW



Description

The IRFF110, IRFF111, IRFF112, and IRFF113 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF110R, IRFF111R, IRFF112R, and IRFF113R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF110 IRFF110R	IRFF111 IRFF111R	IRFF112 IRFF112R	IRFF113 IRFF113R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current T_C = +25°C ..... I_D	3.5	3.5	3.0	3.0	A
Pulsed Drain Current (3) ..... I_{DM}	14	14	12	12	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	15	15	15	15	W
Linear Derating Factor	0.12	0.12	0.12	0.12	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	14	14	12	12	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	19	19	19	19	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 5V, starting T_J = +25°C, L = 2.3mH, R_{GS} = 25Ω, I_{PEAK} = 3.5A. See Figure 15.

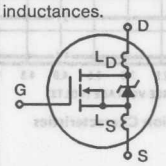
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

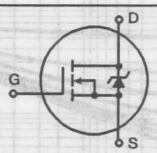
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File Number **1562.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF110/112, IRFF110R/112R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	-	-	V
IRFF111/113, IRFF111R/113R			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRFF110/111, IRFF110R/111R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	3.5	-	-	A
IRFF112/113, IRFF112R/113R			3.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF110/111, IRFF110R/111R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.5A	-	0.5	0.6	Ω
IRFF112/113, IRFF112R/113R			-	0.6	0.8	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.5A	1.0	1.5	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	135	-	pF
Output Capacitance	C_{OSS}		-	80	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	20	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 0.5BV_{DSS}, I_D = 3.5A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	10	20	ns
Rise Time	t_r		-	15	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	15	25	ns
Fall Time	t_f		-	10	20	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	5.0	7.5	nC
Gate-Source Charge	Q_{gs}		-	2.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	3.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	8.33	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	3.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	14	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.5A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 3.5A, dI_F/dt = 100A/µs	-	200	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 3.5A, dI_F/dt = 100A/µs	-	1.0	-	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 5V, starting T_J = +25°C, L = 2.3mH, R_{GS} = 25Ω, I_{PEAK} = 3.5A. (See Figure 15.)

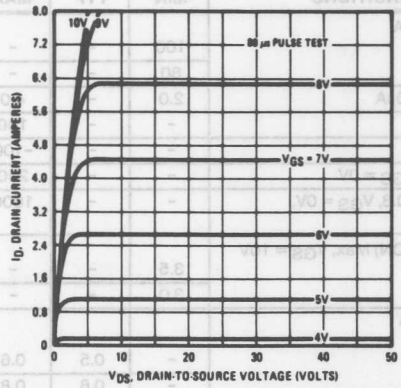


Fig. 1 – Typical Output Characteristics

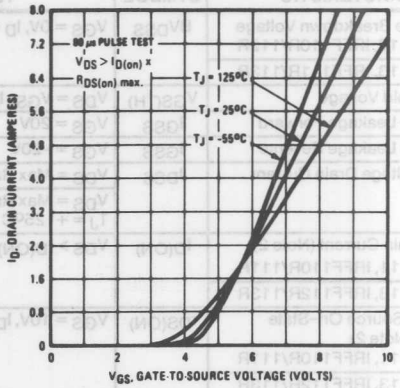


Fig. 2 – Typical Transfer Characteristics

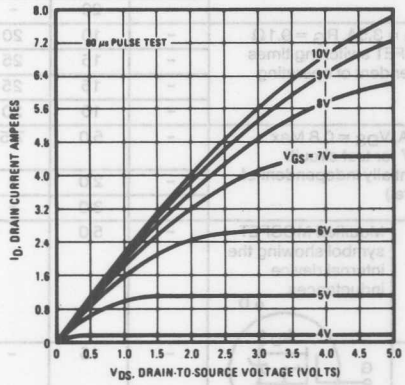


Fig. 3 – Typical Saturation Characteristics

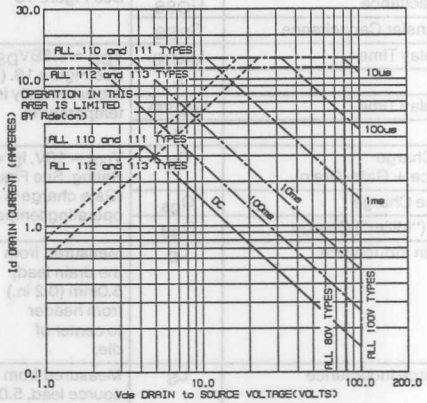


Fig. 4 – Maximum Safe Operating Area

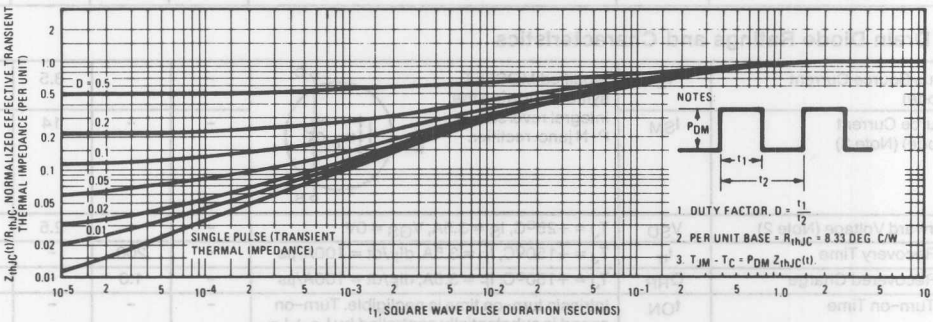


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

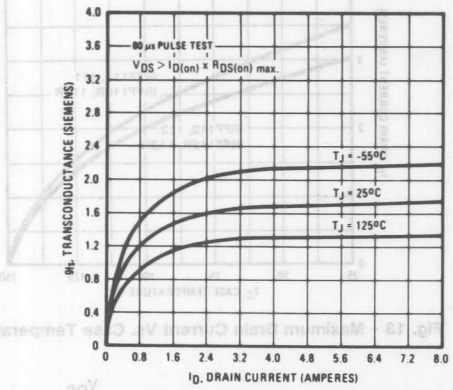


Fig. 6 – Typical Transconductance Vs. Drain Current

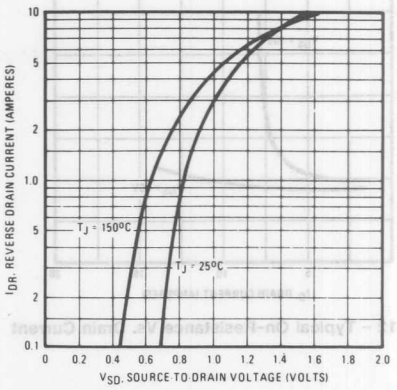


Fig. 7 – Typical Source-Drain Diode Forward Voltage

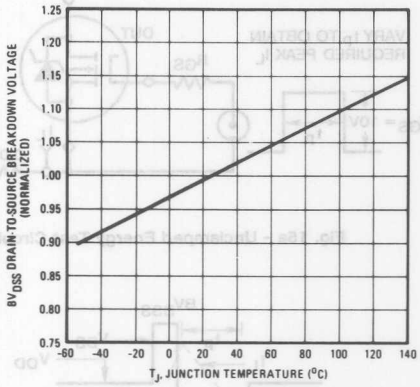


Fig. 8 – Breakdown Voltage Vs. Temperature

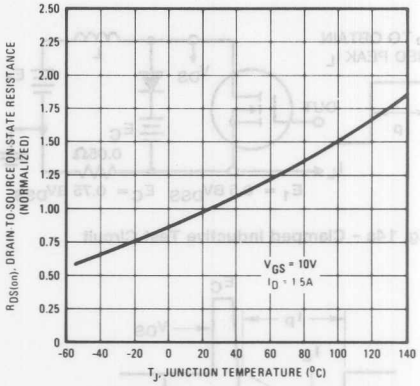


Fig. 9 – Normalized On-Resistance Vs. Temperature

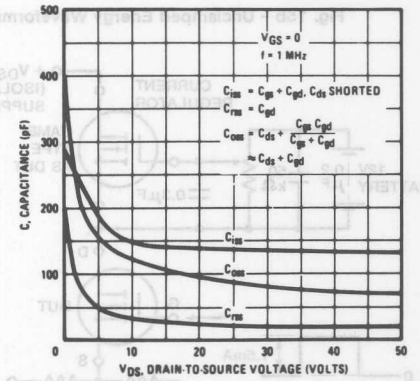


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

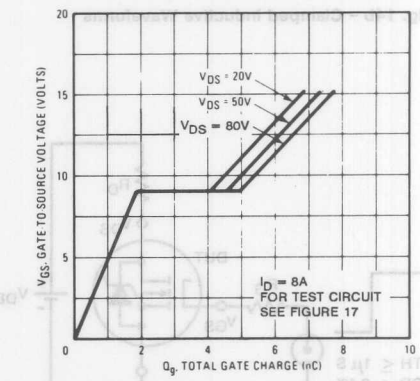


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

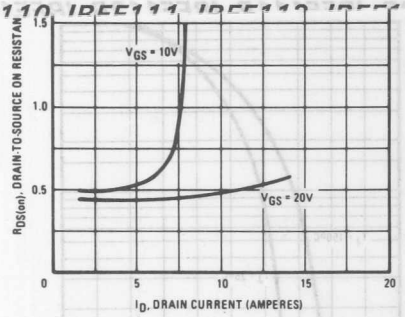


Figure 12 - Typical On-Resistance Vs. Drain Current

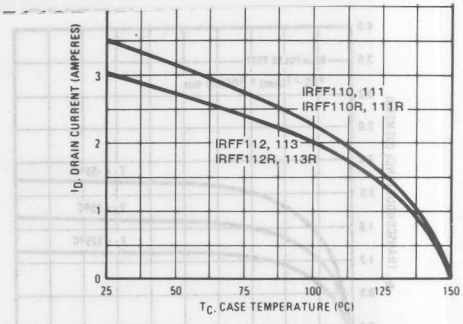


Fig. 13 - Maximum Drain Current Vs. Case Temperature

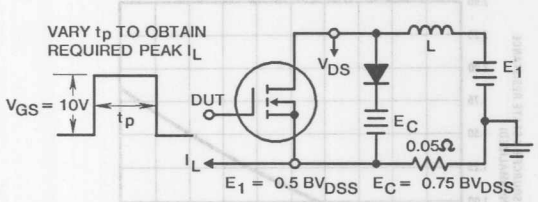


Fig. 14a - Clamped Inductive Test Circuit

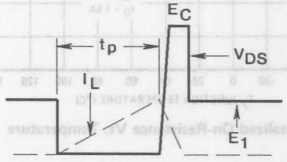


Fig. 14b - Clamped Inductive Waveforms

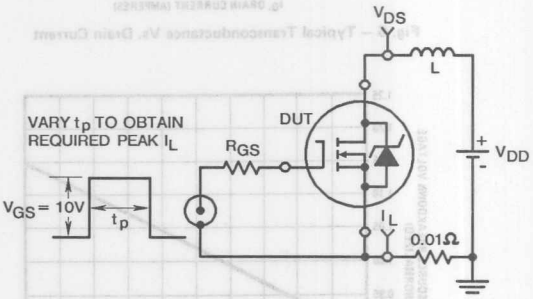


Fig. 15a - Unclamped Energy Test Circuit

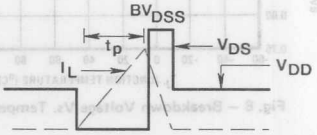


Fig. 15b - Unclamped Energy Waveforms

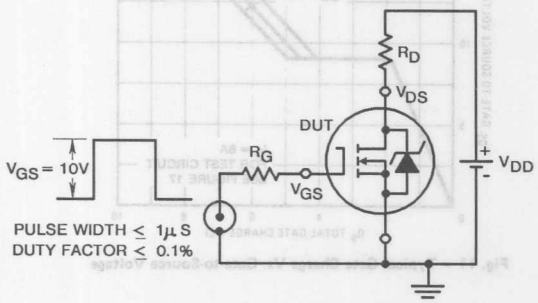


Fig. 16 - Switching Time Test Circuit

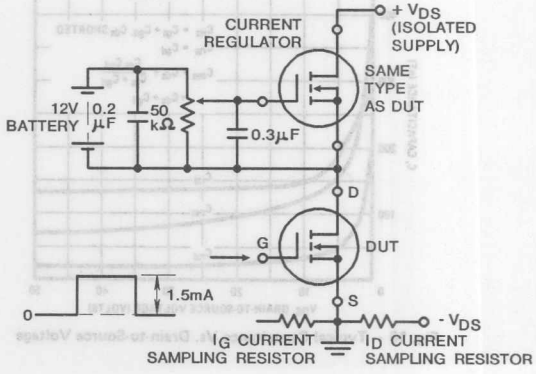


Fig. 17 - Gate Charge Test Circuit

HARRIS IRFF120/121/122/123 IRFF120R/121R/122R/123R

N-Channel Power MOSFETs Avalanche Energy Rated*

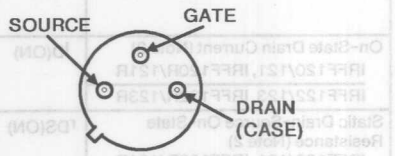
August 1991

Features

- 5.0A and 6.0A, 80V - 100V
- $r_{DS(on)}$ = 0.30Ω and 0.40Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-205AF



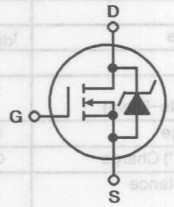
Description

The IRFF120, IRFF121, IRFF122, and IRFF123 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF120R, IRFF121R, IRFF122R, and IRFF123R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF120 IRFF120R	IRFF121 IRFF121R	IRFF122 IRFF122R	IRFF123 IRFF123R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current T_C = +25°C ..... I_D	6.0	6.0	5.0	5.0	A
Pulsed Drain Current (3) ..... I_{DM}	24	24	20	20	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	20	20	20	20	W
Linear Derating Factor	0.16	0.16	0.16	0.16	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	24	24	20	20	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	36	36	36	36	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 1.5mH, R_{GS} = 25Ω, I_{PEAK} = 6.0A. See Figure 15.

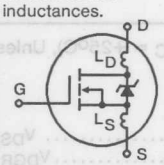
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

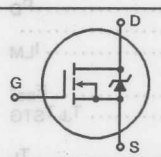
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File Number 1563.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF120/122, IRFF120R/122R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	-	-	V
IRFF121/123, IRFF121R/123R			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFF120/121, IRFF120R/121R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	6.0	-	-	A
IRFF122/123, IRFF122R/123R			5.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF120/121, IRFF120R/121R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.0A	-	0.25	0.30	Ω
IRFF122/123, IRFF122R/123R			-	0.30	0.40	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 3.0A	1.5	2.9	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	450	-	pF
Output Capacitance	C_{OSS}		-	20	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 6.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	20	40	ns
Rise Time	t_r		-	37	70	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	35	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	10	15	nC
Gate-Source Charge	Q_{gs}		-	6.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	4.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	6.25	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	6.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	24	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 6.0A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 6.0A, dI_F/dt = 100A/μs	-	230	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 6.0A, dI_F/dt = 100A/μs	-	1.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 5V, starting T_J = +25°C, L = 1.5mH, R_{GS} = 25Ω, I_{PEAK} = 6.0A. (See Figure 15.)

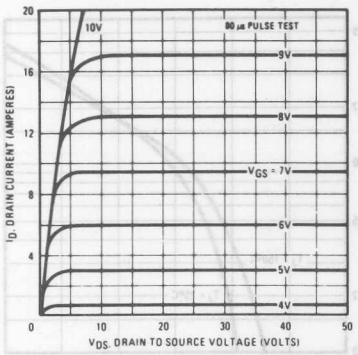


Fig. 1 – Typical Output Characteristics

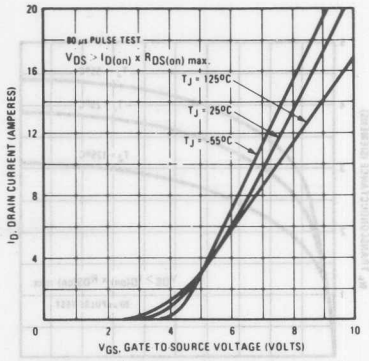


Fig. 2 – Typical Transfer Characteristics

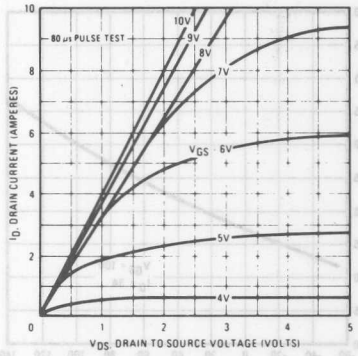


Fig. 3 – Typical Saturation Characteristics

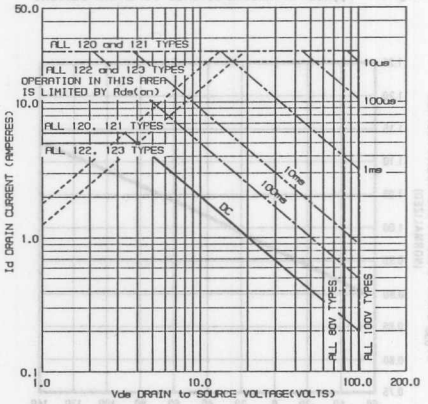


Fig. 4 – Maximum Safe Operating Area

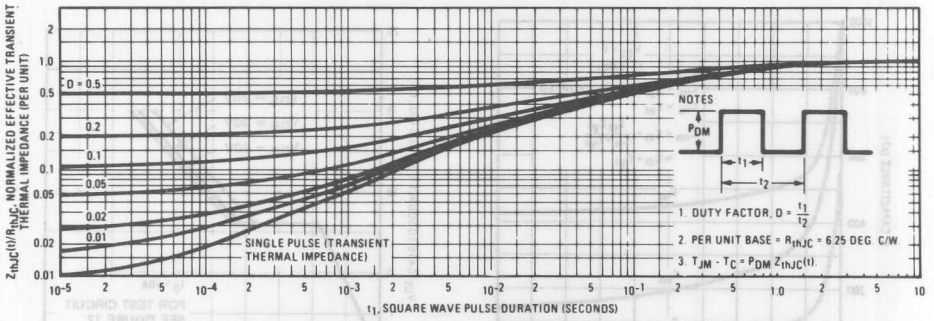


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

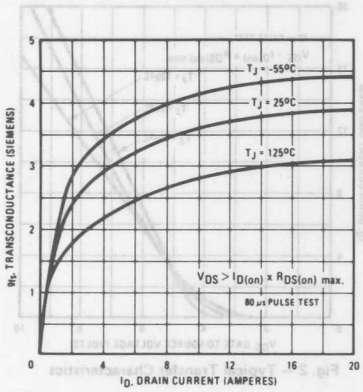


Fig. 6 – Typical Transconductance Vs. Drain Current

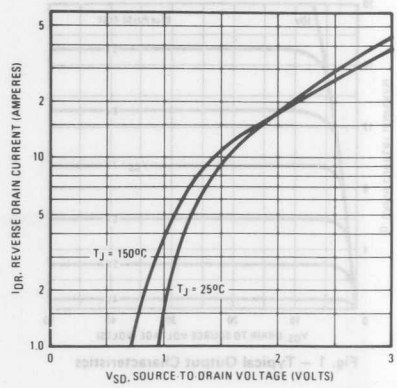


Fig. 7 – Typical Source-Drain Diode Forward Voltage

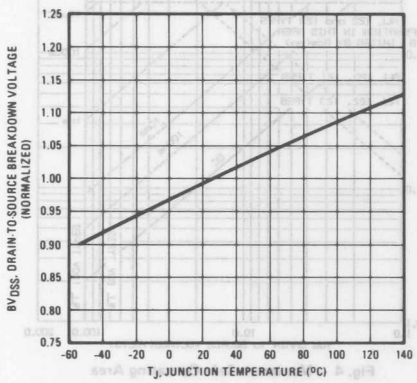


Fig. 8 – Breakdown Voltage Vs. Temperature

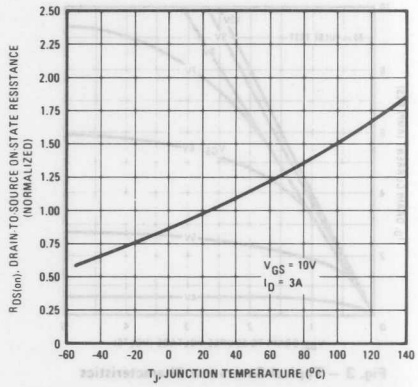


Fig. 9 – Normalized On-Resistance Vs. Temperature

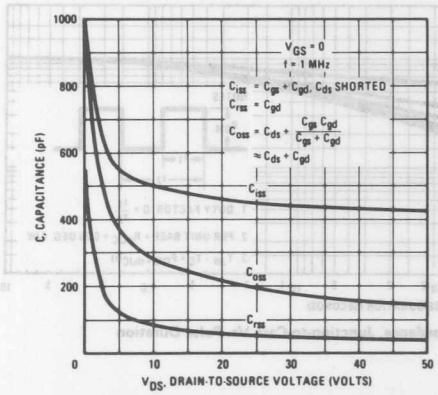


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

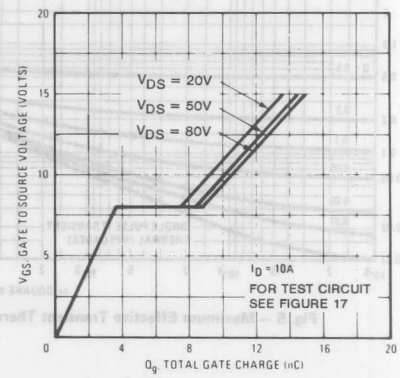


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

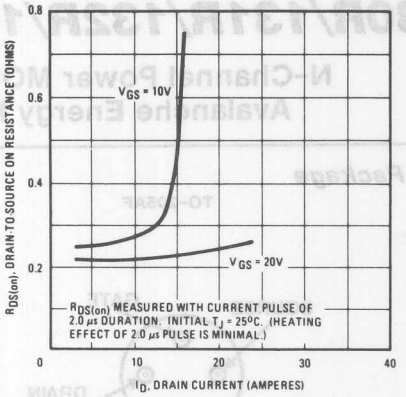


Figure 12 - Typical On-Resistance Vs. Drain Current

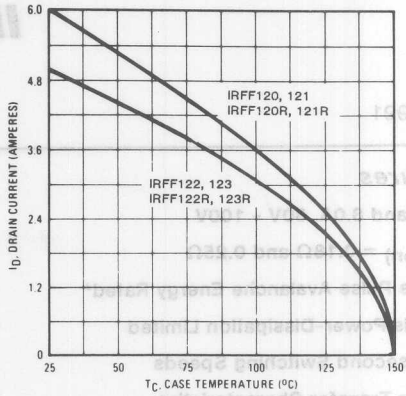


Fig. 13 - Maximum Drain Current Vs. Case Temperature

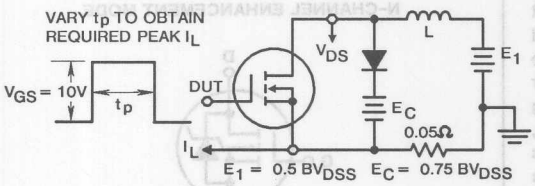


Fig. 14a - Clamped Inductive Test Circuit

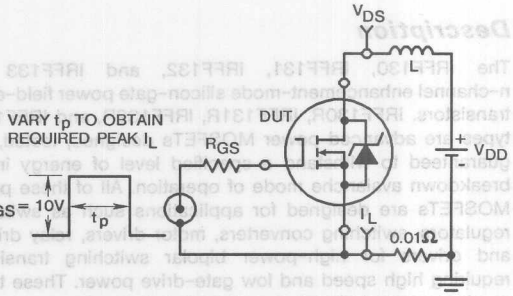


Fig. 15a - Unclamped Energy Test Circuit

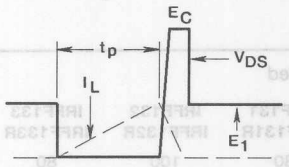


Fig. 14b - Clamped Inductive Waveforms

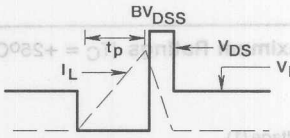


Fig. 15b - Unclamped Energy Waveforms

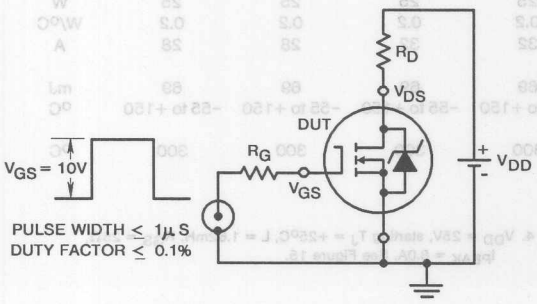


Fig. 16 - Switching Time Test Circuit

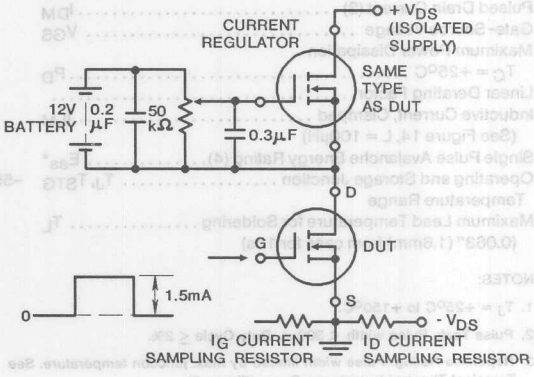


Fig. 17 - Gate Charge Test Circuit

IRFF130/131/132/133
IRFF130R/131R/132R/133R

N-Channel Power MOSFETs
Avalanche Energy Rated*

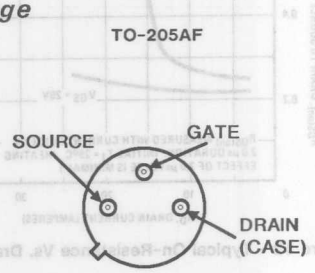
August 1991

Features

- 7.0A and 8.0A, 80V - 100V
- $r_{DS(on)}$ = 0.18Ω and 0.25Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-205AF



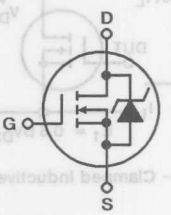
Description

The IRFF130, IRFF131, IRFF132, and IRFF133 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF130R, IRFF131R, IRFF132R, and IRFF133R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF130 IRFF130R	IRFF131 IRFF131R	IRFF132 IRFF132R	IRFF133 IRFF133R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current T_C = +25°C ..... I_D	8.0	8.0	7.0	7.0	A
Pulsed Drain Current (3) ..... I_{DM}	32	32	28	28	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	25	25	25	25	W
Linear Derating Factor	0.2	0.2	0.2	0.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	32	32	28	28	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	69	69	69	69	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 1.62mH, R_{GS} = 25Ω, I_{PEAK} = 8.0A. See Figure 15.

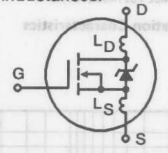
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

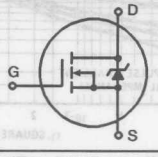
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File Number **1564.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF130/132, IRFF130R/132R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	–	–	V
IRFF131/133, IRFF131R/133R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFF130/131, IRFF130R/131R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	8.0	–	–	A
IRFF132/133, IRFF132R/133R			7.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF130/131, IRFF130R/131R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.0A	–	0.14	0.18	Ω
IRFF132/133, IRFF132R/133R			–	0.20	0.25	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 4.0A	4.0	5.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	300	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	100	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 8.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	30	50	ns
Rise Time	t_r		–	80	150	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	100	ns
Fall Time	t_f		–	80	150	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	18	30	nC
Gate-Source Charge	Q_{gs}		–	9.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	9.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	8.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.0A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 8.0A, dI_F/dt = 100A/μs	–	300	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 8.0A, dI_F/dt = 100A/μs	–	1.5	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 25V, starting T_J = +25°C, L = 1.62mH, R_{GS} = 25Ω, I_{PEAK} = 8.0A. (See Figure 15.)

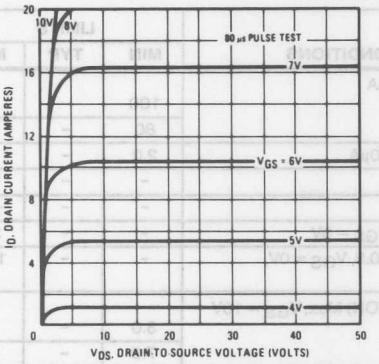


Fig. 1 – Typical Output Characteristics

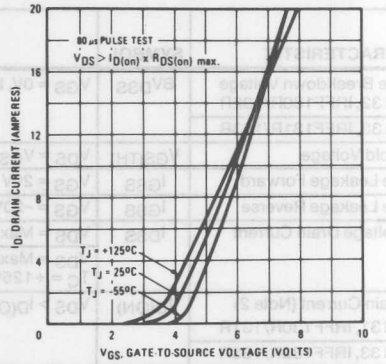


Fig. 2 – Typical Transfer Characteristics

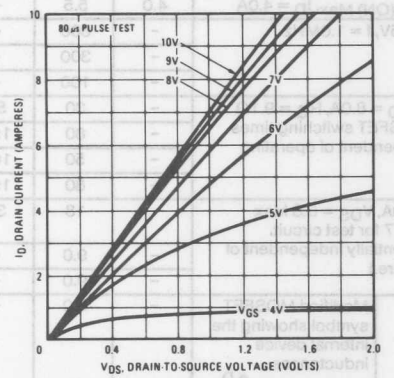


Fig. 3 – Typical Saturation Characteristics

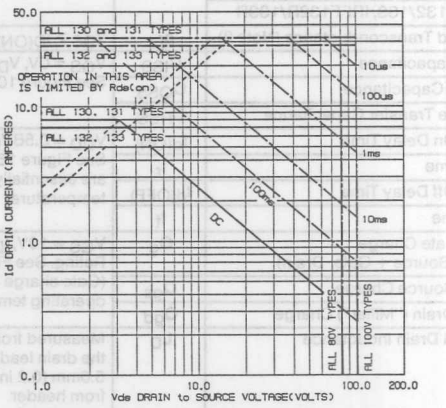


Fig. 4 – Maximum Safe Operating Area

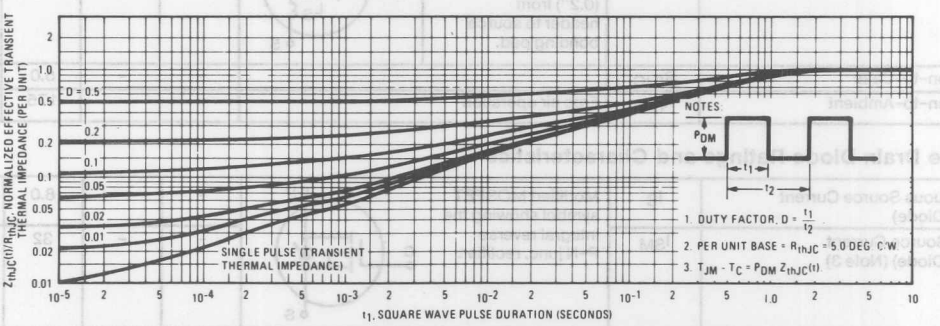


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

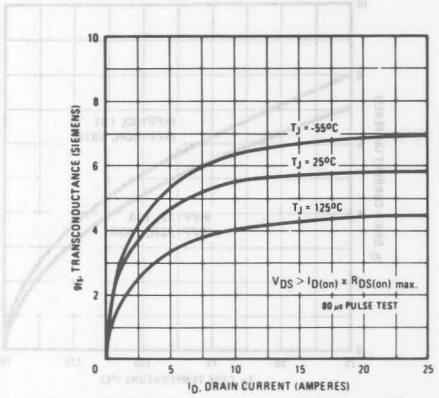


Fig. 6 – Typical Transconductance Vs. Drain Current

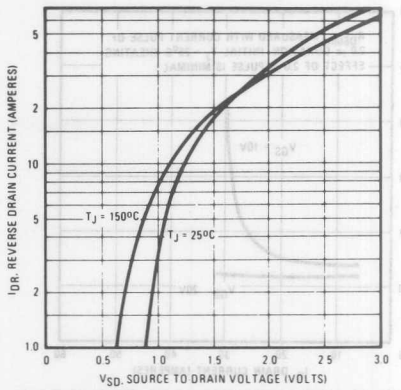


Fig. 7 – Typical Source-Drain Diode Forward Voltage

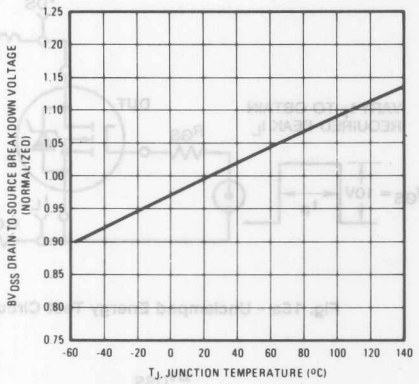


Fig. 8 – Breakdown Voltage Vs. Temperature

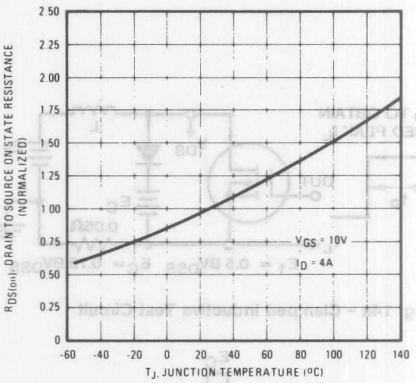


Fig. 9 – Normalized On-Resistance Vs. Temperature

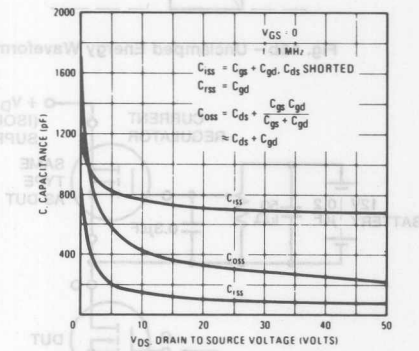


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

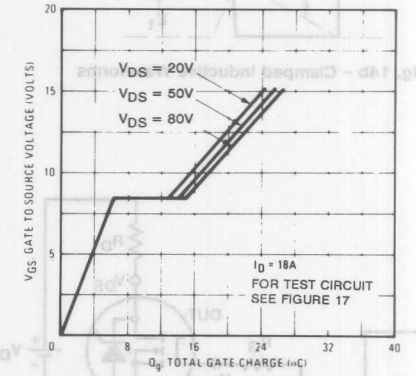


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

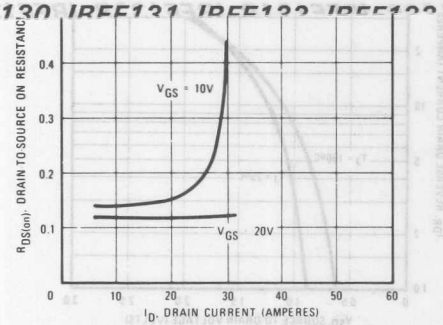


Figure 12 - Typical On-Resistance Vs. Drain Current

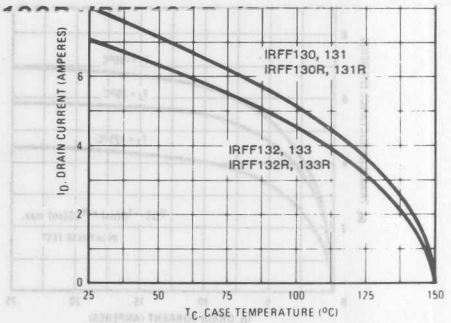


Fig. 13 - Maximum Drain Current Vs. Case Temperature

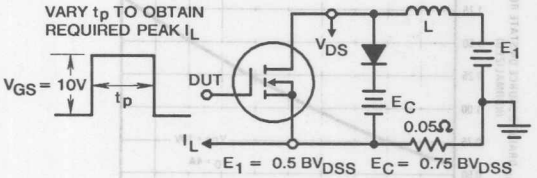


Fig. 14a - Clamped Inductive Test Circuit

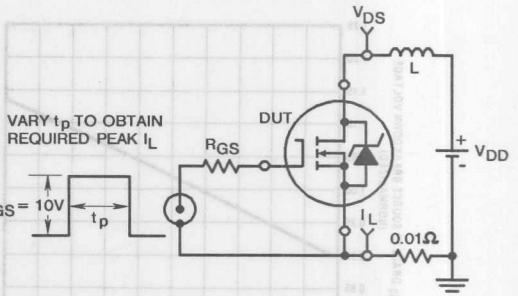


Fig. 15a - Unclamped Energy Test Circuit

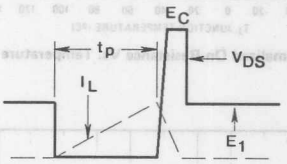


Fig. 14b - Clamped Inductive Waveforms

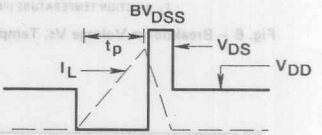


Fig. 15b - Unclamped Energy Waveforms

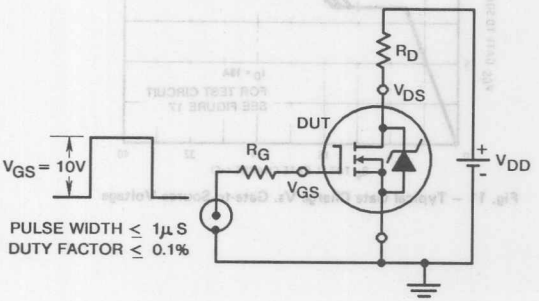


Fig. 16 - Switching Time Test Circuit

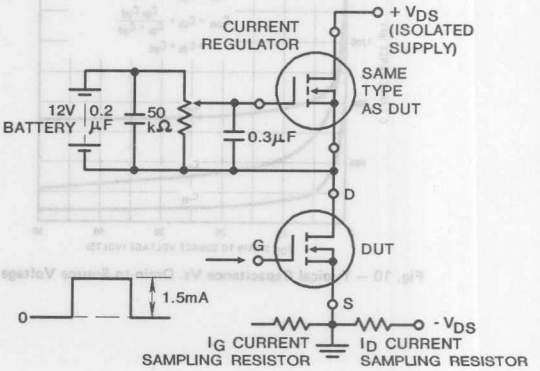


Fig. 17 - Gate Charge Test Circuit

IRFF210/211/212/213
IRFF210R/211R/212R/213R

N-Channel Power MOSFETs
Avalanche Energy Rated*

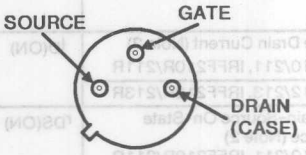
August 1991

Features

- 1.8A and 2.2A, 150V - 200V
- $r_{DS(on)}$ = 1.5Ω and 2.4Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-205AF
BOTTOM VIEW



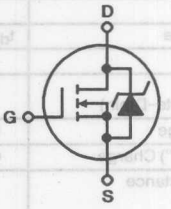
Description

The IRFF210, IRFF211, IRFF212, and IRFF213 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF210R, IRFF211R, IRFF212R, and IRFF213R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF210 IRFF210R	IRFF211 IRFF211R	IRFF212 IRFF212R	IRFF213 IRFF213R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C ..... I_D	2.2	2.2	1.8	1.8	A
Pulsed Drain Current (3) ..... I_{DM}	9.0	9.0	7.5	7.5	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	15	15	15	15	W
Linear Derating Factor	0.12	0.12	0.12	0.12	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	9.0	9.0	7.5	7.5	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	30	30	30	30	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 20V, starting T_J = +25°C, L = 11.16mH, R_{GS} = 50Ω, I_{PEAK} = 2.2A. See Figure 15.

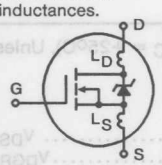
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

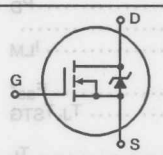
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Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF210/212, IRFF210R/212R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	200	-	-	V
IRFF211/213, IRFF211R/213R			150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFF210/211, IRFF210R/211R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	2.2	-	-	A
IRFF212/213, IRFF212R/213R			1.8	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF210/211, IRFF210R/211R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.25A	-	1.0	1.5	Ω
IRFF212/213, IRFF212R/213R			-	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.25A	0.8	1.3	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	135	-	pF
Output Capacitance	C_{OSS}		-	60	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	16	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 0.5BV_{DSS}, I_D = 2.2A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	8.0	15	ns
Rise Time	t_r		-	15	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	10	15	ns
Fall Time	t_f		-	8.0	15	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 2.2A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	5.0	7.5	nC
Gate-Source Charge	Q_{gs}		-	2.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	3.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	8.33	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	2.2	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	9.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.2A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 2.2A, dI_F/dt = 100A/μs	-	290	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 2.2A, dI_F/dt = 100A/μs	-	2.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width < 300μs, Duty Cycle < 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 20V, starting T_J = +25°C, L = 11.16mH, R_{GS} = 50Ω, I_{PEAK} = 2.2A. (See Figure 15.)

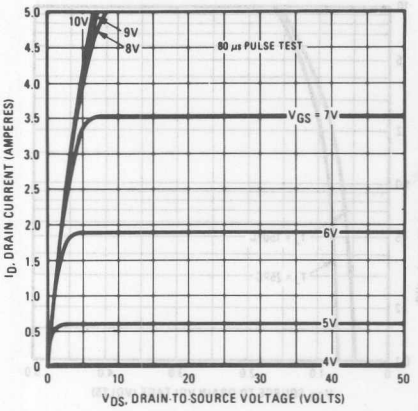


Fig. 1 - Typical output characteristics.

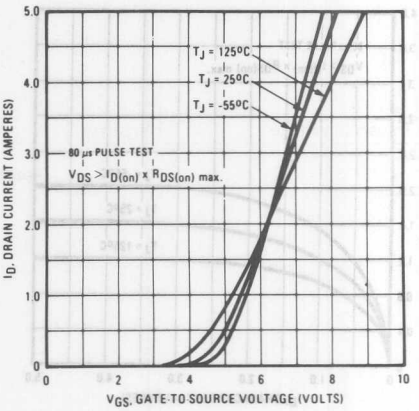


Fig. 2 - Typical transfer characteristics.

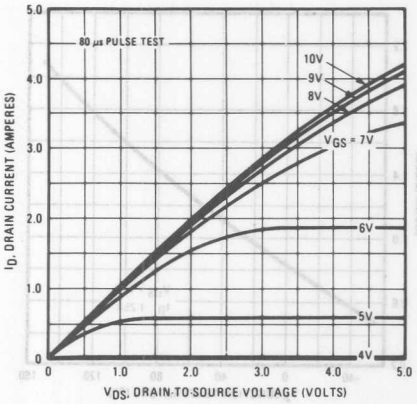


Fig. 3 - Typical saturation characteristics.

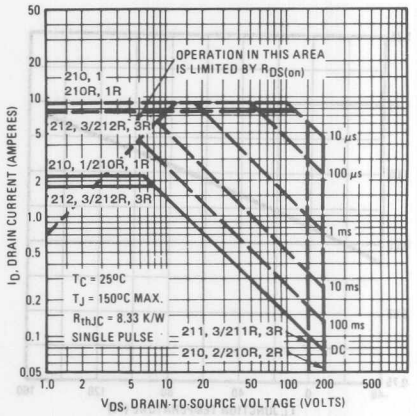


Fig. 4 - Maximum safe operating area.

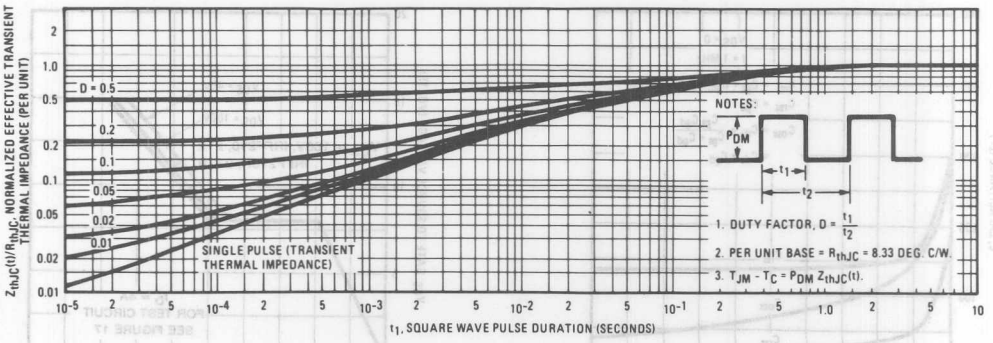


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

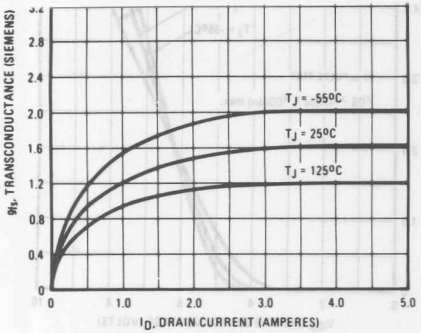


Fig. 6 - Typical transconductance vs. drain current.

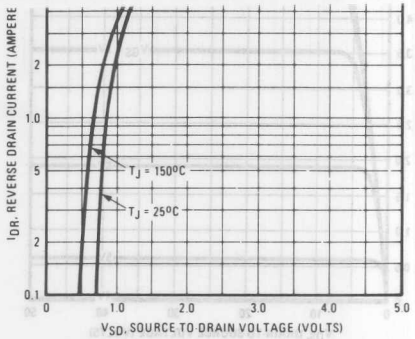


Fig. 7 - Typical source-drain diode forward voltage.

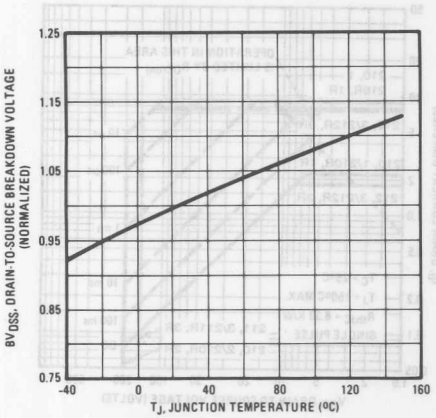


Fig. 8 - Breakdown voltage vs. temperature.

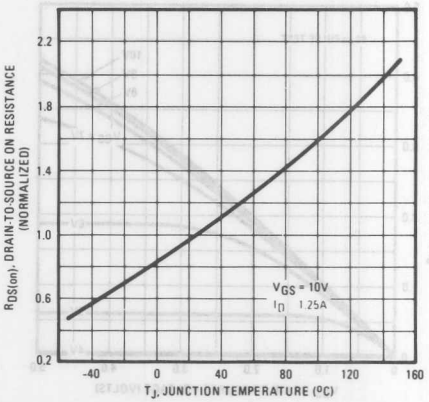


Fig. 9 - Normalized on-resistance vs. temperature.

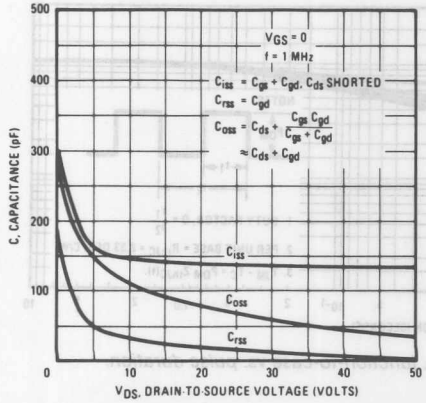


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

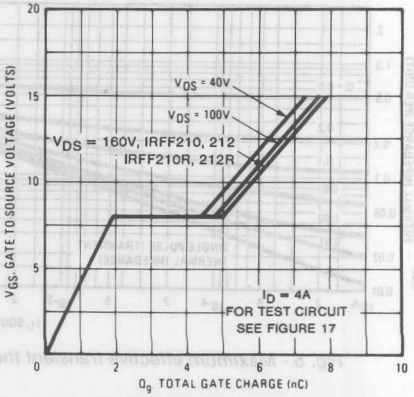


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

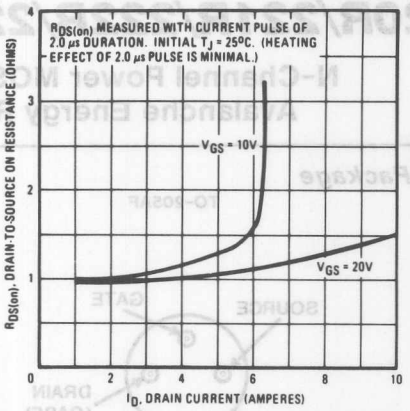


Figure 12 - Typical On-Resistance Vs. Drain Current

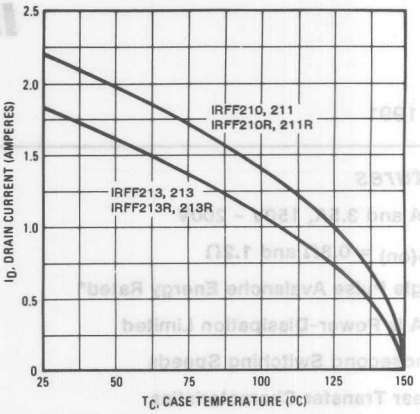


Fig. 13 - Maximum Drain Current Vs. Case Temperature

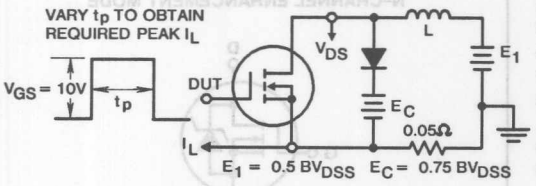


Fig. 14a - Clamped Inductive Test Circuit

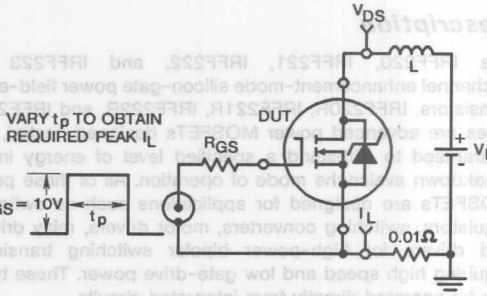


Fig. 15a - Unclamped Energy Test Circuit

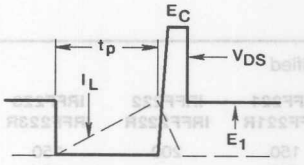


Fig. 14b - Clamped Inductive Waveforms

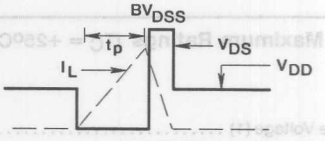


Fig. 15b - Unclamped Energy Waveforms

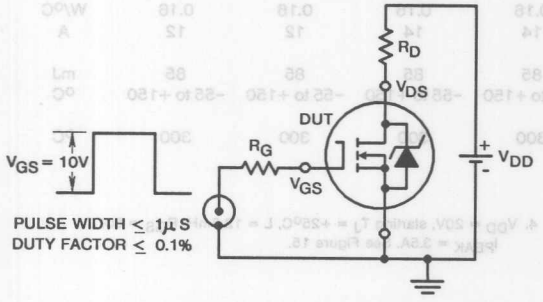


Fig. 16 - Switching Time Test Circuit

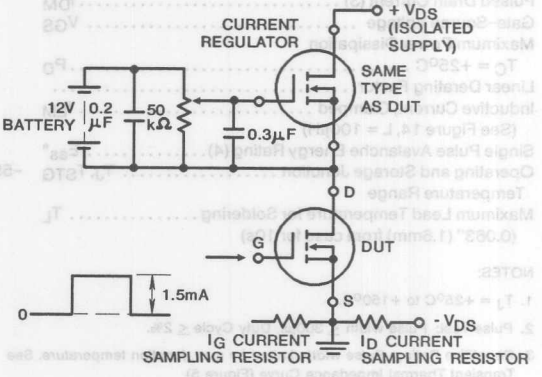


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFF220/221/222/223
IRFF220R/221R/222R/223R

N-Channel Power MOSFETs Avalanche Energy Rated*

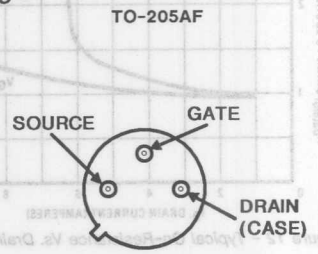
August 1991

Features

- 3.0A and 3.5A, 150V - 200V
- $r_{DS(on)}$ = 0.8Ω and 1.2Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-205AF



Description

The IRFF220, IRFF221, IRFF222, and IRFF223 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF220R, IRFF221R, IRFF222R, and IRFF223R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF220 IRFF220R	IRFF221 IRFF221R	IRFF222 IRFF222R	IRFF223 IRFF223R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C ..... I_D	3.5	3.5	3.0	3.0	A
Pulsed Drain Current (3) ..... I_{DM}	14	14	12	12	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	20	20	20	20	W
Linear Derating Factor	0.16	0.16	0.16	0.16	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	14	14	12	12	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	85	85	85	85	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 20V, starting T_J = +25°C, L = 12.5mH, R_{GS} = 50Ω, I_{PEAK} = 3.5A. See Figure 15.

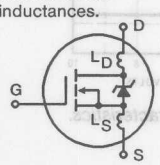
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

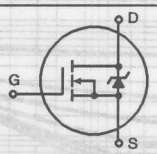
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Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF220/222, IRFF220R/222R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	-	-	V
IRFF221/223, IRFF221R/223R			150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRFF220/221, IRFF220R/221R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	3.5	-	-	A
IRFF222/223, IRFF222R/223R			3.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF220/221, IRFF220R/221R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 2.0A	-	0.5	0.8	Ω
IRFF222/223, IRFF222R/223R			-	0.8	0.2	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 2.0A	1.5	2.25	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	450	-	pF
Output Capacitance	C_{OSS}		-	150	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	40	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 3.5A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	20	40	ns
Rise Time	t_r		-	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	30	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	11	15	nC
Gate-Source Charge	Q_{gs}		-	5.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	6.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	6.25	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	3.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	14	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.5A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 3.5A, dI_F/dt = 100A/µs	-	350	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 3.5A, dI_F/dt = 100A/µs	-	2.3	-	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 20V, starting T_J = +25°C, L = 12.5mH, R_{GS} = 50Ω, I_{PEAK} = 3.5A. (See Figure 15.)

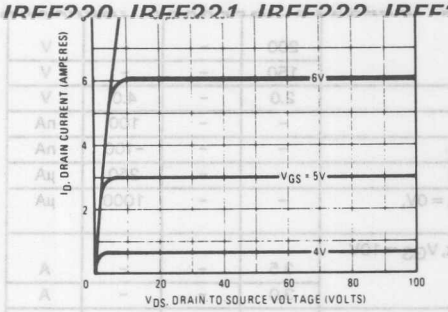


Fig. 1 - Typical output characteristics.

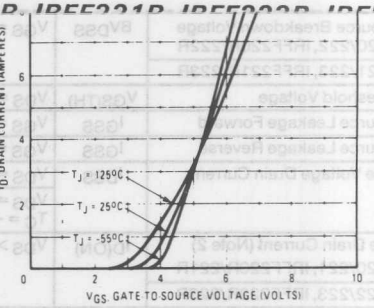


Fig. 2 - Typical transfer characteristics.

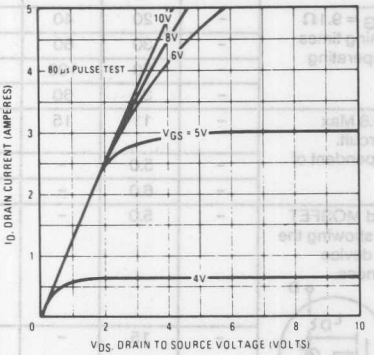


Fig. 3 - Typical saturation characteristics.

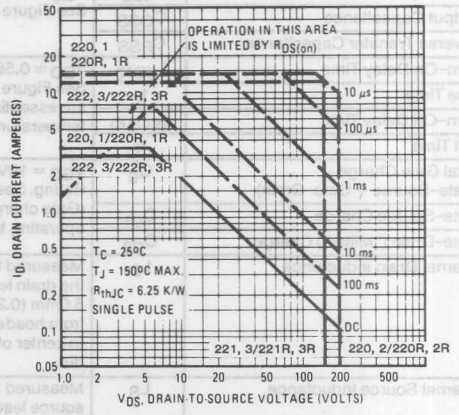


Fig. 4 - Maximum safe operating area.

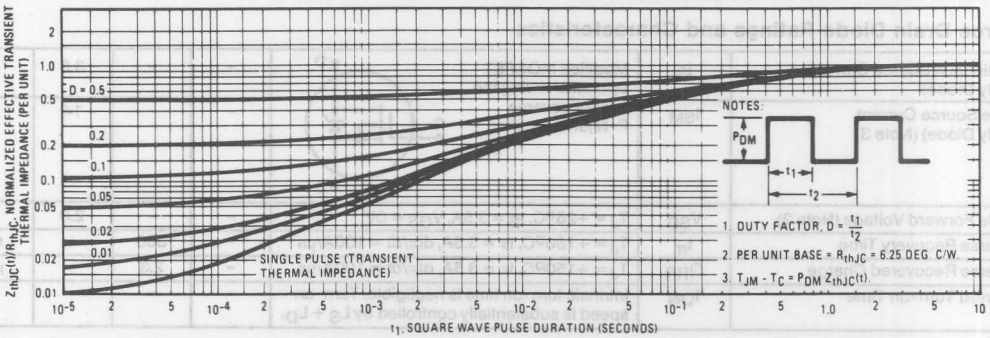


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

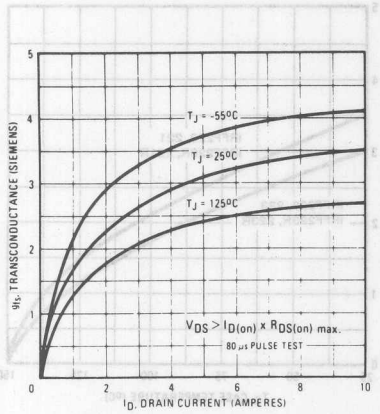


Fig. 6 - Typical transconductance vs. drain current.

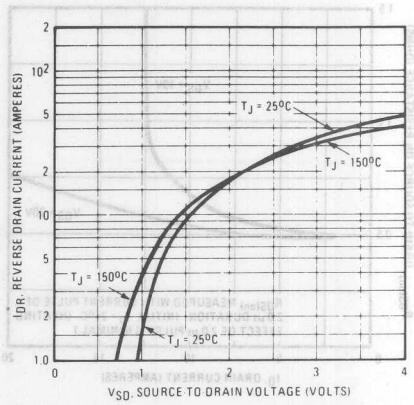


Fig. 7 - Typical source-drain diode forward voltage.

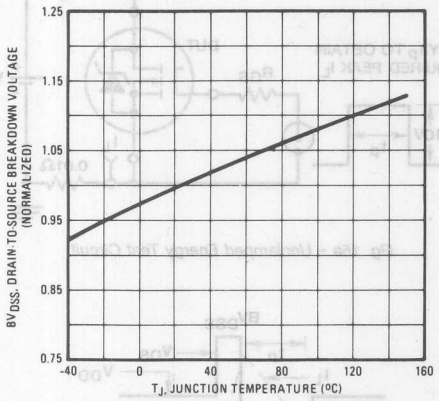


Fig. 8 - Breakdown voltage vs. temperature.

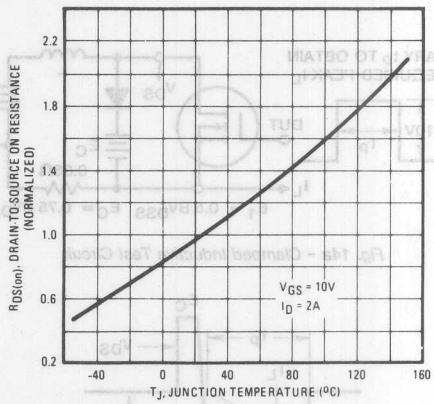


Fig. 9 - Normalized on-resistance vs. temperature.

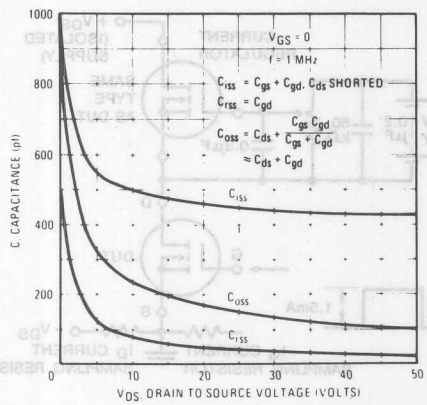


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

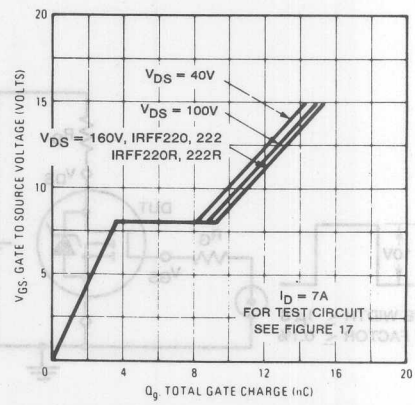


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

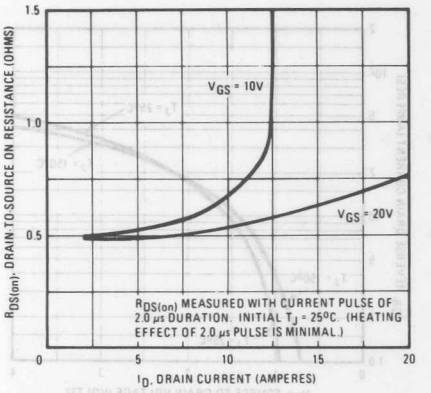


Figure 12 – Typical On-Resistance Vs. Drain Current

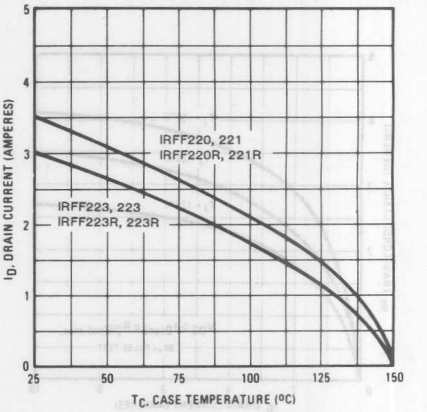


Fig. 13 – Maximum Drain Current Vs. Case Temperature

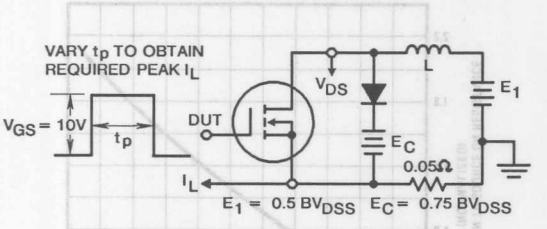


Fig. 14a – Clamped Inductive Test Circuit

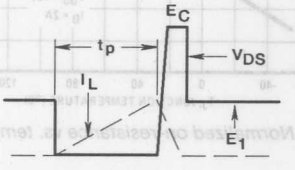


Fig. 14b – Clamped Inductive Waveforms

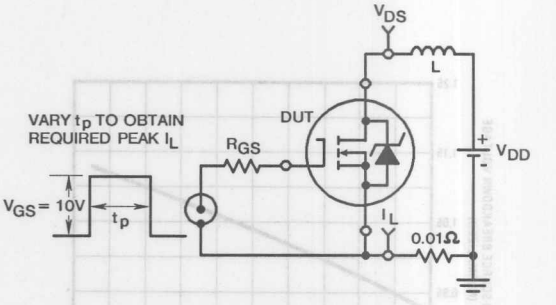


Fig. 15a – Unclamped Energy Test Circuit

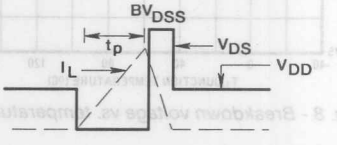


Fig. 15b – Unclamped Energy Waveforms

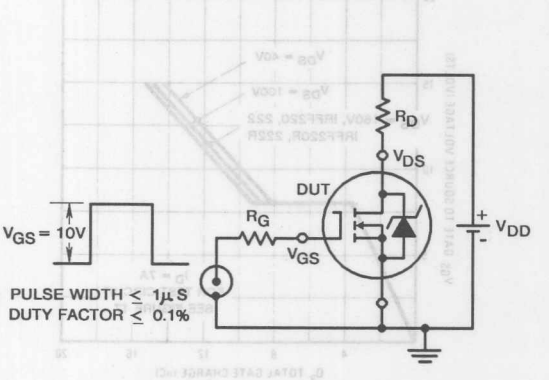


Fig. 16 – Switching Time Test Circuit

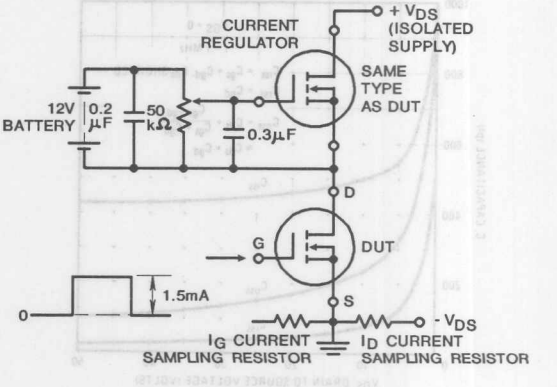


Fig. 17 – Gate Charge Test Circuit

IRFF230/231/232/233
IRFF230R/231R/232R/233R

N-Channel Power MOSFETs Avalanche Energy Rated*

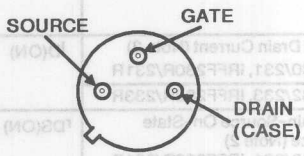
August 1991

Features

- 4.5A and 5.5A, 150V - 200V
- $r_{DS(on)}$ = 0.4Ω and 0.6Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-205AF



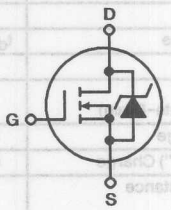
Description

The IRFF230, IRFF231, IRFF232, and IRFF233 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF230R, IRFF231R, IRFF232R, and IRFF233R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF230 IRFF230R	IRFF231 IRFF231R	IRFF232 IRFF232R	IRFF233 IRFF233R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C ..... I_D	5.5	5.5	4.5	4.5	A
Pulsed Drain Current (3) ..... I_{DM}	22	22	18	18	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	25	25	25	25	W
Linear Derating Factor	0.2	0.2	0.2	0.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	22	22	18	18	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	85	85	85	85	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 20V, starting T_J = +25°C, L = 8.9mH, R_{GS} = 50Ω, I_{PEAK} = 5.5A. See Figure 15.

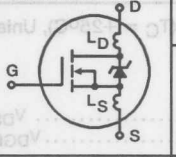
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

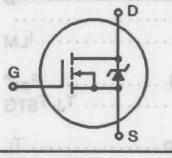
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File Number 1892.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF230/232, IRFF230R/232R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	200	–	–	V
IRFF231/233, IRFF231R/233R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFF230/231, IRFF230R/231R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	5.5	–	–	A
IRFF232/233, IRFF232R/233R			4.5	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF230/231, IRFF230R/231R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.0A	–	0.25	0.4	Ω
IRFF232/233, IRFF232R/233R			–	0.4	0.6	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 3.0A	2.5	4.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	250	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	80	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 0.5BV_{DSS}, I_D = 5.5A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	–	30	ns
Rise Time	t_r		–	–	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	–	50	ns
Fall Time	t_f		–	–	40	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 5.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	19	30	nC
Gate-Source Charge	Q_{gs}		–	10	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	9.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	5.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	22	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 5.5A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 5.5A, dI_F/dt = 100A/μs	–	450	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 5.5A, dI_F/dt = 100A/μs	–	3.0	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 20V, starting T_J = +25°C, L = 8.9mH, R_{GS} = 50Ω, I_{PEAK} = 5.5A. (See Figure 15.)

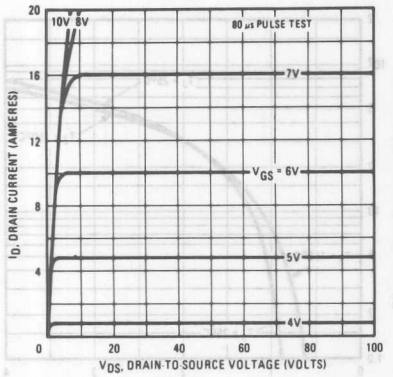


Fig. 1 - Typical output characteristics.

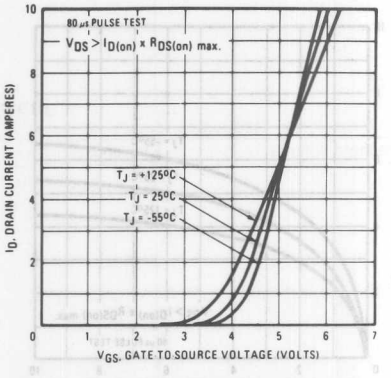


Fig. 2 - Typical transfer characteristics.

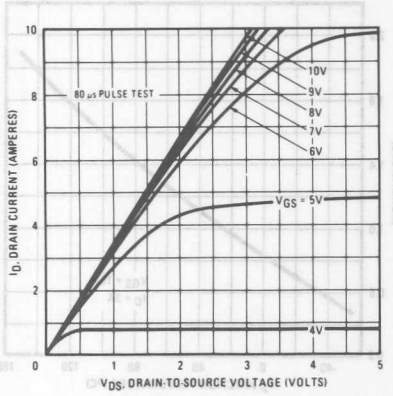


Fig. 3 - Typical saturation characteristics.

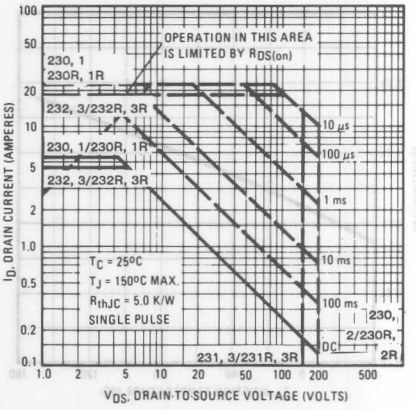


Fig. 4 - Maximum safe operating area.

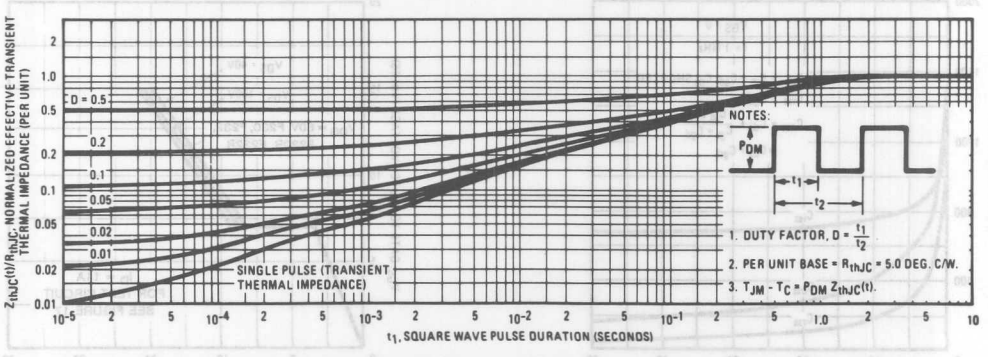


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

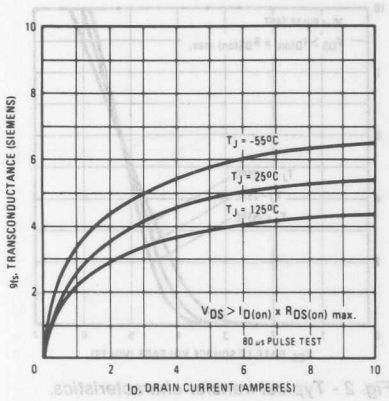


Fig. 6 - Typical transconductance vs. drain current.

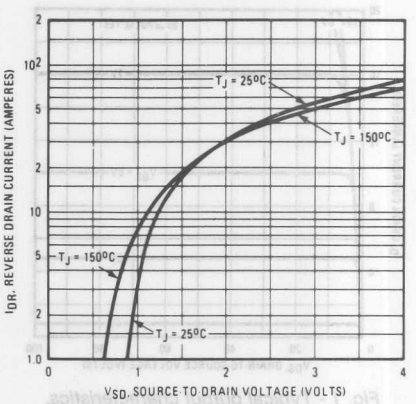


Fig. 7 - Typical source-drain diode forward voltage.

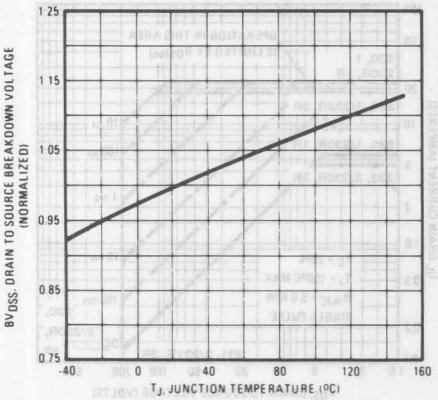


Fig. 8 - Breakdown voltage vs. temperature.

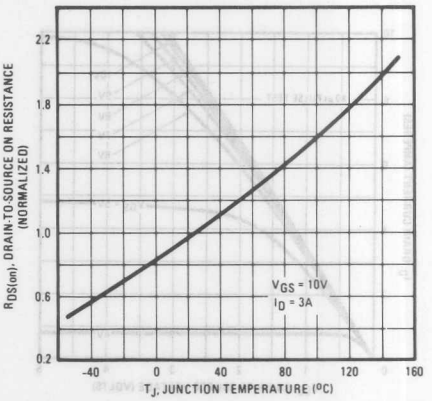


Fig. 9 - Normalized on-resistance vs. temperature.

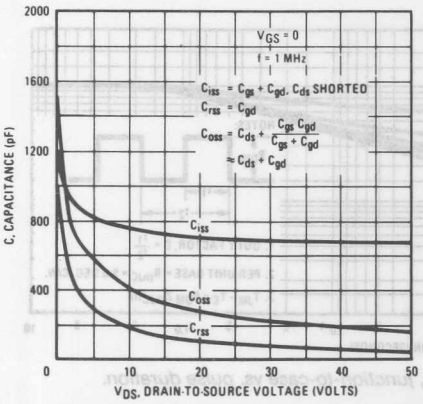


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

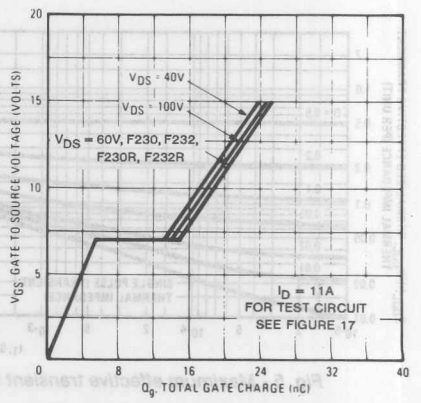


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

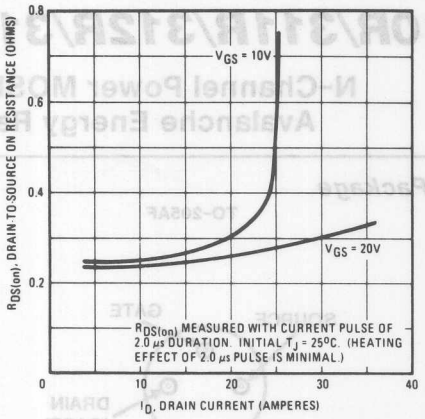


Figure 12 – Typical On-Resistance Vs. Drain Current

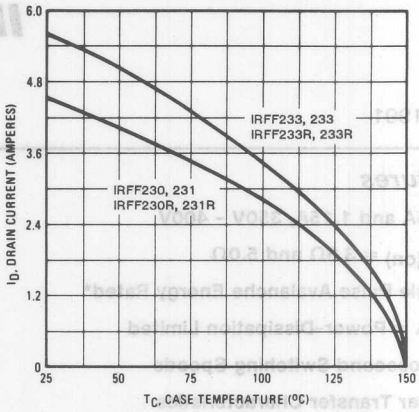


Fig. 13 – Maximum Drain Current Vs. Case Temperature

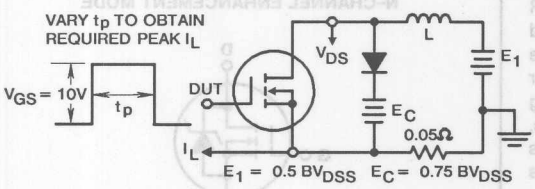


Fig. 14a – Clamped Inductive Test Circuit

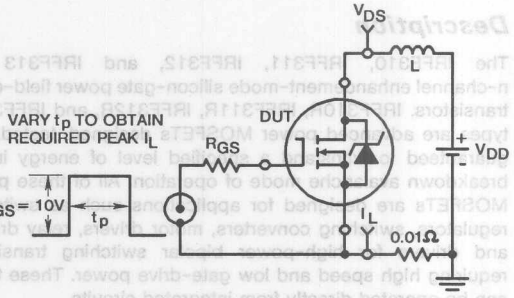


Fig. 15a – Unclamped Energy Test Circuit

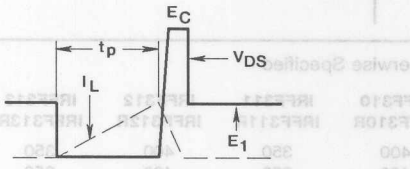


Fig. 14b – Clamped Inductive Waveforms

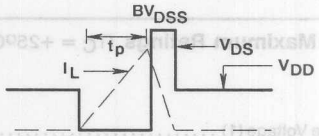


Fig. 15b – Unclamped Energy Waveforms

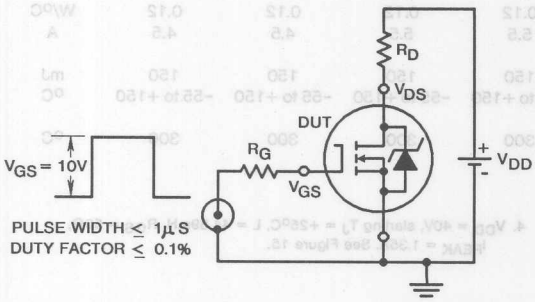


Fig. 16 – Switching Time Test Circuit

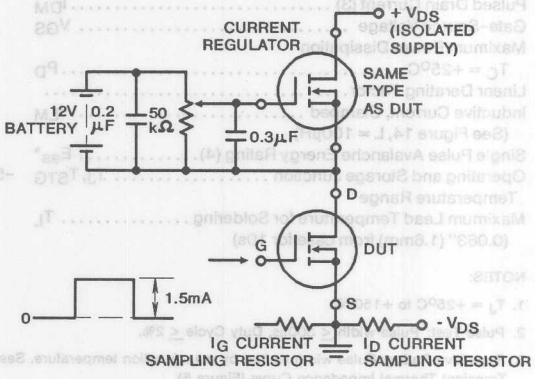


Fig. 17 – Gate Charge Test Circuit

Features

- 1.35A and 1.15A, 350V - 400V
- $r_{DS(on)}$ = 3.6Ω and 5.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

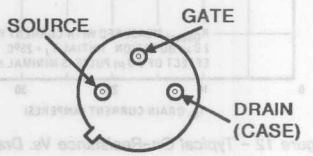
Description

The IRFF310, IRFF311, IRFF312, and IRFF313 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF310R, IRFF311R, IRFF312R, and IRFF313R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

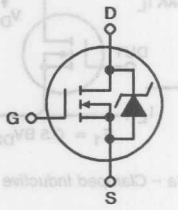
Package

TO-205AF



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF310 IRFF310R	IRFF311 IRFF311R	IRFF312 IRFF312R	IRFF313 IRFF313R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current T_C = +25°C ..... I_D	1.35	1.35	1.15	1.15	A
Pulsed Drain Current (3) ..... I_{DM}	5.5	5.5	4.5	4.5	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	15	15	15	15	W
Linear Derating Factor	0.12	0.12	0.12	0.12	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	5.5	5.5	4.5	4.5	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	150	150	150	150	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 44.89mH, R_{GS} = 50Ω, I_{PEAK} = 1.35A. See Figure 15.

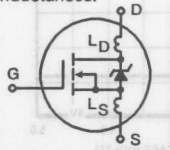
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

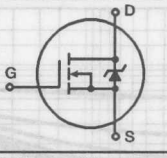
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File Number 1888.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF310/312, IRFF310R/312R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	-	-	V
IRFF311/313, IRFF311R/313R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFF310/311, IRFF310R/311R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	1.35	-	-	A
IRFF312/313, IRFF312R/313R			1.15	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF310/311, IRFF310R/311R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.8A	-	3.3	3.6	Ω
IRFF312/313, IRFF312R/313R			-	3.6	5.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 0.8A	0.5	1.2	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	135	-	pF
Output Capacitance	C_{OSS}		-	35	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	8.0	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 1.35A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	3.0	10	ns
Rise Time	t_r		-	10	20	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	5.0	10	ns
Fall Time	t_f		-	8.0	15	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 1.35A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	6.0	7.5	nC
Gate-Source Charge	Q_{gs}		-	3.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	3.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	8.33	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	1.35	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	5.5	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 1.35A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 1.35A, dI_F/dt = 100A/μs	-	380	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 1.35A, dI_F/dt = 100A/μs	-	2.7	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 40V, starting T_J = +25°C, L = 44.89mH, R_{GS} = 50Ω, I_{PEAK} = 1.35A. (See Figure 15.)

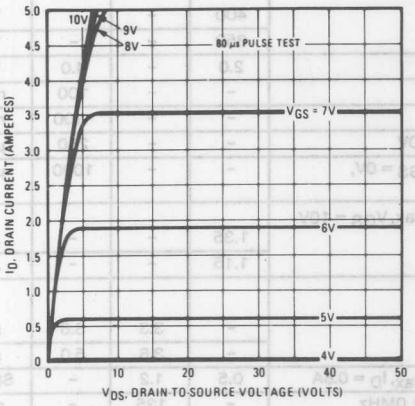


Fig. 1 - Typical output characteristics.

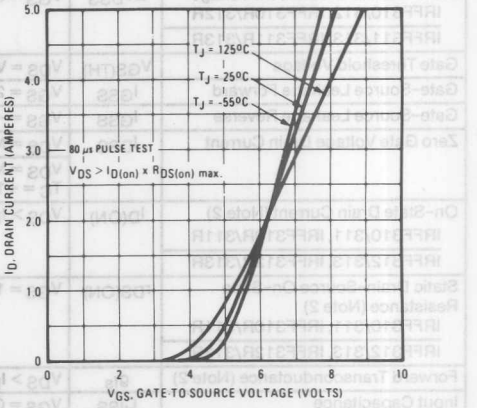


Fig. 2 - Typical transfer characteristics.

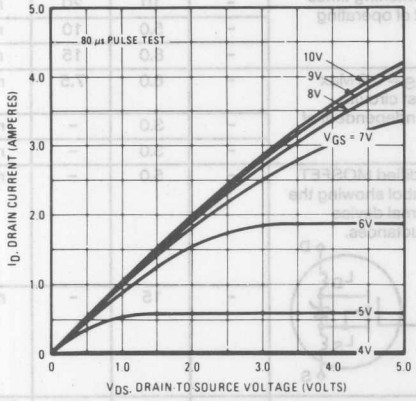


Fig. 3 - Typical saturation characteristics.

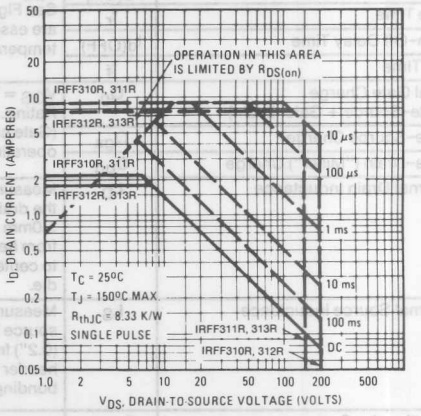


Fig. 4 - Maximum safe operating area.

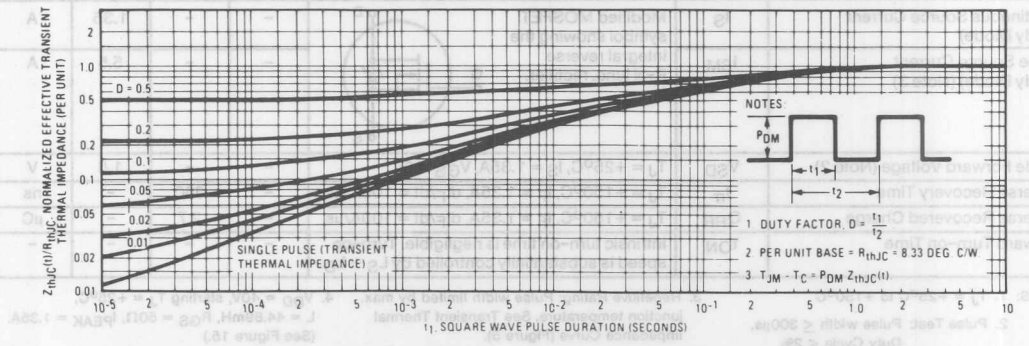


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

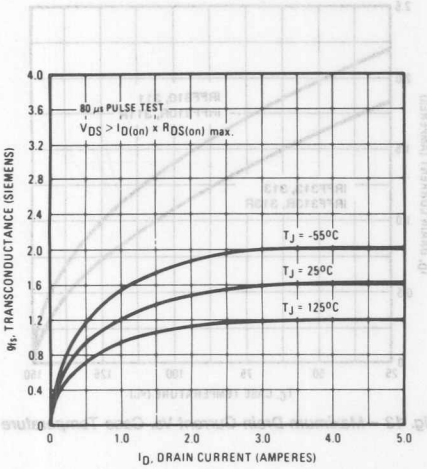


Fig. 6 - Typical transconductance vs. drain current.

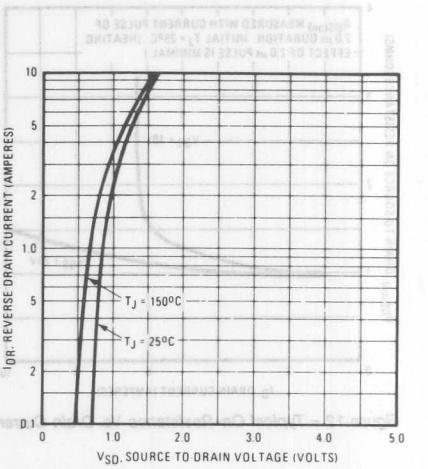


Fig. 7 - Typical source-drain diode forward voltage.

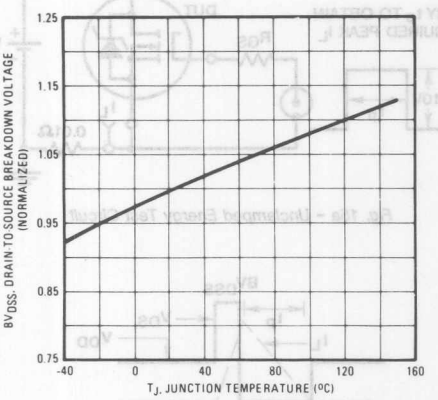


Fig. 8 - Breakdown voltage vs. temperature.

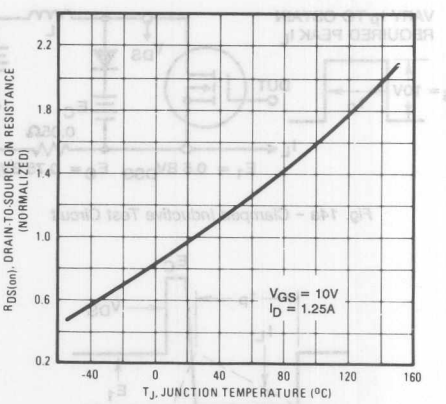


Fig. 9 - Normalized on-resistance vs. temperature.

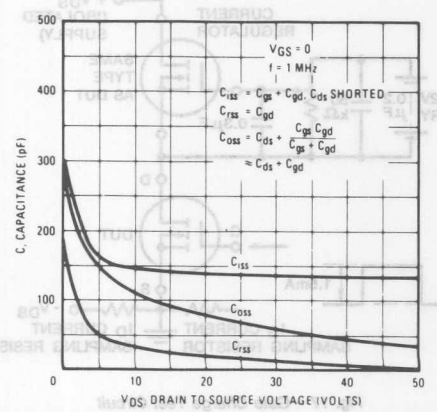


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

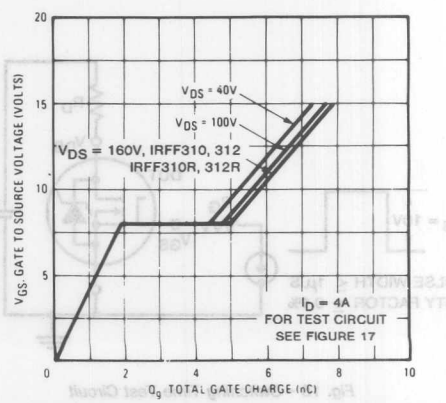


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

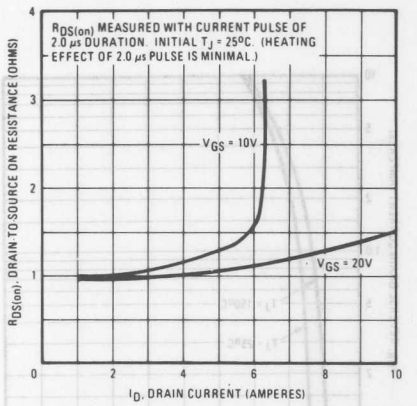


Figure 12 – Typical On-Resistance Vs. Drain Current

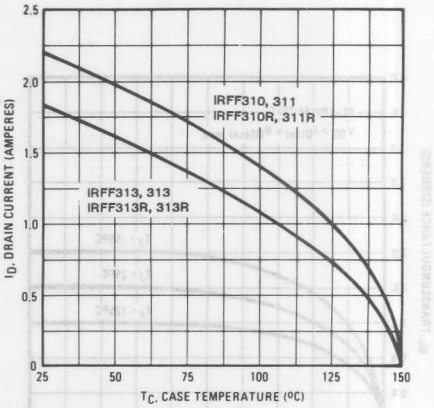


Fig. 13 – Maximum Drain Current Vs. Case Temperature

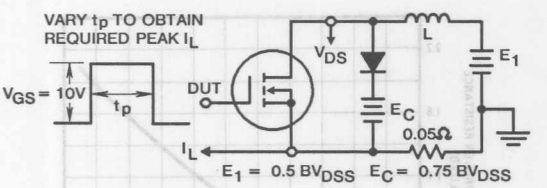


Fig. 14a – Clamped Inductive Test Circuit

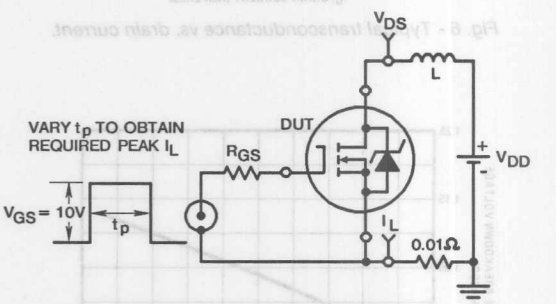


Fig. 15a – Unclamped Energy Test Circuit

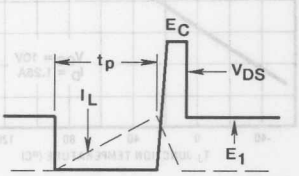


Fig. 14b – Clamped Inductive Waveforms

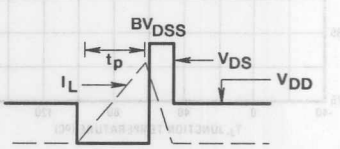


Fig. 15b – Unclamped Energy Waveforms

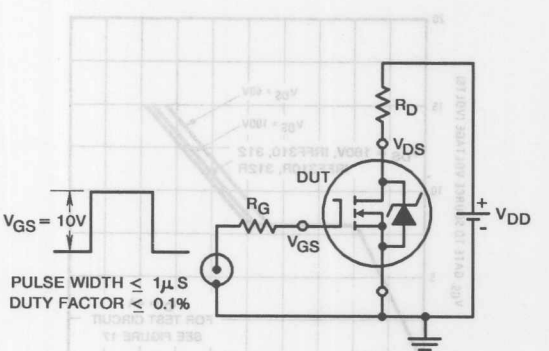


Fig. 16 – Switching Time Test Circuit

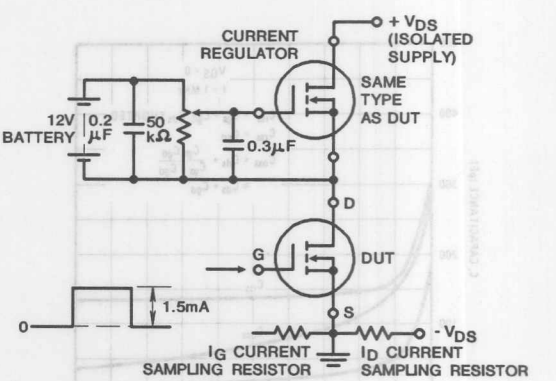


Fig. 17 – Gate Charge Test Circuit

HARRIS

IRFF320/321/322/323
IRFF320R/321R/322R/323R

N-Channel Power MOSFETs
Avalanche Energy Rated*

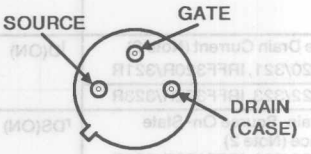
August 1991

Features

- 2.0A and 2.5A, 350V - 400V
- $r_{DS(on)}$ = 1.8Ω and 2.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-205AF



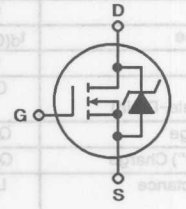
Description

The IRFF320, IRFF321, IRFF322, and IRFF323 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF320R, IRFF321R, IRFF322R, and IRFF323R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF320 IRFF320R	IRFF321 IRFF321R	IRFF322 IRFF322R	IRFF323 IRFF323R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current T_C = +25°C ..... I_D	2.5	2.5	2.0	2.0	A
Pulsed Drain Current (3) ..... I_{DM}	10	10	8.0	8.0	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	20	20	20	20	W
Linear Derating Factor	0.16	0.16	0.16	0.16	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	10	10	8.0	8.0	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	100	100	100	100	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

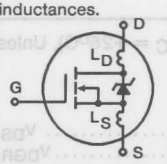
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 29.09mH, R_{GS} = 50Ω, I_{PEAK} = 2.5A. See Figure 15.

* R Suffix Types Only

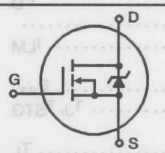
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1890.1**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage IRFF320/322, IRFF320R/322R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	-	-	V
IRFF321/323, IRFF321R/323R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFF320/321, IRFF320R/321R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	2.5	-	-	A
IRFF322/323, IRFF322R/323R			2.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF320/321, IRFF320R/321R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.25A	-	1.5	1.8	Ω
IRFF322/323, IRFF322R/323R			-	1.8	2.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.25A	1.0	2.0	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	450	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	20	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 0.5BV_{DSS}, I_D = 2.5A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	20	40	ns
Rise Time	t_r		-	25	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	25	50	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 2.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	12	15	nC
Gate-Source Charge	Q_{gs}		-	6.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	6.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	6.25	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	2.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	10	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.5A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 2.5A, dI_F/dt = 100A/μs	-	450	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 2.5A, dI_F/dt = 100A/μs	-	3.1	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 40V, starting T_J = +25°C, L = 29.09mH, R_{GS} = 50Ω, I_{PEAK} = 2.5A. (See Figure 15.)

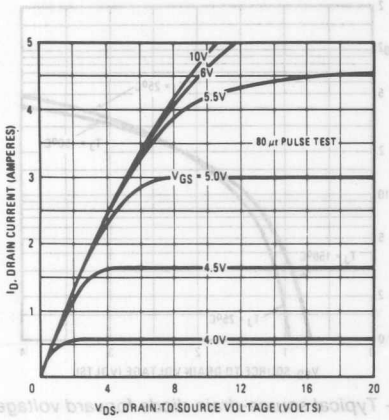


Fig. 1 - Typical output characteristics.

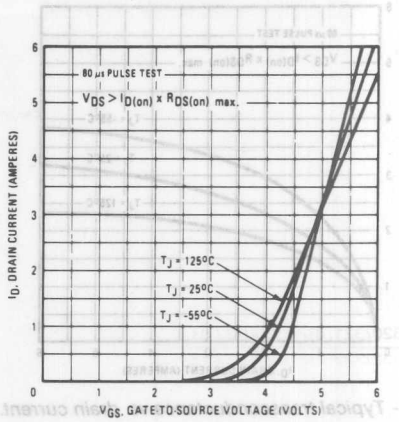


Fig. 2 - Typical transfer characteristics.

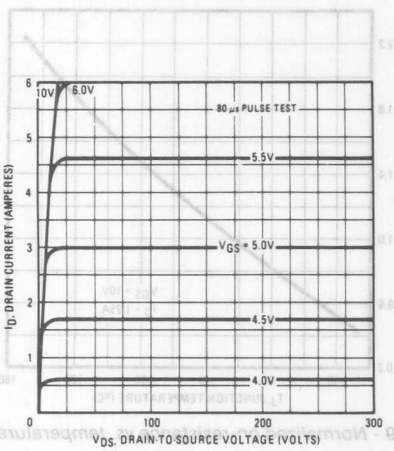


Fig. 3 - Typical saturation characteristics.

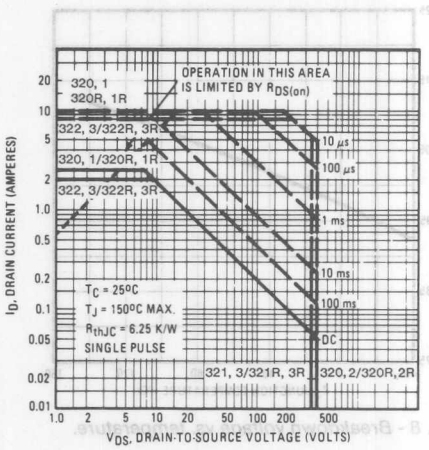


Fig. 4 - Maximum safe operating area.

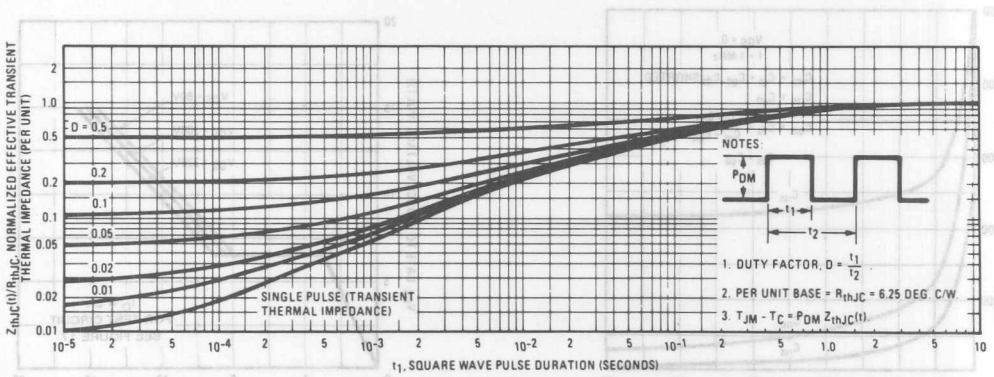


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

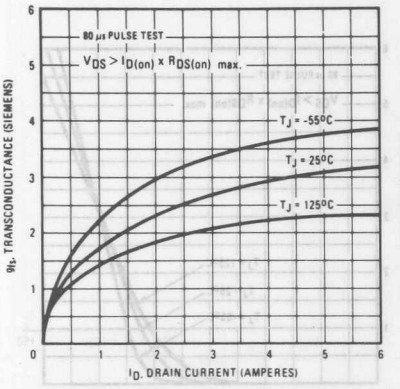


Fig. 6 - Typical transconductance vs. drain current.

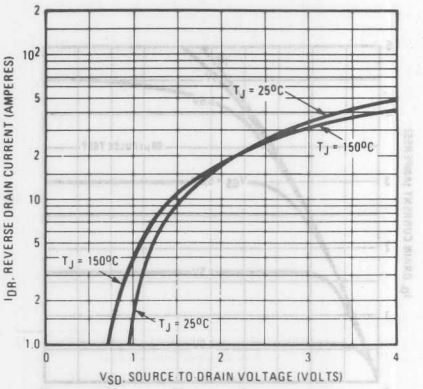


Fig. 7 - Typical source-drain diode forward voltage.

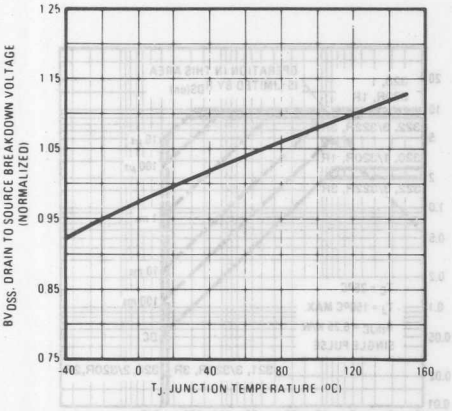


Fig. 8 - Breakdown voltage vs. temperature.

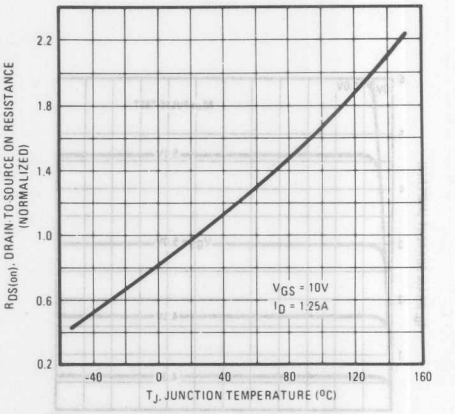


Fig. 9 - Normalized on-resistance vs. temperature.

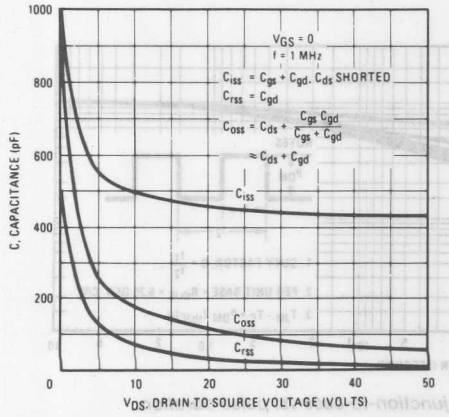


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

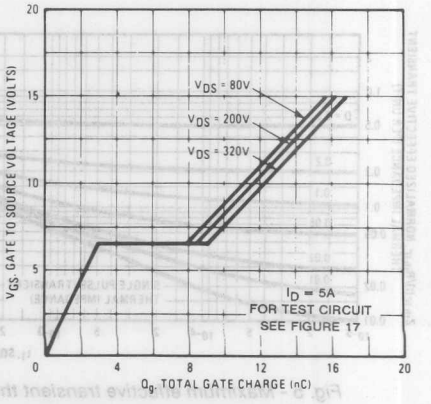


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

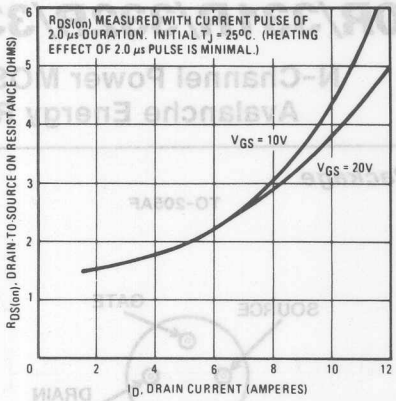


Figure 12 – Typical On-Resistance Vs. Drain Current

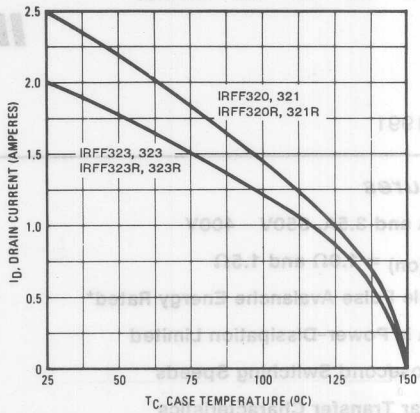


Fig. 13 – Maximum Drain Current Vs. Case Temperature

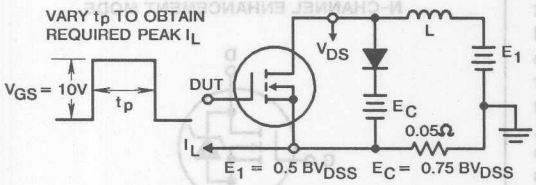


Fig. 14a – Clamped Inductive Test Circuit

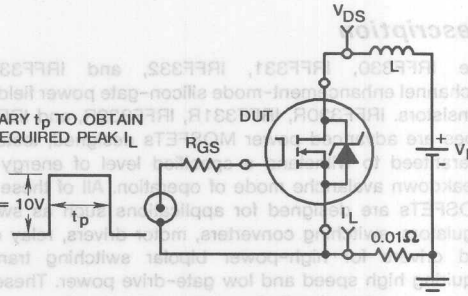


Fig. 15a – Unclamped Energy Test Circuit

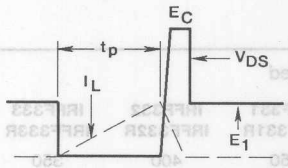


Fig. 14b – Clamped Inductive Waveforms

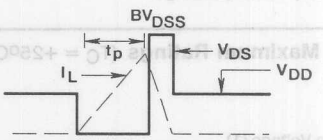


Fig. 15b – Unclamped Energy Waveforms

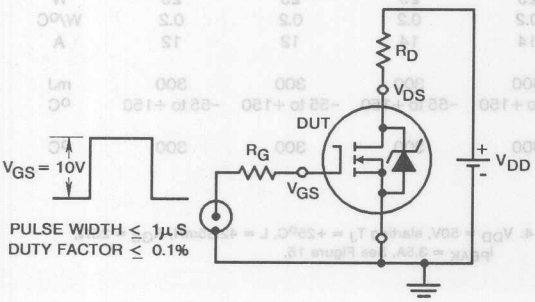


Fig. 16 – Switching Time Test Circuit

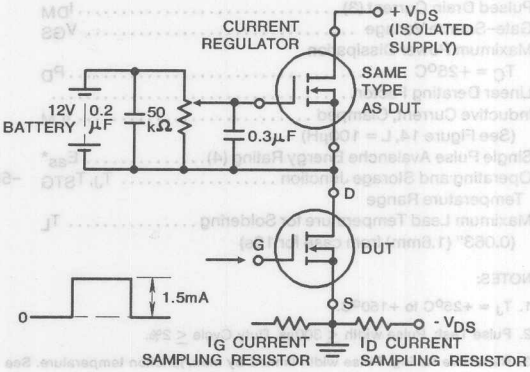


Fig. 17 – Gate Charge Test Circuit

Features

- 3.0A and 3.5A, 350V - 400V
- $r_{DS(on)}$ = 1.0Ω and 1.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

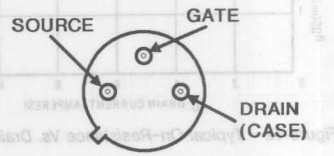
Description

The IRFF330, IRFF331, IRFF332, and IRFF333 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF330R, IRFF331R, IRFF332R, and IRFF333R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Package

TO-205AF



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF330 IRFF330R	IRFF331 IRFF331R	IRFF332 IRFF332R	IRFF333 IRFF333R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current T_C = +25°C ..... I_D	3.5	3.5	3.0	3.0	A
Pulsed Drain Current (3) ..... I_{DM}	14	14	12	12	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	25	25	25	25	W
Linear Derating Factor	0.2	0.2	0.2	0.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	14	14	12	12	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	300	300	300	300	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

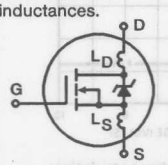
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 42.85mH, R_{GS} = 25Ω, I_{PEAK} = 3.5A. See Figure 15.

* R Suffix Types Only

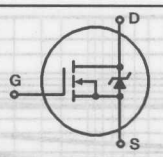
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1893.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF330/332, IRFF330R/332R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	-	-	V
IRFF331/333, IRFF331R/333R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRFF330/331, IRFF330R/331R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	3.5	-	-	A
IRFF332/333, IRFF332R/333R			3.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF330/331, IRFF330R/331R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 2.0A	-	0.8	1.0	Ω
IRFF332/333, IRFF332R/333R			-	1.0	1.5	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, I_D = 2.0A	2.0	3.5	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	700	-	pF
Output Capacitance	C_{OSS}		-	150	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	40	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq$ 175V, I_D = 3.5A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	-	30	ns
Rise Time	t_r		-	-	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	55	ns
Fall Time	t_f		-	-	35	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	18	30	nC
Gate-Source Charge	Q_{gs}		-	11	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	3.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	14	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.5A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 3.5A, dI_F/dt = 100A/µs	-	600	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 3.5A, dI_F/dt = 100A/µs	-	4.0	-	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 50V, starting T_J = +25°C, L = 42.85mH, R_{GS} = 25Ω, I_{PEAK} = 3.5A. (See Figure 15.)

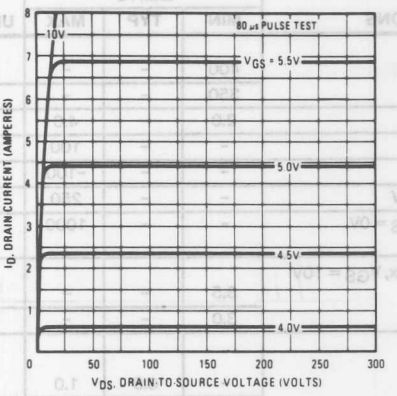


Fig. 1 - Typical output characteristics.

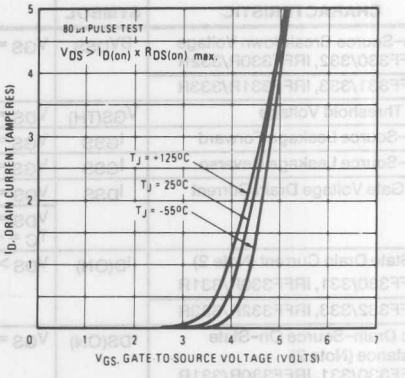


Fig. 2 - Typical transfer characteristics.

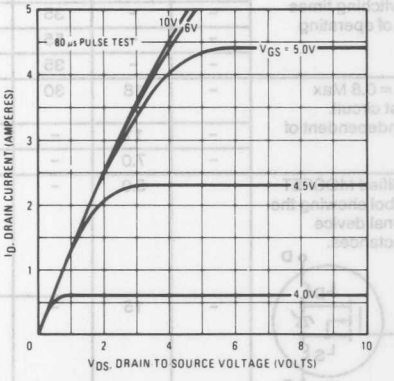


Fig. 3 - Typical saturation characteristics.

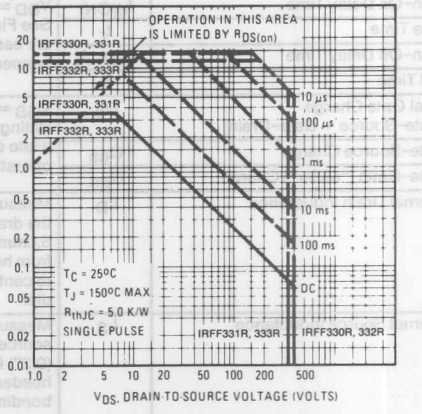


Fig. 4 - Maximum safe operating area.

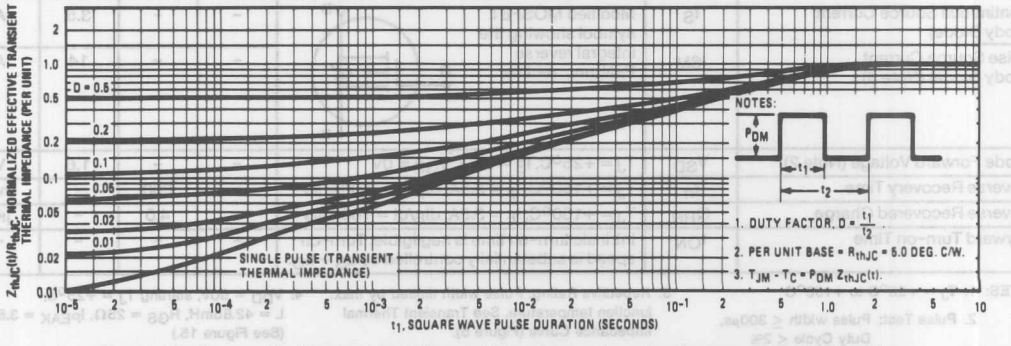


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

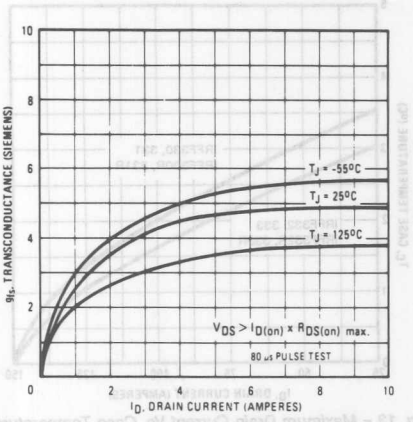


Fig. 6 - Typical transconductance vs. drain current.

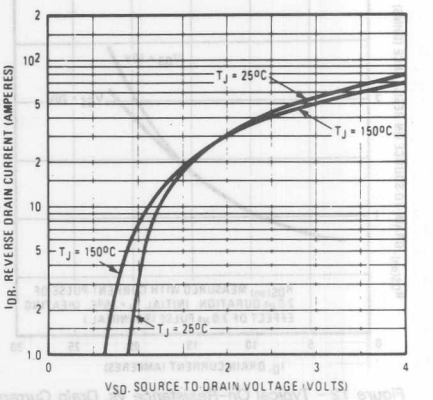


Fig. 7 - Typical source-drain diode forward voltage.

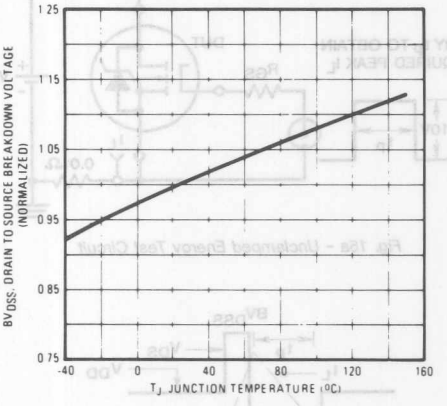


Fig. 8 - Breakdown voltage vs. temperature.

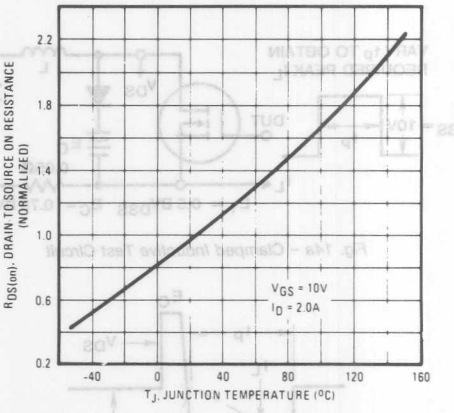


Fig. 9 - Normalized on-resistance vs. temperature.

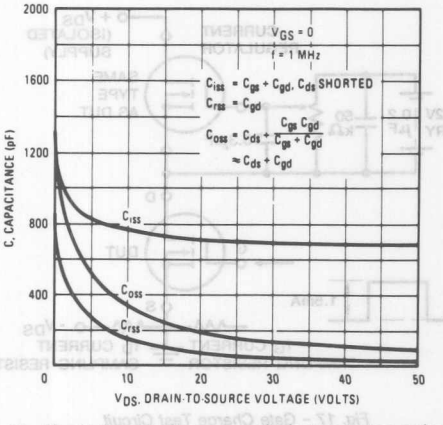


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

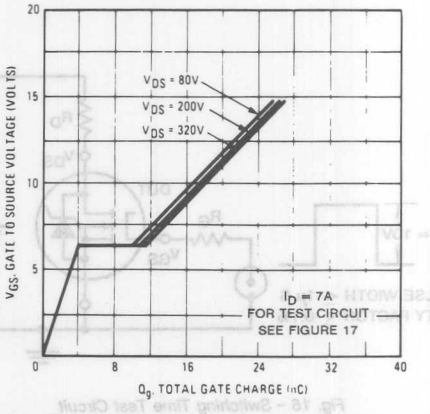


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

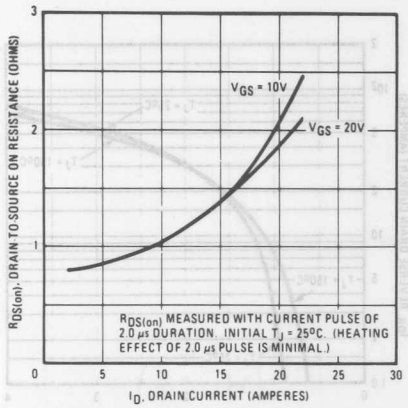


Figure 12 – Typical On-Resistance Vs. Drain Current

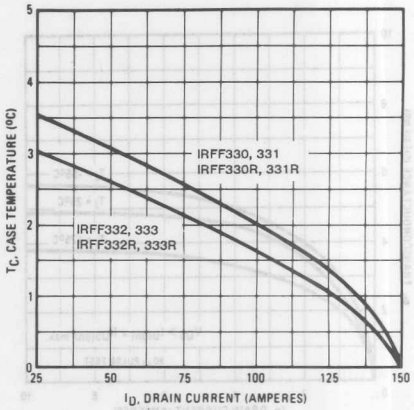


Fig. 13 – Maximum Drain Current Vs. Case Temperature

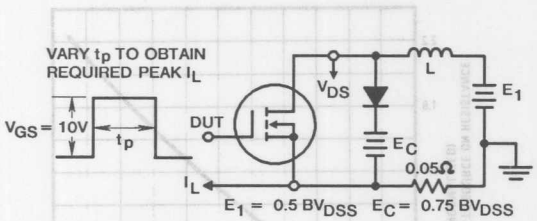


Fig. 14a – Clamped Inductive Test Circuit

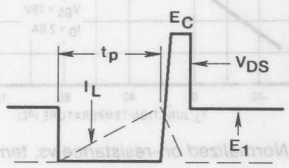


Fig. 14b – Clamped Inductive Waveforms

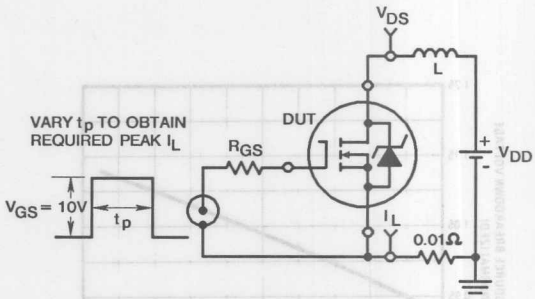


Fig. 15a – Unclamped Energy Test Circuit

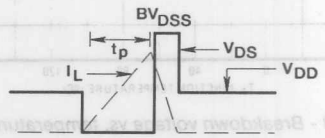


Fig. 15b – Unclamped Energy Waveforms

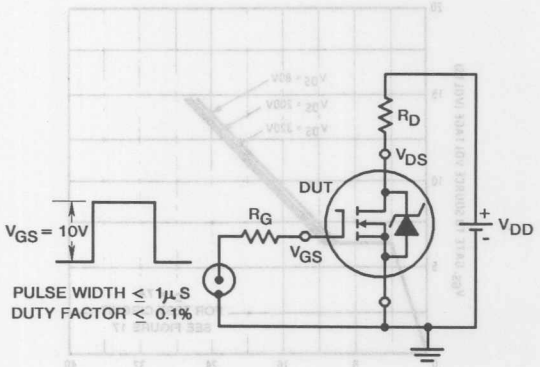


Fig. 16 – Switching Time Test Circuit

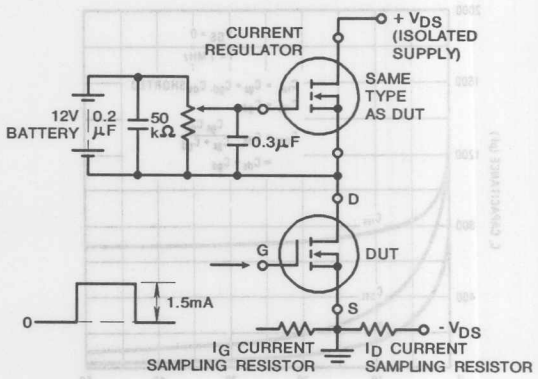


Fig. 17 – Gate Charge Test Circuit

IRFF420/421/422/423
IRFF420R/421R/422R/423R

N-Channel Power MOSFETs
Avalanche Energy Rated*

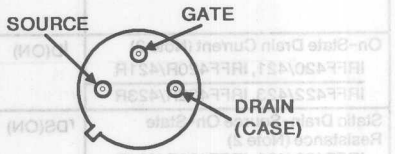
August 1991

Features

- 1.4A and 1.6A, 450V - 500V
- $r_{DS(on)}$ = 3.0Ω and 4.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-205AF



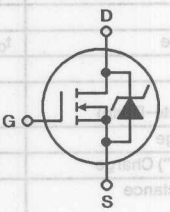
Description

The IRFF420, IRFF421, IRFF422, and IRFF423 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF420R, IRFF421R, IRFF422R, and IRFF423R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF420 IRFF420R	IRFF421 IRFF421R	IRFF422 IRFF422R	IRFF423 IRFF423R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current T_C = +25°C ..... I_D	1.6	1.6	1.4	1.4	A
Pulsed Drain Current (3) ..... I_{DM}	6.5	6.5	5.5	5.5	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	20	20	20	20	W
Linear Derating Factor	0.16	0.16	0.16	0.16	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	6.5	6.5	5.5	5.5	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	210	210	210	210	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

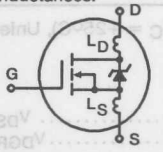
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 143.5mH, R_{GS} = 25Ω, I_{PEAK} = 1.6A. See Figure 15.

* R Suffix Types Only

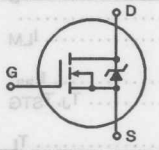
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
Copyright © Harris Corporation 1991

File Number **1891.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF420/422, IRFF420R/422R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500	–	–	V
IRFF421/423, IRFF421R/423R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFF420/421, IRFF420R/421R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	1.6	–	–	A
IRFF422/423, IRFF422R/423R			1.4	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF420/421, IRFF420R/421R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.0A	–	2.5	3.0	Ω
IRFF422/423, IRFF422R/423R			–	3.0	4.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.0A	1.0	1.75	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	300	–	pF
Output Capacitance	C_{OSS}		–	75	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 1.6A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	30	60	ns
Rise Time	t_r		–	25	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	30	60	ns
Fall Time	t_f		–	15	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 1.6A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	11	15	nC
Gate-Source Charge	Q_{gs}		–	5.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	6.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	6.25	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	1.6	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	6.5	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 1.6A, V_{GS} = 0V	–	–	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 1.6A, dI_F/dt = 100A/μs	–	600	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 1.6A, dI_F/dt = 100A/μs	–	3.5	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 50V, starting T_J = +25°C, L = 143.5mH, R_{GS} = 25Ω, I_{PEAK} = 1.6A. (See Figure 15.)

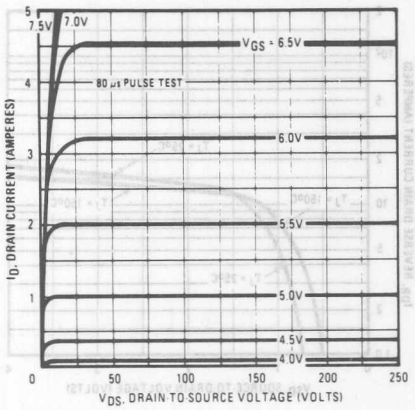


Fig. 1 - Typical output characteristics.

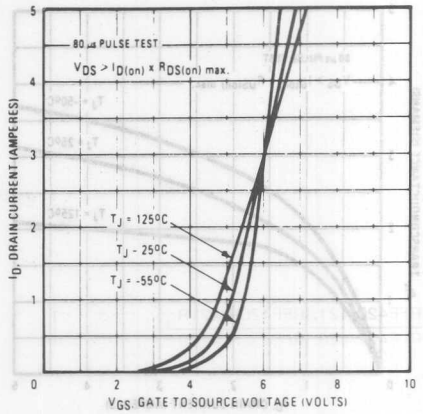


Fig. 2 - Typical transfer characteristics.

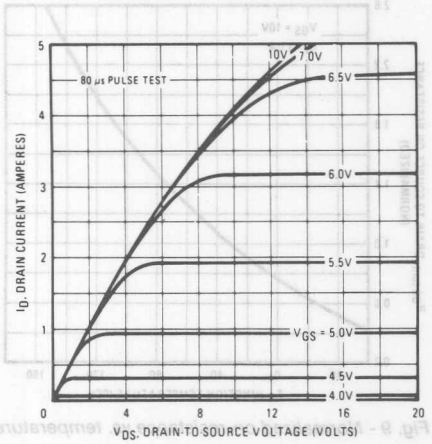


Fig. 3 - Typical saturation characteristics.

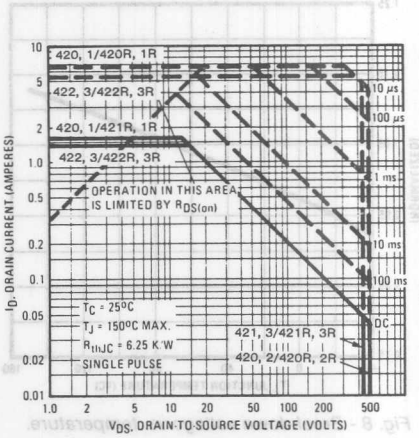


Fig. 4 - Maximum safe operating area.

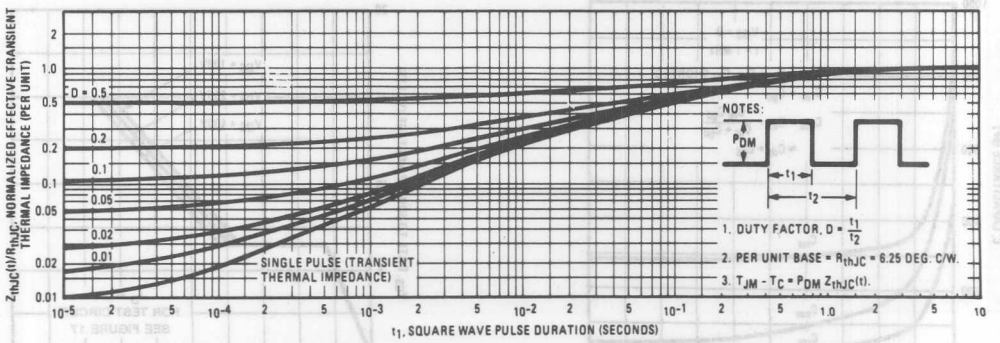


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

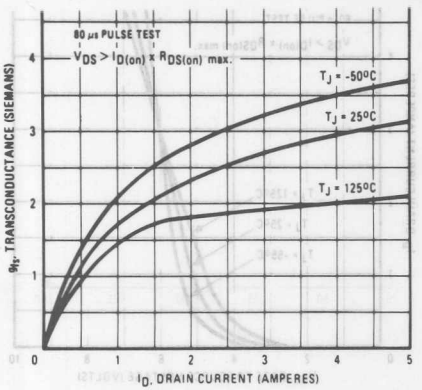


Fig. 6 - Typical transconductance vs. drain current.

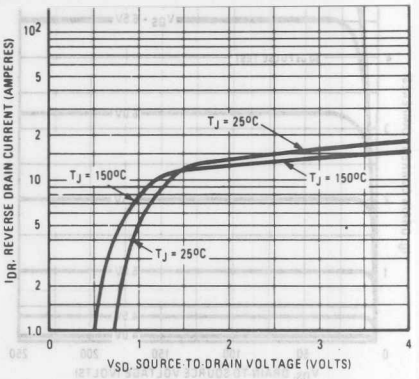


Fig. 7 - Typical source-drain diode forward voltage.

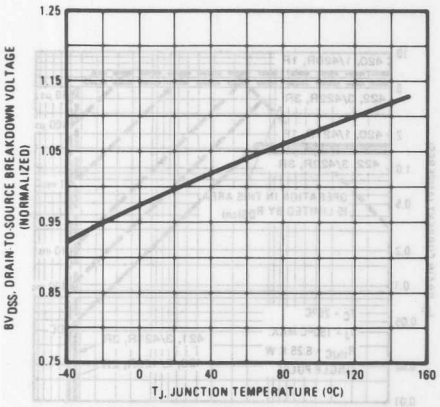


Fig. 8 - Breakdown voltage vs. temperature.

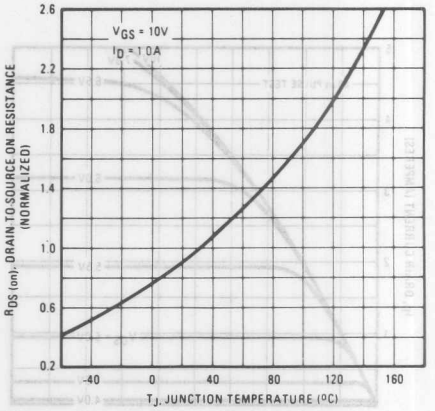


Fig. 9 - Normalized on-resistance vs. temperature.

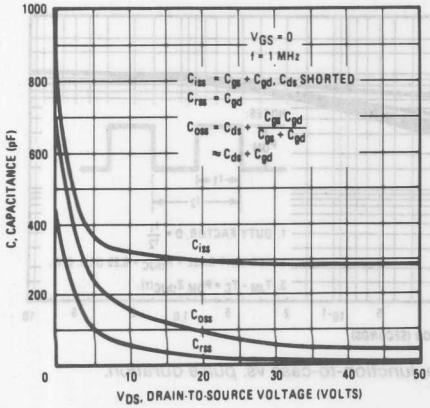


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

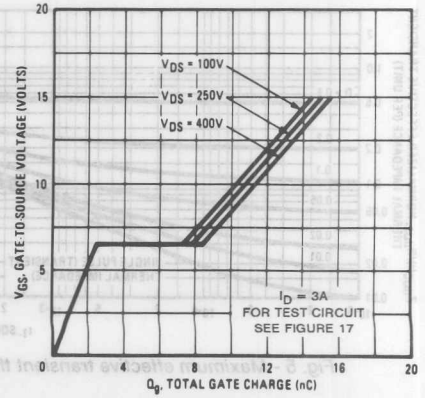


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

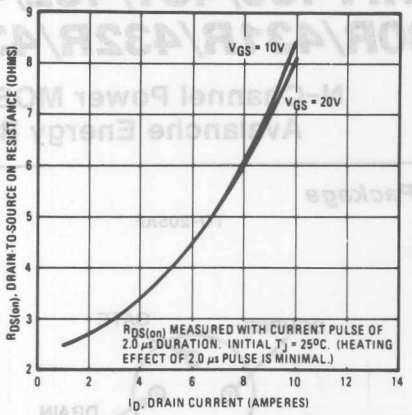


Figure 12 – Typical On-Resistance Vs. Drain Current

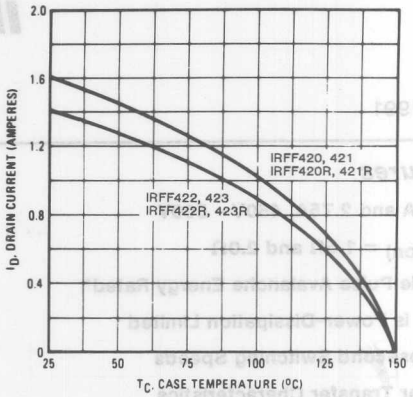


Fig. 13 – Maximum Drain Current Vs. Case Temperature

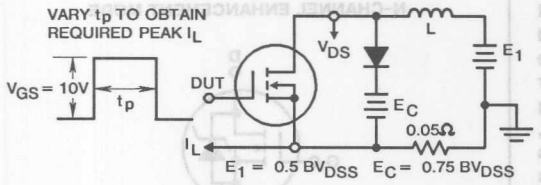


Fig. 14a – Clamped Inductive Test Circuit

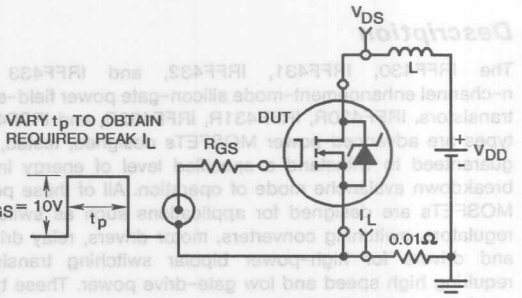


Fig. 15a – Unclamped Energy Test Circuit

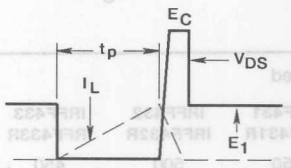


Fig. 14b – Clamped Inductive Waveforms

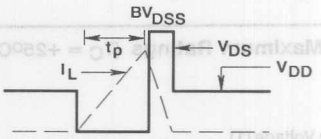


Fig. 15b – Unclamped Energy Waveforms

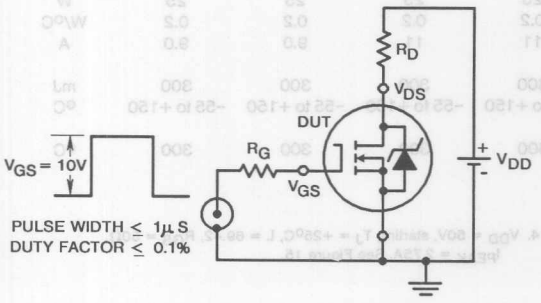


Fig. 16 – Switching Time Test Circuit

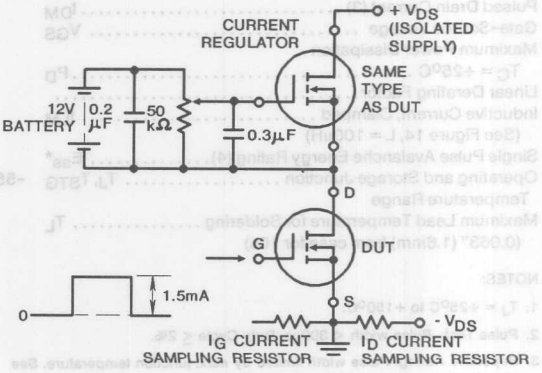


Fig. 17 – Gate Charge Test Circuit

IRFF430/431/432/433
IRFF430R/431R/432R/433R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 2.25A and 2.75A, 450V - 500V
- $r_{DS(on)}$ = 1.5Ω and 2.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

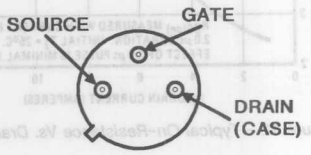
Description

The IRFF430, IRFF431, IRFF432, and IRFF433 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF430R, IRFF431R, IRFF432R, and IRFF433R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Package

TO-205AF



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF430 IRFF430R	IRFF431 IRFF431R	IRFF432 IRFF432R	IRFF433 IRFF433R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current T_C = +25°C ..... I_D	2.75	2.75	2.25	2.25	A
Pulsed Drain Current (3) ..... I_{DM}	11	11	9.0	9.0	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	25	25	25	25	W
Linear Derating Factor	0.2	0.2	0.2	0.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	11	11	9.0	9.0	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	300	300	300	300	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 69.42, R_{GS} = 50Ω, I_{PEAK} = 2.75A. See Figure 15.

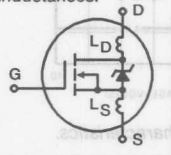
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

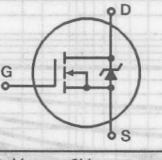
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File Number **1894.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF430/432, IRFF430R/432R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500	–	–	V
IRFF431/433, IRFF431R/433R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFF430/431, IRFF430R/431R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	2.75	–	–	A
IRFF432/433, IRFF432R/433R			2.25	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF430/431, IRFF430R/431R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.5A	–	1.3	1.5	Ω
IRFF432/433, IRFF432R/433R			–	1.5	2.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.5A	1.5	2.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	100	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	30	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 225V, I_D = 2.75A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	–	30	ns
Rise Time	t_r		–	–	30	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	–	55	ns
Fall Time	t_f		–	–	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 2.75A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	22	30	nC
Gate-Source Charge	Q_{gs}		–	11	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	11	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	2.75	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	11	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.75A, V_{GS} = 0V	–	–	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 2.75A, dI_F/dt = 100A/μs	–	800	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 2.75A, dI_F/dt = 100A/μs	–	4.6	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 50V, starting T_J = +25°C, L = 69.42mH, R_{GS} = 50Ω, I_{PEAK} = 2.75A. (See Figure 15.)

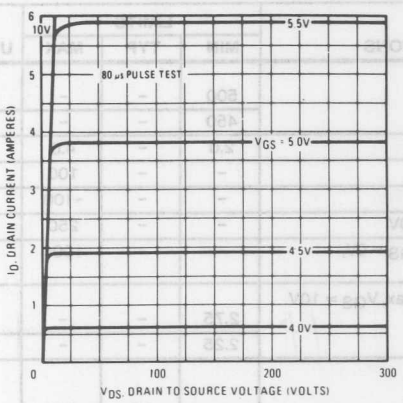


Fig. 1 - Typical output characteristics.

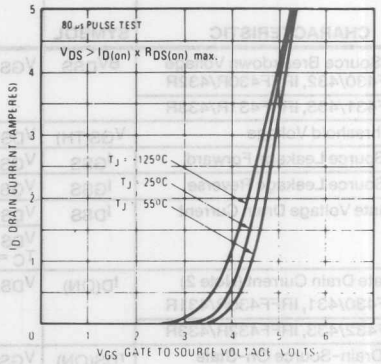


Fig. 2 - Typical transfer characteristics.

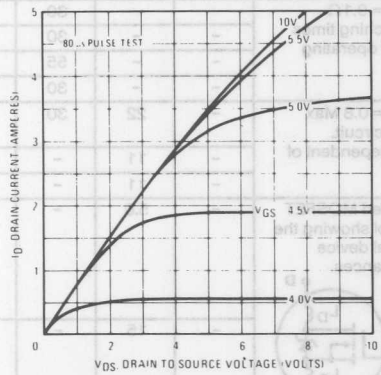


Fig. 3 - Typical saturation characteristics.

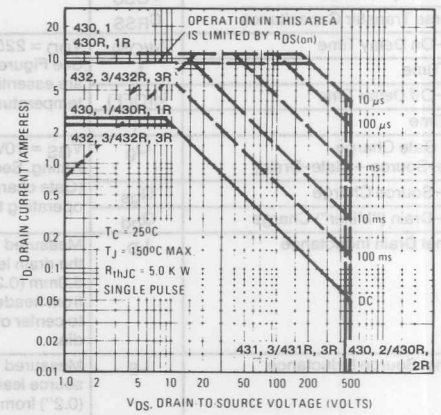


Fig. 4 - Maximum safe operating area.

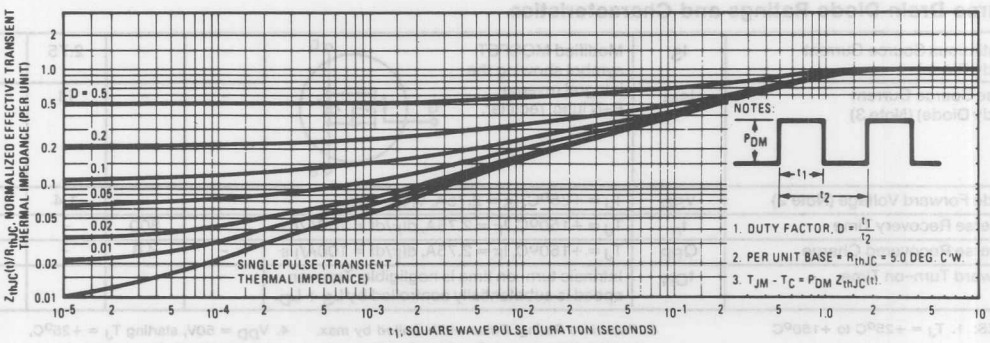


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

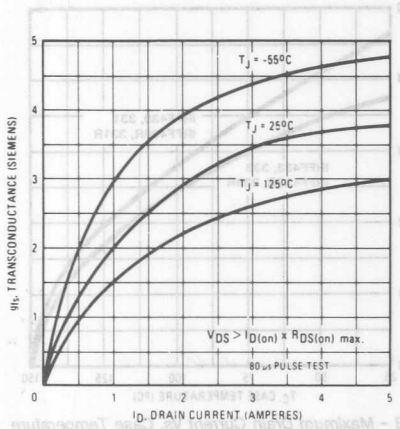


Fig. 6 - Typical transconductance vs. drain current.

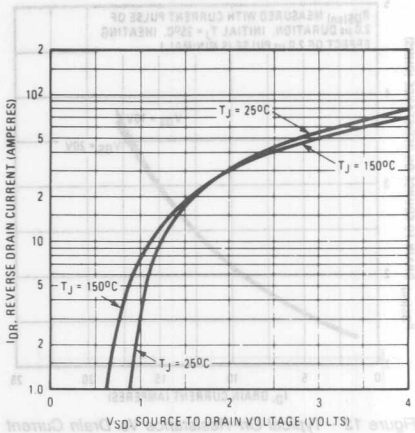


Fig. 7 - Typical source-drain diode forward voltage.

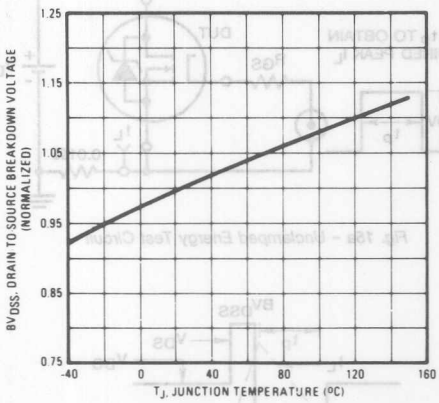


Fig. 8 - Breakdown voltage vs. temperature.

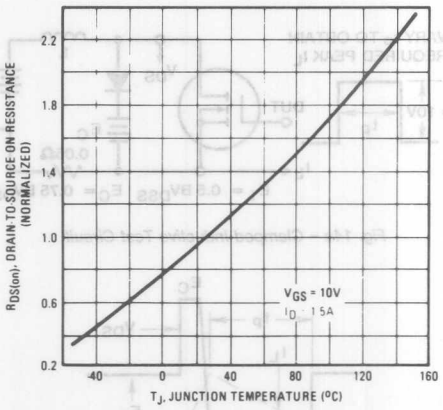


Fig. 9 - Normalized on-resistance vs. temperature.

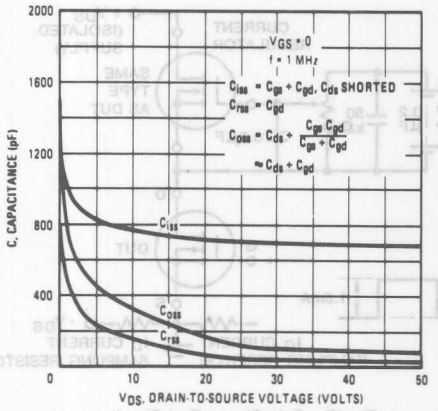


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

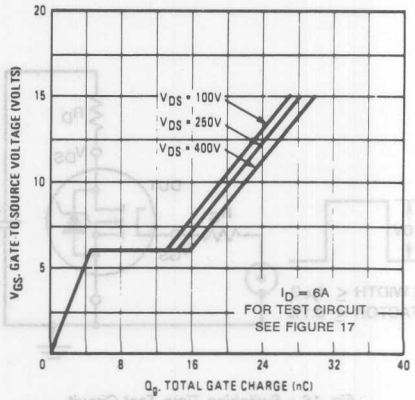


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

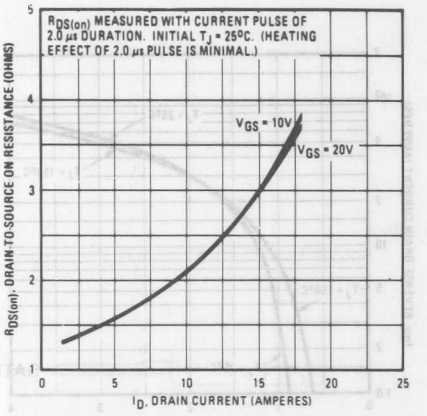


Figure 12 - Typical On-Resistance Vs. Drain Current

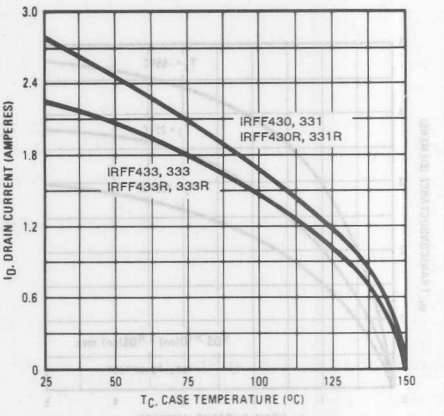


Fig. 13 - Maximum Drain Current Vs. Case Temperature

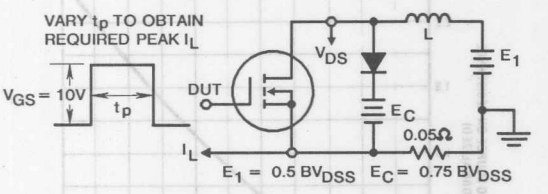


Fig. 14a - Clamped Inductive Test Circuit

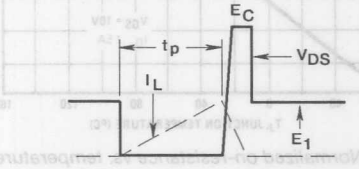


Fig. 14b - Clamped Inductive Waveforms

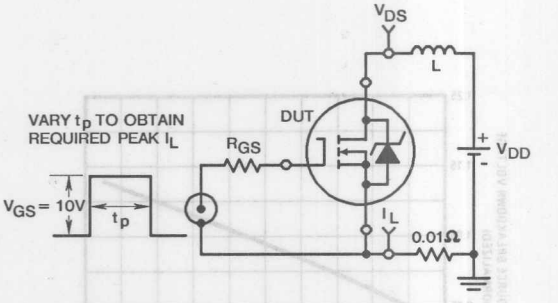


Fig. 15a - Unclamped Energy Test Circuit

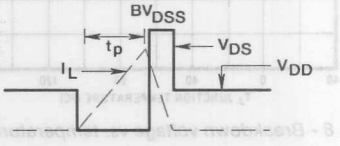


Fig. 15b - Unclamped Energy Waveforms

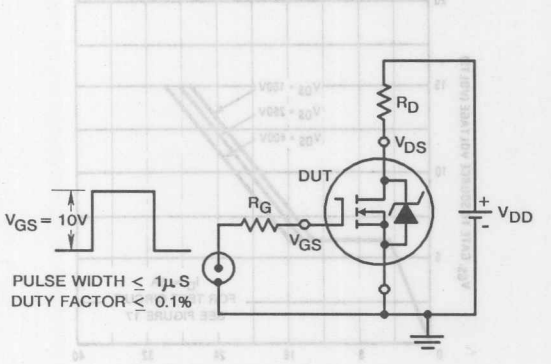


Fig. 16 - Switching Time Test Circuit

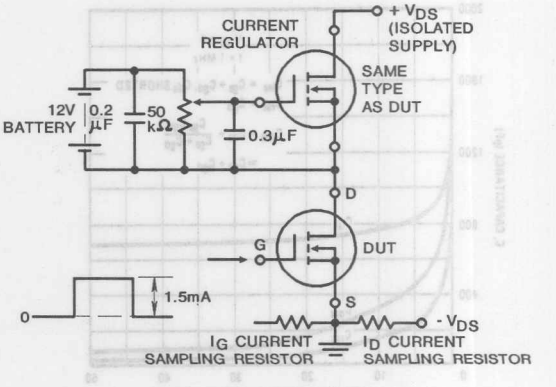


Fig. 17 - Gate Charge Test Circuit

HARRIS IRFP140R, IRFP141R IRFP142R, IRFP143R

N-Channel Power MOSFETs Avalanche Energy Rated

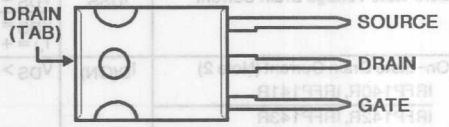
August 1991

Features

- 27A and 31A, 80V - 100V
- $r_{DS(on)}$ = 0.077Ω and 0.099Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-247
TOP VIEW



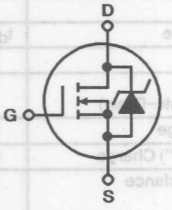
Description

The IRFP140R, IRFP141R, IRFP142R, and IRFP143R are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFP140R	IRFP141R	IRFP142R	IRFP143R	UNITS
Drain-Source Voltage (1)	V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	100	80	100	80	V
Continuous Drain Current						
T_C = +25°C	I_D	31	31	27	27	A
T_C = +100°C	I_D	22	22	19	19	A
Pulsed Drain Current (3)	I_{DM}	120	120	110	110	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	180	180	180	180	W
Linear Derating Factor		1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	100	100	100	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

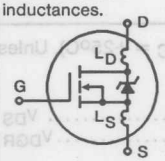
NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 160μH, R_{GS} = 50Ω, I_{PEAK} = 31A. See Figures 14 and 15.

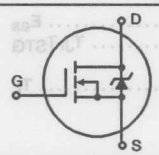
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2086.1

Drain-Source Breakdown Voltage IRFP140R, IRFP142R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	-	-	V
IRFP141R, IRFP143R			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFP140R, IRFP141R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	31	-	-	A
IRFP142R, IRFP143R			27	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP140R, IRFP141R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 19A	-	0.055	0.077	Ω
IRFP142R, IRFP143R			-	0.077	0.099	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 19A	9.3	14	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	1275	-	pF
Output Capacitance	C_{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	160	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D ≈ 28A, R_G = 9.1Ω, RD = 1.8Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	15	23	ns
Rise Time	t_r		-	72	110	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	40	60	ns
Fall Time	t_f		-	50	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	38	59	nC
Gate-Source Charge	Q_{gs}		-	10	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	21	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	31	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	120	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 31A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 28A, dI_F/dt = 100A/μs	70	150	300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 28A, dI_F/dt = 100A/μs	0.44	0.91	1.9	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 160μH, R_{GS} = 50Ω, I_{PEAK} = 31A. (See Figures 14 & 15)

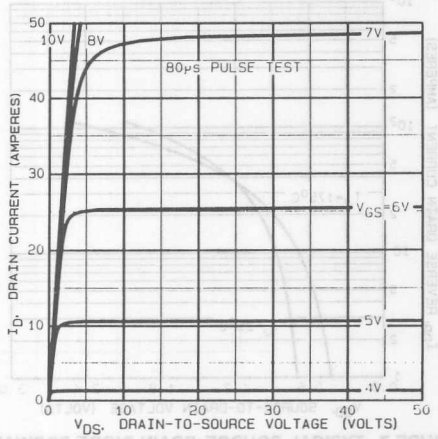


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

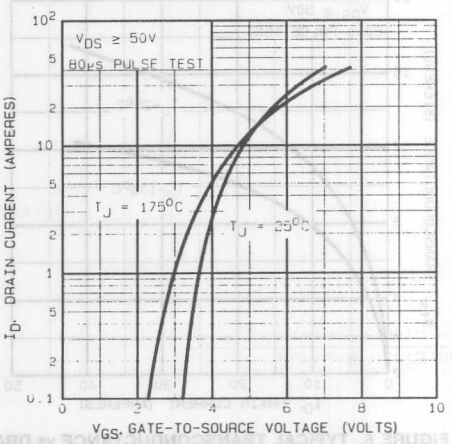


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

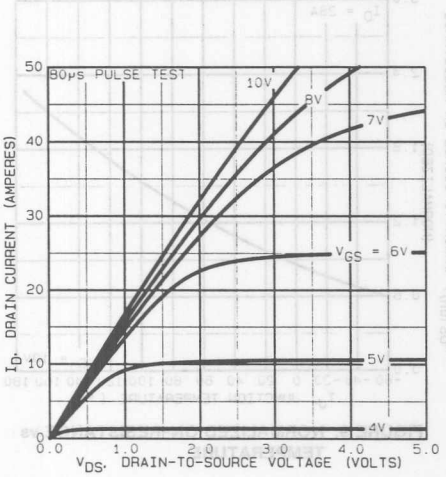


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

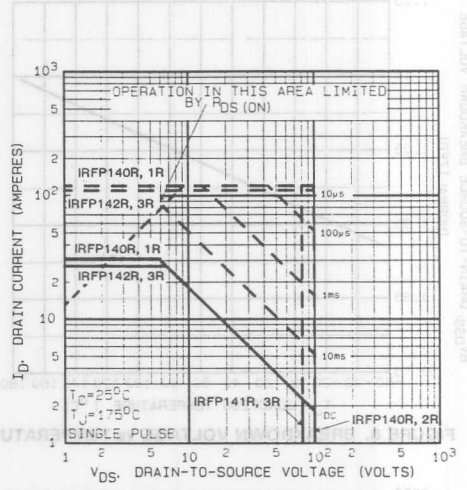


FIGURE 4. MAXIMUM SAFE OPERATING AREA

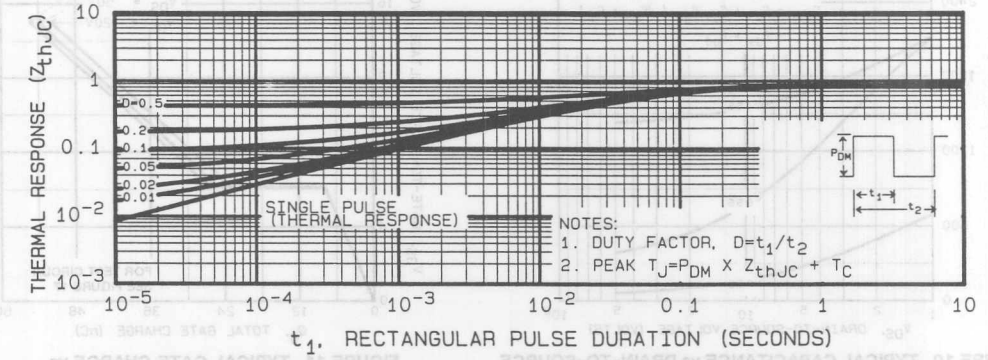


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

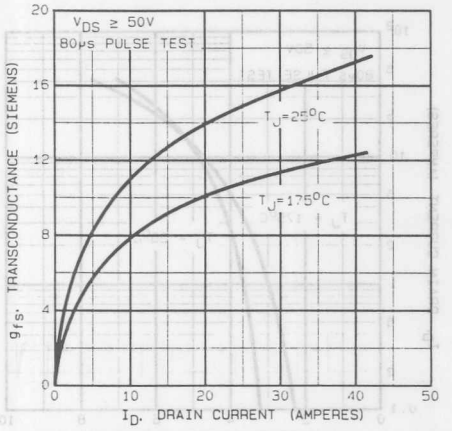


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

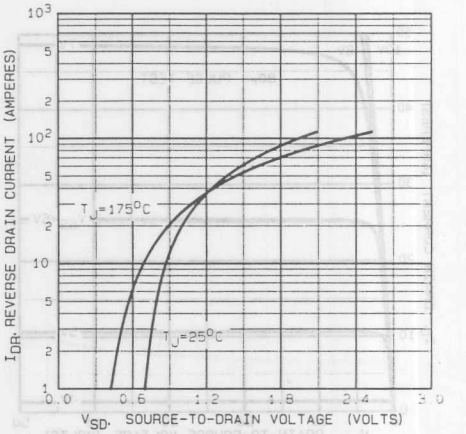


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

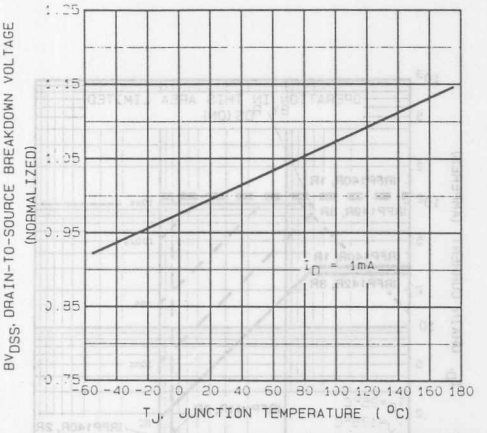


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

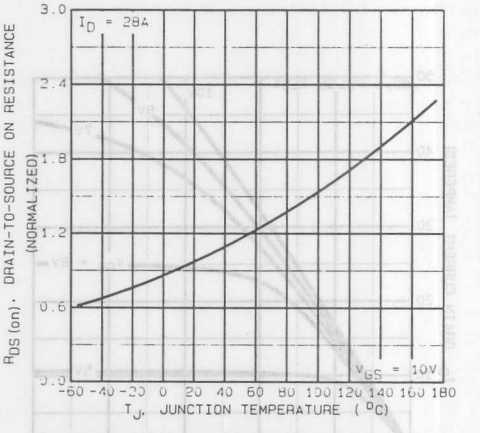


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

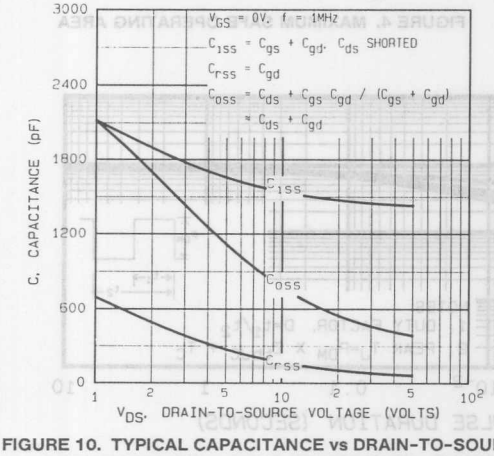


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

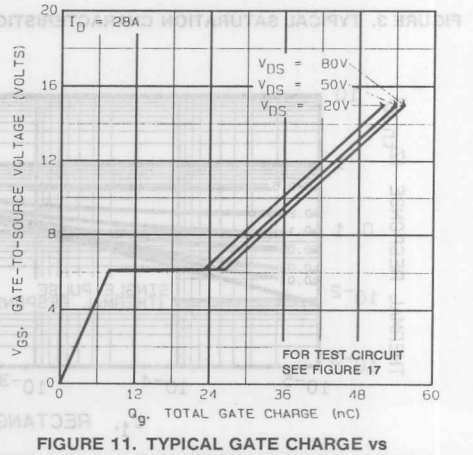


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

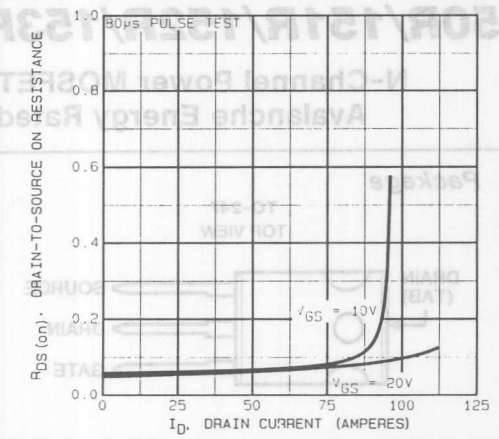


FIGURE 12. TYPICAL ON-RESISTANCE VS DRAIN CURRENT

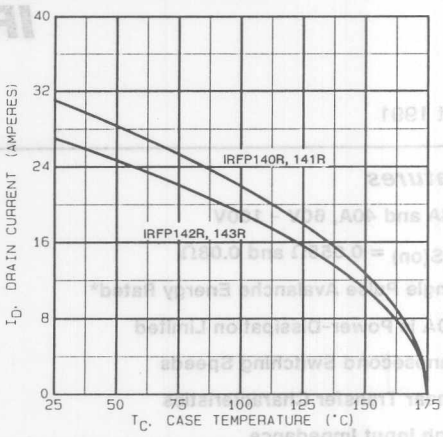


FIGURE 13. MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

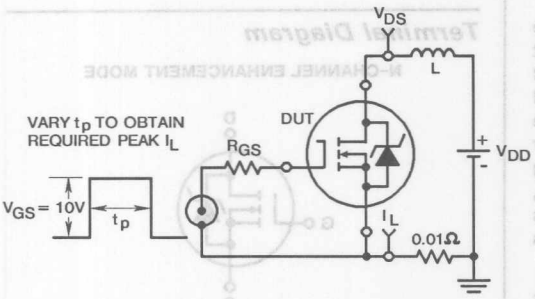


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

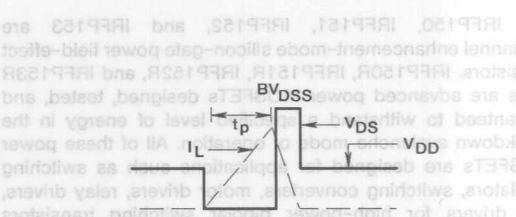


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

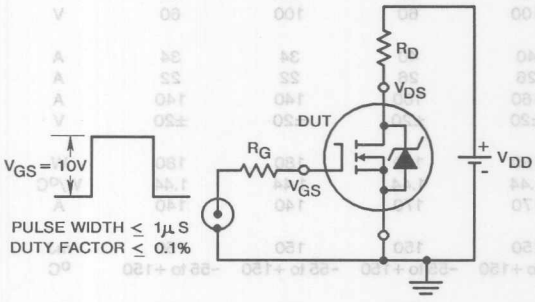


FIGURE 16. SWITCHING TIME TEST CIRCUIT

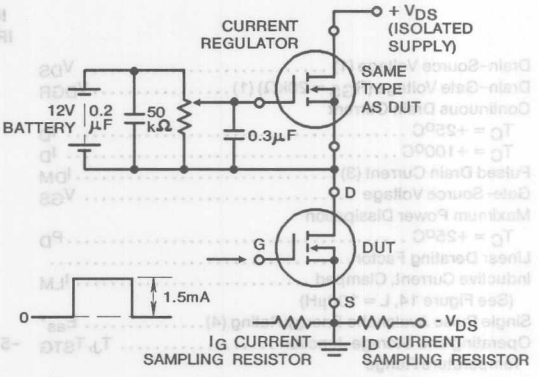


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRFP150/151/152/153
IRFP150R/151R/152R/153R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 34A and 40A, 60V - 100V
- $r_{DS(on)}$ = 0.055Ω and 0.08Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

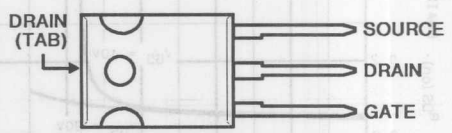
Description

The IRFP150, IRFP151, IRFP152, and IRFP153 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFP150R, IRFP151R, IRFP152R, and IRFP153R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

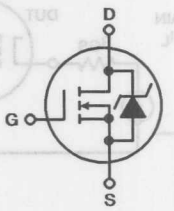
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP150 IRFP150R	IRFP151 IRFP151R	IRFP152 IRFP152R	IRFP153 IRFP153R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	60	100	60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	60	100	60	V
Continuous Drain Current					
T_C = +25°C ..... I_D	40	40	34	34	A
T_C = +100°C ..... I_D	26	26	22	22	A
Pulsed Drain Current (3) ..... I_{DM}	160	160	140	140	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	180	180	180	180	W
Linear Derating Factor	1.44	1.44	1.44	1.44	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	170	170	140	140	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	150	150	150	150	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 10V, starting T_J = +25°C, L = 170μH, R_{GS} = 50Ω, I_{PEAK} = 40A. See Figure 15.

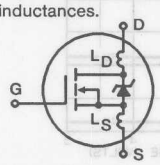
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

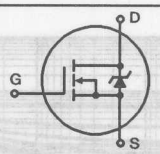
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File Number **2318.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP150/152, IRFP150R/152R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	-	-	V
IRFP151/153, IRFP151R/153R			60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRFP150/151, IRFP150R/151R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	40	-	-	A
IRFP152/153, IRFP152R/153R			34	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP150/151, IRFP150R/151R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 22A	-	0.045	0.055	Ω
IRFP152/153, IRFP152R/153R			-	0.06	0.08	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 2 x VGS, I_D = 20A	13	20	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	2000	-	pF
Output Capacitance	C_{OSS}		-	1000	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	350	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D = 40A, R_G = 6.8Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	15	24	ns
Rise Time	t_r		-	140	210	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	60	89	ns
Fall Time	t_f		-	90	140	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 40A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	70	110	nC
Gate-Source Charge	Q_{gs}		-	20	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	30	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.70	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	40	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	170	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 40A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 40A, dI_F/dt = 100A/µs	98	-	530	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 40A, dI_F/dt = 100A/µs	0.41	-	2.5	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 10V, Start T_J = +25°C, L = 170µH, R_{GS} = 50Ω, I_{PEAK} = 40A (See Figure 15)

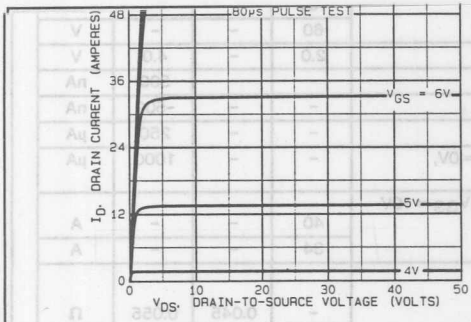


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

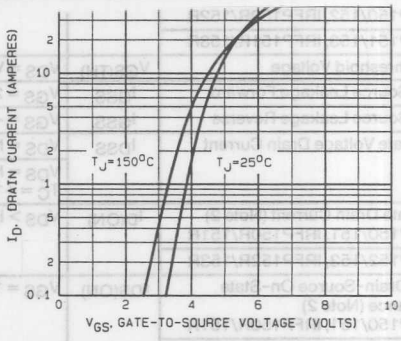


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

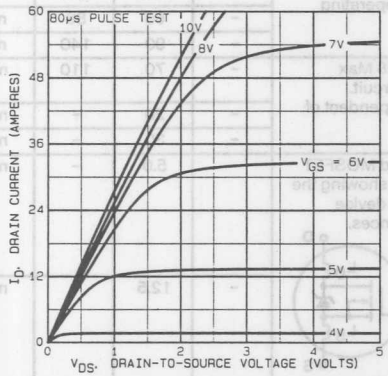


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

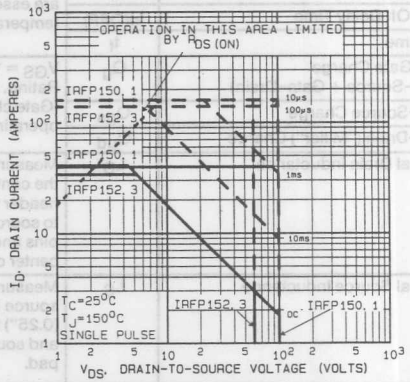


FIGURE 4. MAXIMUM SAFE OPERATING AREA

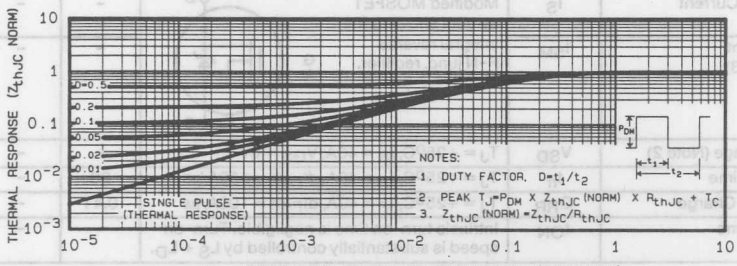


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

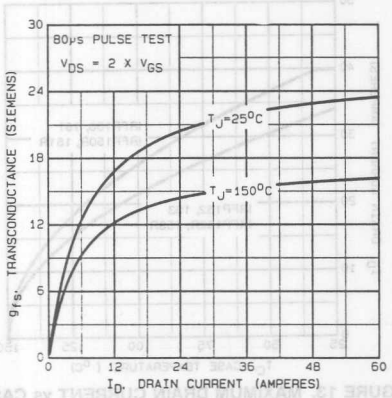


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

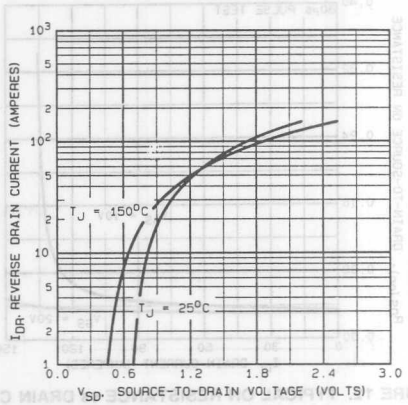


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

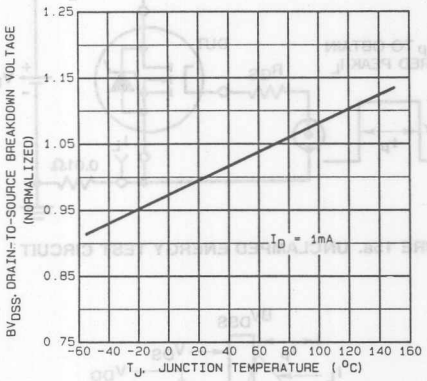


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

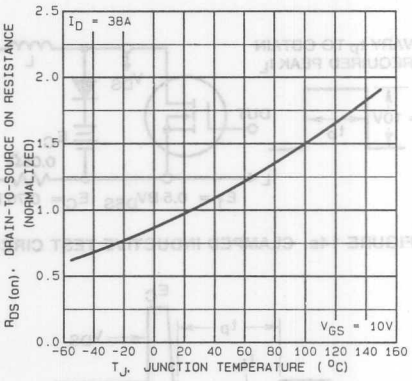


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

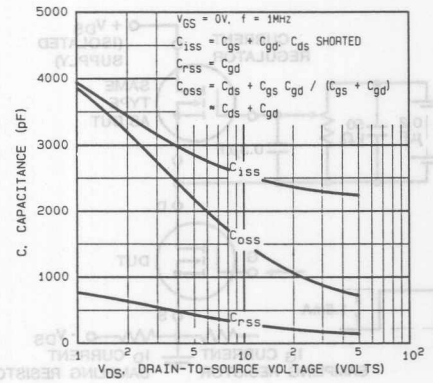


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

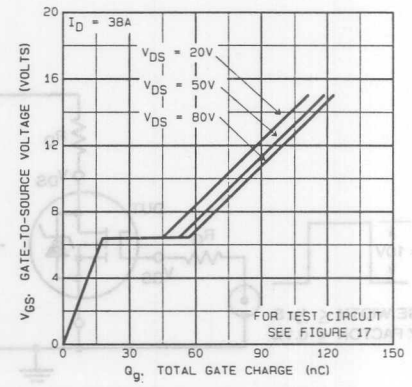


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

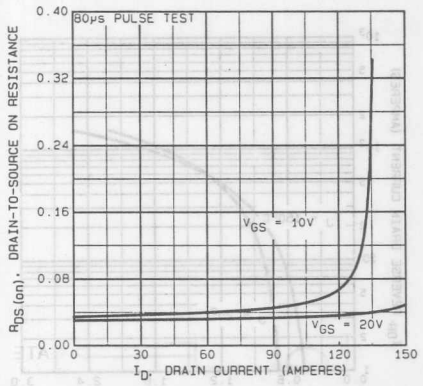


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

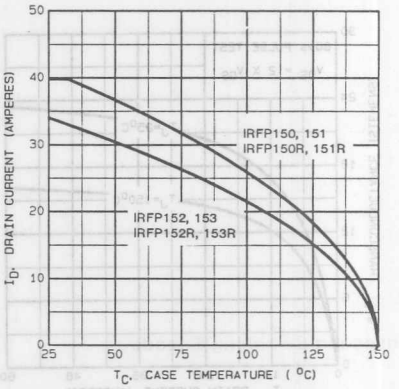


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

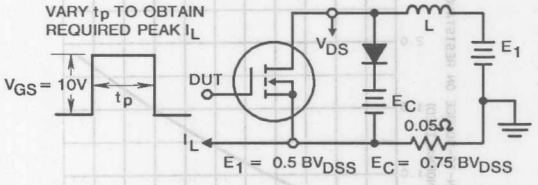


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

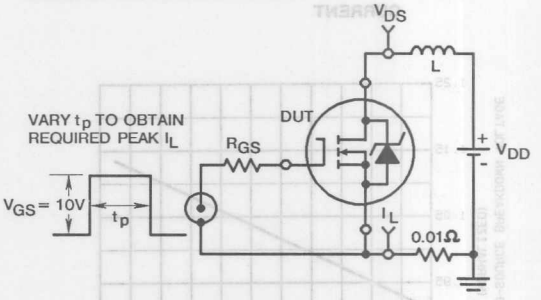


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

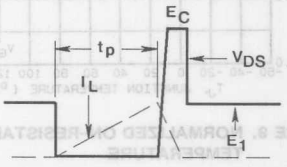


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

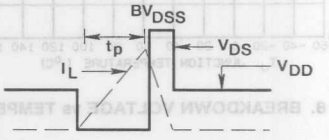


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

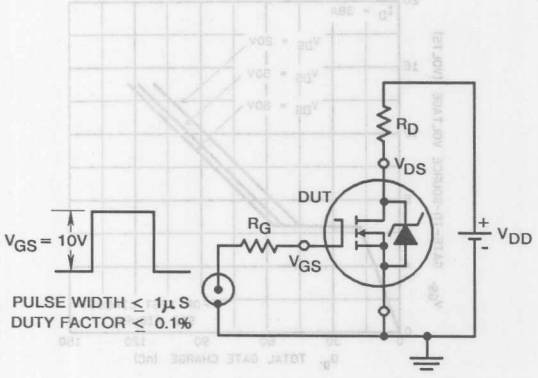


FIGURE 16. SWITCHING TIME TEST CIRCUIT

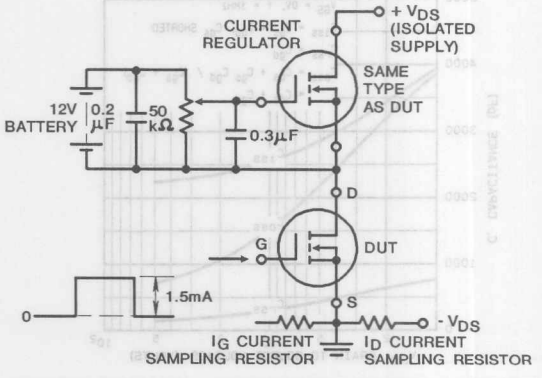


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS IRFP240R, IRFP241R IRFP242R, IRFP243R

N-Channel Power MOSFETs Avalanche Energy Rated

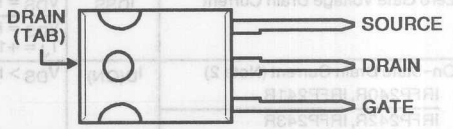
August 1991

Features

- 18A and 20A, 200V - 150V
- $r_{DS(on)}$ = 0.18Ω and 0.22Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-247
TOP VIEW



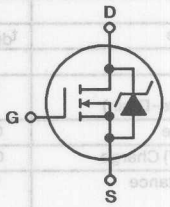
Description

The IRFP240R, IRFP241R, IRFP242R, and IRFP243R are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFP240R	IRFP241R	IRFP242R	IRFP243R	UNITS
Drain-Source Voltage (1)	V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	200	150	120	150	V
Continuous Drain Current						
T_C = +25°C	I_D	20	20	18	18	A
T_C = +100°C	I_D	12	12	11	11	A
Pulsed Drain Current (3)	I_{DM}	80	80	72	72	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	150	150	150	150	W
Linear Derating Factor		1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	510	510	510	510	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

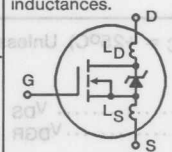
NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 1.9mH, R_{GS} = 50Ω, I_{PEAK} = 20A. See Figures 14 and 15.

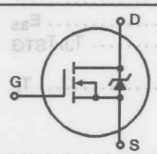
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2087.1

Drain-Source Breakdown Voltage IRFP240R, IRFP242R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	200	–	–	V
IRFP241R, IRFP243R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFP240R, IRFP241R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 11V	20	–	–	A
IRFP242R, IRFP243R			18	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP240R, IRFP241R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 10A	–	0.14	0.18	Ω
IRFP242R, IRFP243R			–	0.20	0.22	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 11A	7.3	11	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1275	–	pF
Output Capacitance	C_{OSS}		–	500	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	160	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, I_D = 18A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	14	21	ns
Rise Time	t_r		–	51	77	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	45	68	ns
Fall Time	t_f		–	36	54	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	43	60	nC
Gate-Source Charge	Q_{gs}		–	10	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	32	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	20	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	80	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 18A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 18A, dI_F/dt = 100A/μs	120	250	530	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 18A, dI_F/dt = 100A/μs	1.3	2.6	5.6	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 1.9mH, R_{GS} = 50Ω, I_{PEAK} = 20A. (See Figures 14 & 15)

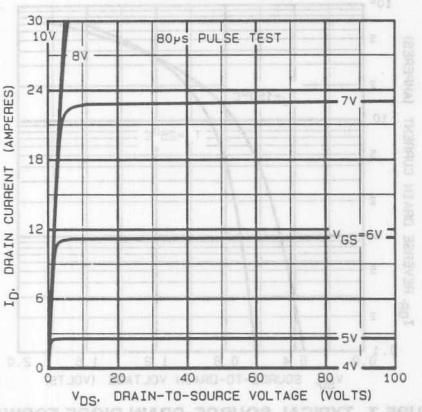


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

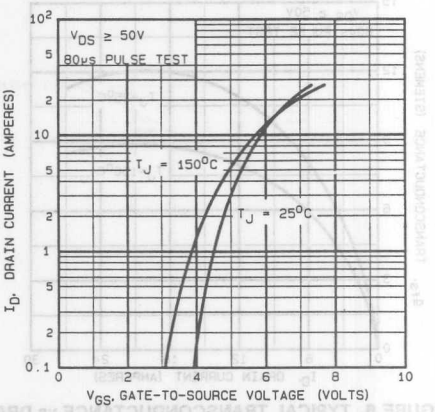


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

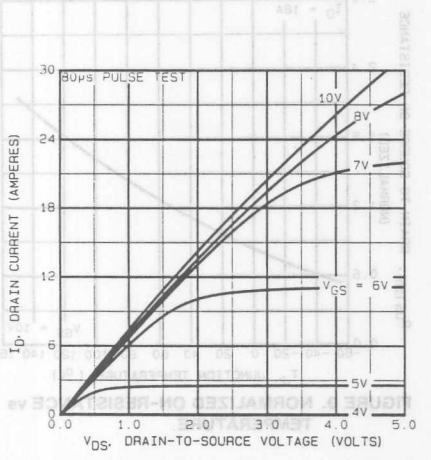


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

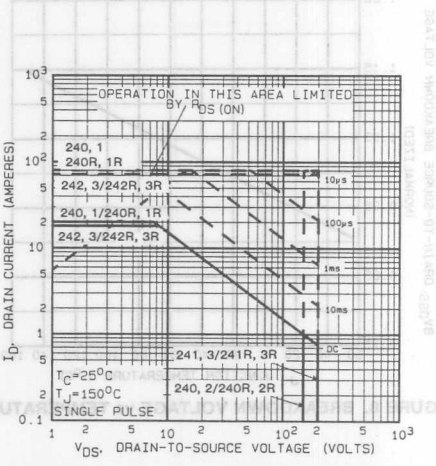


FIGURE 4. MAXIMUM SAFE OPERATING AREA

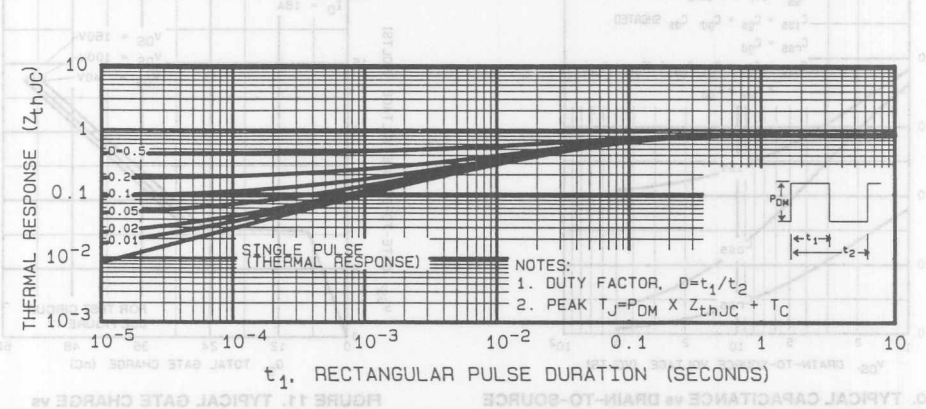


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

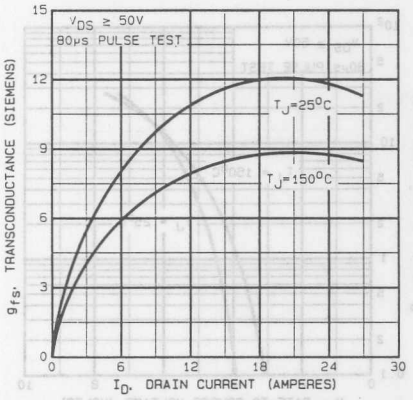


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

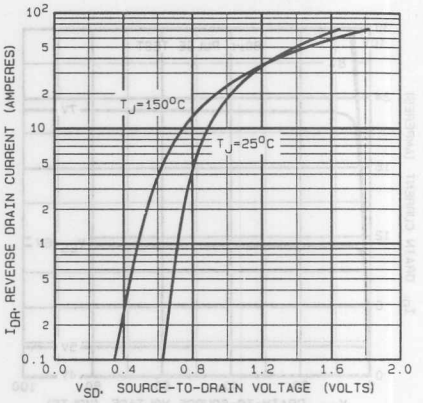


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

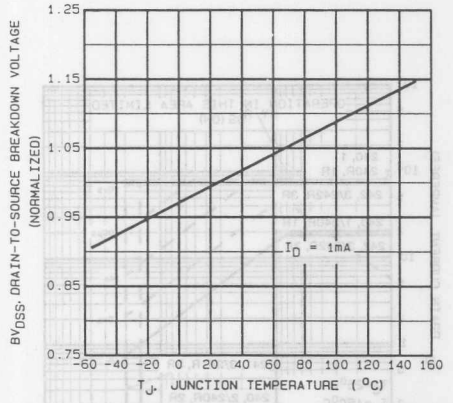


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

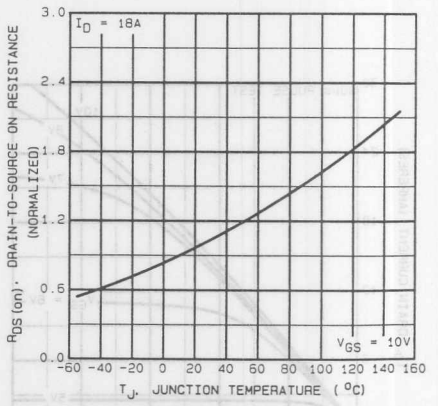


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

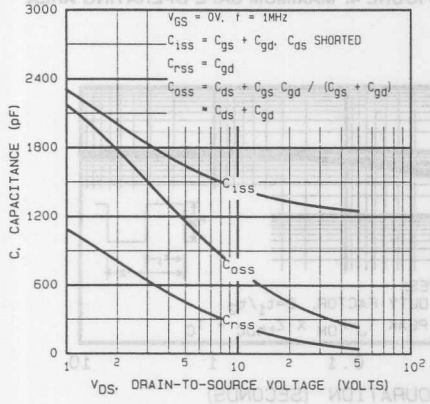


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

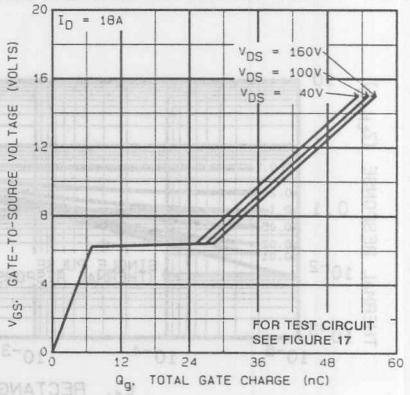


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

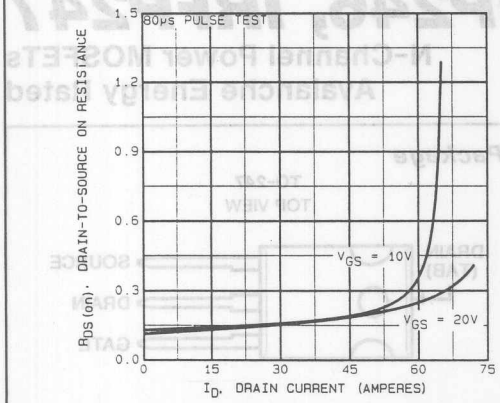


FIGURE 12. TYPICAL ON-RESISTANCE VS DRAIN CURRENT

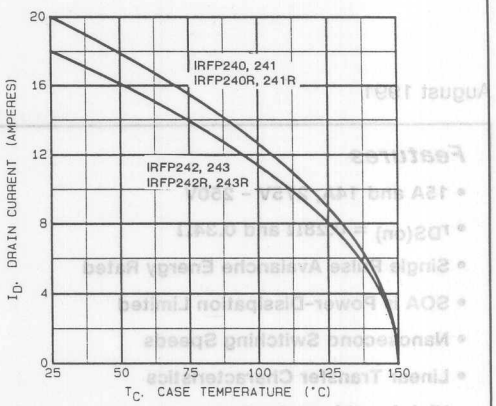


FIGURE 13. MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

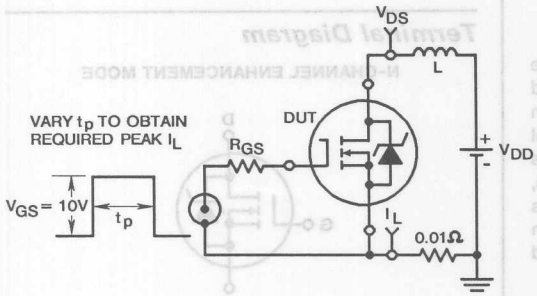


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

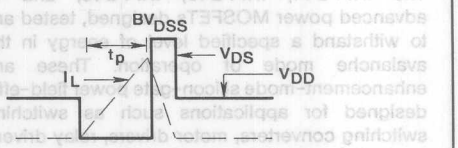


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

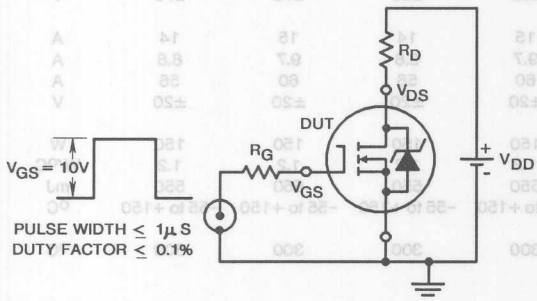


FIGURE 16. SWITCHING TIME TEST CIRCUIT

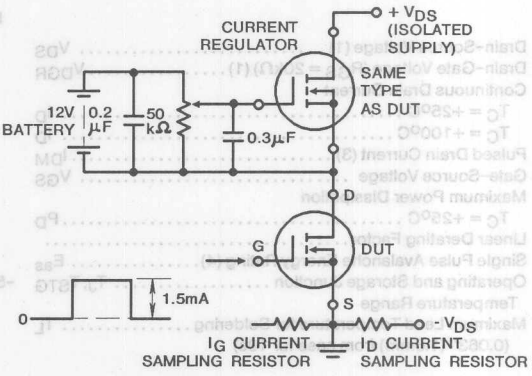


FIGURE 17. GATE CHARGE TEST CIRCUIT

4

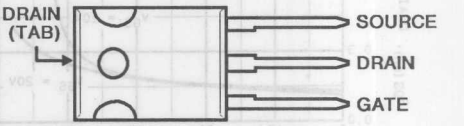
N-CHANNEL POWER MOSFETs

Features

- 15A and 14A, 275V - 250V
- $r_{DS(on)}$ = 0.28Ω and 0.34Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275V, 250V DC Rated - 120V AC Line System Operation

Package

TO-247
TOP VIEW



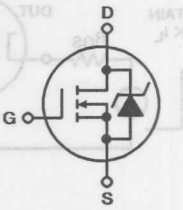
Description

The IRFP244, IRFP245, IRFP246, and IRFP247 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP244	IRFP245	IRFP246	IRFP247	UNITS
Drain-Source Voltage (1) ..... V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	250	250	275	275	V
Continuous Drain Current					
T_C = +25°C ..... I_D	15	14	15	14	A
T_C = +100°C ..... I_D	9.7	8.8	9.7	8.8	A
Pulsed Drain Current (3) ..... I_{DM}	60	56	60	56	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	550	550	550	550	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

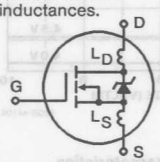
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 4.0mH, R_{GS} = 25Ω, I_{PEAK} = 15A. See Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

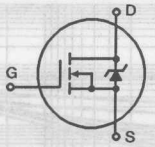
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File Number 2211.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP244, IRFP245	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	250	–	–	V
IRFP246, IRFP247			275	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFP244, IRFP246	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	15	–	–	A
IRFP245, IRFP247			14	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP244, IRFP246	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 10A	–	0.20	0.28	Ω
IRFP245, IRFP247			–	0.24	0.34	V
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 10A	6.7	11	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1300	–	pF
Output Capacitance	C_{OSS}		–	320	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	69	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 15A, R_G = 9.1Ω, See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	16	24	ns
Rise Time	t_r		–	67	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	53	80	ns
Fall Time	t_f		–	49	74	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 15A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	39	59	nC
Gate-Source Charge	Q_{gs}		–	6.6	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	20	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from package to source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	15	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	60	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 15A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/μs	150	300	640	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/μs	1.6	3.4	7.2	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.0mH, R_{GS} = 25Ω, I_{PEAK} = 15A. (See Figures 14 & 15)

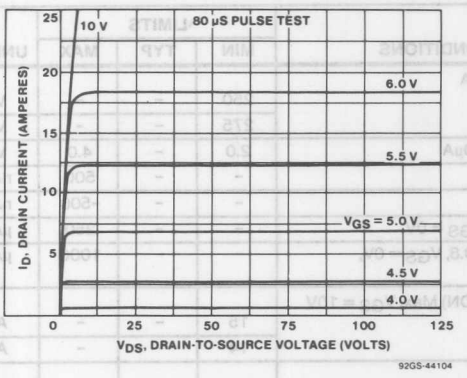


Fig. 1 - Typical output characteristics.

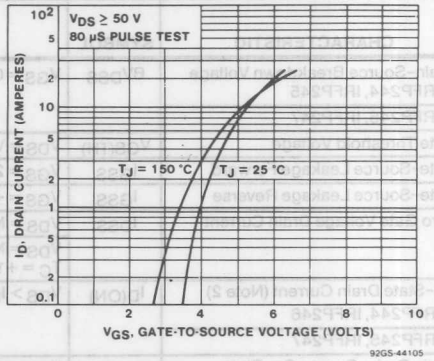


Fig. 2 - Typical transfer characteristics.

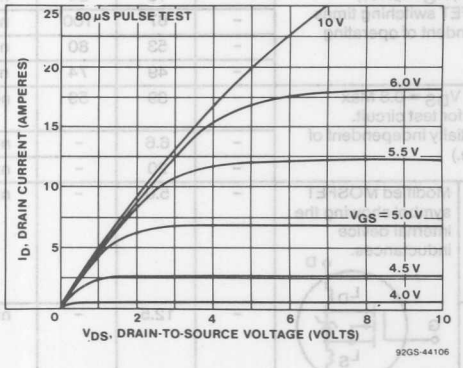


Fig. 3 - Typical saturation characteristics.

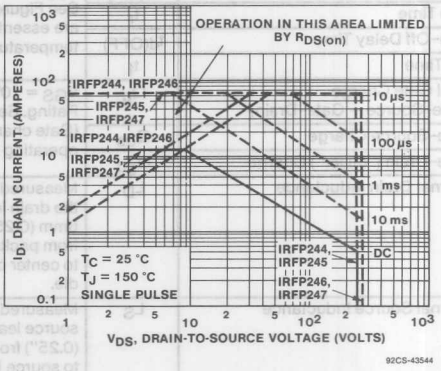


Fig. 4 - Maximum safe operating area.

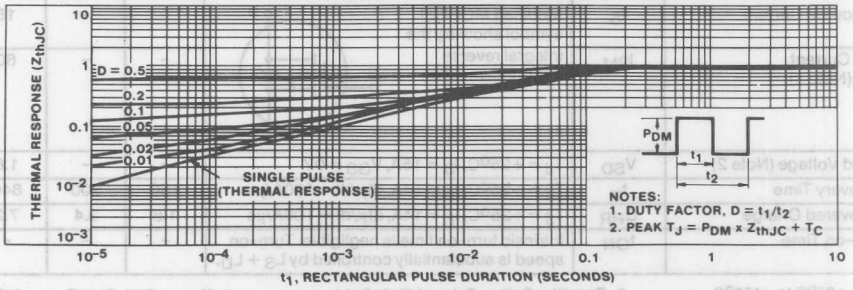


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

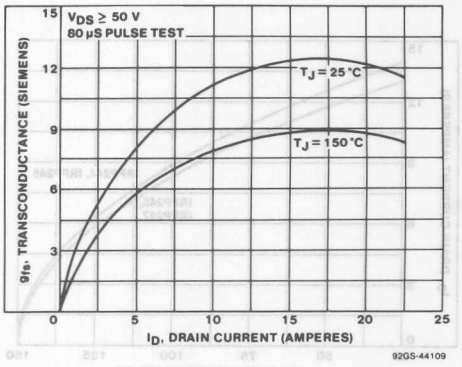


Fig. 6 - Typical transconductance vs. drain current.

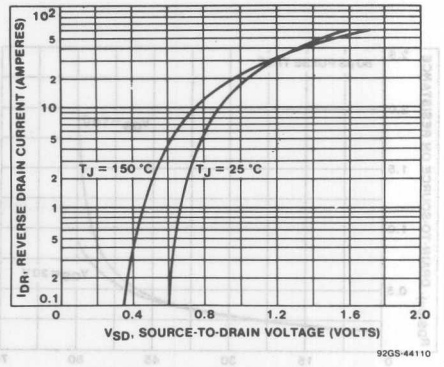


Fig. 7 - Typical source-drain diode forward voltage.

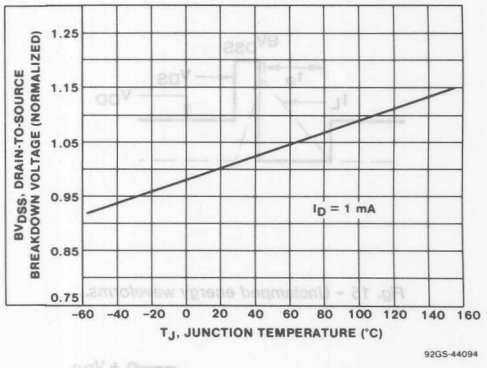


Fig. 8 - Breakdown voltage vs. temperature.

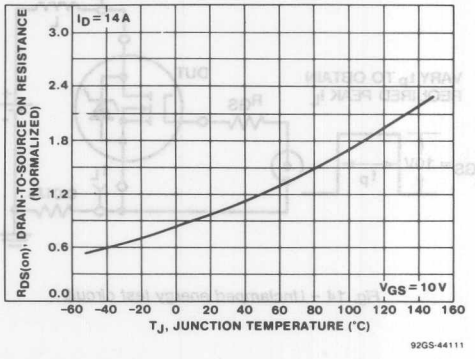


Fig. 9 - Normalized on-resistance vs. temperature.

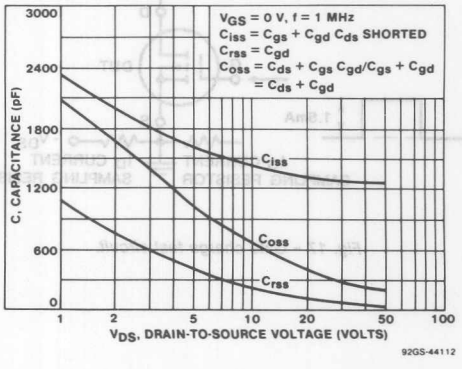


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

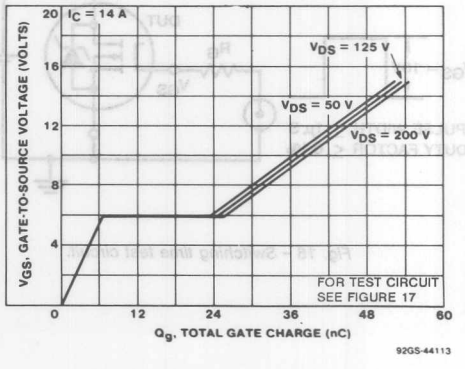


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

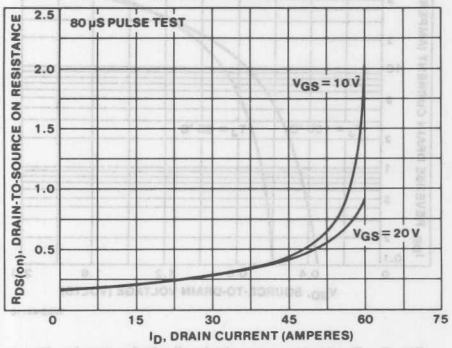


Fig. 12 - Typical on-resistance vs. drain current.

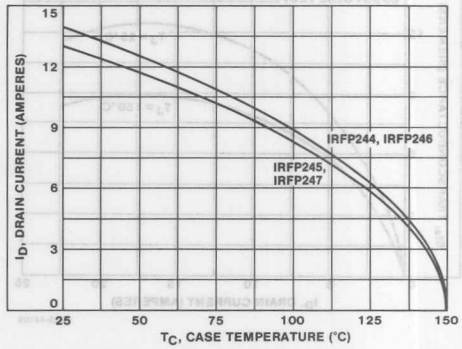


Fig. 13 - Maximum drain current vs case temperature.

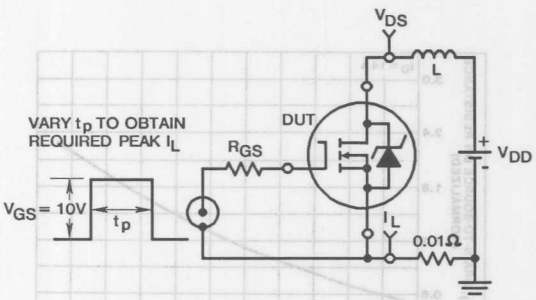


Fig. 14 - Unclamped energy test circuit.

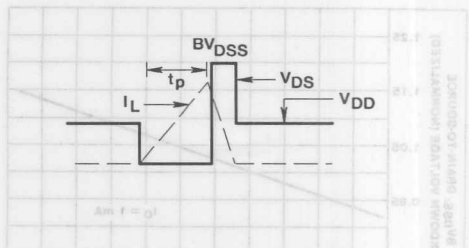


Fig. 15 - Unclamped energy waveforms.

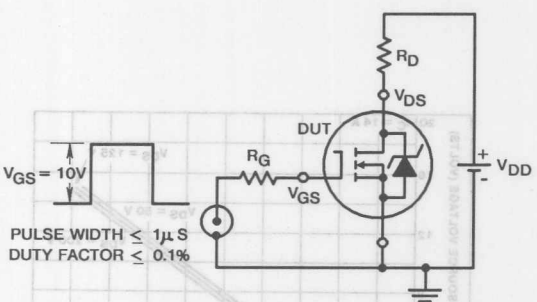


Fig. 16 - Switching time test circuit.

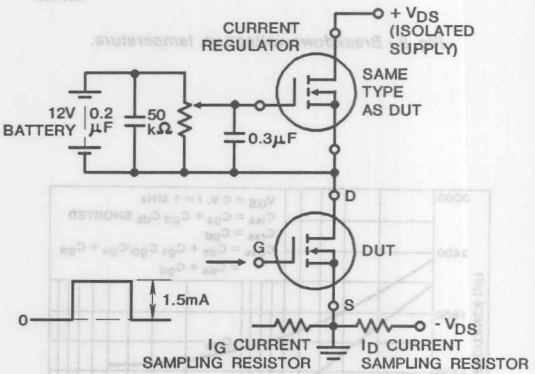


Fig. 17 - Gate charge test circuit.

HARRIS IRFP250/251/252/253 IRFP250R/251R/252R/253R

N-Channel Power MOSFETs Avalanche Energy Rated*

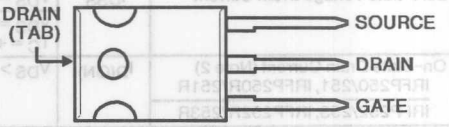
August 1991

Features

- 27A and 33A, 150V - 200V
- $r_{DS(on)}$ = 0.085Ω and 0.120Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-247
TOP VIEW



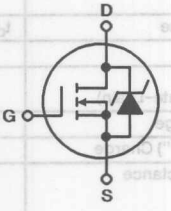
Description

The IRFP250, IRFP251, IRFP252, and IRFP253 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFP250R, IRFP251R, IRFP252R, and IRFP253R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP250 IRFP250R	IRFP251 IRFP251R	IRFP252 IRFP252R	IRFP253 IRFP253R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	33	33	27	27	A
T_C = +100°C ..... I_D	21	21	17	17	A
Pulsed Drain Current (3) ..... I_{DM}	130	130	110	110	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	180	180	180	180	W
Linear Derating Factor	1.44	1.44	1.44	1.44	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	120	120	100	100	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	810	810	810	810	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 1.1mH, R_{GS} = 50Ω, I_{PEAK} = 33A. See Figure 15.

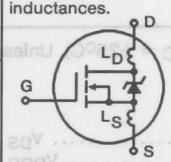
* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

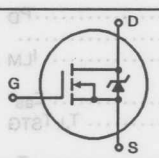
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File Number 2330.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP250/252, IRFP250R/252R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	200	–	–	V
IRFP251/253, IRFP251R/253R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFP250/251, IRFP250R/251R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, V_{GS} = 10V	33	–	–	A
IRFP252/253, IRFP252R/253R			27	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP250/251, IRFP250R/251R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 17A	–	0.07	0.085	Ω
IRFP252/253, IRFP252R/253R			–	0.09	0.120	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 17A	13	19	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2000	–	pF
Output Capacitance	C_{OSS}		–	800	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	300	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, I_D = 30A, R_G = 6.2Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	18	30	ns
Rise Time	t_r		–	125	180	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	70	100	ns
Fall Time	t_f		–	80	120	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 30A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	79	120	nC
Gate-Source Charge	Q_{gs}		–	12	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	42	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.70	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	33	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	130	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 33A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 30A, dI_F/dt = 100A/μs	140	–	630	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 30A, dI_F/dt = 100A/μs	1.8	–	8.1	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 1.1mH, R_{GS} = 50Ω, I_{PEAK} = 33A (See Figure 15)

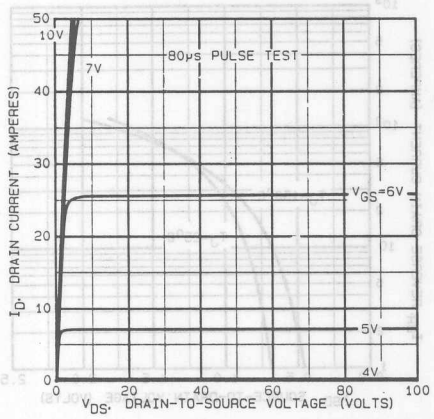


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

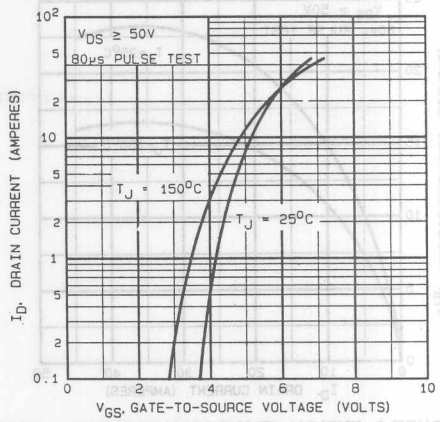


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

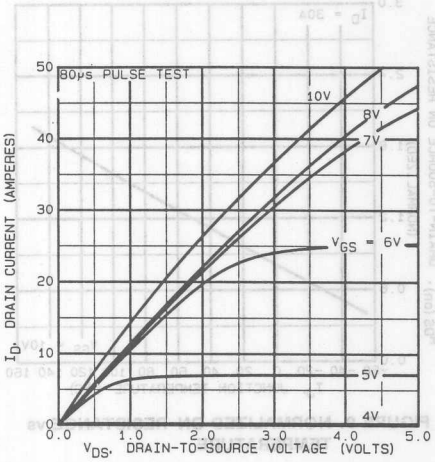


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

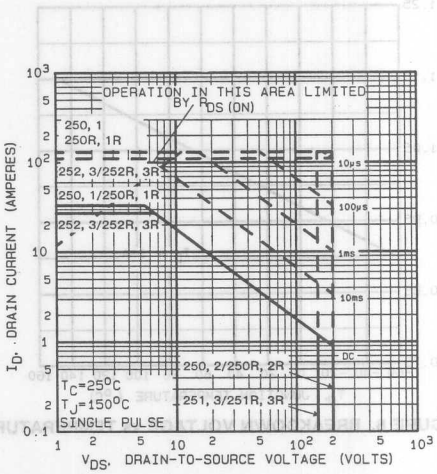


FIGURE 4. MAXIMUM SAFE OPERATING AREA

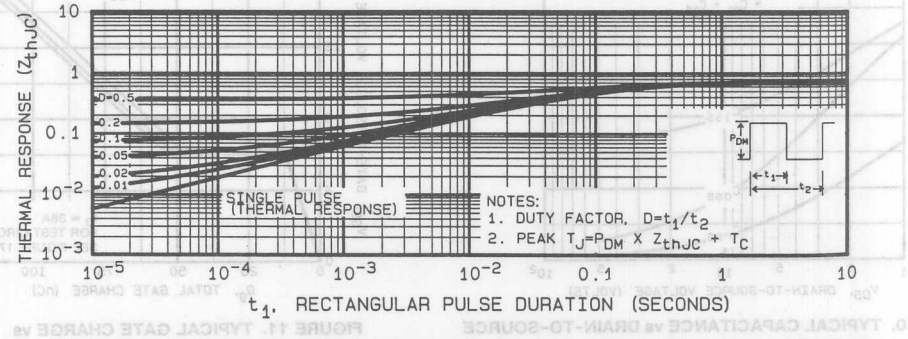


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

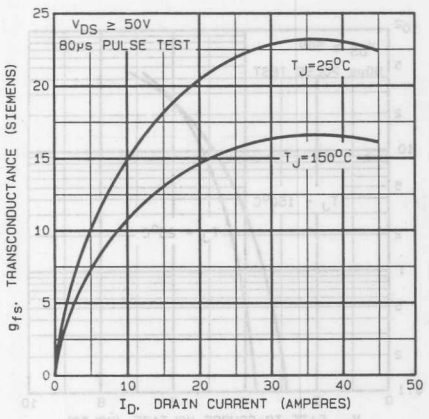


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

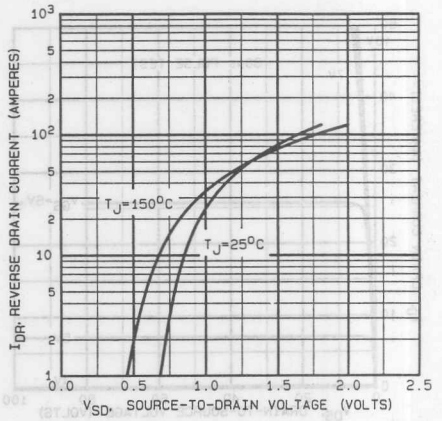


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

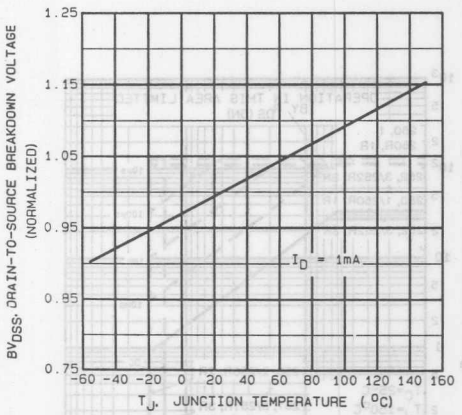


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

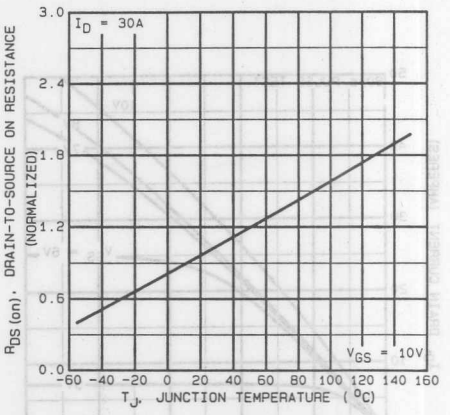


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

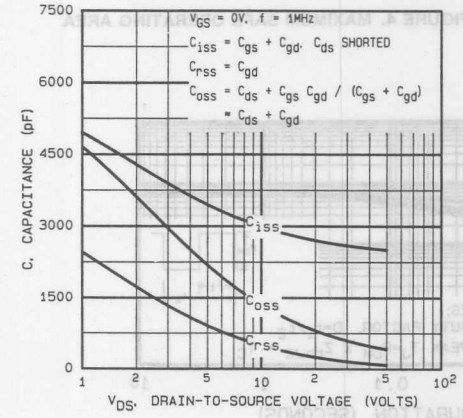


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

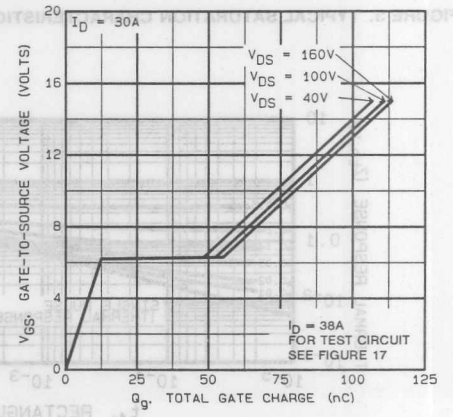


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

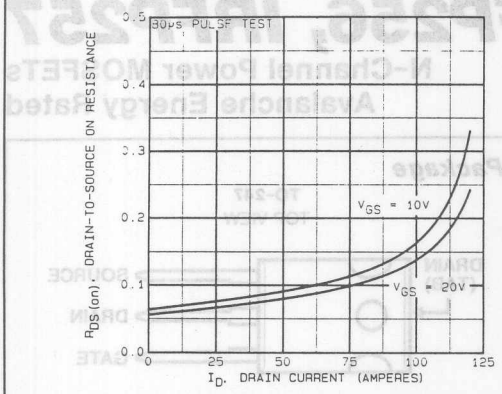


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

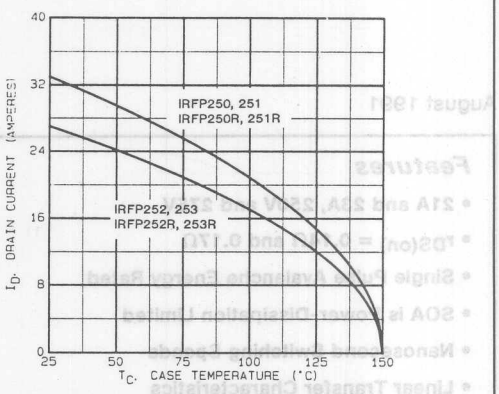


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

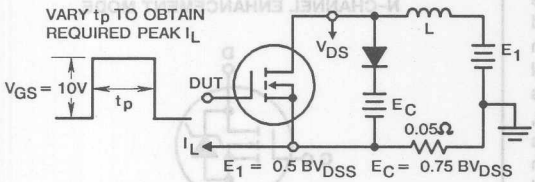


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

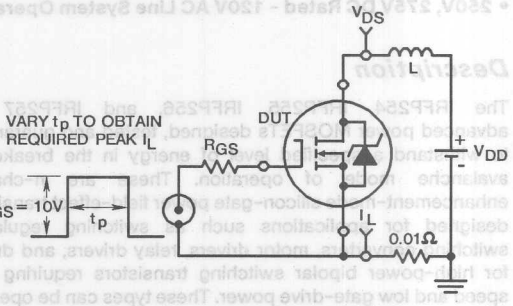


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

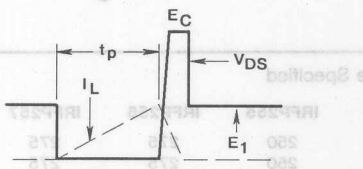


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

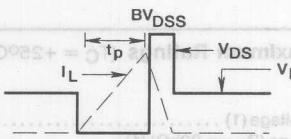


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

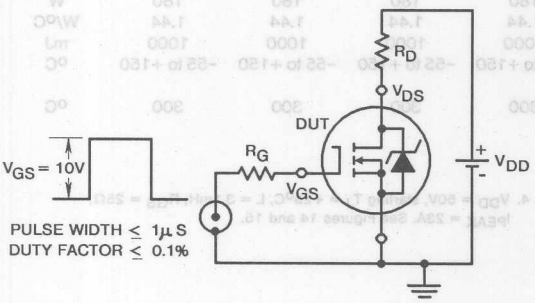


FIGURE 16. SWITCHING TIME TEST CIRCUIT

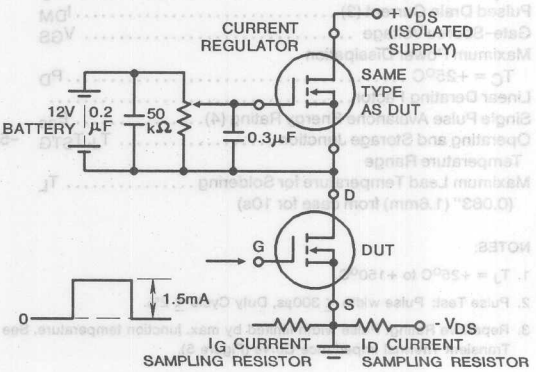


FIGURE 17. GATE CHARGE TEST CIRCUIT

4 N-CHANNEL POWER MOSFETs

HARRIS

IRFP254, IRFP255 IRFP256, IRFP257

N-Channel Power MOSFETs Avalanche Energy Rated

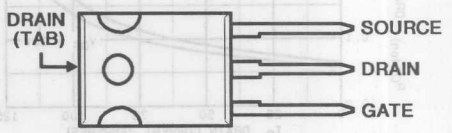
August 1991

Features

- 21A and 23A, 250V and 275V
- $r_{DS(on)} = 0.14\Omega$ and 0.17Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 250V, 275V DC Rated - 120V AC Line System Operation

Package

TO-247
TOP VIEW



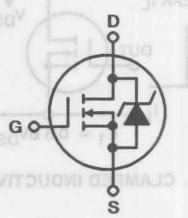
Description

The IRFP254, IRFP255, IRFP256, and IRFP257 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP254	IRFP255	IRFP256	IRFP257	UNITS
Drain-Source Voltage (1) ..... V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	250	250	275	275	V
Continuous Drain Current					
T_C = +25°C ..... I_D	23	21	23	21	A
T_C = +100°C ..... I_D	15	13	15	13	A
Pulsed Drain Current (3) ..... I_{DM}	92	84	92	84	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	180	180	180	180	W
Linear Derating Factor	1.44	1.44	1.44	1.44	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	1000	1000	1000	1000	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 3.1mH, R_{GS} = 25Ω, I_{PEAK} = 23A. See Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

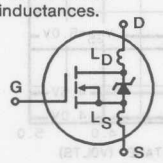
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File Number 2289.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

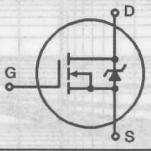
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP254, IRFP255	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	250	–	–	V
IRFP256, IRFP257			275	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFP254, IRFP256	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	23	–	–	A
IRFP255, IRFP257			21	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP254, IRFP256	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 13A	–	0.11	0.14	Ω
IRFP255, IRFP257			–	0.14	0.17	V
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 13A	11	17	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2700	–	pF
Output Capacitance	C_{OSS}		–	580	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	130	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 23A, R_G = 6.2Ω, See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	19	29	ns
Rise Time	t_r		–	84	130	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	75	110	ns
Fall Time	t_f		–	65	98	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 23A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	87	130	nC
Gate-Source Charge	Q_{gs}		–	14	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	73	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die.	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from package to source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.70	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.10	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Modified MOSFET symbol showing the internal device inductances.



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	23	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	92	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 23A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 22A, dI_F/dt = 100A/µs	150	310	650	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 22A, dI_F/dt = 100A/µs	1.9	4	8.4	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 3.1mH, R_{GS} = 25Ω, I_{PEAK} = 23A. (See Figures 14 & 15)

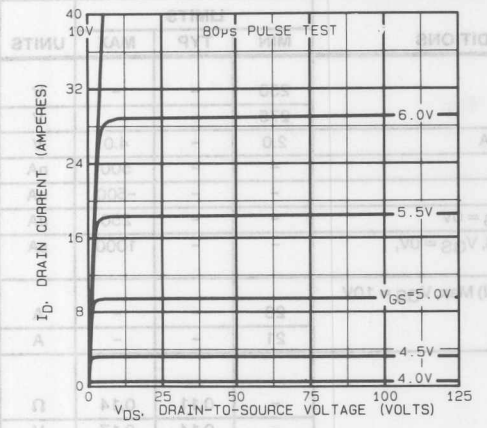


Fig. 1 - Typical output characteristics.

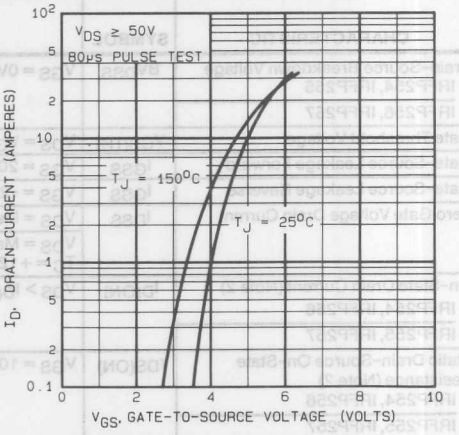


Fig. 2 - Typical transfer characteristics.

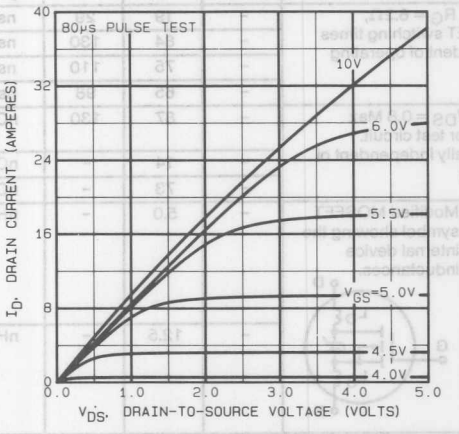


Fig. 3 - Typical saturation characteristics.

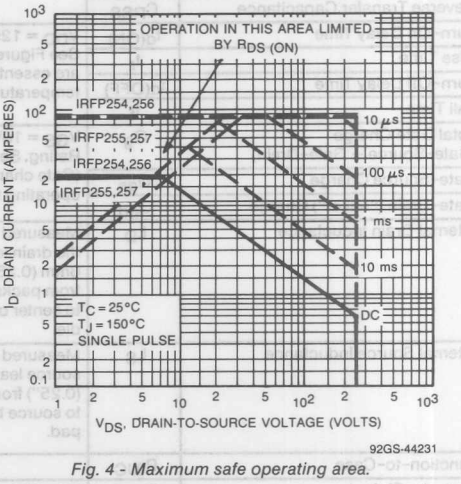


Fig. 4 - Maximum safe operating area.

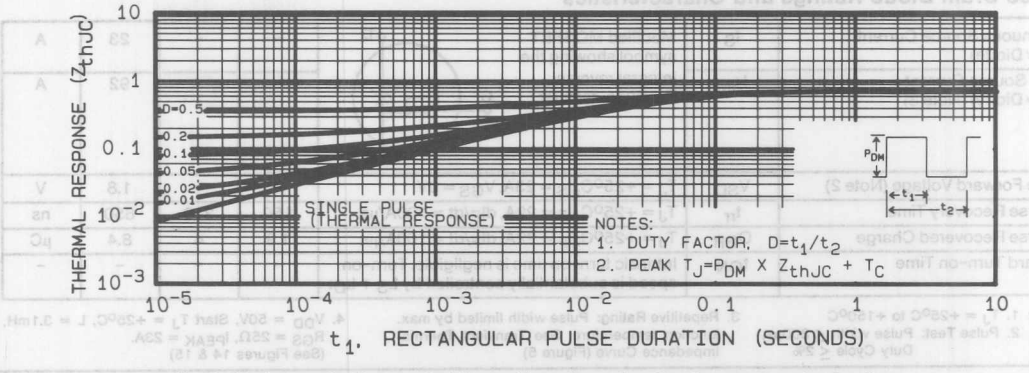


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

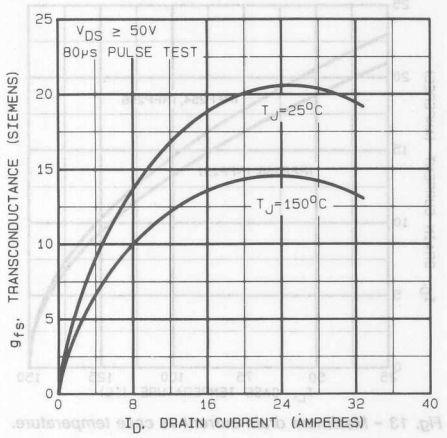


Fig. 6 - Typical transconductance vs. drain current.

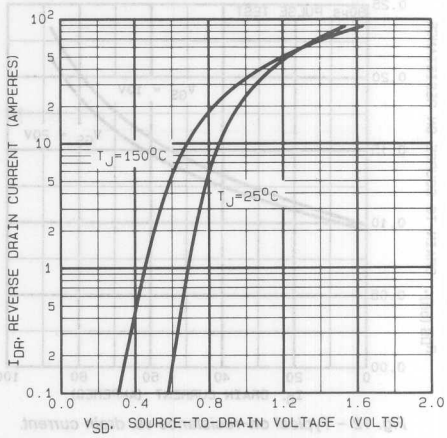


Fig. 7 - Typical source-drain diode forward voltage.

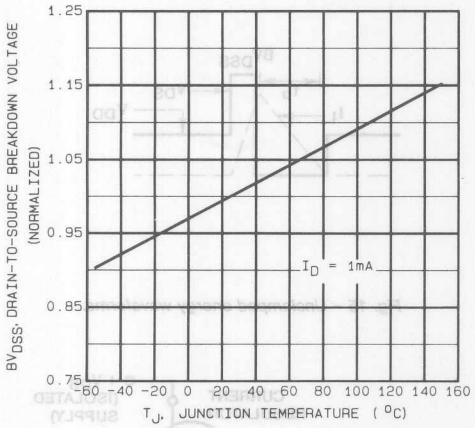


Fig. 8 - Breakdown voltage vs. temperature.

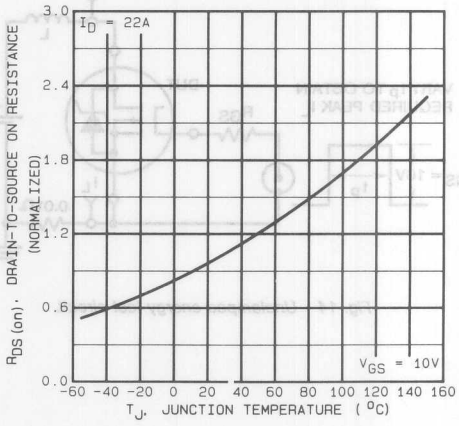


Fig. 9 - Normalized on-resistance vs. temperature.

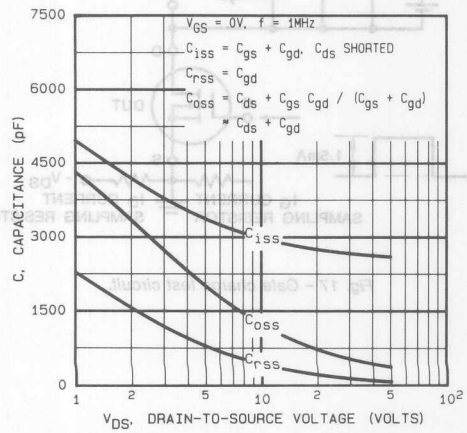


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

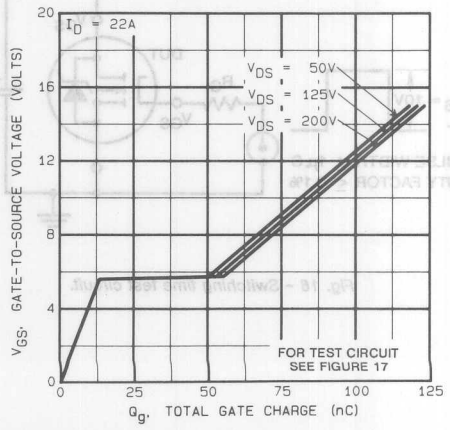


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

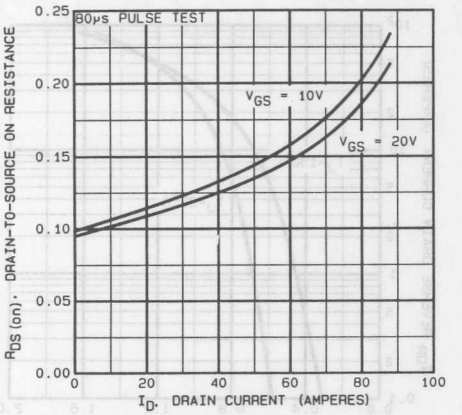


Fig. 12 – Typical on-resistance vs. drain current.

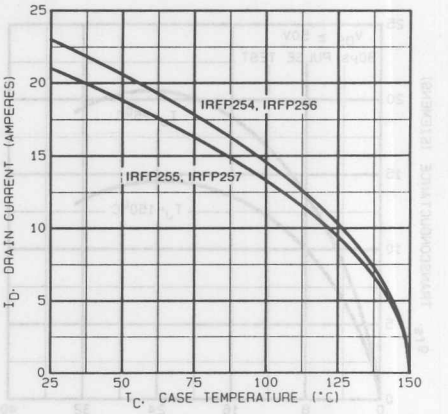


Fig. 13 – Maximum drain current vs case temperature.

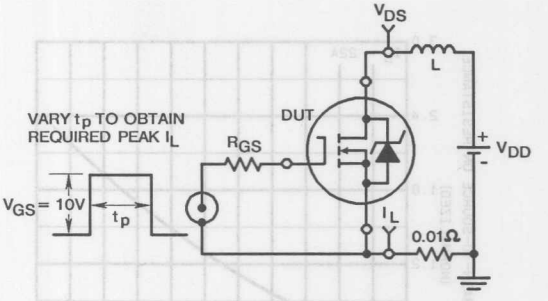


Fig. 14 – Unclamped energy test circuit.

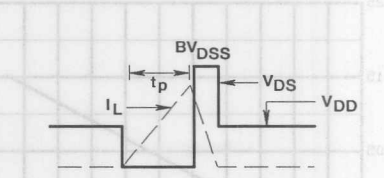


Fig. 15 – Unclamped energy waveforms.

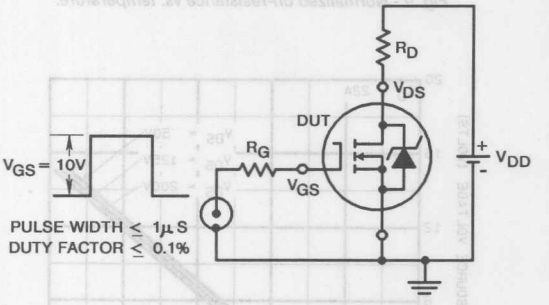


Fig. 16 – Switching time test circuit.

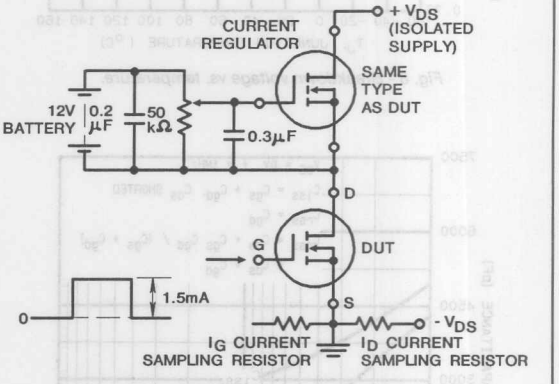


Fig. 17 – Gate charge test circuit.

HARRIS IRFP340R, IRFP341R IRFP342R, IRFP343R

N-Channel Power MOSFETs Avalanche Energy Rated

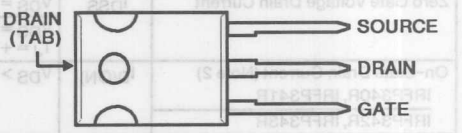
August 1991

Features

- 11A and 8.7A, 350V and 400V
- $r_{DS(on)}$ = 0.55Ω and 0.80Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-247
TOP VIEW



Description

The IRFP340R, IRFP341R, IRFP342R, and IRFP343R are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFP340R	IRFP341R	IRFP342R	IRFP343R	UNITS
Drain-Source Voltage (1)	V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	400	350	400	350	V
Continuous Drain Current						
T_C = +25°C	I_D	11	11	8.7	8.7	A
T_C = +100°C	I_D	6.8	6.8	5.5	5.5	A
Pulsed Drain Current (3)	I_{DM}	44	44	35	35	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	150	150	150	150	W
Linear Derating Factor		1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	480	480	480	480	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

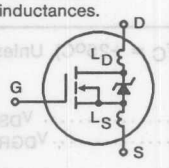
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 7.0mH, R_{GS} = 50Ω, I_{PEAK} = 11A. See Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

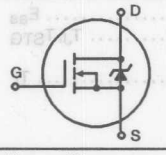
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File Number **2088.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP340R, IRFP342R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	–	–	V
IRFP341R, IRFP343R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFP340R, IRFP341R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	11	–	–	A
IRFP342R, IRFP343R			8.7	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP340R, IRFP341R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.5A	–	0.47	0.55	Ω
IRFP342R, IRFP343R			–	0.68	0.80	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 5.5A	6.1	9.1	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1250	–	pF
Output Capacitance	C_{OSS}		–	300	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	80	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 200V, I_D = 11A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	14	21	ns
Rise Time	t_r		–	27	41	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	75	ns
Fall Time	t_f		–	24	36	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	41	63	nC
Gate-Source Charge	Q_{gs}		–	6.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	23	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	11	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	44	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 11A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 10A, dI_F/dt = 100A/μs	170	370	790	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 10A, dI_F/dt = 100A/μs	1.6	3.8	8.2	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 7.0mH, R_{GS} = 50Ω, I_{PEAK} = 11A. (See Figures 14 & 15)

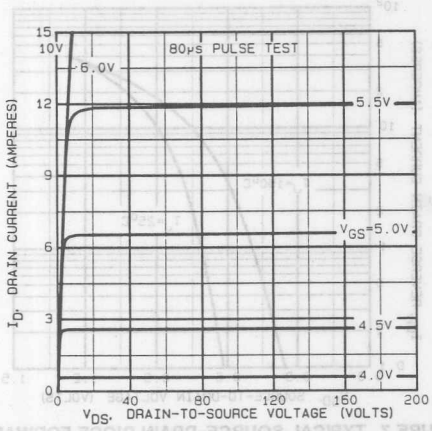


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

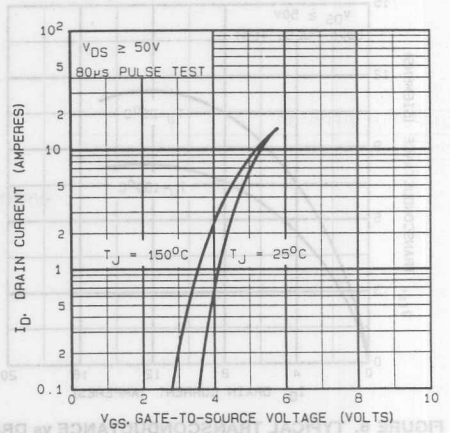


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

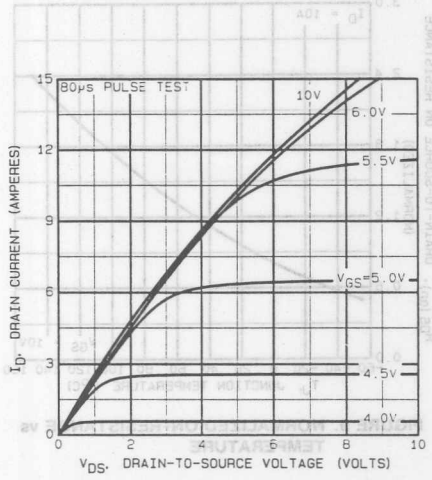


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

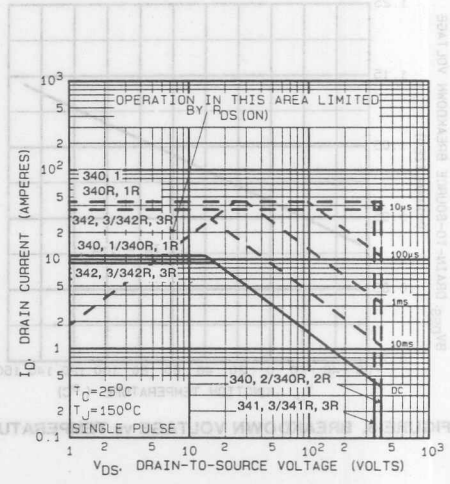


FIGURE 4. MAXIMUM SAFE OPERATING AREA

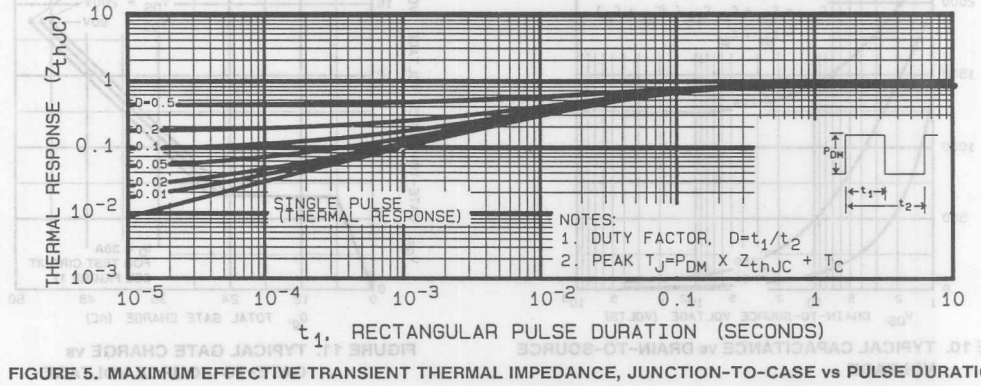


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

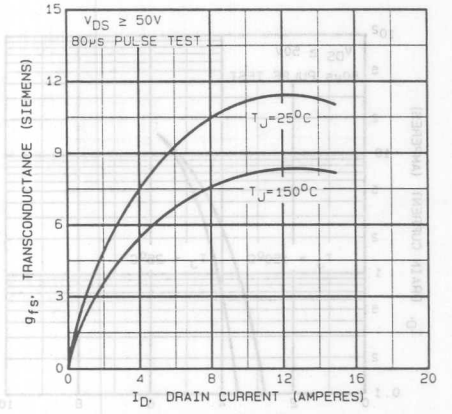


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

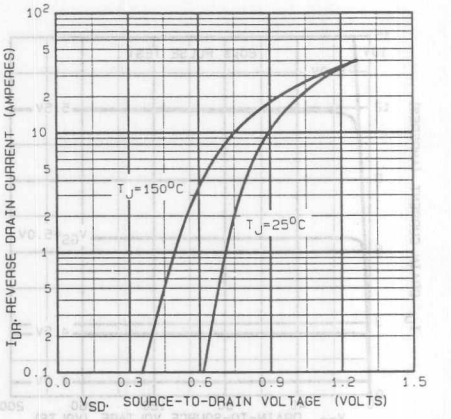


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

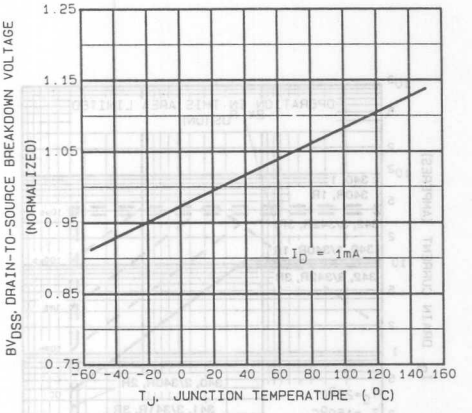


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

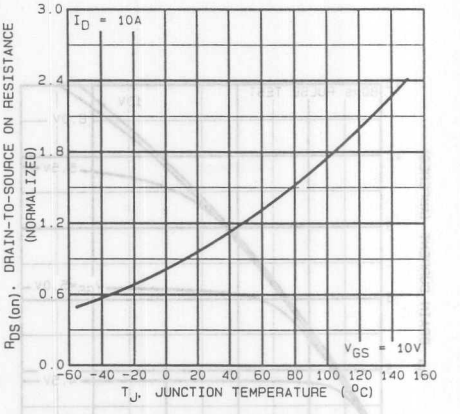


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

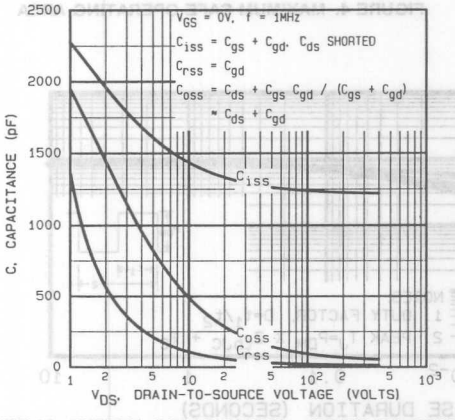


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

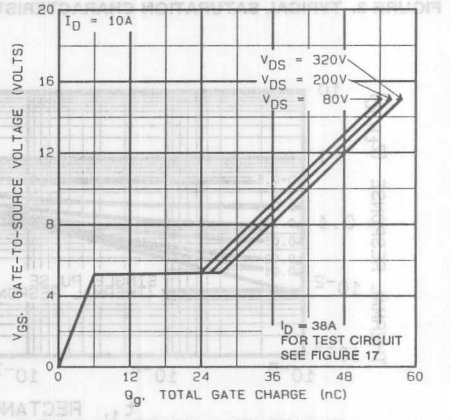


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

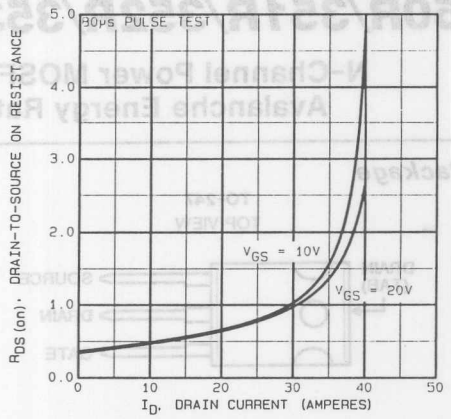


FIGURE 12. TYPICAL ON-RESISTANCE VS DRAIN CURRENT

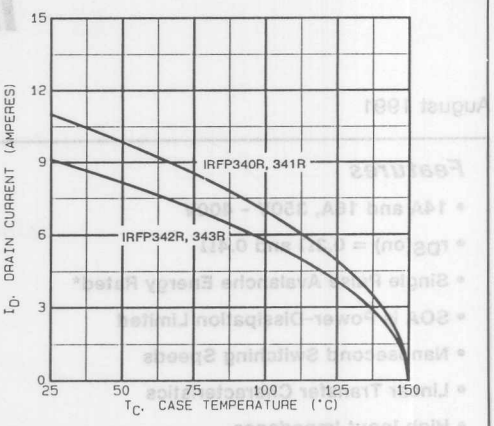


FIGURE 13. MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

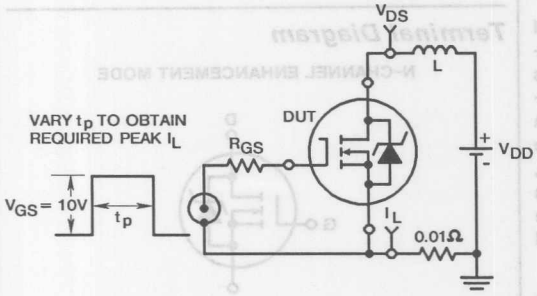


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

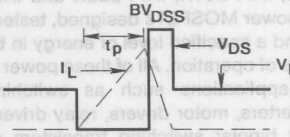


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

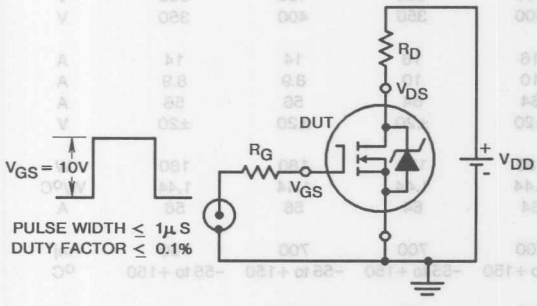


FIGURE 16. SWITCHING TIME TEST CIRCUIT

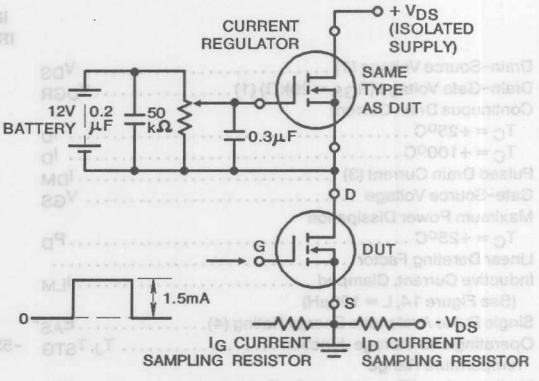


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRFP350/351/352/353
IRFP350R/351R/352R/353R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 14A and 16A, 350V - 400V
- $r_{DS}(on)$ = 0.3Ω and 0.4Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

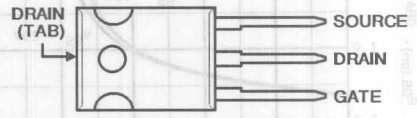
Description

The IRFP350, IRFP351, IRFP352, and IRFP353 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFP350R, IRFP351R, IRFP352R and IRFP353R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

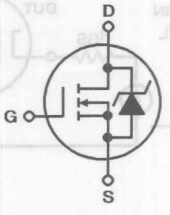
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP350 IRFP350R	IRFP351 IRFP351R	IRFP352 IRFP352R	IRFP353 IRFP353R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	16	16	14	14	A
T_C = +100°C ..... I_D	10	10	8.9	8.9	A
Pulsed Drain Current (3) ..... I_{DM}	64	64	56	56	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	180	180	180	180	W
Linear Derating Factor	1.44	1.44	1.44	1.44	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	64	64	56	56	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	700	700	700	700	mj
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

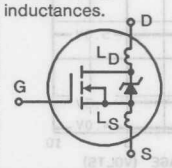
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 40V, starting T_J = +25°C, L = 5.66mH, R_{GS} = 50Ω, I_{PEAK} = 15A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

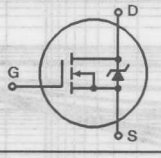
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File Number 2319.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP350/352, IRFP350R/352R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	–	–	V
IRFP351/353, IRFP351R/353R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFP350/351, IRFP350R/351R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\,Max}$, V_{GS} = 10V	16	–	–	A
IRFP352/353, IRFP352R/353R			14	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP350/351, IRFP350R/351R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8.9A	–	0.25	0.3	Ω
IRFP352/353, IRFP352R/353R			–	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 2 x V_{GS}, I_D = 8.0A	8.0	10	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2000	–	pF
Output Capacitance	C_{OSS}		–	400	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	100	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 16A, R_G = 6.2Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	11	18	ns
Rise Time	t_r		–	53	77	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	70	110	ns
Fall Time	t_f		–	45	71	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 16A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	83	130	nC
Gate-Source Charge	Q_{gs}		–	10	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	33	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.70	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.10	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	16	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	64	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 16A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 15A, dI_F/dt = 100A/µs	270	–	1300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 15A, dI_F/dt = 100A/µs	1.7	–	8.1	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 40V, Start T_J = +25°C, L = 5.66mH, R_{GS} = 50Ω, I_{PEAK} = 15A (See Figure 15)

Performance Curves

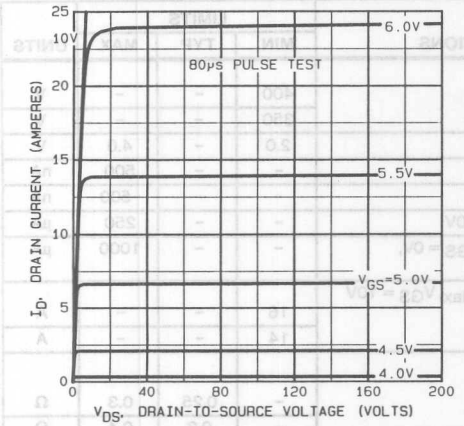


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

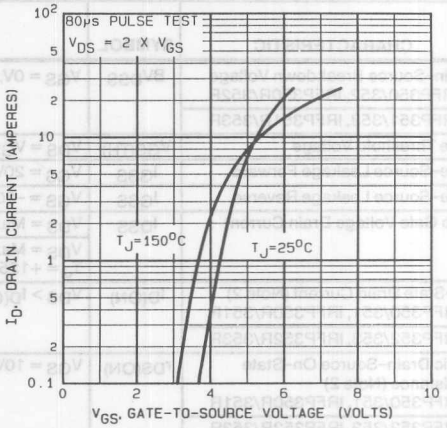


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

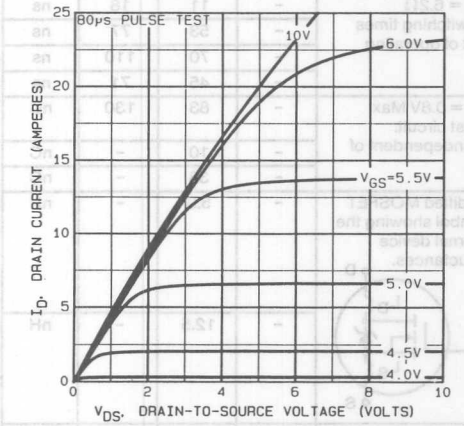


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

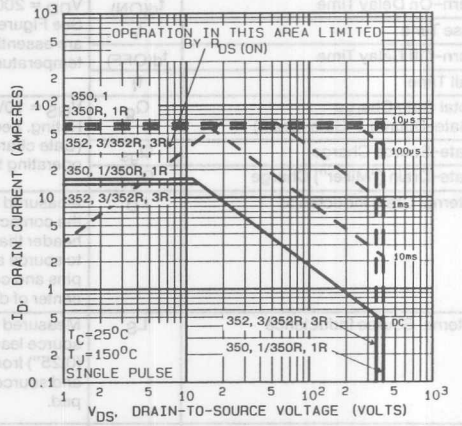


FIGURE 4. MAXIMUM SAFE OPERATING AREA

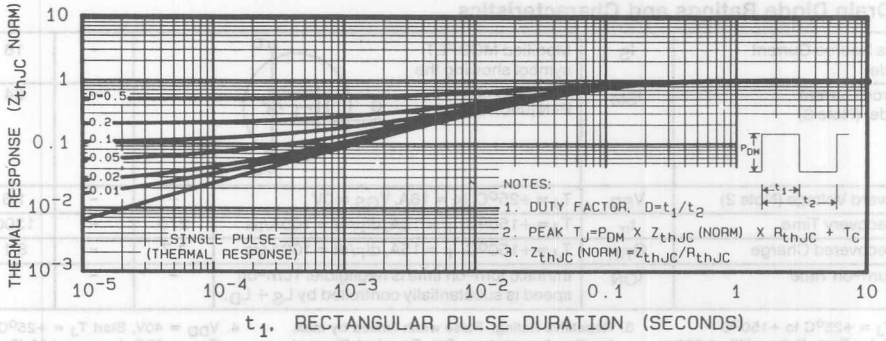


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

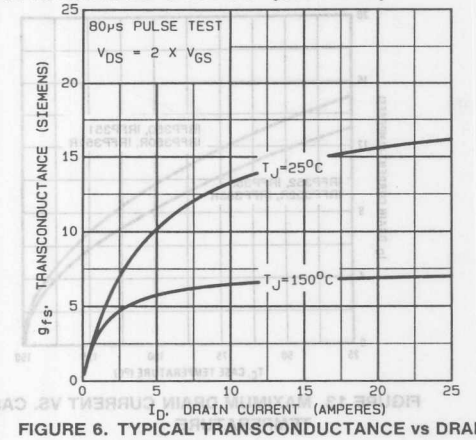


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

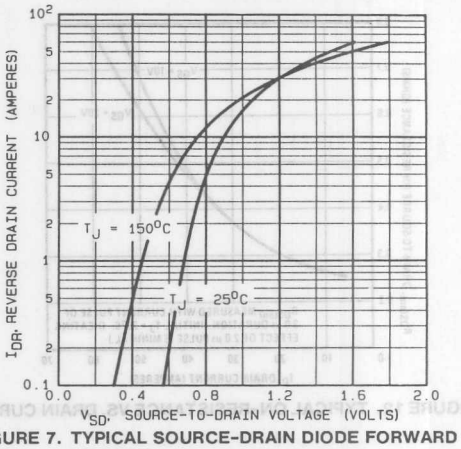


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

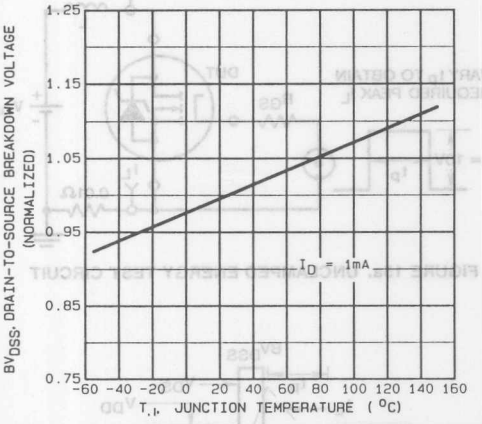


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

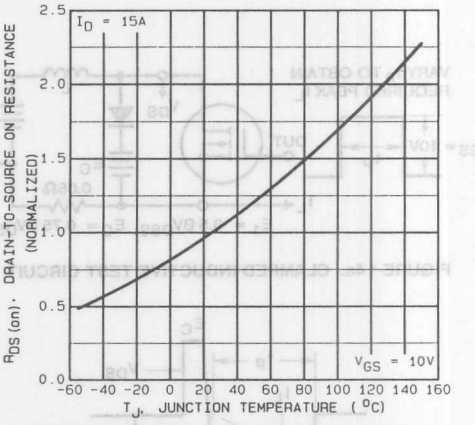


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

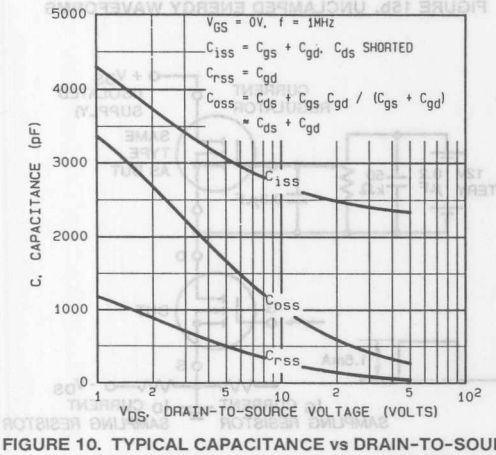


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

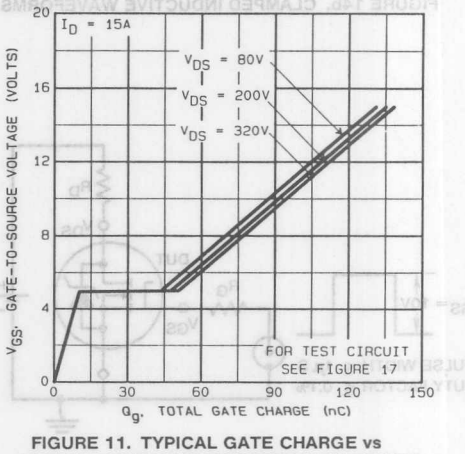


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

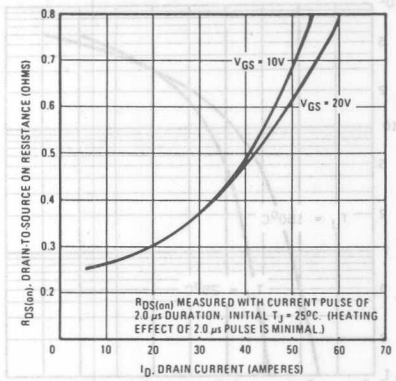


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

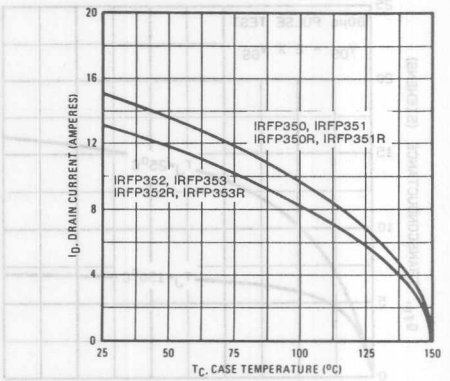


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

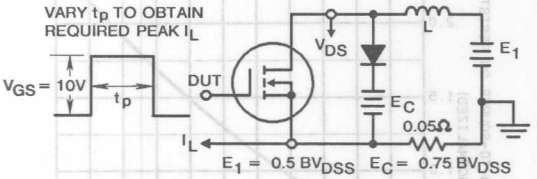


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

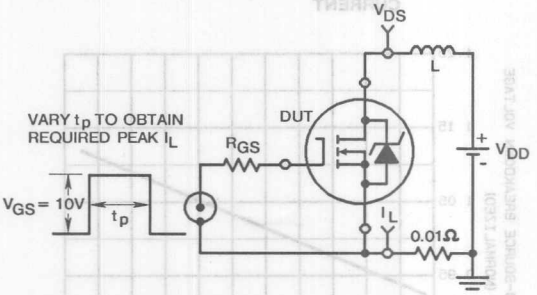


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

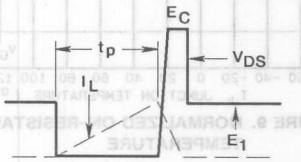


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

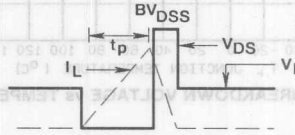


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

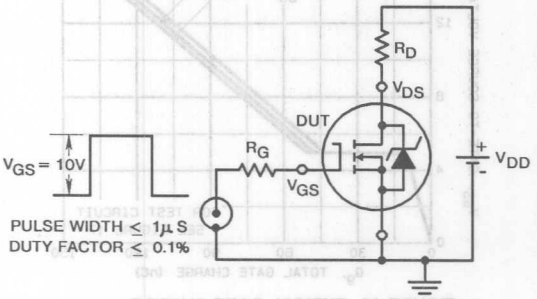


FIGURE 16. SWITCHING TIME TEST CIRCUIT

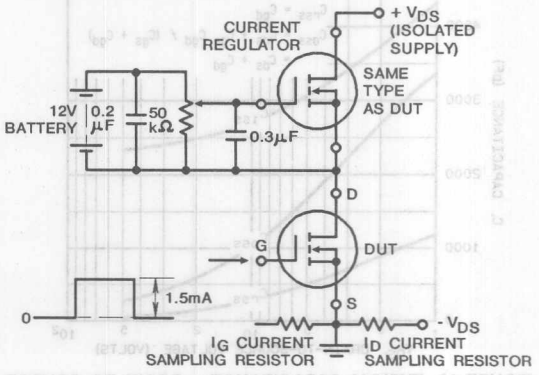


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRFP360
IRFP362

N-Channel Power MOSFETs
Avalanche-Energy Rated

August 1991

Features

- 20A and 23A, 400V
- $r_{DS}(on)$ = 0.20Ω and 0.25Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

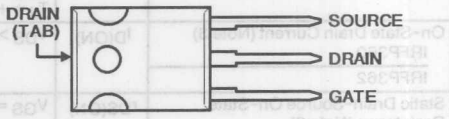
Description

The IRFP360 and IRFP362 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

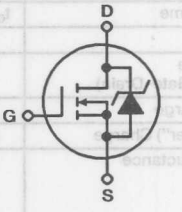
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4

N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFP360	IRFP362	UNITS
Continuous Drain Current				
T_C = +25°C	I_D	23	20	A
T_C = +100°C	I_D	14	13	A
Pulsed Drain Current (1)	I_{DM}	92	80	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	250	250	W
Linear Derating Factor		2.0	2.0	W/°C
Single Pulse Avalanche Energy Rating (2) See Figure 14	E_{AS}	1200	1200	mj
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

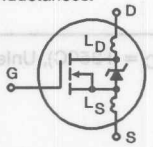
1. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
2. V_{DD} = 50V, starting T_J = +25°C, L = 4.0mH, R_{GS} = 25Ω, Peak I_L = 23A.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

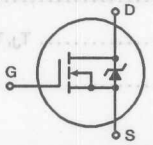
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File Number 2290.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 3) IRFP360	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, V_{GS} = 10V	23	-	-	A
IRFP362			20	-	-	A
Static Drain-Source On-State Resistance (Note 3) IRFP360	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 13A	-	0.18	0.20	Ω
IRFP362			-	0.20	0.25	Ω
Forward Transconductance (Note 3)	g_{fs}	$V_{DS} \geq$ 50V, I_{DS} > 13A	14	21	-	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	4000	-	pF
Output Capacitance	C_{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	97	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 25A, R_G = 4.3Ω R_D = 7.5Ω. (MOSFET switching times are essentially independent of operating temperature)	-	22	33	ns
Rise Time	t_r		-	94	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	120	ns
Fall Time	t_f		-	66	99	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 25A, V_{DS} = 0.8V x Max Rating. See Figure 16 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	68	100	nC
Gate-Source Charge	Q_{gs}		-	17	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	24	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.50	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.10	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	23	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	92	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 23A, V_{GS} = 0V	-	-	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	200	460	1000	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	3.1	7.1	16	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES:
1. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
2. V_{DD} = 50V, Start T_J = +25°C, L = 4.0mH, R_G = 25Ω, I_{PEAK} = 23A (See Figure 14)
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

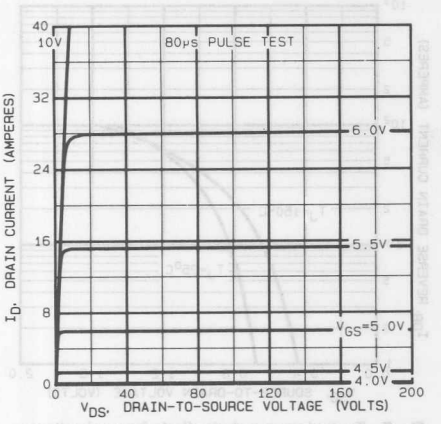


Fig. 1 - Typical output characteristics.

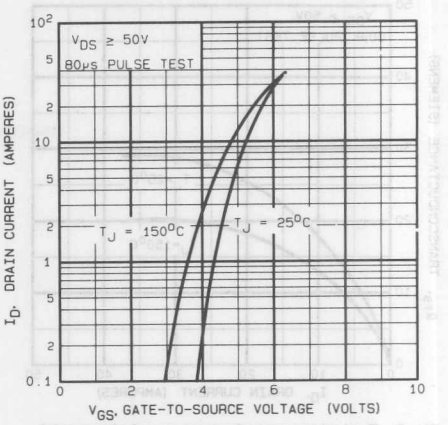


Fig. 2 - Typical transfer characteristics.

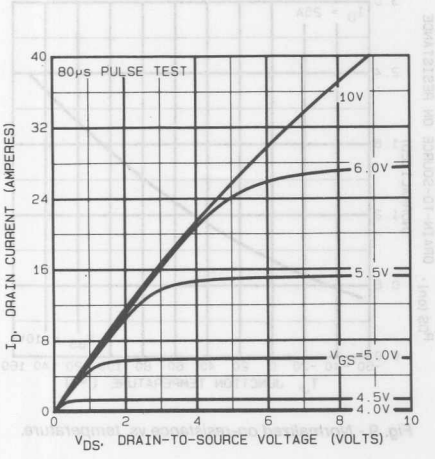


Fig. 3 - Typical saturation characteristics.

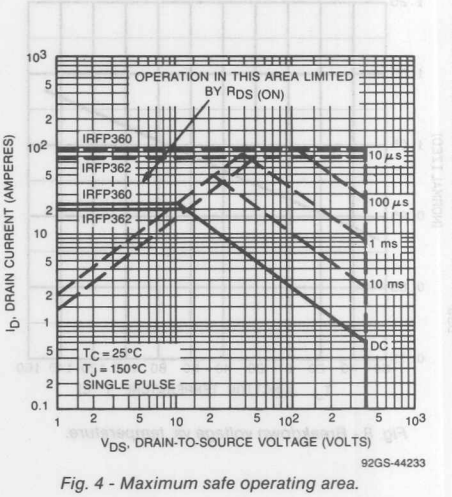


Fig. 4 - Maximum safe operating area.

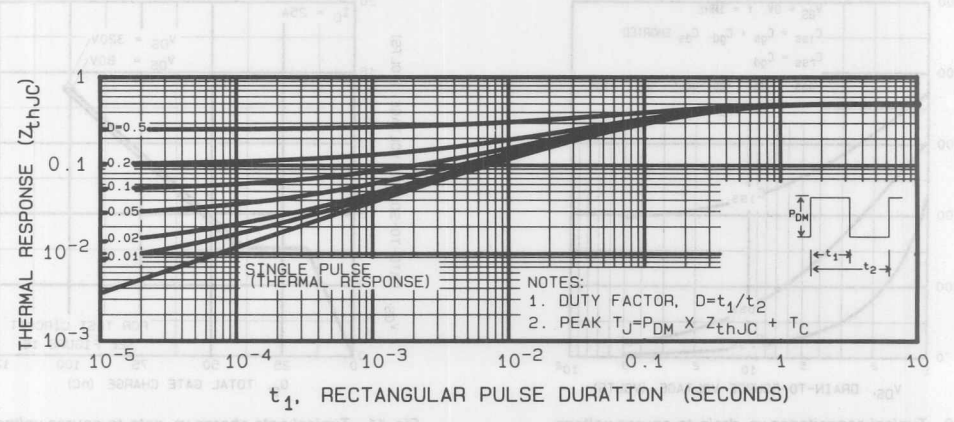


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

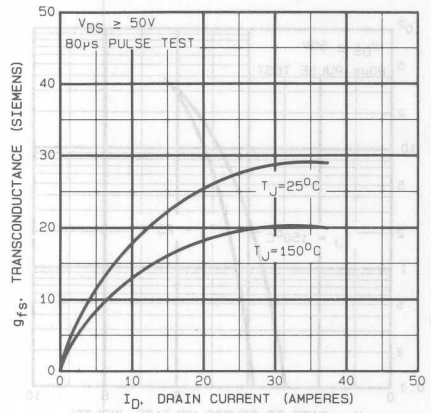


Fig. 6 - Typical transconductance vs. drain current.

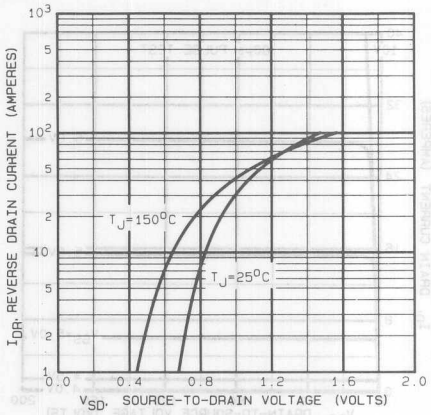


Fig. 7 - Typical source-drain diode forward voltage.

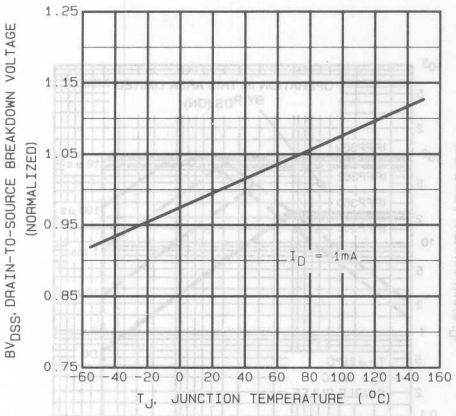


Fig. 8 - Breakdown voltage vs. temperature.

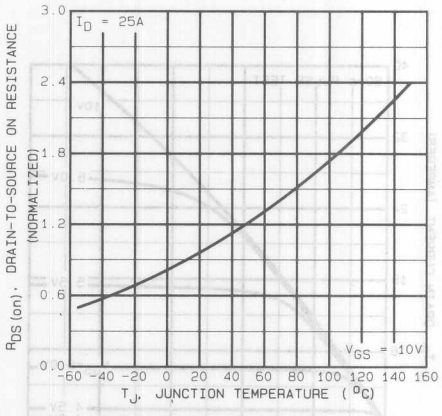


Fig. 9 - Normalized on-resistance vs. temperature.

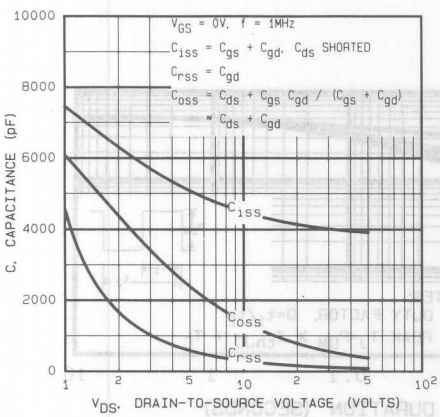


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

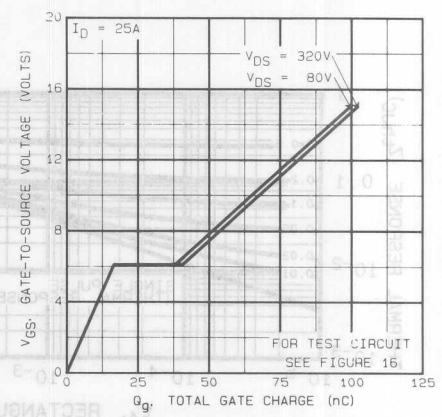


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

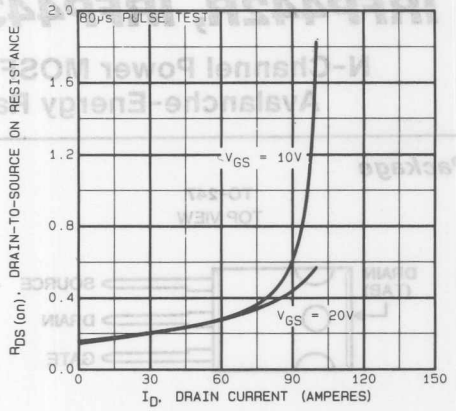


Fig. 12 - Typical on-resistance vs. drain current.

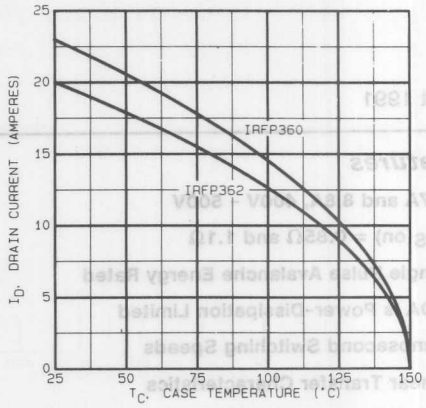


Fig. 13 - Maximum drain current vs. case temperature.

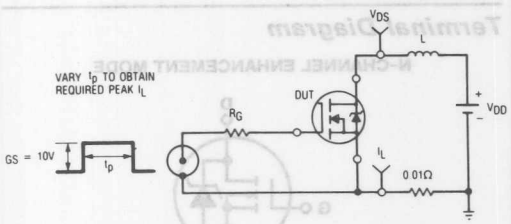


Fig. 14a - Unclamped inductive test circuit.

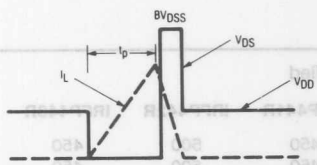


Fig. 14b - Unclamped inductive waveforms.

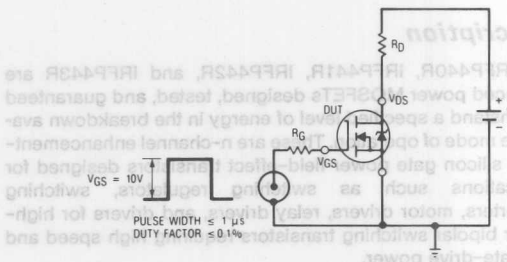


Fig. 15a - Switching time test circuit.

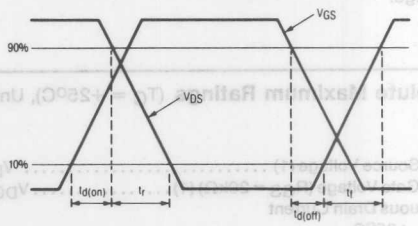


Fig. 15b - Switching time waveforms.

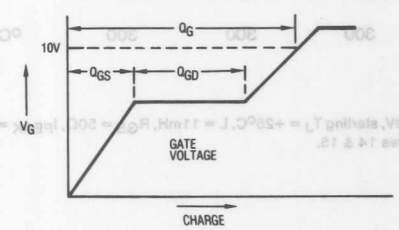


Fig. 16a - Basic gate charge waveform.

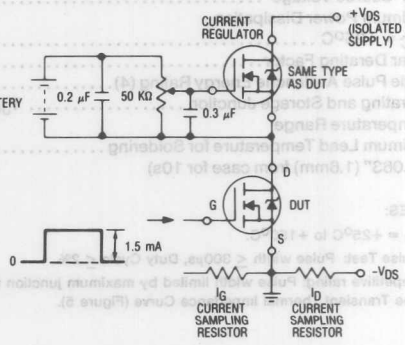


Fig. 16b - Gate charge test circuit.

HARRIS

IRFP440R, IRFP441R IRFP442R, IRFP443R

N-Channel Power MOSFETs Avalanche-Energy Rated

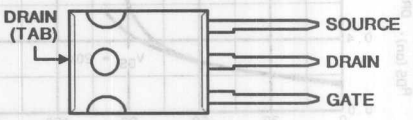
August 1991

Features

- 7.7A and 8.8A, 400V - 500V
- $r_{DS}(on)$ = 0.85Ω and 1.1Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-247
TOP VIEW



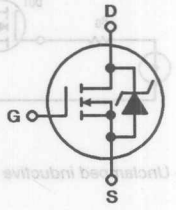
Description

The IRFP440R, IRFP441R, IRFP442R, and IRFP443R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP440R	IRFP441R	IRFP442R	IRFP443R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	8.8	8.8	7.7	7.7	A
T_C = +100°C ..... I_D	5.6	5.6	4.9	4.9	A
Pulsed Drain Current (3) ..... I_{DM}	35	35	31	31	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}	480	480	480	480	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

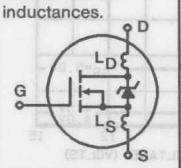
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 11mH, R_{GS} = 50Ω, I_{PEAK} = 8.8A. See Figures 14 & 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

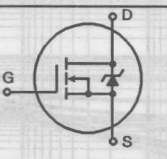
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File Number 2089.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP440R, IRFP442R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	–	–	V
IRFP441R, IRFP443R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFP440R, IRFP441R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	8.8	–	–	A
IRFP442R, IRFP443R			7.7	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP440R, IRFP441R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.9A	–	0.8	0.85	Ω
IRFP442R, IRFP443R			–	1.0	1.1	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 4.9A	5.3	8.2	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1225	–	pF
Output Capacitance	C_{OSS}		–	200	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	85	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 8A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	17	21	ns
Rise Time	t_r		–	23	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	42	74	ns
Fall Time	t_f		–	18	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	42	63	nC
Gate-Source Charge	Q_{gs}		–	7	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	22	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	8.8	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	35	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.8A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 8.0A, dI_F/dt = 100A/µs	210	460	970	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 8.0A, dI_F/dt = 100A/µs	2	4.2	8.9	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 11mH, R_{GS} = 50Ω, I_{PEAK} = 8.8A (See Figures 14 & 15)

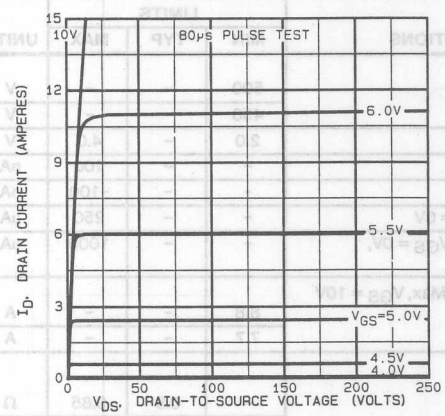


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

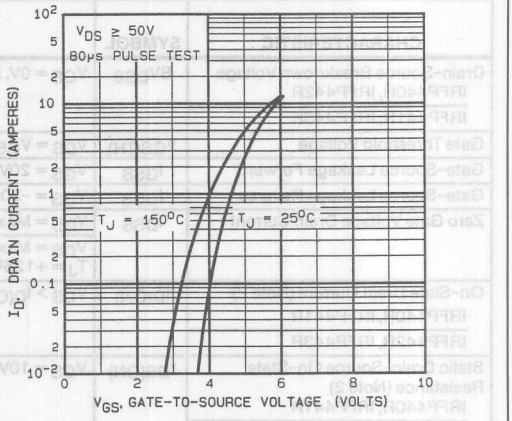


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

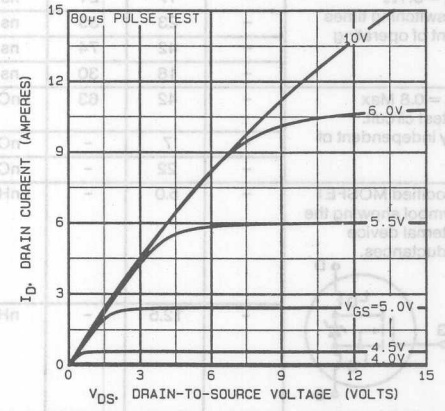


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

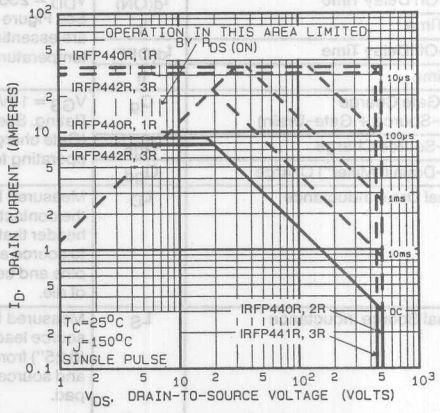


FIGURE 4. MAXIMUM SAFE OPERATING AREA

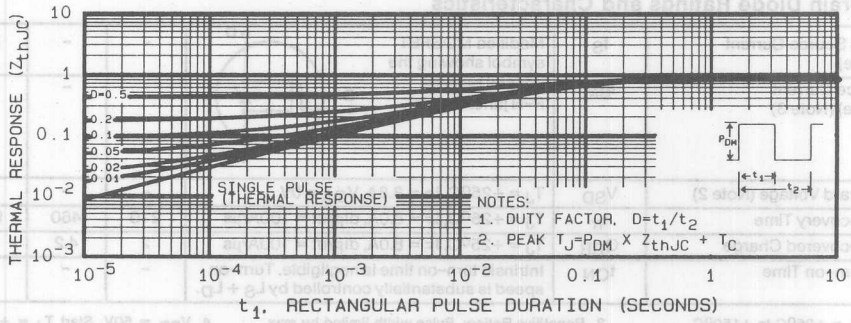


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

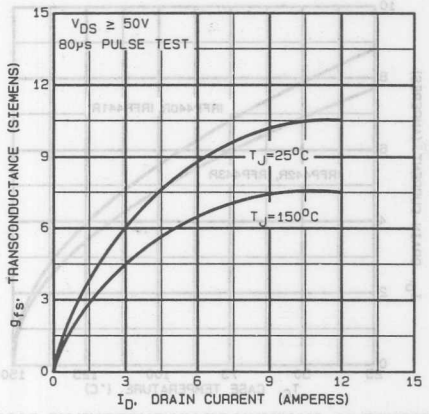


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

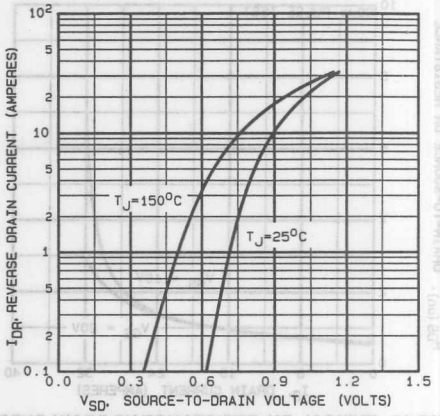


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

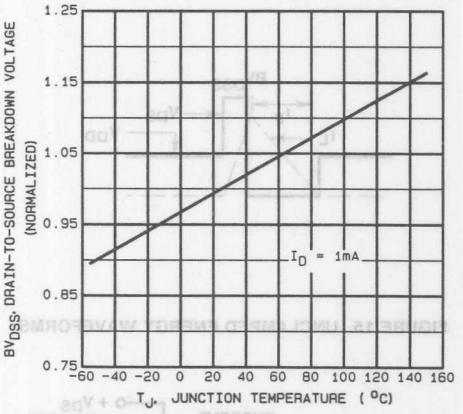


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

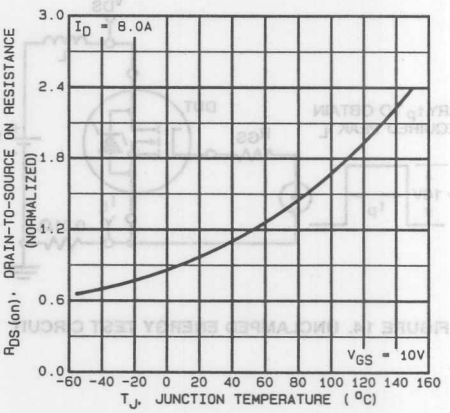


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

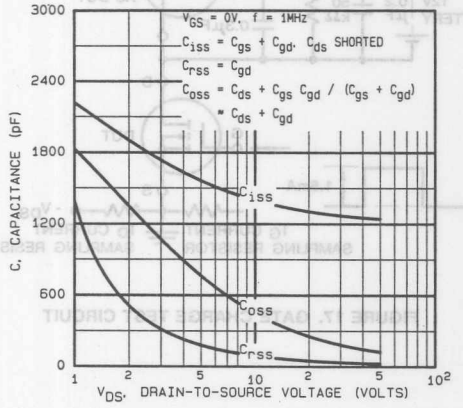


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

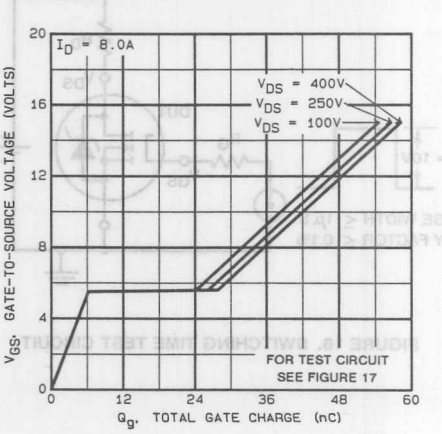


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

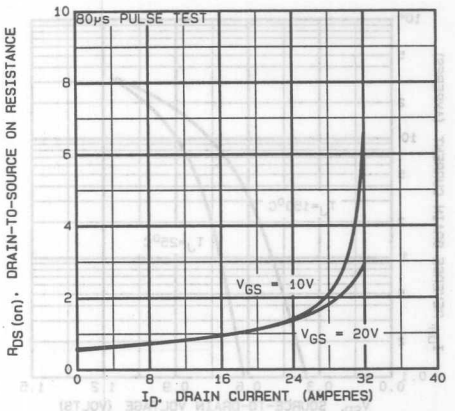


FIGURE 12. TYPICAL ON-RESISTANCE VS DRAIN CURRENT

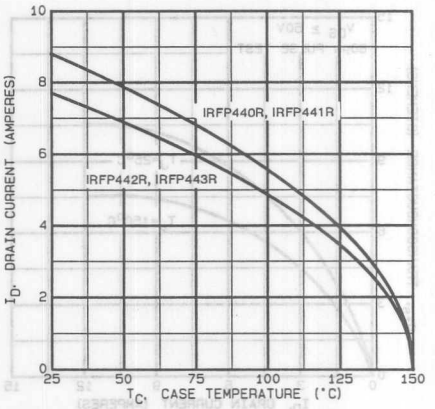


FIGURE 13. MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

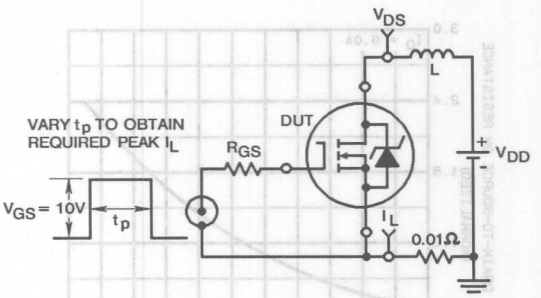


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

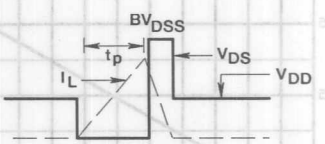


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

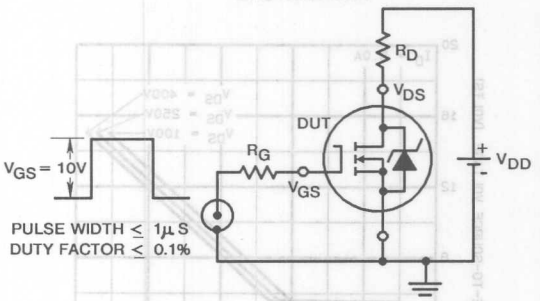


FIGURE 16. SWITCHING TIME TEST CIRCUIT

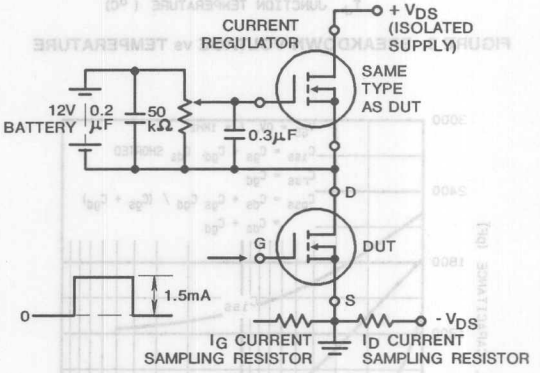


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS IRFP450/451/452/453 IRFP450R/451R/452R/453R

N-Channel Power MOSFETs Avalanche Energy Rated*

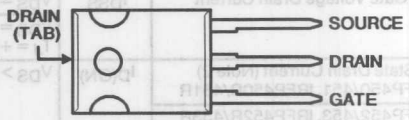
August 1991

Features

- 12A and 14A, 450V - 500V
- $r_{DS}(on)$ = 0.4Ω and 0.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-247
TOP VIEW



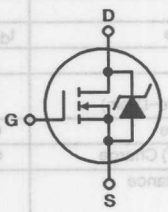
Description

The IRFP450, IRFP451, IRFP452, and IRFP453 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFP450R, IRFP451R, IRFP452R and IRFP453R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP450 IRFP450R	IRFP451 IRFP451R	IRFP452 IRFP452R	IRFP453 IRFP453R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	14	14	12	12	A
T_C = +100°C ..... I_D	8.8	8.8	7.9	7.9	A
Pulsed Drain Current (3) ..... I_{DM}	56	56	48	48	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	180	180	180	180	W
Linear Derating Factor	1.44	1.44	1.44	1.44	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	52	52	48	48	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	860	860	860	860	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

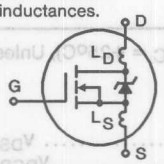
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 7.9mH, R_{GS} = 25Ω, I_{PEAK} = 14A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

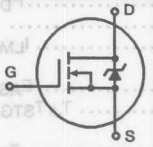
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File Number 2331.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP450/452, IRFP450R/452R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	–	–	V
IRFP451/453, IRFP451R/453R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFP450/451, IRFP450R/451R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, V_{GS} = 10V	14	–	–	A
IRFP452/453, IRFP452R/453R			12	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP450/451, IRFP450R/451R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 7.9A	–	0.3	0.4	Ω
IRFP452/453, IRFP452R/453R			–	0.4	0.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 7.9A	9.3	13.8	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2000	–	pF
Output Capacitance	C_{OSS}		–	400	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	100	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 14A, R_G = 6.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	16	27	ns
Rise Time	t_r		–	45	66	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	68	100	ns
Fall Time	t_f		–	41	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	82	130	nC
Gate-Source Charge	Q_{gs}		–	12	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	42	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.70	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.10	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	14	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	56	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 14A, V_{GS} = 0V	–	–	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 13A, dI_F/dt = 100A/µs	–	1300	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 13A, dI_F/dt = 100A/µs	–	7.4	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 7.9mH, R_{GS} = 25Ω, I_{PEAK} = 14A (See Figure 15)

Performance Curves

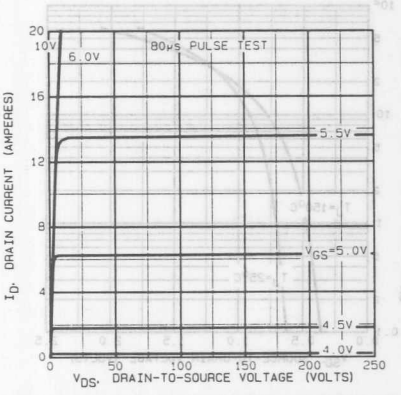


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

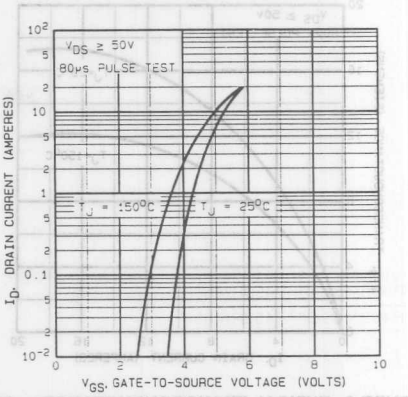


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

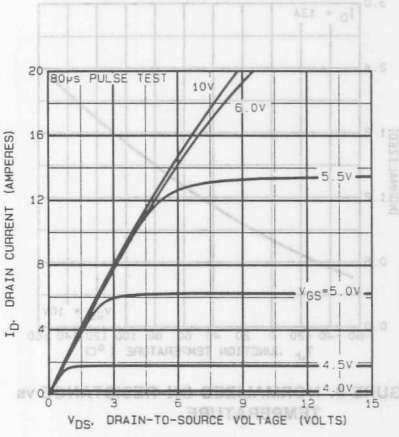


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

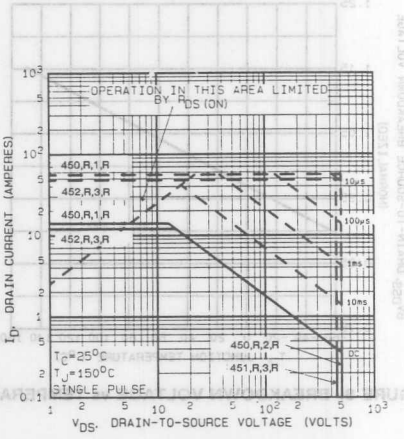


FIGURE 4. MAXIMUM SAFE OPERATING AREA

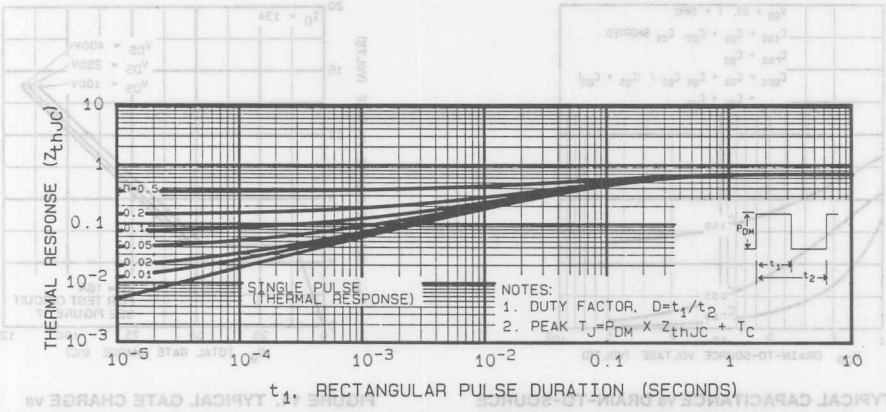


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

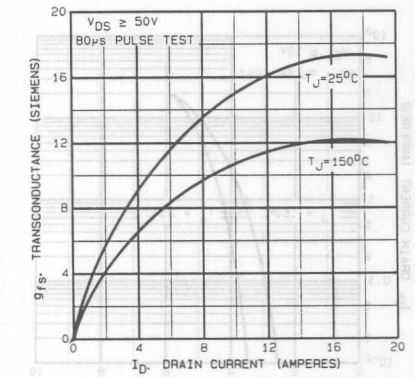


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

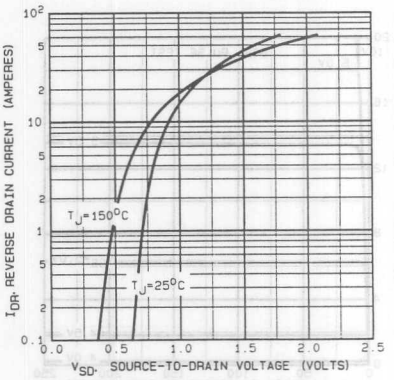


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

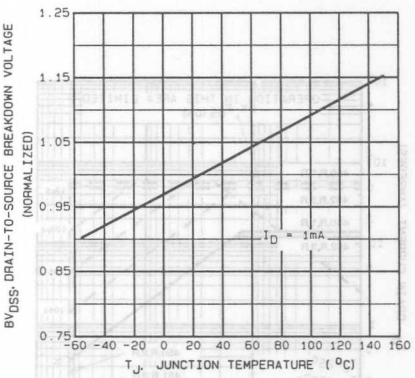


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

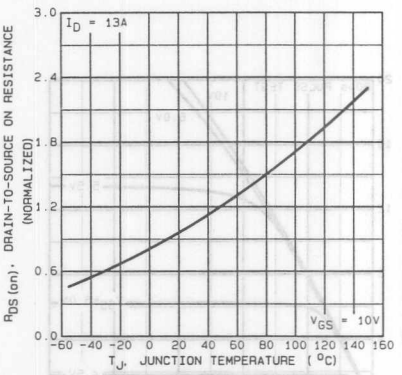


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

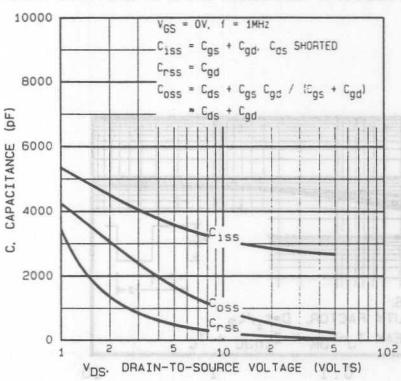


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

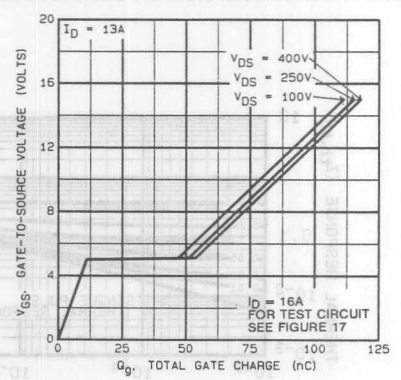


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

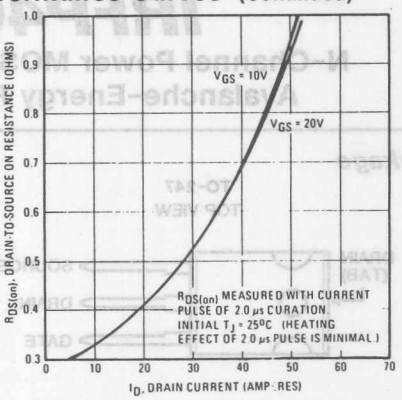


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

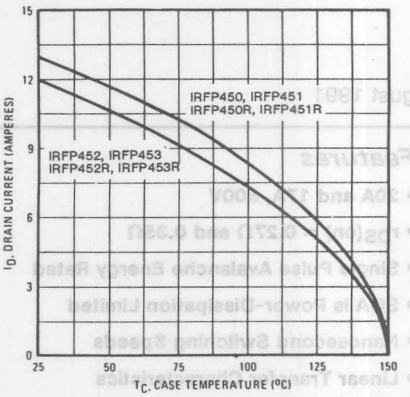


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

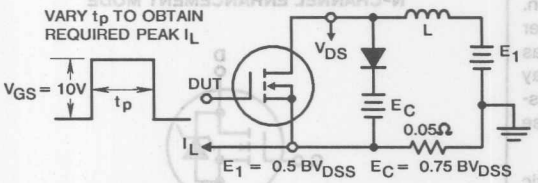


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

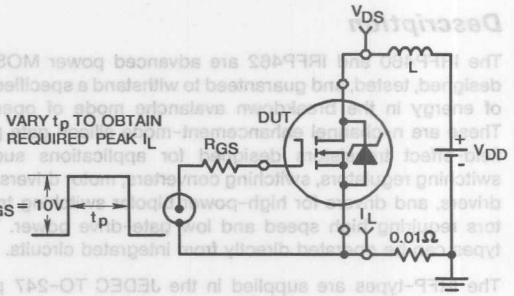


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

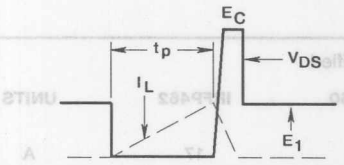


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

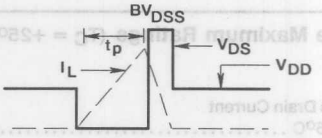


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

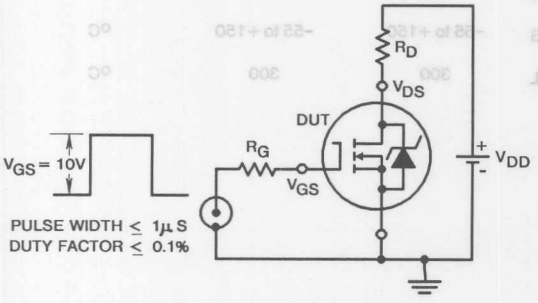


FIGURE 16. SWITCHING TIME TEST CIRCUIT

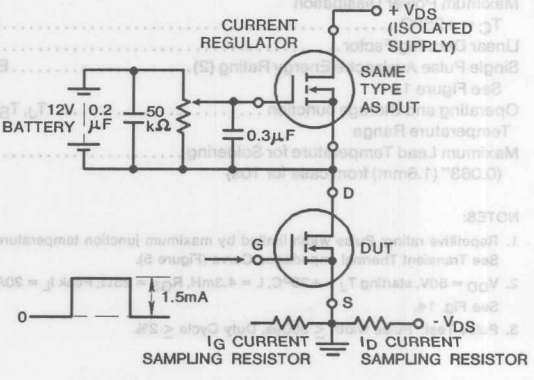


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRFP460
IRFP462

N-Channel Power MOSFETs
Avalanche-Energy Rated

August 1991

Features

- 20A and 17A, 500V
- $r_{DS}(on)$ = 0.27Ω and 0.35Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

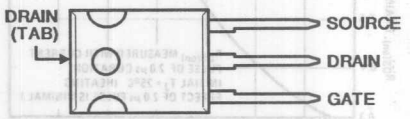
Description

The IRFP460 and IRFP462 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP460	IRFP462	UNITS
Continuous Drain Current			
T_C = +25°C ..... I_D	20	17	A
T_C = +100°C ..... I_D	12	11	A
Pulsed Drain Current (1) ..... I_{DM}	80	68	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = +25°C ..... P_D	250	250	W
Linear Derating Factor	2.0	2.0	W/°C
Single Pulse Avalanche Energy Rating (2) ..... E_{AS} See Figure 14	960	960	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	°C

NOTES:

1. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
2. V_{DD} = 50V, starting T_J = +25°C, L = 4.3mH, R_{GS} = 25Ω, Peak I_L = 20A. See Fig. 14.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2291.1

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_J) = 25° C Unless Otherwise Specified*

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	ALL	500	–	–	V	V_{GS} = 0V, I_D = 250 μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFP460	–	0.24	0.27	Ω	V_{GS} = 10V, I_D = 11A
		IRFP462	–	0.27	0.35		
$I_{D(on)}$	On-State Drain Current ③	IRFP460	20	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ Max., V_{GS} = 10V
		IRFP462	17				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
g_{fs}	Forward Transconductance ③	ALL	13	19	–	S (℧)	V_{DS} = ≥ 50V, I_{DS} = 11A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000		V_{DS} = 0.8 x Max. Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	–	–	−500	nA	V_{GS} = −20V
Q_g	Total Gate Charge	ALL	–	120	190	nC	V_{GS} = 10V, I_D = 21A, V_{DS} = 0.8 x Max. Rating, See Fig. 16 (Independent of operating temperature)
Q_{gs}	Gate-to-Source Charge	ALL	–	18	—	nC	
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	–	62	—	nC	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	23	35	ns	V_{DD} = 250V, I_D ≈ 21A, R_G = 4.3Ω, R_D = 12Ω, See Fig. 15 (Independent of operating temperature)
t_r	Rise Time	ALL	–	81	120	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	85	130	ns	
t_f	Fall Time	ALL	–	65	98	ns	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. Modified MOSFET symbol showing the internal inductances
L_S	Internal Source Inductance	ALL	–	13	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad
C_{iss}	Input Capacitance	ALL	–	4100	–	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	–	480	–	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	–	84	–	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	–	–	0.50	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.10	–	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free air operation
	Mounting Torque	ALL	–	–	10	in. • lbs	Standard 6-32 screw

① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 4.3 mH, R_G = 25Ω, Peak I_L = 20A. See Fig. 14.

③ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	–	–	20	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	–	–	80	A	
V_{SD}	Diode Forward Voltage ③	ALL	–	–	1.8	V	T_J = 25°C, I_S = 21A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	280	580	1200	ns	T_J = 25°C, I_F = 21A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	3.8	8.1	18	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D				

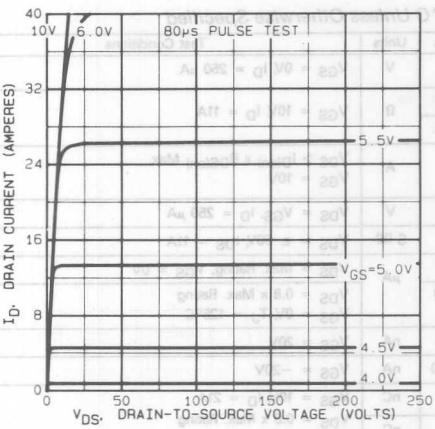


Fig. 1 - Typical output characteristics.

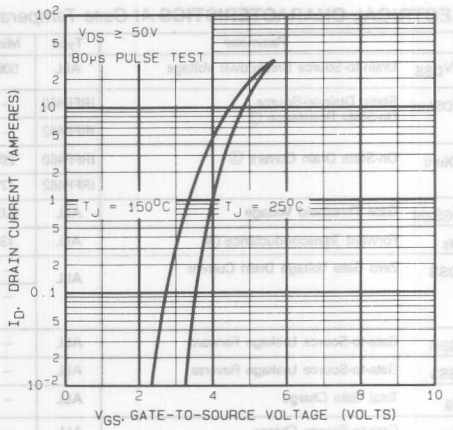


Fig. 2 - Typical transfer characteristics.

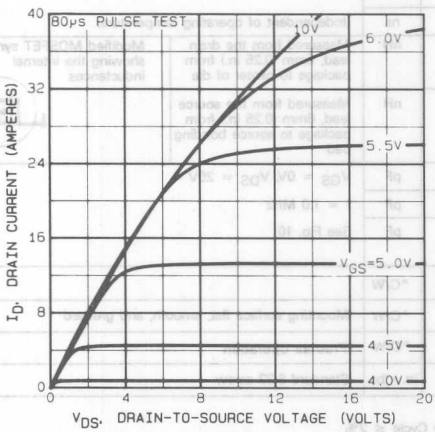


Fig. 3 - Typical saturation characteristics.

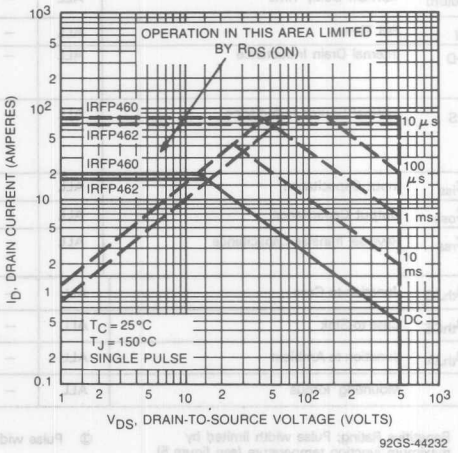


Fig. 4 - Maximum safe operating area.

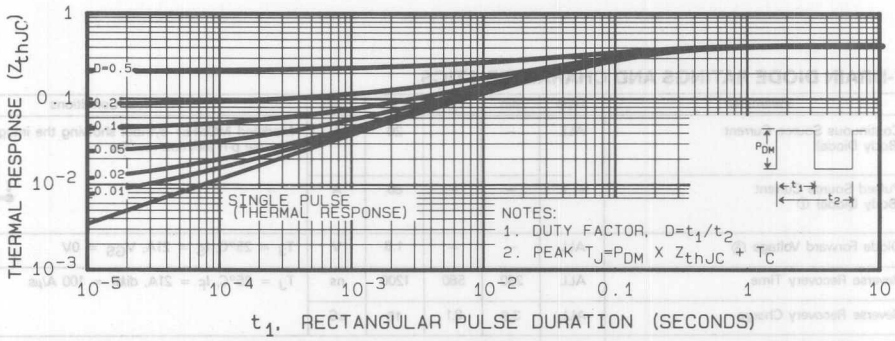


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

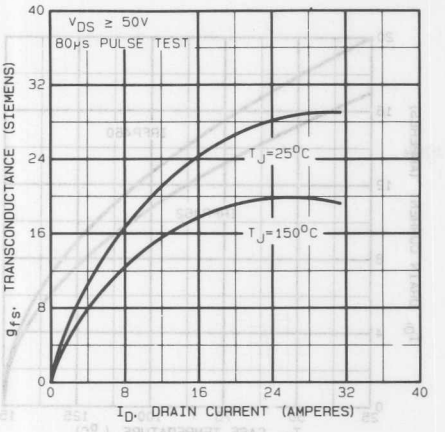


Fig. 6 - Typical transconductance vs. drain current.

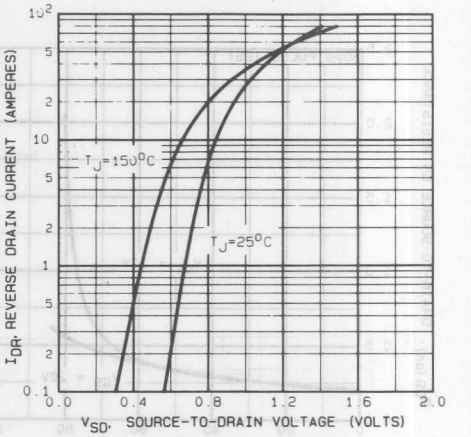


Fig. 7 - Typical source-drain diode forward voltage.

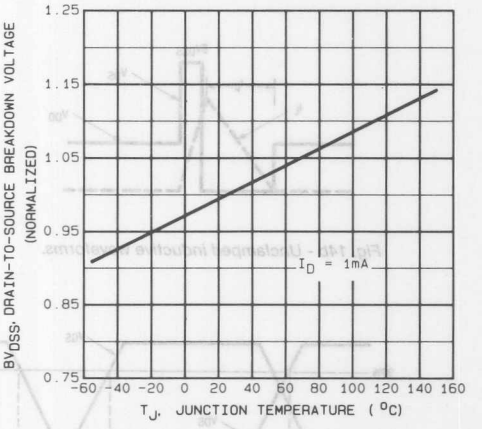


Fig. 8 - Breakdown voltage vs. temperature.

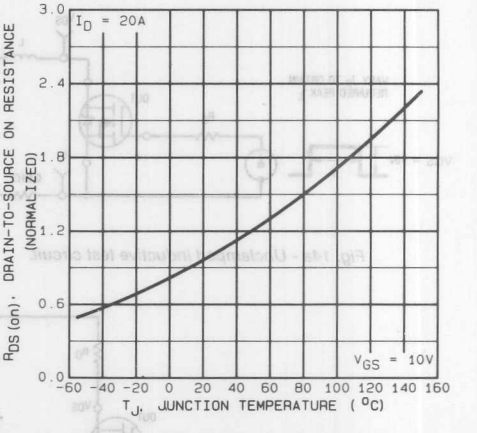


Fig. 9 - Normalized on-resistance vs. temperature.

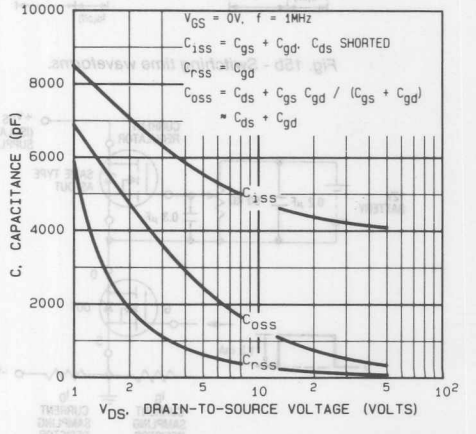


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

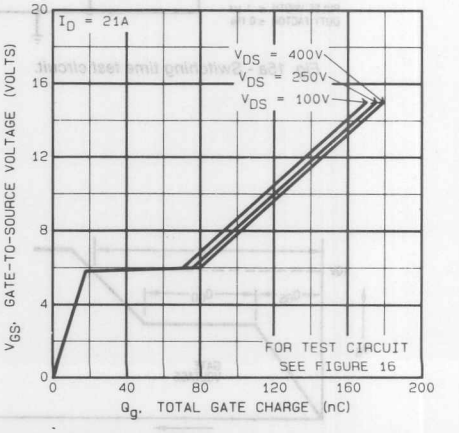


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

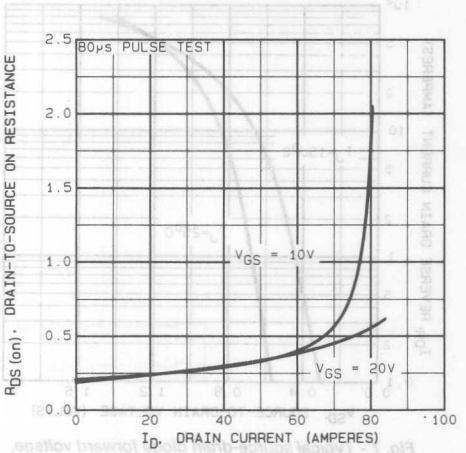


Fig. 12 - Typical on-resistance vs. drain current.

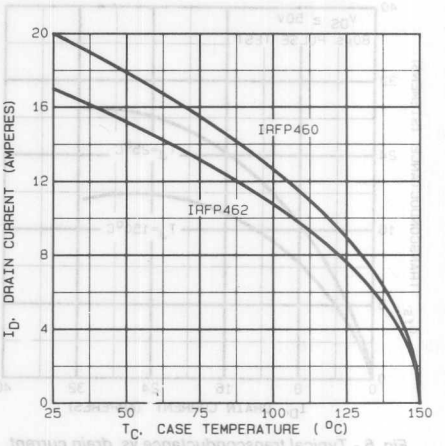


Fig. 13 - Maximum drain current vs. case temperature.

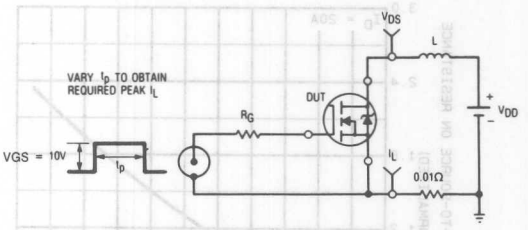


Fig. 14a - Unclamped inductive test circuit.

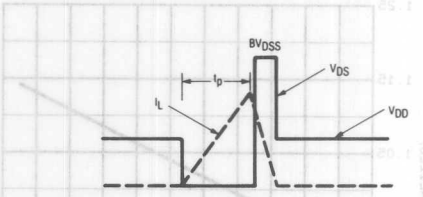


Fig. 14b - Unclamped inductive waveforms.

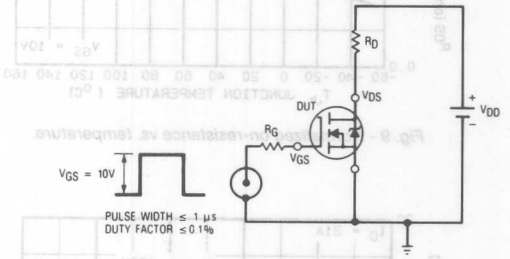


Fig. 15a - Switching time test circuit.

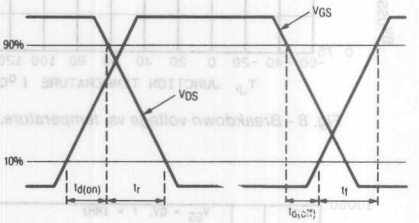


Fig. 15b - Switching time waveforms.

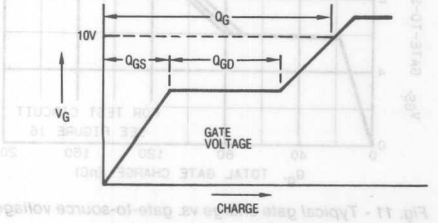


Fig. 16a - Basic gate charge waveform.

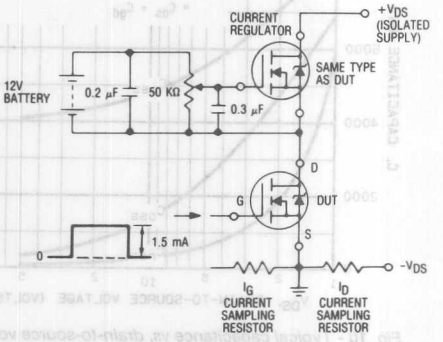


Fig. 16b - Gate charge test circuit.

HARRIS

IRFPC40R
IRFPC42R

N-Channel Power MOSFETs
Avalanche-Energy-Rated

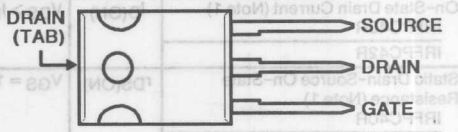
May 1992

Features

- 6.8A, 5.9A and 600V
- $r_{DS(ON)}$ = 1.2Ω and 1.6Ω
- Isolated Central Mounting Hole
- Repetitive Avalanche Ratings
- Simple Drive Requirements
- Ease of Paralleling

Package

TO-247
TOP VIEW



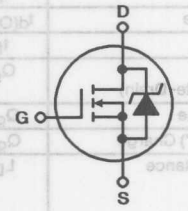
Description

The IRFPC40R and IRFPC42R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFPC types are supplied in the JEDEC TO-247 plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4

N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFPC40R	IRFPC42R	UNITS
Continuous Drain Current				
T_C = +25°C	I_D	6.8	5.9	A
T_C = +100°C	I_D	4.3	3.7	A
Pulsed Drain Current (2)	I_{DM}	27	24	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (3) (See Figure 14)	E_{as}	410	410	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

NOTES:

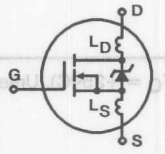
1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 50V, Start T_J = +25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

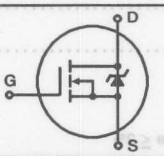
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File Number 2158.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	600	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 1) IRFPC40R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	6.8	–	–	A
IRFPC42R			5.9	–	–	A
Static Drain-Source On-State Resistance (Note 1) IRFPC40R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.7A	–	0.97	1.2	Ω
IRFPC42R			–	1.2	1.6	Ω
Forward Transconductance (Note 1)	g_{fs}	I_{DS} = 3.7A, $V_{DS} \geq$ 100V	4.9	7.3	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1300	–	pF
Output Capacitance	C_{OSS}		–	160	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	45	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 6.2A, R_G = 9.1Ω R_D = 47Ω. (Independent of operating temperature) See Figure 15.	–	13	20	ns
Rise Time	t_r		–	18	27	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	55	83	ns
Fall Time	t_f		–	20	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 6.2A, V_{DS} = 0.6V x Max Rating. See Figure 16 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	40	60	nC
Gate-Source Charge	Q_{gs}		–	5.5	8.3	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	20	30	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from package to source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.10	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	6.8	A
Pulse Source Current (Body Diode) (Note 1)	I_{SM}		–	–	27	A
Diode Forward Voltage (Note 3)	V_{SD}	T_J = +25°C, I_S = 6.2A, V_{GS} = 0V	–	–	1.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 6.2A, dI_F/dt = 100A/µs	200	450	940	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 6.2A, dI_F/dt = 100A/µs	1.8	3.8	7.9	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES:

1. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 50V, Start T_J = +25°C, L = 16mH, R_{GS} = 25Ω, I_{PEAK} = 6.8A

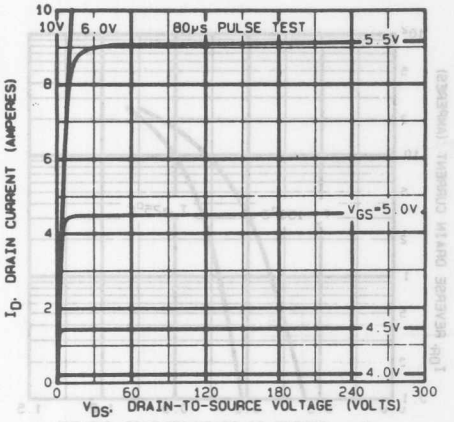


Fig. 1 - Typical Output Characteristics

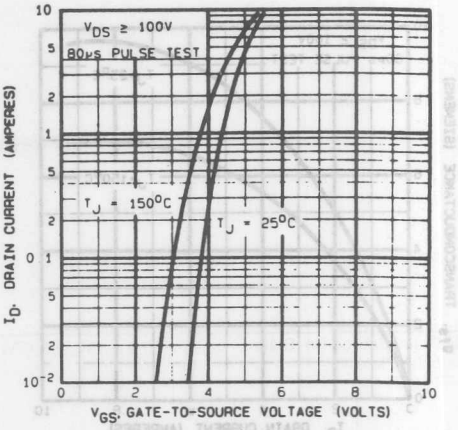


Fig. 2 - Typical Transfer Characteristics

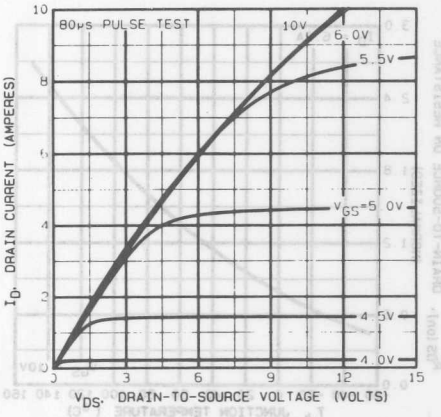


Fig. 3 - Typical Saturation Characteristics

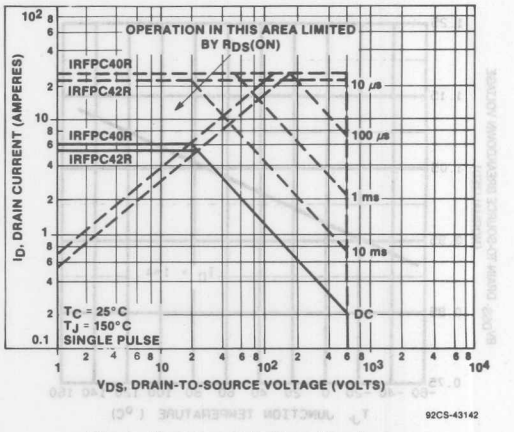


Fig. 4 - Maximum Safe Operating Area

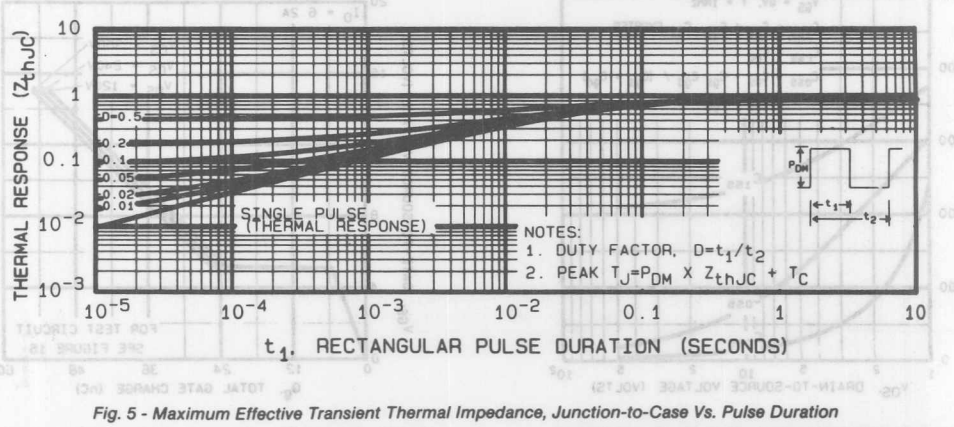


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

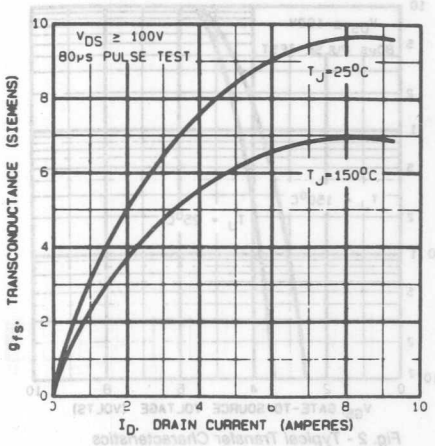


Fig. 6 - Typical Transconductance Vs. Drain Current

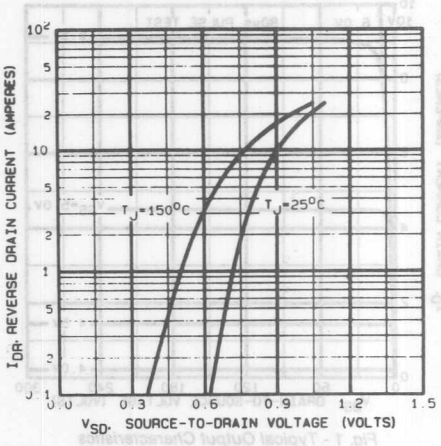


Fig. 7 - Typical Source-Drain Diode Forward Voltage

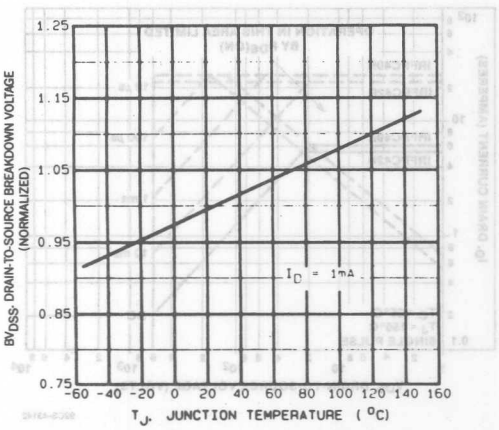


Fig. 8 - Breakdown Voltage Vs. Temperature

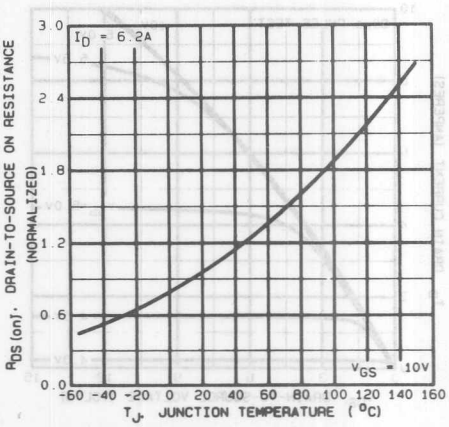


Fig. 9 - Normalized On-Resistance Vs. Temperature

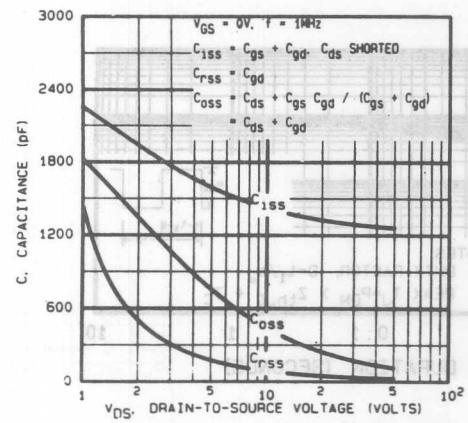


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

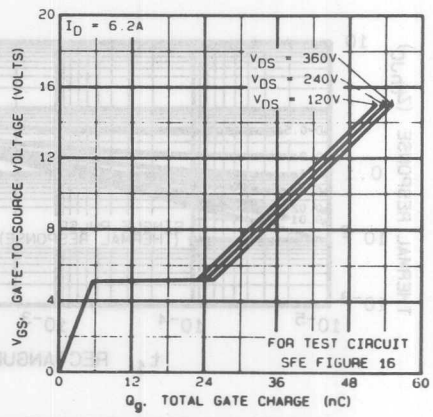


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

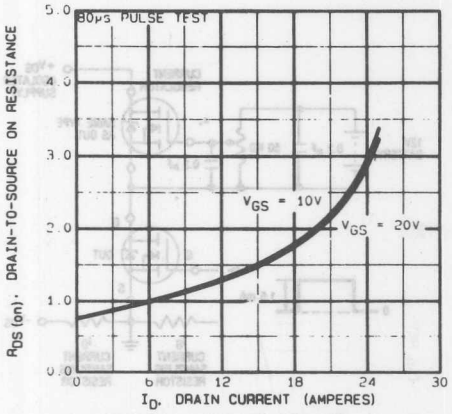


Fig. 12 - Typical On-Resistance Vs. Drain Current

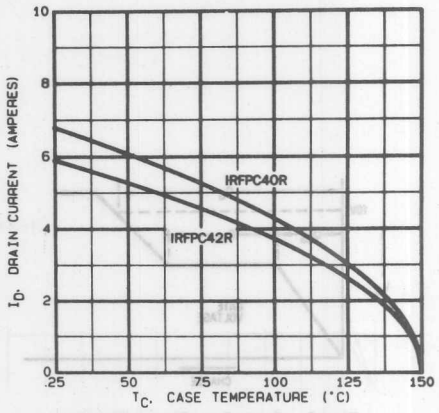


Fig. 13 - Maximum Drain Current Vs. Case Temperature

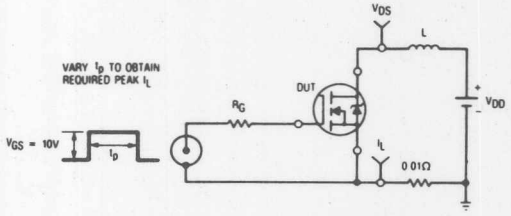


Fig. 14a - Unclamped Inductive Test Circuit

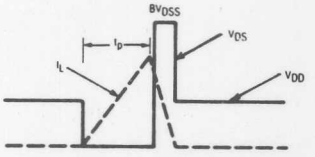


Fig. 14b - Unclamped Inductive Waveforms

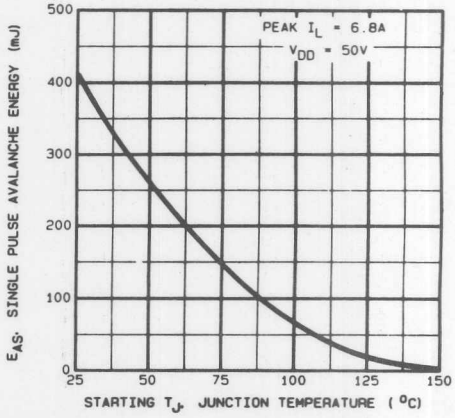


Fig. 14c - Maximum Avalanche Energy Vs. Starting Junction Temperature

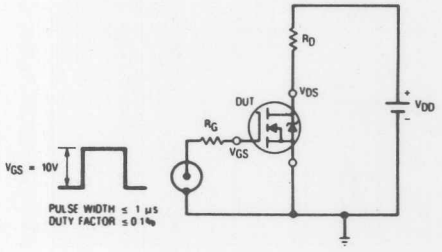


Fig. 15a - Switching Time Test Circuit

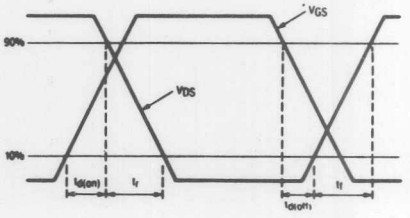


Fig. 15b - Switching Time Waveforms

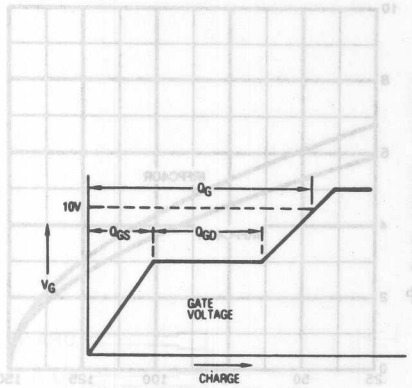
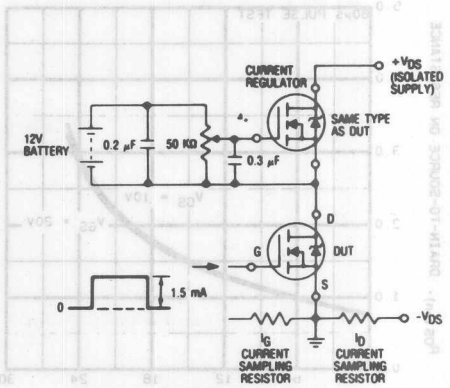


Fig. 16a - Basic Gate Charge Waveform



Fib. 16b - Gate Charge Test Circuit

HARRIS

IRFPG40
IRFPG42

High Voltage N-Channel Enhancement Mode Power Field Effect Transistor

August 1991

Features

- IRFPG40: 4.3A, 1000V, $r_{DS(ON)} = 3.5\Omega$
- IRFPG42: 3.9A, 1000V, $r_{DS(ON)} = 4.2\Omega$
- UIS SOA Rating Curve (Single Pulse)
- -55°C to 150°C Operating and Storage Temperature

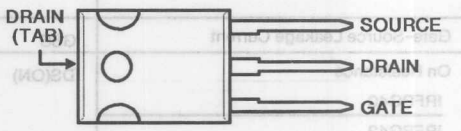
Description

The IRFPG40 and IRFPG42 are n-channel enhancement mode silicon-gate power field effect transistors. They are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFPG40 and IRFPG42 are supplied in the JEDEC TO-247 plastic package.

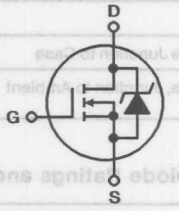
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25°C$) Unless Otherwise Specified

		IRFPG40	IRFPG42	UNITS
Drain-Souce	V_{DSS}	1000	1000	V
Drain-Gate	V_{DGR}	1000	1000	V
Continuous Drain Current	I_D	4.3	3.9	A
Pulsed Drain Current	I_{DM}	17	16	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
$T_C = 25°C$	P_D	150	150	W
Derate Above $T_C = 25°C$		0.83	0.83	W/°C
Single Pulse Avalanche Energy Rating (See Figure 13)	E_{as}	490	490	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2879

Electrical Characteristics (T_C = 25°C), Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V	1000	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA	2.0	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0V	–		μA
		V_{DS} = 1000V T_C = 25°C	–	250	μA
		V_{DS} = 800V T_C = 150°C	–	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V	–	±500	nA
On Resistance	$r_{DS(ON)}$	I_D = 2.5A, V_{GS} = 10V			
IRFPG40			–	3.5	Ω
IRFPG42			–	4.2	Ω
Forward Transconductance	g_{fs}	I_D = 2.5A, V_{DS} = 100V	3.5	–	s
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 500V, I = 3.9A	–	30	ns
Rise Time	t_r	R_G = 9.1Ω	–	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$	R_D = 120Ω	–	170	ns
Fall Time	t_f	See Figure 14	–	50	ns
Total Gate Charge	Q_g	I_D = 3.9A, V_{DS} = 800V, V_{GS} = 10V	–	120	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		–	0.83	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$		–	40	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Forward Voltage	V_{SD}	I_{SD} = 4.3A	–	1.8	V
Reverse Recovery Time	t_{rr}	I_F = 3.9A, d_{IF}/dT = 100 A/μs	–	1000	ns

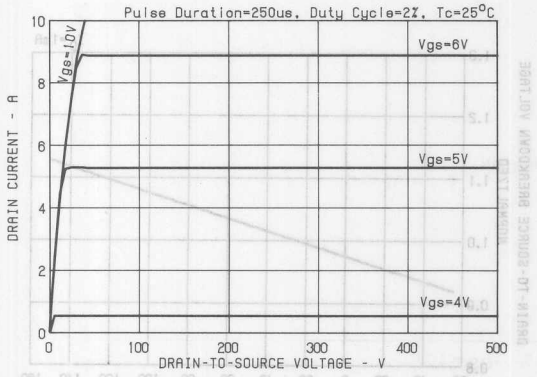


Figure 1 – Typical output characteristics.

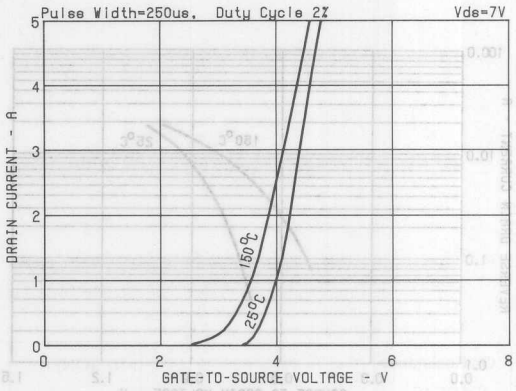


Figure 2 – Typical transfer characteristics.

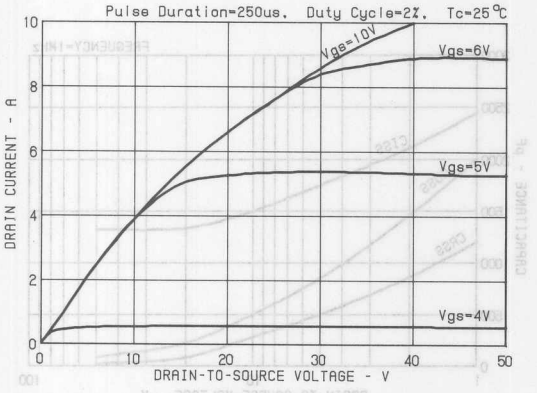


Figure 3 – Typical saturation characteristics.

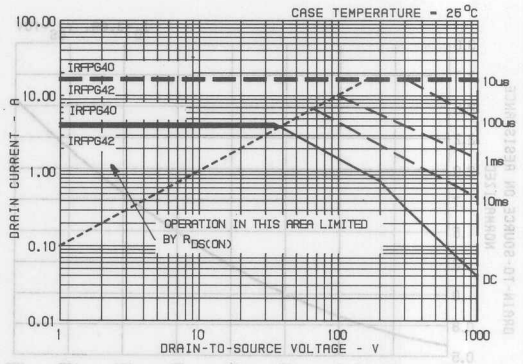


Figure 4 – Maximum safe operating area.

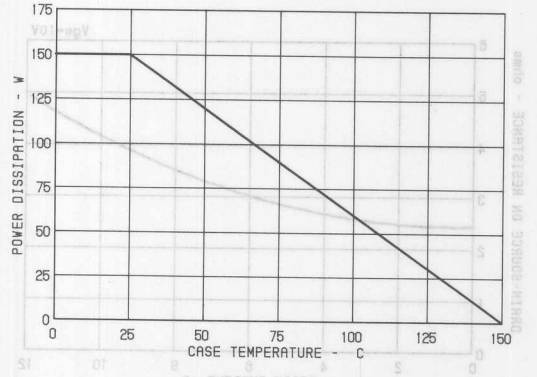


Figure 5 – Power vs. temperature derating curve.

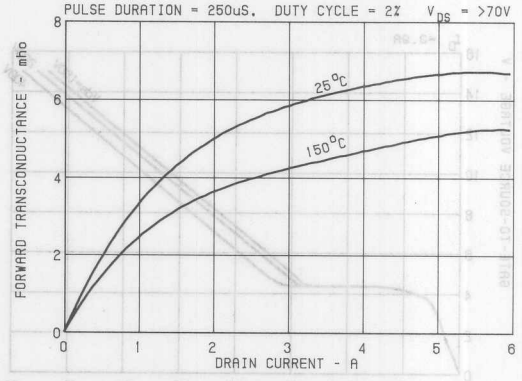


Figure 6 – Typical forward transconductance.

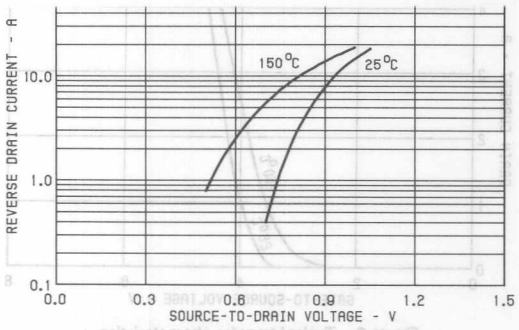


Figure 7 – Typical source-to-drain diode forward voltage.

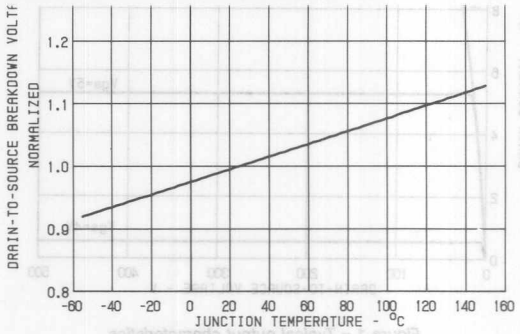


Figure 8 – Breakdown voltage vs. temperature.

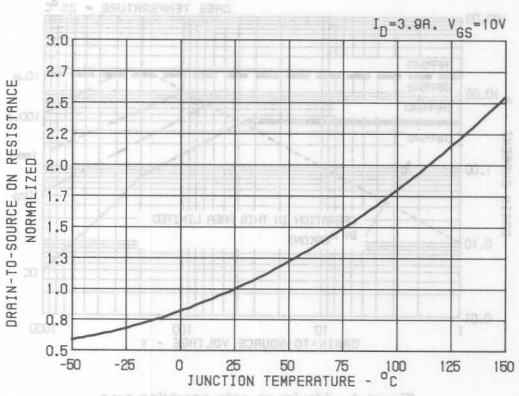


Figure 9 – Normalized drain-to-source on resistance.

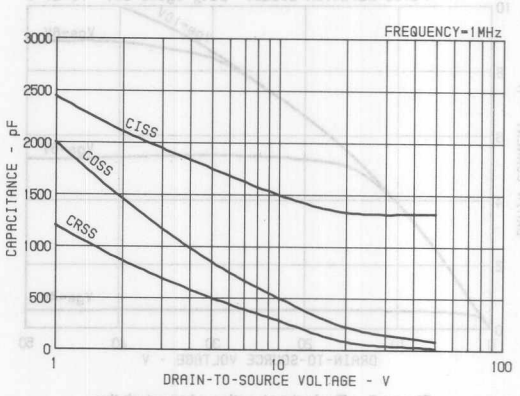


Figure 10 – Typical capacitance vs. voltage.

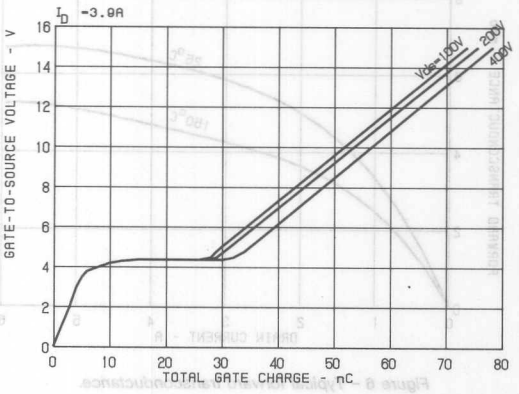


Figure 11 – Typical gate charge.

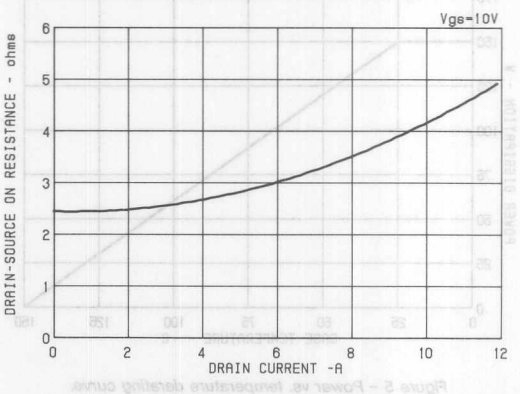


Figure 12 – Typical drain-source on resistance.

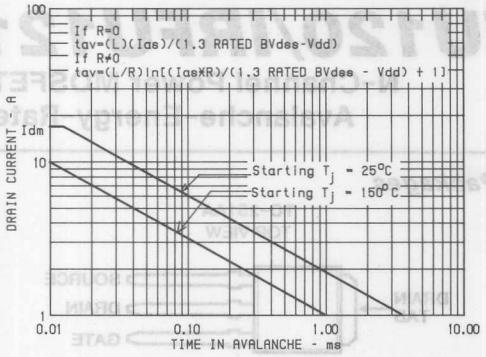


Figure 13 – Unclamped inductive switching SOA.

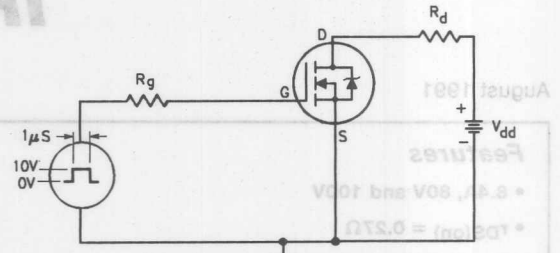


Figure 14 – Switching time test circuit.

HARRIS

IRFR120/IRFR121
IRFU120/IRFU121

N-Channel Power MOSFETs
Avalanche-Energy-Rated

August 1991

Features

- 8.4A, 80V and 100V
- $r_{DS(on)} = 0.27\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

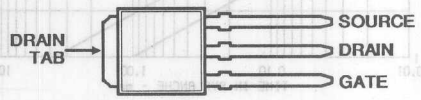
The IRFR120, IRFR121, IRFU120, IRFU121 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFU series is supplied in the TO-251AA plastic package and the IRFR series is supplied in the TO-252AA surface-mount plastic package.

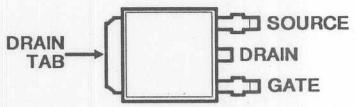
Because of space limitations branding (marking) on type IRFR120 is IRF120, IRFR121 is IFR121, IRFU120 is IFU120 and IRFU121 is IFU121.

Packages

TO-251AA
TOP VIEW

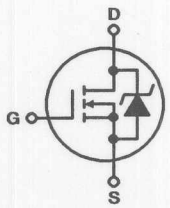


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

Gate-Source Voltage, V_{GS}	±20V
Continuous Drain Current, I_D	
$T_C = 25^oC$	8.4A
$T_C = 100^oC$	5.9A
Pulsed Drain Current (1), I_{DM}	34A
Single-Pulse Avalanche Energy Rating (2), E_{AS} (See Figure 14)	36mJ
Maximum Power Dissipation, P_D	50W
Linear Derating Factor	0.4W/^{o}C
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55 to +175°C
Maximum Lead Temperature for Soldering, T_L (0.063" (1.6mm) from case for 10s)	300°C

NOTES:

1. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
2. V_{DD} = 25V, Start T_J = +25°C, L = 770µH, R_G = 25Ω, Peak I_L = 8.4A (See Figures 14 and 15)
3. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
4. Mounting pad must cover heatsink surface area. See Packages.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

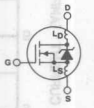
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File Number 2414

ELECTRICAL CHARACTERISTICS, At T_J = 25°C (Unless Otherwise Specified)

	CHARACTERISTIC	TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFR120 IRFU120	100	—	—	V	V_{GS} = 0 V, I_D = 250 μA
		IRFR121 IRFU121	80				
$R_{DS}(on)$	Static Drain-to-Source On-State Resistance ③	ALL	—	0.25	0.27	Ω	V_{GS} = 10 V, I_D = 5.9 A
$I_D(on)$	On-State Drain Current ③	ALL	8.4	—	—	A	$V_{DS} > I_D(on) \times R_{DS}(on)$ Max. V_{GS} = 10 V
$V_{GS}(th)$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250 μA
g_{fs}	Forward Transconductance ③	ALL	2.8	4.2	—	S(℧)	$V_{DS} \geq 50$ V, I_{DS} = 5.9 A
I_{DSS}	Zero-Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0 V, T_J = 150°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20 V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500		V_{GS} = -20 V
Q_g	Total Gate Charge	ALL	—	9.7	15	nC	V_{GS} = 10 V, I_D = 8.4 A
Q_{gs}	Gate-to-Source Charge	ALL	—	2.2	3.3		V_{DS} = 0.8 x Max. Rating
Q_{gd}	Gate-to-Drain ("Miller") Charge		—	2.3	3.4		See Fig. 16. (Independent of operating temperature)
$t_d(on)$	Turn-On Delay Time	ALL	—	8.8	13	ns	V_{DD} = 50 V, $I_D \approx$ 8.4 A, R_G = 18 Ω
t_r	Rise Time	ALL	—	30	45		R_D = 5.1 Ω
$t_d(off)$	Turn-Off Delay Time	ALL	—	19	29		See Fig. 15
t_f	Fall Time	ALL	—	20	30		(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	350	—	pF	V_{GS} = 0 V, V_{DS} = 25 V
C_{oss}	Output Capacitance	ALL	—	130	—		f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	24	—		See Fig. 10

Modified MOSFET symbol showing the internal inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC	TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_S	Continuous Source Current (Body Diode)	ALL	—	—	8.4	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier.
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	—	—	34		
V_{SD}	Diode Forward Voltage ③	ALL	—	—	2.5	V	T_J = 25°C, I_S = 8.4 A, V_{GS} = 0 V
t_{rr}	Reverse Recovery Time	ALL	55	110	240	ns	T_J = 25°C, I_F = 8.4 A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	0.25	0.53	1.1	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



THERMAL RESISTANCE

$R_{\theta JC}$	Junction-to-Case	ALL	—	—	3.0	°C/W	
$R_{\theta CS}$	Case-to-Sink	ALL	—	1.7	—		Typical solder mount ④
$R_{\theta JA}$	Junction-to-Ambient	ALL	—	—	110		Typical socket mount

① Repetitive Rating; Pulse width limited by maximum junction temperature (see Fig. 5).

② At V_{DD} = 25 V, Starting T_J = 25°C, L = 770 μH, R_G = 25 Ω, Peak I_L = 8.4 A.

③ Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

④ Mounting pad must cover heatsink surface area. See Case Style drawing on front page.

The information shown on the following graphs applies also to the IRFU devices.

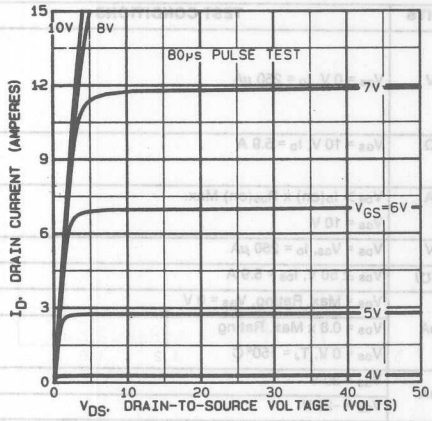


Fig. 1 - Typical output characteristics.

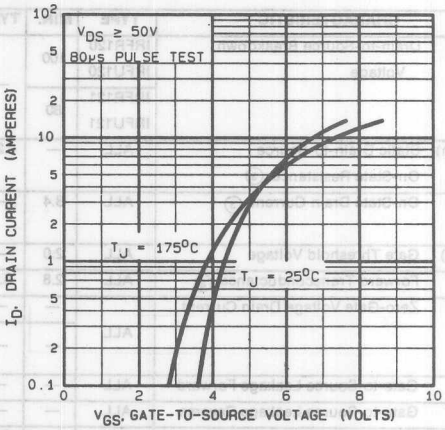


Fig. 2 - Typical transfer characteristics.

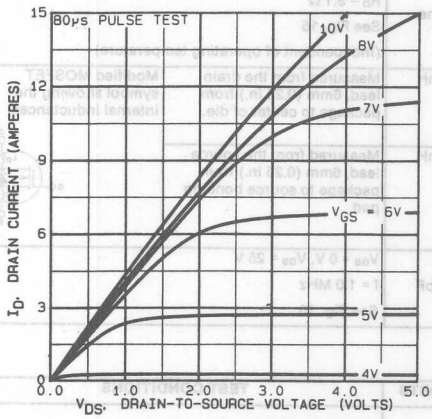


Fig. 3 - Typical saturation characteristics.

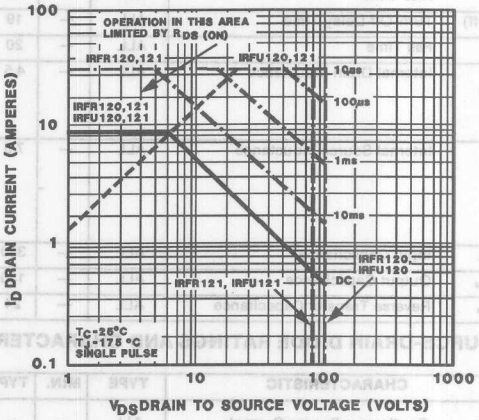


Fig. 4 - Maximum safe operating area.

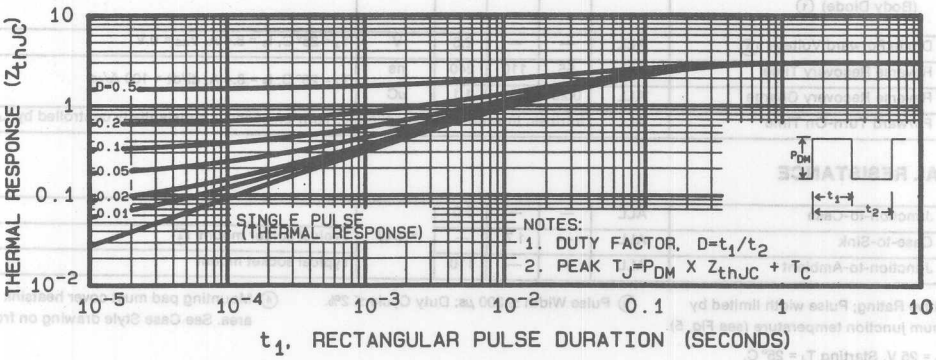


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

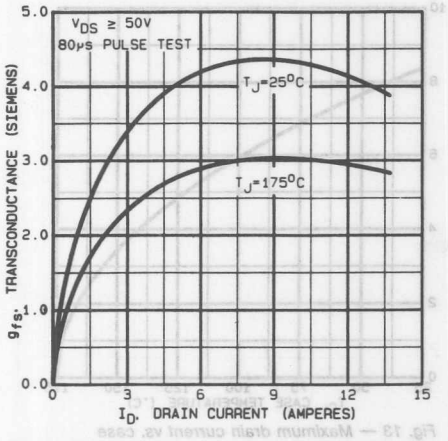


Fig. 6 - Typical transconductance vs. drain current.

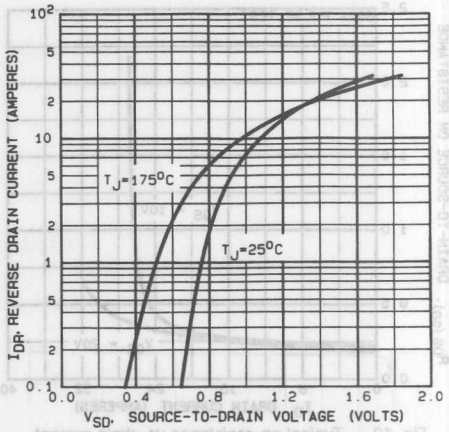


Fig. 7 - Typical source-drain diode forward voltage.

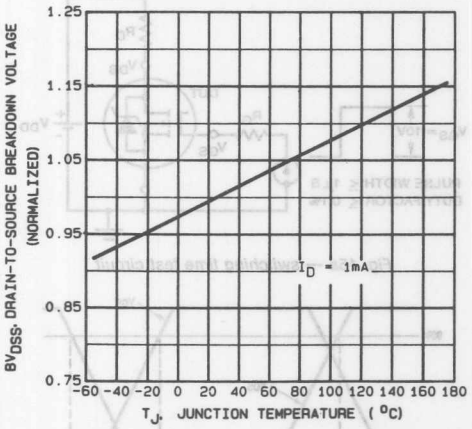


Fig. 8 - Breakdown voltage vs. temperature.

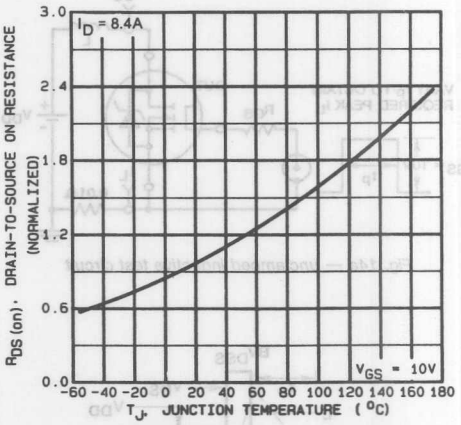


Fig. 9 - Normalized on-resistance vs. temperature.

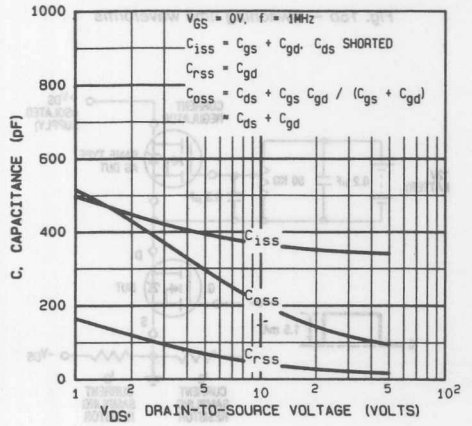


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

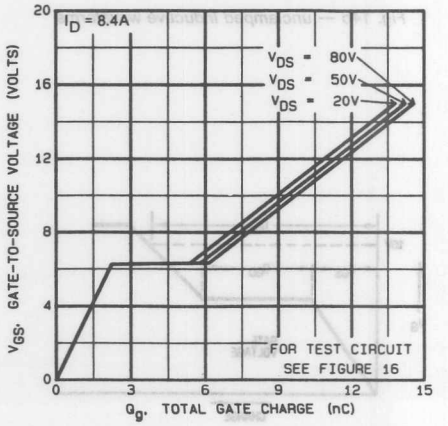


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

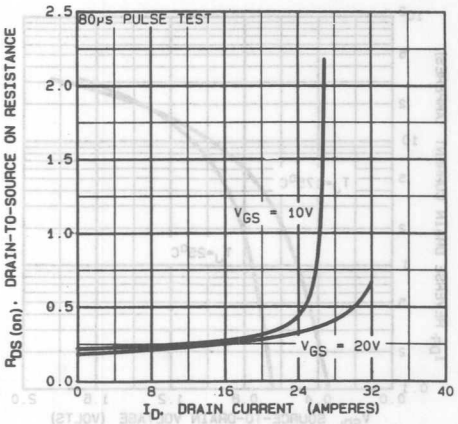


Fig. 12 — Typical on-resistance vs. drain current

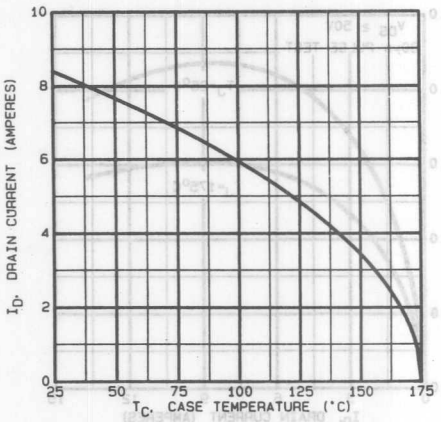


Fig. 13 — Maximum drain current vs. case temperature

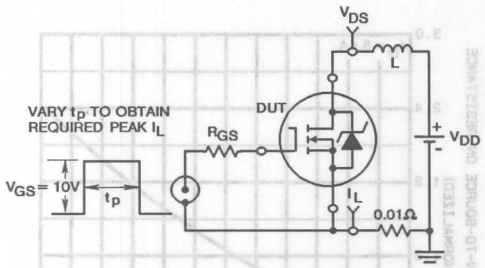


Fig. 14a — unclamped inductive test circuit

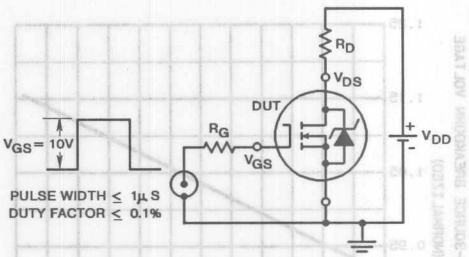


Fig. 15a — switching time test circuit

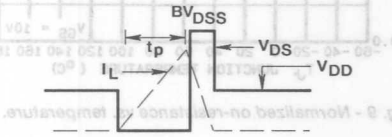


Fig. 14b — unclamped inductive waveforms

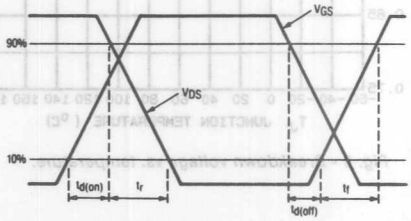


Fig. 15b — switching time waveforms

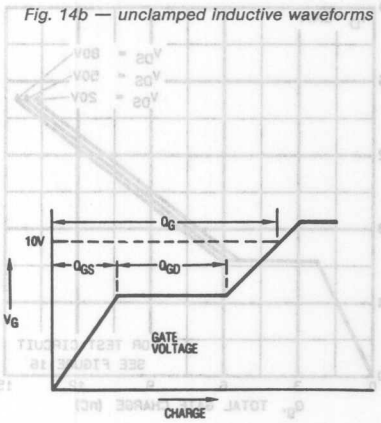


Fig. 16a — Basic gate charge waveform

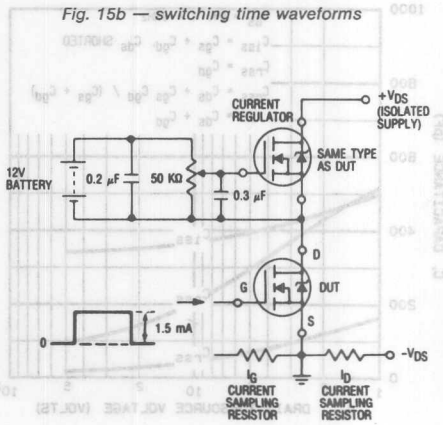


Fig. 16b — Gate charge test circuit

IRFR220/221/222
IRFU220/221/222

N-Channel Power MOSFETs
Avalanche-Energy-Rated

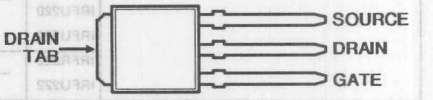
August 1991

Features

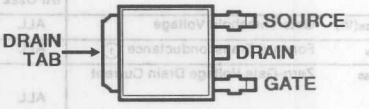
- 3.8A and 4.6A, 150V and 200V
- $r_{DS(on)}$ = 0.80Ω and 1.2Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Packages

TO-251AA
TOP VIEW



TO-252AA
TOP VIEW



Description

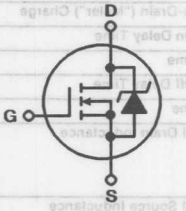
The IRFR220, IRFR221, IRFR222, IRFU220, IRFU221 and IRFU222 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFU series is supplied in the TO-251AA plastic package and the IRFR series is supplied in the TO-252AA surface-mount plastic package.

Because of space limitations branding (marking) on type IRFR220 is IRF220, IRFR221 is IFR221, IRFR222 is IRF222, IRFU220 is IFU220 and IRFU221 is IFU221, IRFU222 is IFU222.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFR220/221 IRFU220/221	IRFR222 IRFU222	UNITS
Continuous Drain Current				
T_C = 25°C	I_D	4.6	3.8	A
T_C = 100°C	I_D	2.9	2.4	A
Pulsed Drain Current	I_{DM}	18	15	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = 25°C	P_D	50	50	W
Linear Derating Factor		0.4	0.4	W/°C
Single Pulse Avalanche Energy Rating (2)	E_{AS}	85	85	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. V_{DD} = 10V, Start T_J = +25°C, L = 6.18mH, R_G = 50Ω, Peak I_L = 4.6A
3. Mounting pad must cover heatsink surface area. See Packages.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

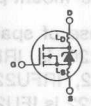
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File Number 2410

ELECTRICAL CHARACTERISTICS, At T_J = 25°C (Unless Otherwise Specified)

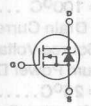
CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFR221, IRFU221	150	—	—	V	V_{GS} = 0 V, I_D = 250 μA
		IRFR220, IRFR222, IRFU220, IRFU222	200	—	—		
$R_{DS}(on)$	Static Drain-to-Source On-State Resistance ①	IRFR220, IRFR221, IRFU220, IRFU221	—	0.47	0.80	Ω	V_{GS} = 10 V, I_D = 2.4 A
		IRFR222, IRFU222	—	0.80	1.2		
$I_D(on)$	On-State Drain Current ①	IRFR220, IRFR221, IRFU220, IRFU221	4.6	—	—	A	$V_{DS} > I_D(on) \times R_{DS}(on)$ Max. V_{GS} = 10 V
		IRFR222, IRFU222	3.8				
$V_{GS}(th)$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250 μA
g_{fs}	Forward Transconductance ①	ALL	1.7	2.6	—	S (℧)	$V_{DS} \geq$ 50 V, I_{DS} = 2.4 A
I_{DSS}	Zero-Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0 V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20 V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500		V_{GS} = -20 V
Q_g	Total Gate Charge	ALL	—	12	18	nC	V_{GS} = 10 V, I_D = 4.6 A V_{DS} = 0.8 x Max. Rating See Fig. 16. (Independent of operating temperature)
Q_{gs}	Gate-to-Source Charge	ALL	—	2.3	3.4		
Q_{gd}	Gate-to-Drain ("Miller") Charge		—	4.5	6.8		
$t_d(on)$	Turn-On Delay Time	ALL	—	8.8	13	ns	V_{DD} = 100 V, $I_D \approx$ 4.6 A, R_G = 18 Ω R_D = 18 Ω See Fig. 15 (Independent of operating temperature)
t_r	Rise Time	ALL	—	27	41		
$t_d(off)$	Turn-Off Delay Time	ALL	—	21	32		
t_f	Fall Time	ALL	—	14	21		
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	330	—	pF	V_{GS} = 0 V, V_{DS} = 25 V f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	120	—		
C_{rss}	Reverse Transfer Capacitance	ALL	—	41	—		

Modified MOSFET symbol showing the internal inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_S	Continuous Source Current (Body Diode)	ALL	—	—	4.6	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier.
I_{SM}	Pulsed Source Current (Body Diode)	ALL	—	—	18		
V_{SD}	Diode Forward Voltage ①	ALL	—	—	1.8	V	T_J = 25°C, I_S = 4.6 A, V_{GS} = 0 V
t_{rr}	Reverse Recovery Time	ALL	69	170	400	ns	T_J = 25°C, I_F = 4.6 A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	0.30	0.72	1.8	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



THERMAL RESISTANCE

$R_{\theta JC}$	Junction-to-Case	ALL	—	—	2.5	°C/W	
$R_{\theta CS}$	Case-to-Sink	ALL	—	1.7	—		Typical solder mount ③
$R_{\theta JA}$	Junction-to-Ambient	ALL	—	—	110		Typical socket mount

① Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

② V_{DD} = 10 V, Starting T_J = 25°C, L = 6.18 mH, R_G = 50 Ω, Peak I_L = 4.6 A.

③ Mounting pad must cover heatsink surface area. See Case Style drawing on front page.

The information shown on the following graphs applies also to the IRFU devices.

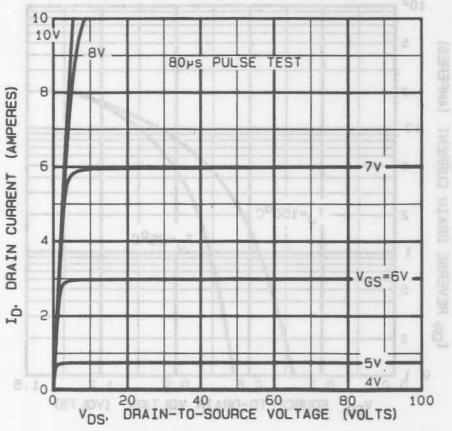


Fig. 1 - Typical output characteristics.

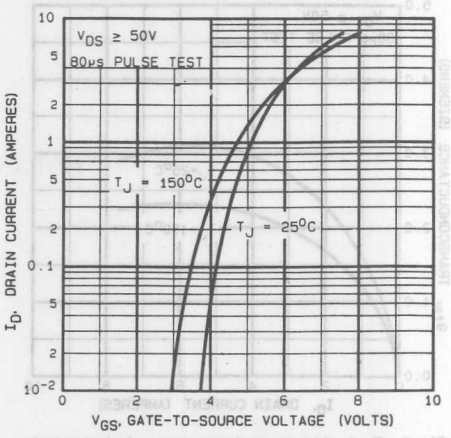


Fig. 2 - Typical transfer characteristics.

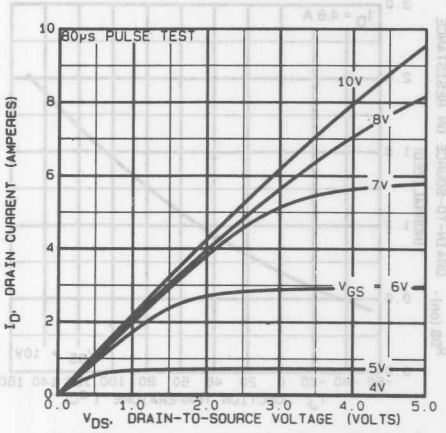


Fig. 3 - Typical saturation characteristics.

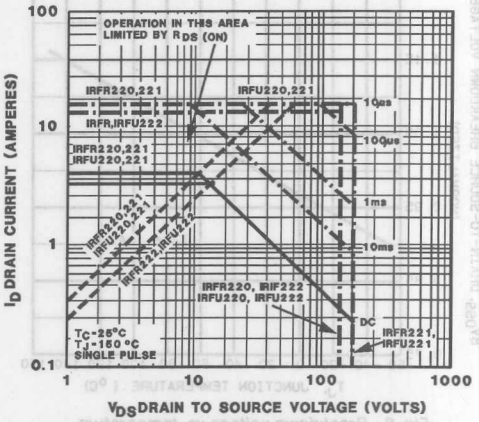


Fig. 4 - Maximum safe operating area.

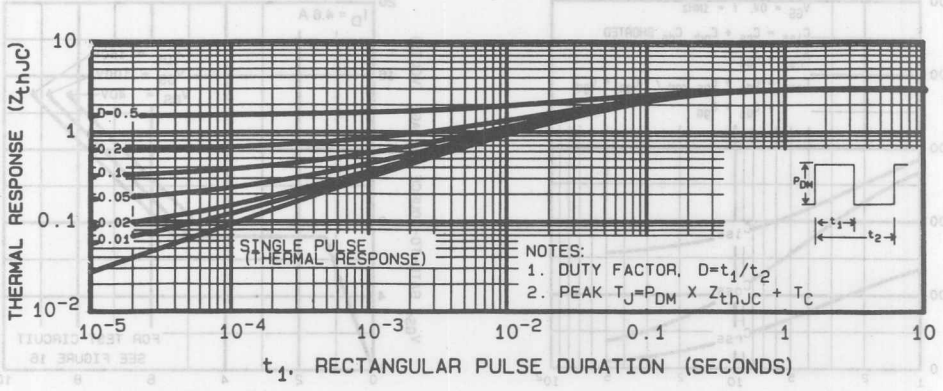


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

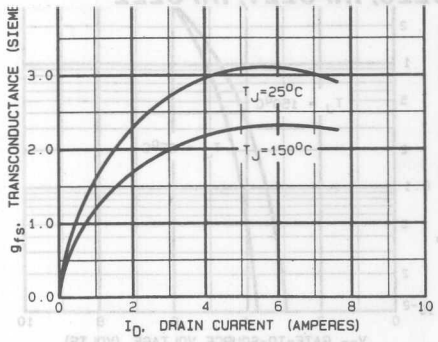


Fig. 6 - Typical transconductance vs. drain current.

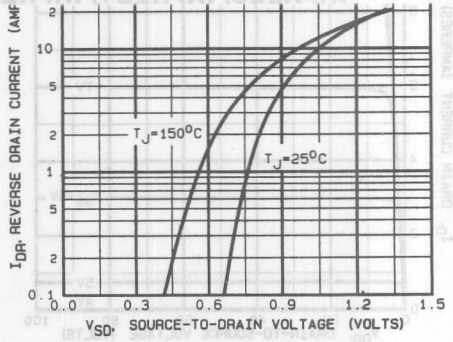


Fig. 7 - Typical source-drain diode forward voltage.

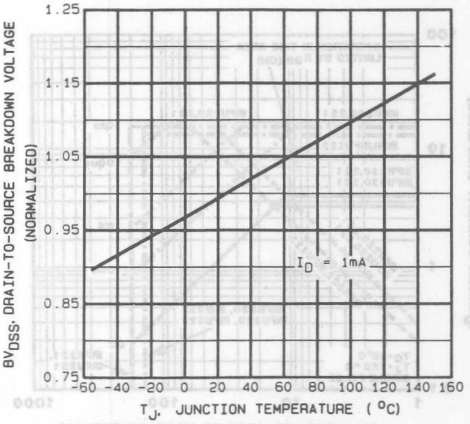


Fig. 8 - Breakdown voltage vs. temperature.

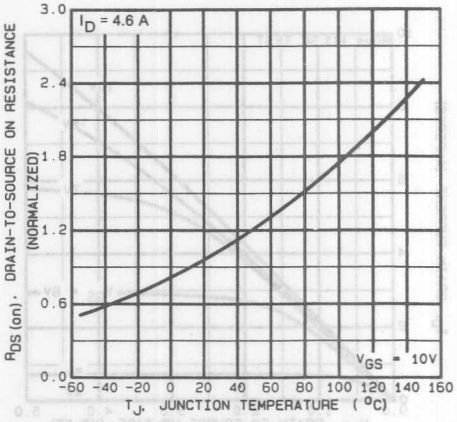


Fig. 9 - Normalized on-resistance vs. temperature.

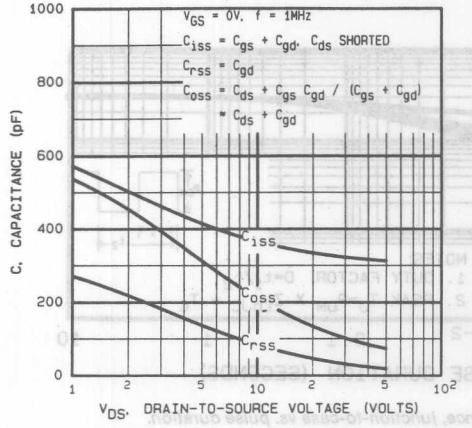


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

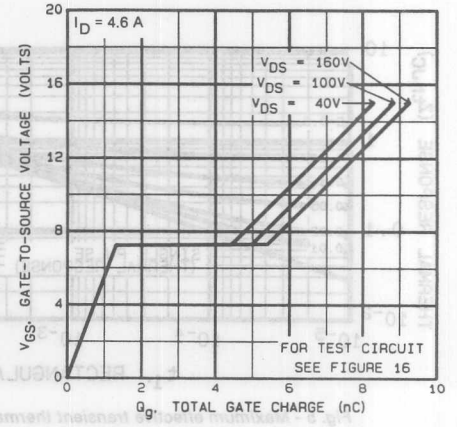


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

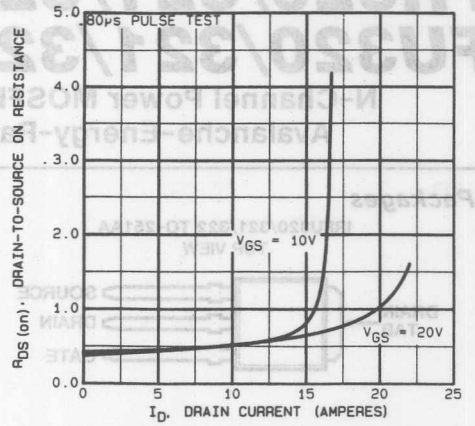


Fig. 12 — Typical on-resistance vs. drain current

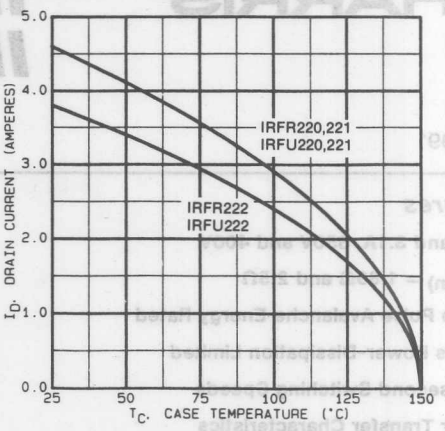


Fig. 13 — Maximum drain current vs. case temperature

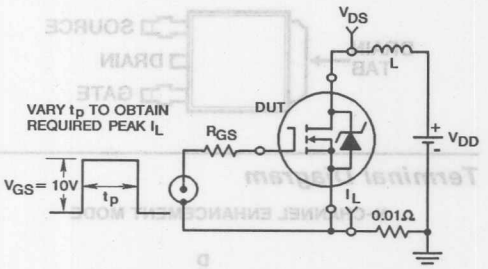


Fig. 14a — unclamped inductive test circuit

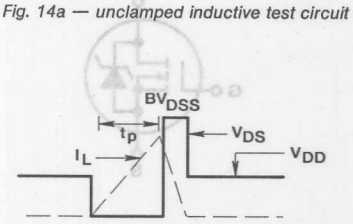


Fig. 14b — unclamped inductive waveforms

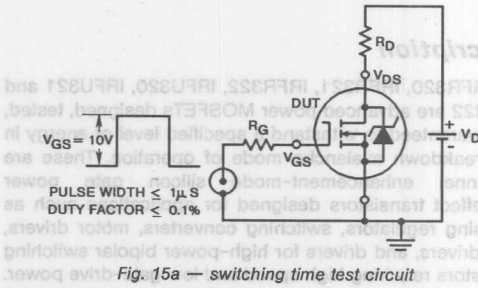


Fig. 15a — switching time test circuit

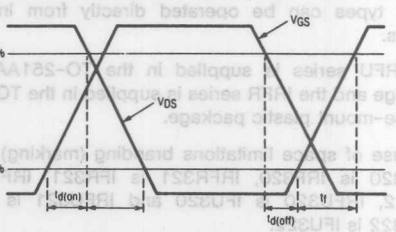


Fig. 15b — switching time waveforms

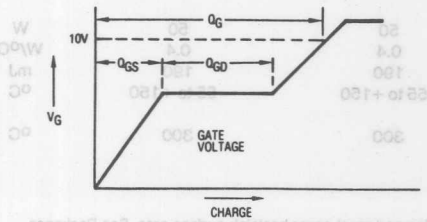


Fig. 16a — Basic gate charge waveform

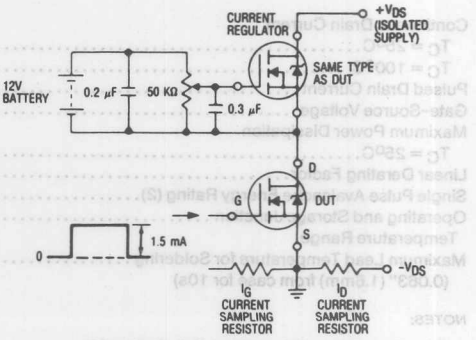


Fig. 16b — Gate charge test circuit

IRFR320/321/322
IRFU320/321/322

N-Channel Power MOSFETs
Avalanche-Energy-Rated

August 1991

Features

- 2.6A and 3.1A, 350V and 400V
- $r_{DS(on)}$ = 1.80Ω and 2.5Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

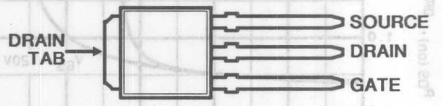
The IRFR320, IRFR321, IRFR322, IRFU320, IRFU321 and IRFU322 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFU series is supplied in the TO-251AA plastic package and the IRFR series is supplied in the TO-252AA surface-mount plastic package.

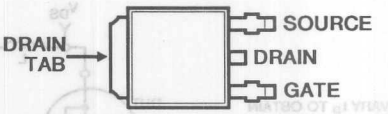
Because of space limitations branding (marking) on type IRFR320 is IRF320, IRFR321 is IFR321, IRFR322 is IRF322, IRFU320 is IFU320 and IRFU321 is IFU321, IRFU322 is IFU322.

Packages

IRFU320/321/322 TO-251AA
TOP VIEW



IRFR320/321/322 TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

	IRFU320/321 IRFR320/321	IRFU322 IRFR322	UNITS
Continuous Drain Current			
T_C = 25°C ..... I_D	3.1	2.6	A
T_C = 100°C ..... I_D	2.0	1.7	A
Pulsed Drain Current ..... I_{DM}	12	10	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = 25°C ..... P_D	50	50	W
Linear Derating Factor	0.4	0.4	W/°C
Single Pulse Avalanche Energy Rating (2) ..... E_{AS}	190	190	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	°C

NOTES:

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. V_{DD} = 50V, Start T_J = +25°C, L = 3.1mH, R_G = 25Ω, Peak I_L = 3.1A
3. Mounting pad must cover heatsink surface area. See Packages.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

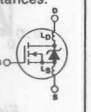
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File Number 2412

ELECTRICAL CHARACTERISTICS, At T_J = 25°C (Unless Otherwise Specified)

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFR321, IRFU321	350	—	—	V	V_{GS} = 0 V, I_D = 250 μA
		IRFR320, IRFU322, IRFR320, IRFU322	400	—	—		
$R_{DS}(on)$	Static Drain-to-Source On-State Resistance ①	IRFR320, IRFR321, IRFU320, IRFU321	—	1.6	1.8	Ω	V_{GS} = 10 V, I_D = 1.7 A
		IRFR322, IRFU322	—	1.6	2.5		
$I_D(on)$	On-State Drain Current ①	IRFR320, IRFU320, IRFR321, IRFU321	3.1	—	—	A	$V_{DS} > I_D(on) \times R_{DS}(on)$ Max. V_{GS} = 10 V
		IRFR322, IRFU322	2.6				
$V_{GS}(th)$	Gate Threshold Voltage ①	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250 μA
g_{fs}	Forward Transconductance	ALL	1.7	2.6	—	S (℧)	$V_{DS} \geq 50$ V, I_{DS} = 1.7 A
I_{DSS}	Zero-Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0 V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20 V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500		V_{GS} = -20 V
Q_g	Total Gate Charge	ALL	—	13	20	nC	V_{GS} = 10 V, I_D = 3.1 A
Q_{gs}	Gate-to-Source Charge	ALL	—	2.2	3.3		V_{DS} = 0.8 x Max. Rating
Q_{gd}	Gate-to-Drain ("Miller") Charge		—	7.2	11		See Fig. 16. (Independent of operating temperature)
$t_d(on)$	Turn-On Delay Time	ALL	—	10	15	ns	V_{DD} = 200 V, $I_D \approx$ 3.1 A, R_G = 18 Ω
t_r	Rise Time	ALL	—	14	21		R_D = 56 Ω
$t_d(off)$	Turn-Off Delay Time	ALL	—	30	45		See Fig. 15
t_f	Fall Time	ALL	—	13	20		(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	350	—	pF	V_{GS} = 0 V, V_{DS} = 25 V
C_{oss}	Output Capacitance	ALL	—	64	—		f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	8.1	—		See Fig. 10

Modified MOSFET symbol showing the internal inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_S	Continuous Source Current (Body Diode)	ALL	—	—	3.1	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier.
I_{SM}	Pulsed Source Current (Body Diode)	ALL	—	—	12		
V_{SD}	Diode Forward Voltage ①	ALL	—	—	1.6	V	T_J = 25°C, I_S = 3.1 A, V_{GS} = 0 V
t_{rr}	Reverse Recovery Time	ALL	120	270	600	ns	T_J = 25°C, I_F = 3.1 A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	0.64	1.4	3.0	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



THERMAL RESISTANCE

$R_{\theta JC}$	Junction-to-Case	ALL	—	—	2.5	°C/W	
$R_{\theta CS}$	Case-to-Sink	ALL	—	1.7	—		Typical solder mount ③
$R_{\theta JA}$	Junction-to-Ambient	ALL	—	—	110		Typical socket mount

① Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

② V_{DD} = 50 V, Starting T_J = 25°C, L = 3.1 mH, R_G = 25 Ω, Peak I_L = 3.1 A.

③ Mounting pad must cover heatsink surface area. See Case Style drawing on front page.

The information shown on the following graphs applies also to the IRFU devices.

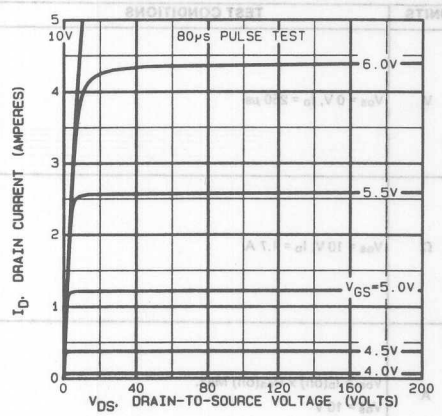


Fig. 1 - Typical output characteristics.

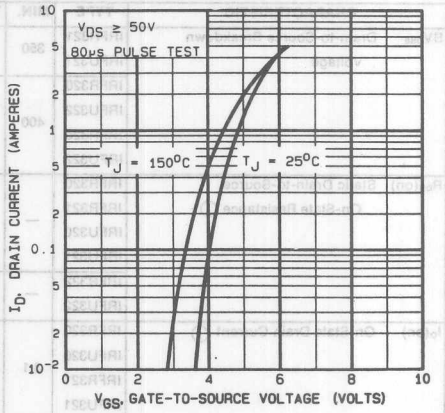


Fig. 2 - Typical transfer characteristics.

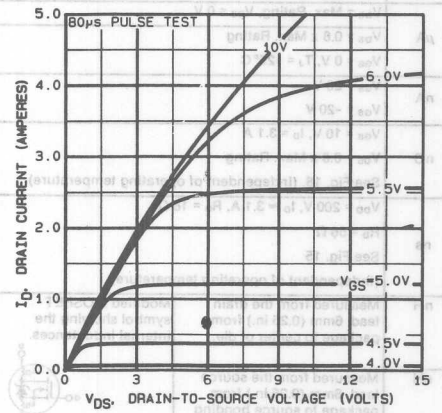


Fig. 3 - Typical saturation characteristics.

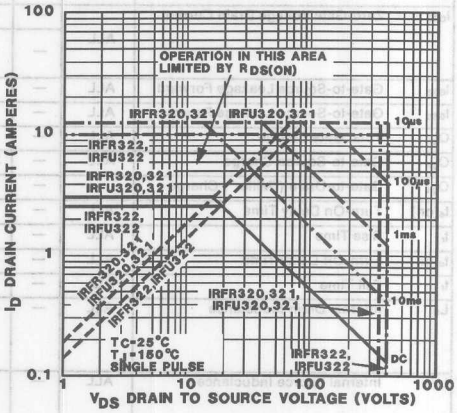


Fig. 4 - Maximum safe operating area.

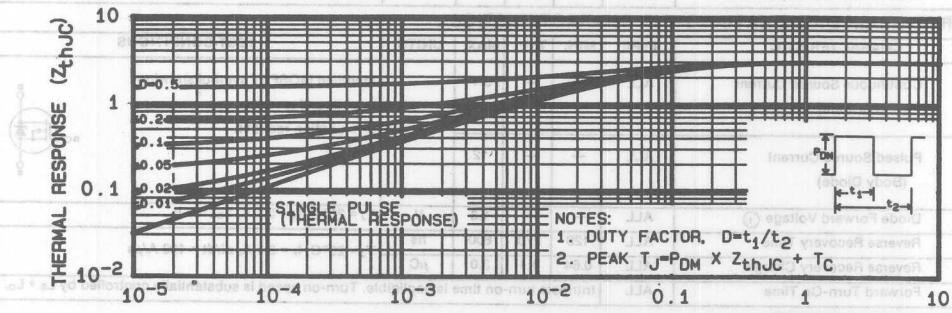


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

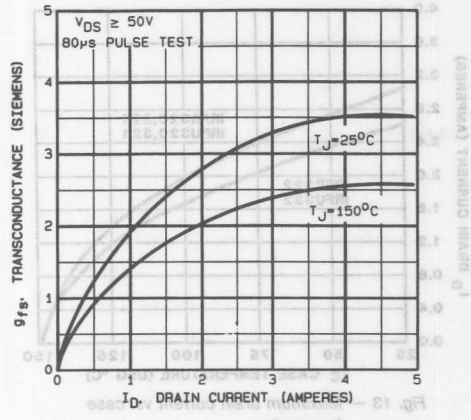


Fig. 6 - Typical transconductance vs. drain current.

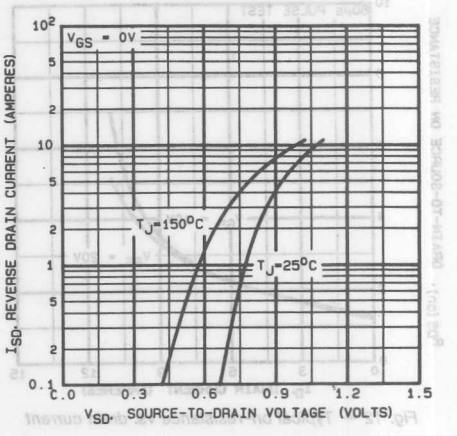


Fig. 7 - Typical source-drain diode forward voltage.

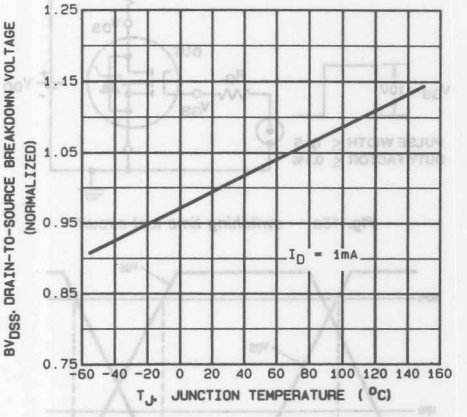


Fig. 8 - Breakdown voltage vs. temperature.

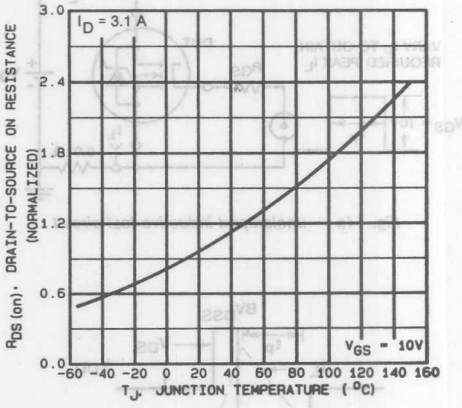


Fig. 9 - Normalized on-resistance vs. temperature.

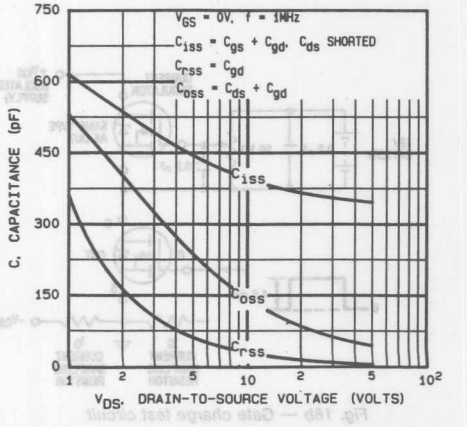


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

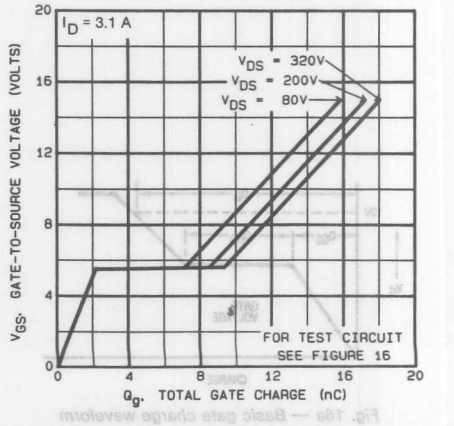


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

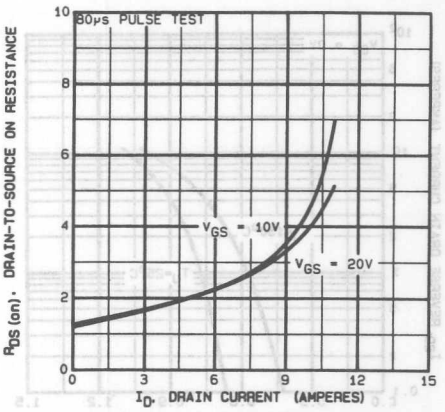


Fig. 12 — Typical on-resistance vs. drain current

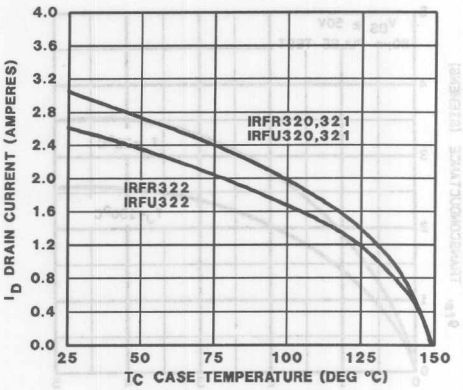


Fig. 13 — Maximum drain current vs. case temperature

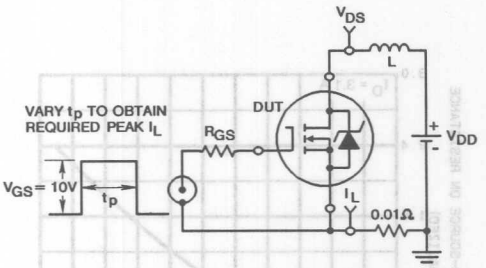


Fig. 14a — unclamped inductive test circuit

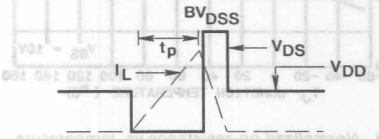


Fig. 14b — unclamped inductive waveforms

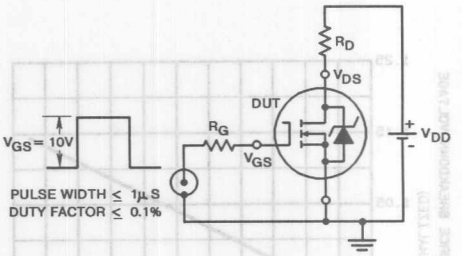


Fig. 15a — switching time test circuit

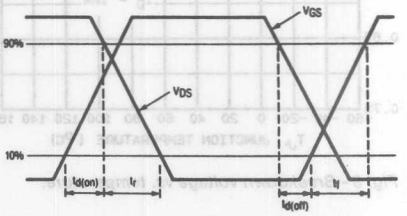


Fig. 15b — switching time waveforms

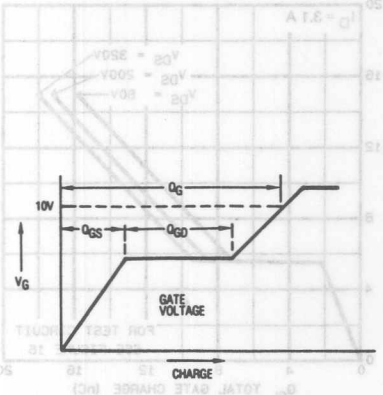


Fig. 16a — Basic gate charge waveform

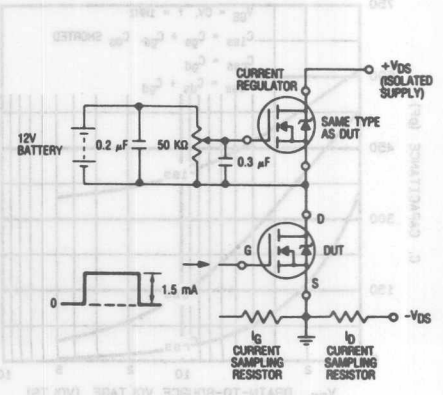


Fig. 16b — Gate charge test circuit

IRFR420/421/422
IRFU420/421/422

N-Channel Power MOSFETs
Avalanche-Energy-Rated

August 1991

Features

- 2.2A and 2.5A, 450V and 500V
- $r_{DS(on)}$ = 3.0Ω and 4.0Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

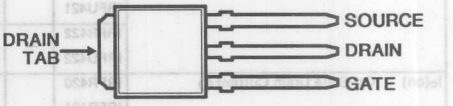
The IRFR420, IRFR421, IRFR422, IRFU420, IRFU421 and IRFU422 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFU series is supplied in the TO-251AA plastic package and the IRFR series is supplied in the TO-252AA surface-mount plastic package.

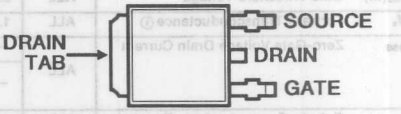
Because of space limitations branding (marking) on type IRFR420 is IRF420, IRFR421 is IFR421, IRFR422 is IRF422, IRFU420 is IFU420 and IRFU421 is IFU421, IRFU422 is IFU422.

Packages

IRFU420/421/422 TO-251AA
TOP VIEW

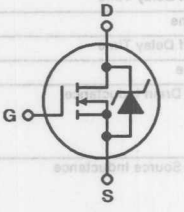


IRFR420/421/422 TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		IRFU420/421 IRFR420/421	IRFU422 IRFR422	UNITS
Continuous Drain Current				
T_C = 25°C	I_D	2.5	2.2	A
T_C = 100°C	I_D	1.6	1.4	A
Pulsed Drain Current	I_{DM}	8	7	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = 25°C	P_D	50	50	W
Linear Derating Factor		0.4	0.4	W/°C
Single Pulse Avalanche Energy Rating (2)	E_{AS}	210	210	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. V_{DD} = 50V, Start T_J = +25°C, L = 60mH, R_G = 25Ω, Peak I_L = 2.5A
3. Mounting pad must cover heatsink surface area. See Packages.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

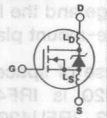
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File Number **2411**

ELECTRICAL CHARACTERISTICS, At T_J = 25°C (Unless Otherwise Specified)

	CHARACTERISTIC	TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFR421, IRFU421	450	—	—	V	V_{GS} = 0 V, I_D = 250 μA
		IRFR420, IRFR422, IRFU420, IRFU422	500	—	—		
$R_{DS}(on)$	Static Drain-to-Source On-State Resistance ①	IRFR420, IRFR421, IRFU420, IRFU421	—	2.9	3.0	Ω	V_{GS} = 10 V, I_D = 1.3 A
		IRFR422, IRFU422	—	—	4.0		
$I_D(on)$	On-State Drain Current ①	IRFR420, IRFR421, IRFU420, IRFU421	2.5	—	—	A	$V_{DS} > I_D(on) \times R_{DS}(on)$ Max.; V_{GS} = 10 V
		IRFR422, IRFU422	2.2				
$V_{GS}(th)$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250 μA
gf_s	Forward Transconductance ①	ALL	1.5	2.2	—	S (℧)	$V_{DS} \geq$ 50 V, I_{DS} = 1.4 A
I_{DSS}	Zero-Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000		V_{DS} = 0.8 x Max. Rating, V_{GS} = 0 V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20 V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500		V_{GS} = -20 V
Q_g	Total Gate Charge	ALL	—	13	19	nC	V_{GS} = 10 V, I_D = 2.5 A
Q_{gs}	Gate-to-Source Charge	ALL	—	2.2	3.3		V_{DS} = 0.8 x Max. Rating
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	—	6.8	10		See Fig. 16. (Independent of operating temperature)
$t_{d}(on)$	Turn-On Delay Time	ALL	—	10	15	ns	V_{DD} = 250 V, $I_D \approx$ 2.5 A, R_G = 18 Ω, R_D = 100 Ω
t_r	Rise Time	ALL	—	12	18		See Fig. 15
$t_{d}(off)$	Turn-Off Delay Time	ALL	—	28	42		(Independent of operating temperature)
t_f	Fall Time	ALL	—	12	18		
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	350	—	pF	V_{GS} = 0 V, V_{DS} = 25 V
C_{oss}	Output Capacitance	ALL	—	54	—		f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	9.6	—		See Fig. 10

Modified MOSFET symbol showing the internal inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC	TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_S	Continuous Source Current (Body Diode)	ALL	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier.
I_{SM}	Pulsed Source Current (Body Diode)	ALL	—	—	8		
V_{SD}	Diode Forward Voltage ①	ALL	—	—	1.6	V	T_J = 25°C, I_S = 2.5 A, V_{GS} = 0 V
t_{rr}	Reverse Recovery Time	ALL	130	270	540	ns	T_J = 25°C, I_F = 2.5 A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	0.57	1.2	2.3	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



THERMAL RESISTANCE

$R_{\theta JC}$	Junction-to-Case	ALL	—	—	2.5	°C/W	
$R_{\theta CS}$	Case-to-Sink	ALL	—	1.7	—		Typical solder mount ③
$R_{\theta JA}$	Junction-to-Ambient	ALL	—	—	110		Typical socket mount

① Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

② V_{DD} = 50 V, Starting T_J = 25°C, L = 60 mH, R_G = 25 Ω, Peak I_L = 2.5 A.

③ Mounting pad must cover heatsink surface area. See Case Style drawing on front page.

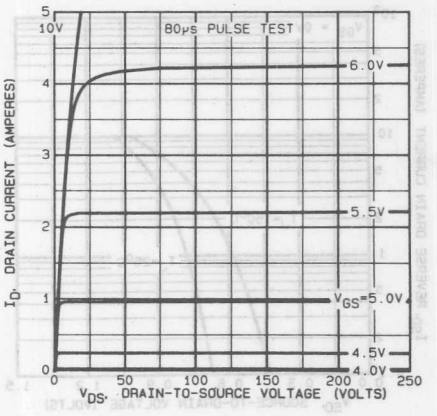


Fig. 1 - Typical output characteristics.

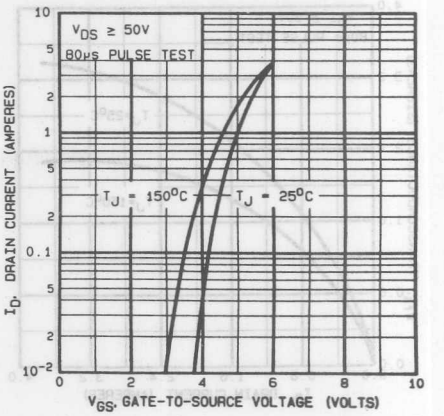


Fig. 2 - Typical transfer characteristics.

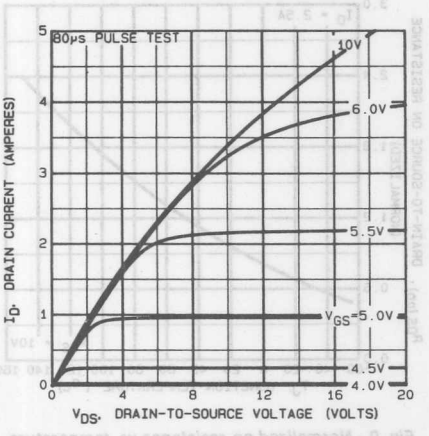


Fig. 3 - Typical saturation characteristics.

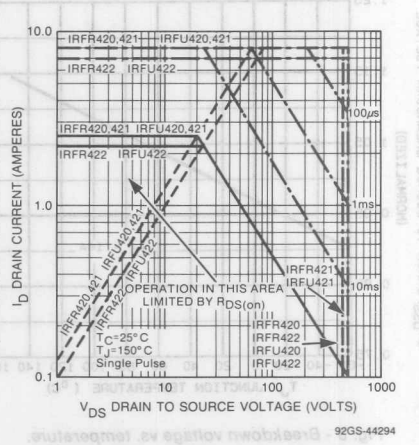


Fig. 4 - Maximum safe operating area.

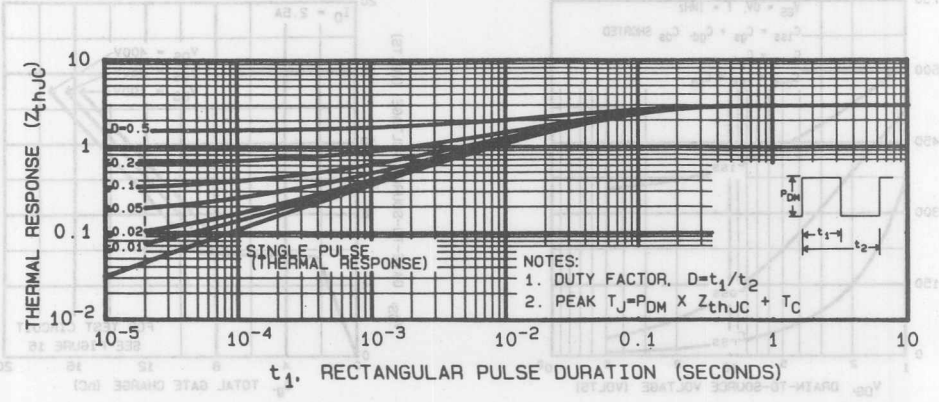


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

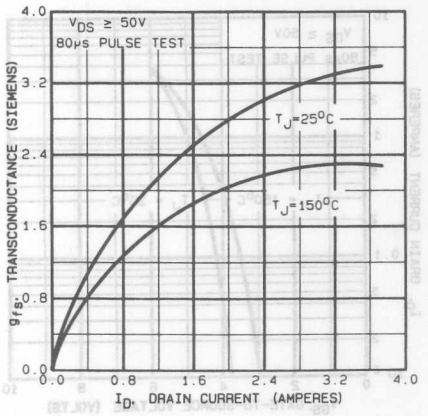


Fig. 6 - Typical transconductance vs. drain current.

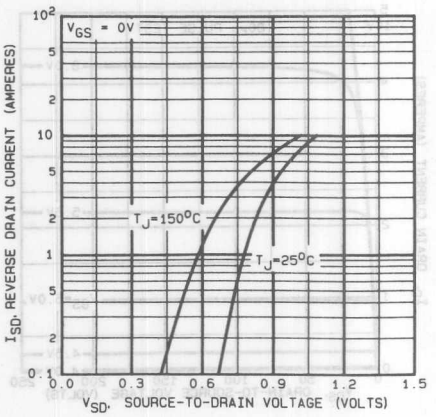


Fig. 7 - Typical source-drain diode forward voltage.

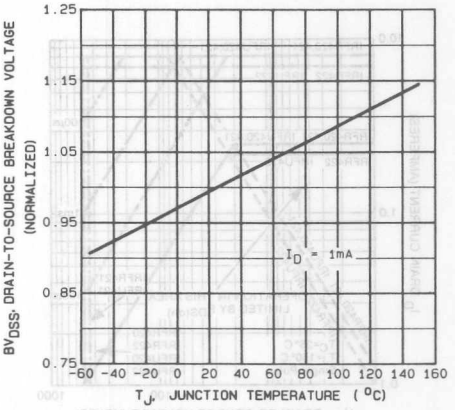


Fig. 8 - Breakdown voltage vs. temperature.

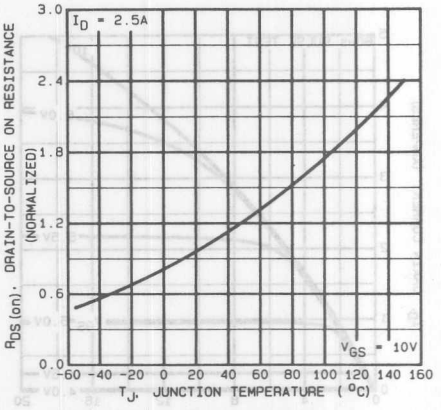


Fig. 9 - Normalized on-resistance vs. temperature.

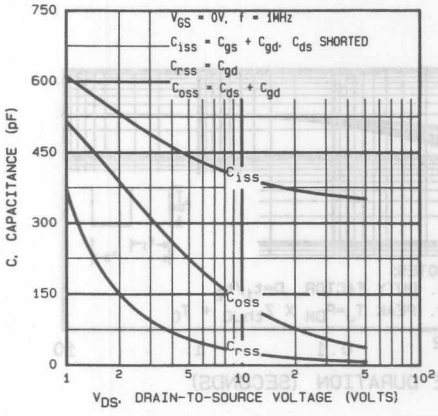


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

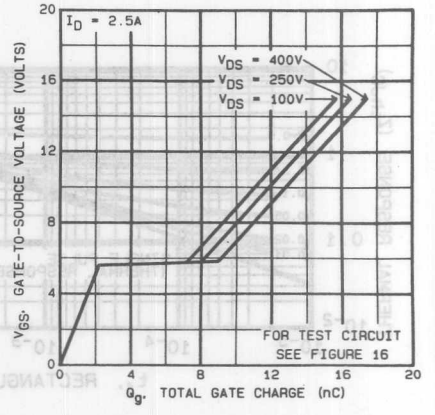


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

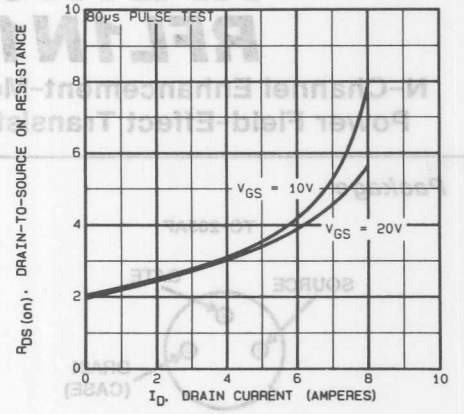


Fig. 12 — Typical on-resistance vs. drain current

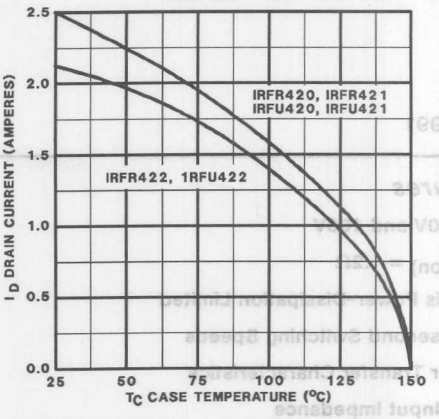


Fig. 13 — Maximum drain current vs. case temperature

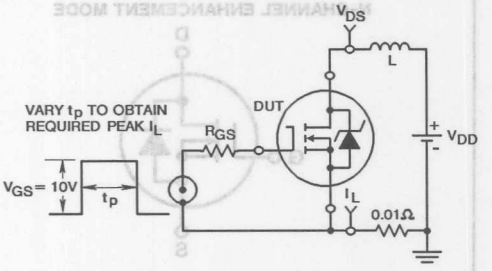


Fig. 14a — unclamped inductive test circuit

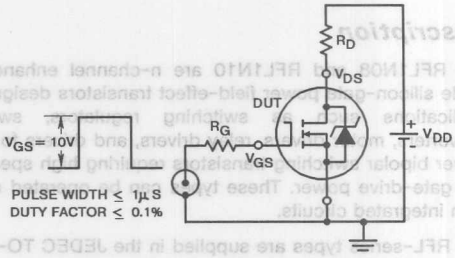


Fig. 15a — switching time test circuit

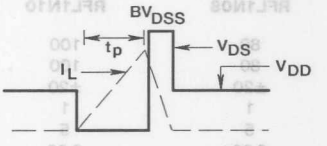


Fig. 14b — unclamped inductive waveforms

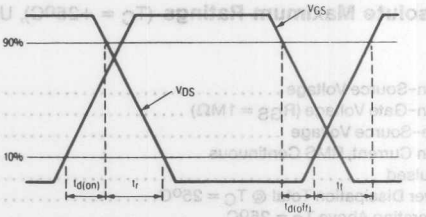


Fig. 15b — switching time waveforms

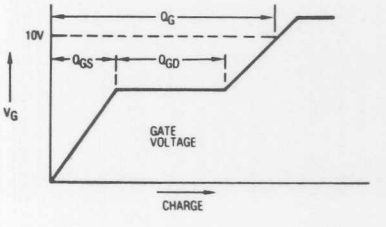


Fig. 16a — Basic gate charge waveform

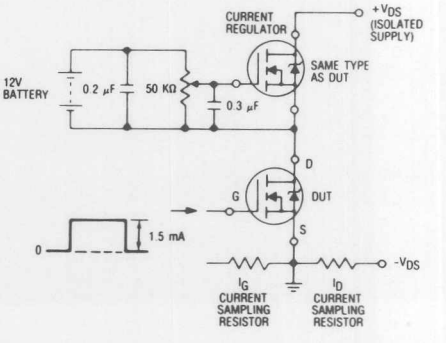


Fig. 16b — Gate charge test circuit

HARRIS

RFL1N08
RFL1N10

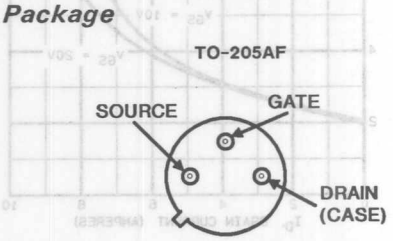
N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

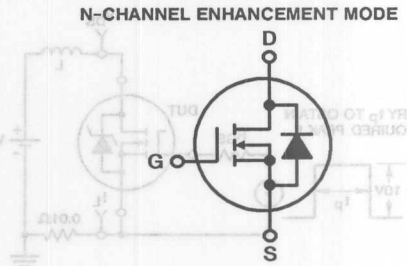
Features

- 1A, 80V and 100V
- $R_{DS(on)} = 1.2\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package



Terminal Diagram



Description

The RFL1N08 and RFL1N10 are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package.

Absolute Maximum Ratings ($T_C = +25^oC$), Unless Otherwise Specified

		RFL1N08	RFL1N10	UNITS
Drain-Source Voltage	V_{DSS}	80	100	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	80	100	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Drain Current, RMS Continuous	I_D	1	1	A
Pulsed	I_{DM}	5	5	A
Power Dissipation Total @ $T_C = 25^oC$	P_D	8.33	8.33	W
Derating Above $T_C = 25^oC$		0.0667	0.0667	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

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File Number **1385.1**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N08		RFL1N10		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	80	–	100	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V	–	1	–	–	μA
		V_{DS} = 80V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 65V	–	50	–	–	μA
		V_{DS} = 80V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.2	–	1.2	V
		I_D = 2A, V_{GS} = 10V	–	3.3	–	3.3	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.2	–	1.2	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse-Transfer Capacitance	C_{RSS}		–	25	–	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 50V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	17 (typ)	25	17 (typ)	25	ns
Rise Time	t_r		30 (typ)	45	30 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		30 (typ)	45	30 (typ)	45	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N08		RFL1N10		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

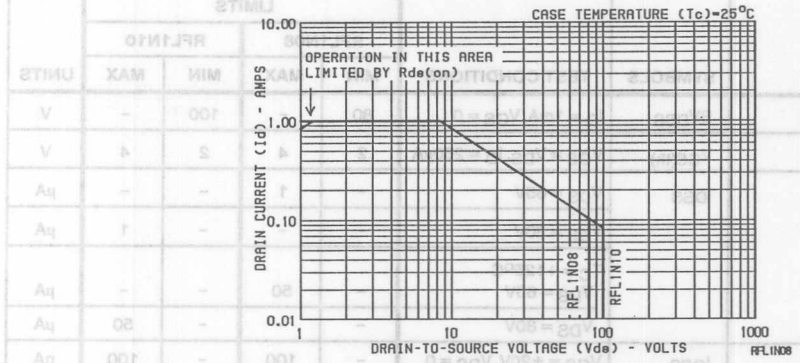


Fig 1 - Maximum operating areas for all types.

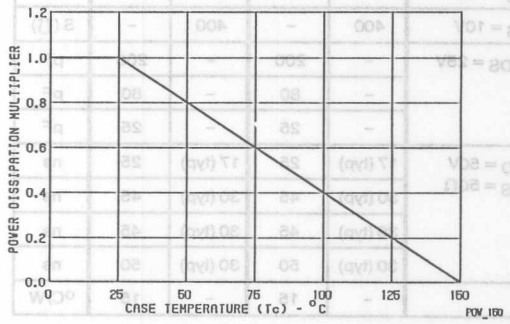


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

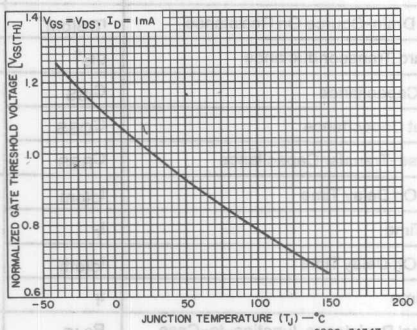


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

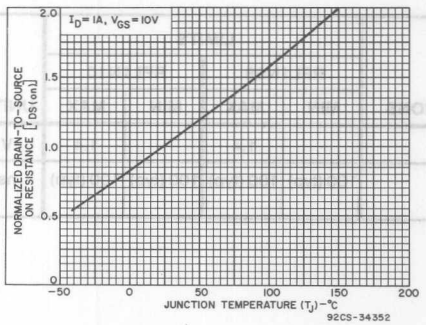


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

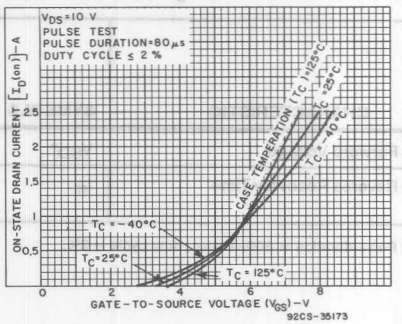


Fig. 5 - Typical transfer characteristics for all types.

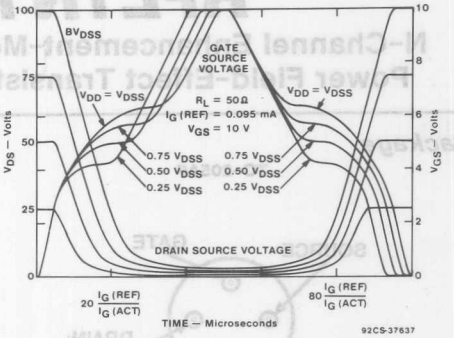


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

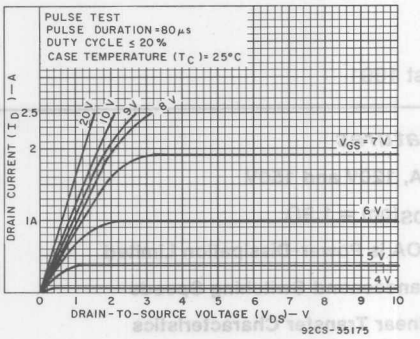


Fig. 7 - Typical saturation characteristics for all types.

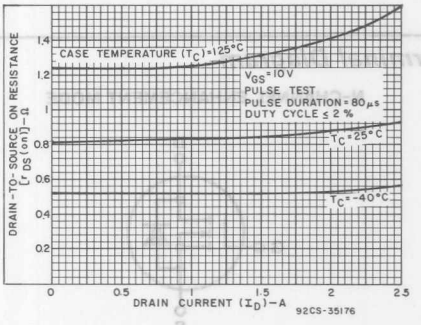


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

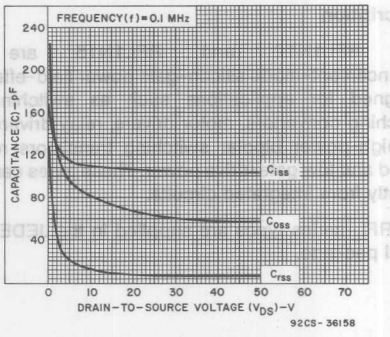


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

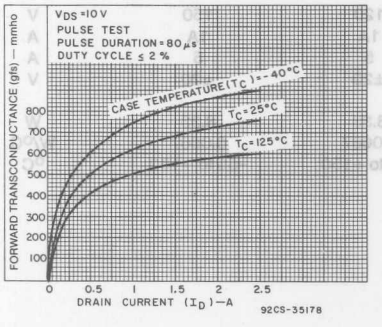


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

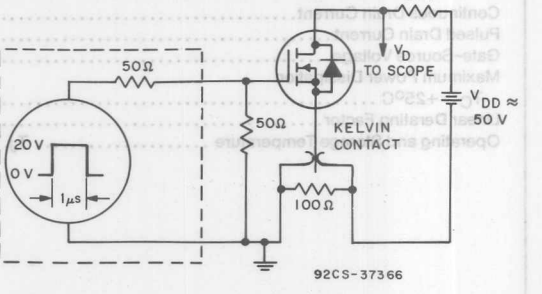


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFL1N12
RFL1N15

N-Channel Enhancement-Mode Power Field-Effect Transistors

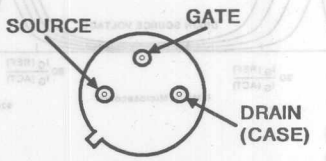
August 1991

Features

- 1A, 120V and 150V
- $r_{DS}(on) = 1.9\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-205AF



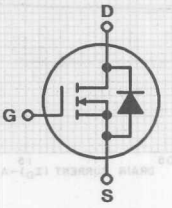
Description

The RFL1N12 and RFL1N15 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFL1N12	RFL1N15	UNITS
Drain-Source Voltage	V_{DSS}	120	150	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	120	150	V
Continuous Drain Current	I_D	1A	1A	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	8.33	8.33	W
Linear Derating Factor		0.0667	0.0667	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1444.1

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL1N12 MIN	LIMITS RFL1N12 MAX	LIMITS RFL1N15 MIN	LIMITS RFL1N15 MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	120	–	120	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V	–	1	–	–	μA
		V_{DS} = 120V	–	–	–	1	μA
		T_C = +125°C V_{DS} = 100V	–	50	–	–	μA
		V_{DS} = 120V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.9	–	1.9	V
		I_D = 2A, V_{GS} = 10V	–	6.3	–	6.3	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.9	–	1.9	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse-Transfer Capacitance	C_{RSS}		–	25	–	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 75V R_{GEN} = R_{GS} = 50Ω V_{GS} = 10V	17 (typ)	25	17 (typ)	25	ns
Rise Time	t_r		30 (typ)	45	30 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		30 (typ)	45	30 (typ)	45	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL1N12 MIN	LIMITS RFL1N12 MAX	LIMITS RFL1N15 MIN	LIMITS RFL1N15 MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A d_{IF}/dt = 50A/μs	150 (typ)	150 (typ)	150 (typ)	150 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

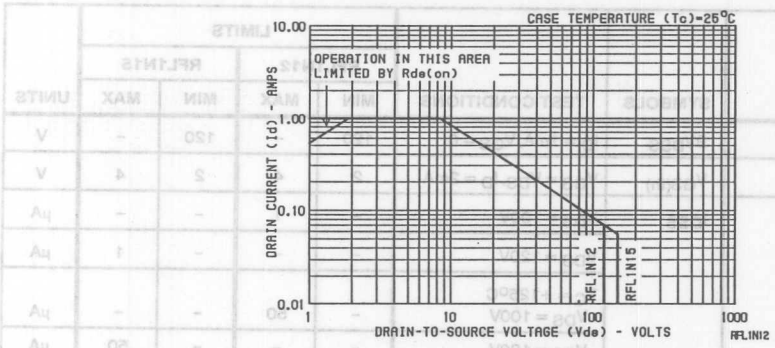


Fig. 1 — Maximum operating areas for all types.

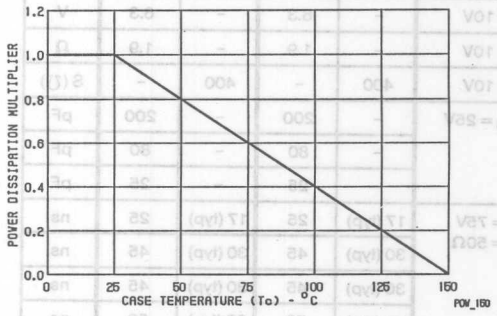


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

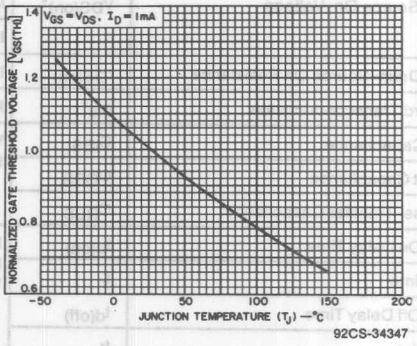


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

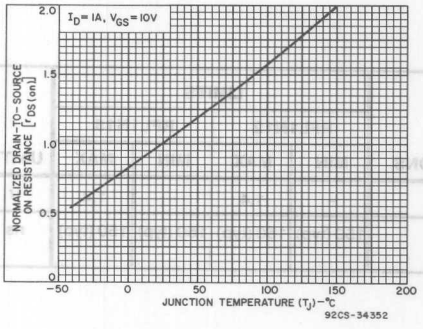


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

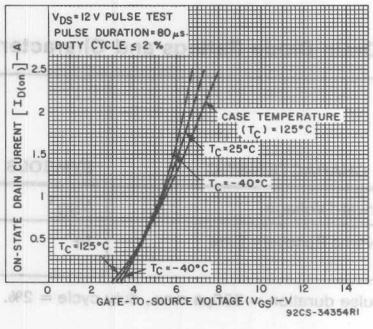


Fig. 5 — Typical transfer characteristics for all types.

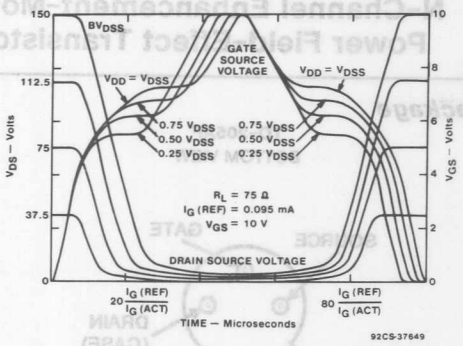


Fig. 6. Normalized switching waveforms for constant gate-current drive.

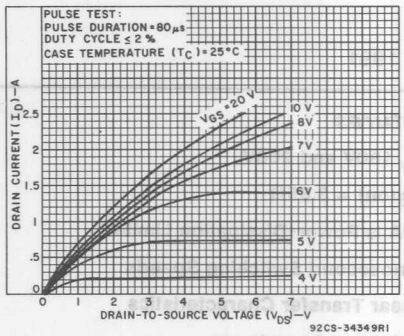


Fig. 7. Typical saturation characteristics for all types.

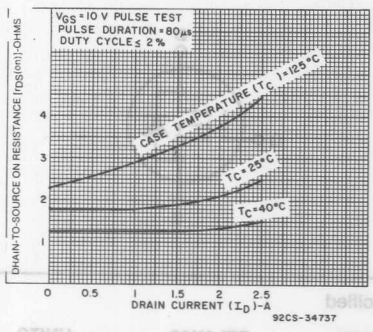


Fig. 8. Typical drain-to-source on resistance as a function of drain current for all types.

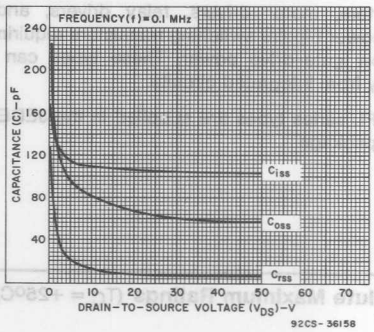


Fig. 9. Capacitance as a function of drain-to-source voltage for all types.

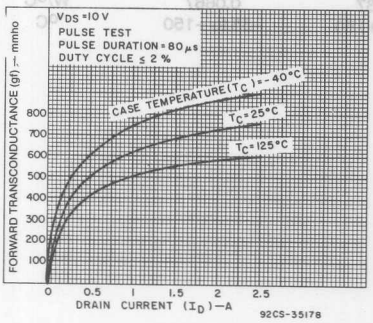


Fig. 10. Typical forward transconductance as a function of drain current for all types.

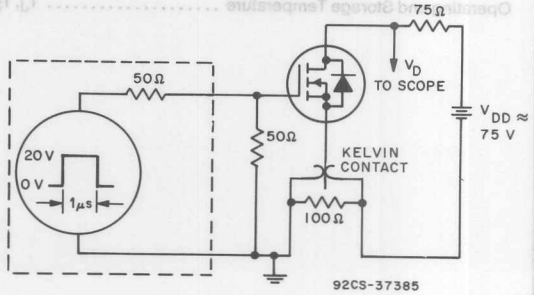


Fig. 11. Switching Time Test Circuit.

HARRIS

RFL1N18
RFL1N20

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 1A, 180V and 200V
- $r_{DS(on)} = 3.65\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

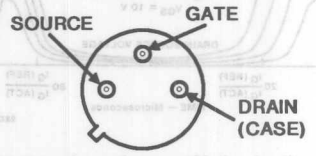
Description

The RFL1N18 and RFL1N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL series types are supplied in the JEDEC TO-205AF metal package.

Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFL1N18	RFL1N20	UNITS
Drain-Source Voltage	V_{DSS}	180	200	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	180	200	V
Continuous Drain Current	I_D	1	1	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	8.33	8.33	W
Derate Above T_C = +25°C		0.0667	0.0667	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1442.1

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N18		RFL2N20		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	180	–	200	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145V	–	1	–	–	μA
		V_{DS} = 160V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 145V	–	50	–	–	μA
		V_{DS} = 160V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	3.65	–	3.65	V
		I_D = 2A, V_{GS} = 10V	–	8.3	–	8.3	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	3.65	–	3.65	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	60	–	60	pF
Reverse-Transfer Capacitance	C_{RSS}		–	25	–	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 100V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	15 (typ)	25	15 (typ)	25	ns
Rise Time	t_r		20 (typ)	30	20 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		25 (typ)	40	25 (typ)	40	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N18		RFL2N20		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	200 (typ)	200 (typ)	200 (typ)	200 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

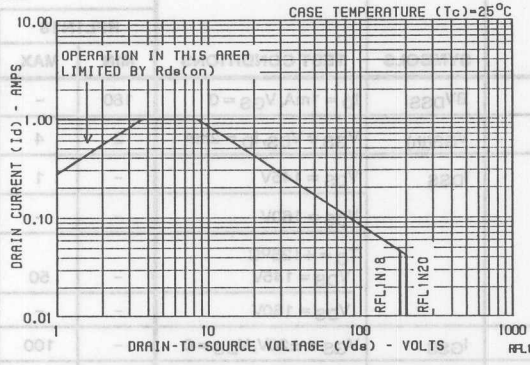


Fig. 1 - Maximum operating areas for all types.

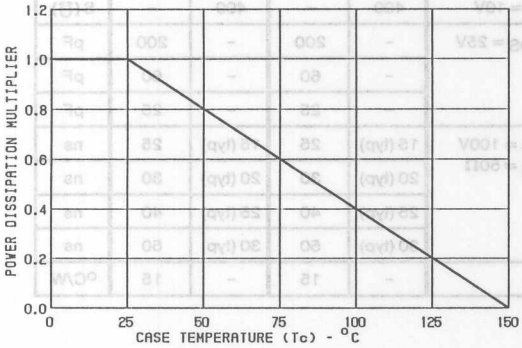


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

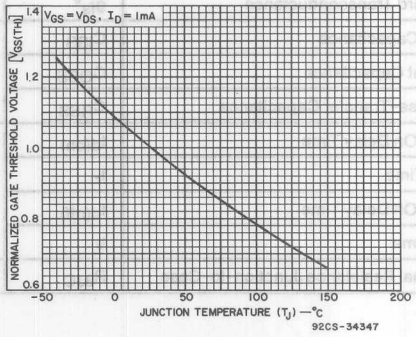


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

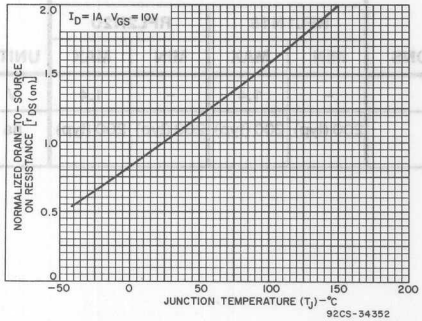


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

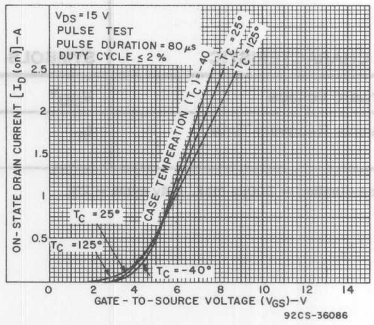


Fig. 5 - Typical transfer characteristics for all types.

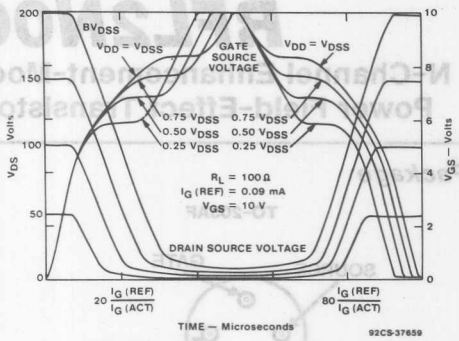


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

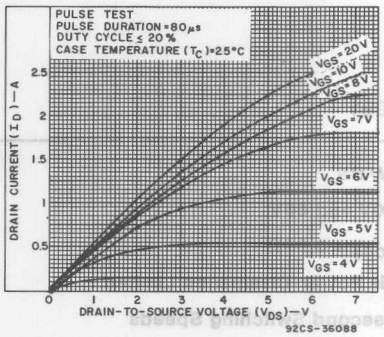


Fig. 7 - Typical saturation characteristics for all types.

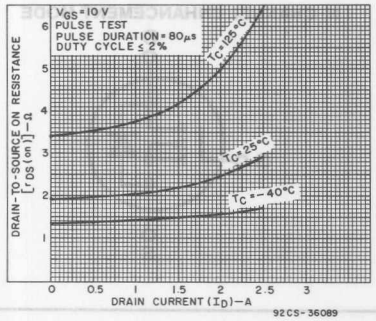


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

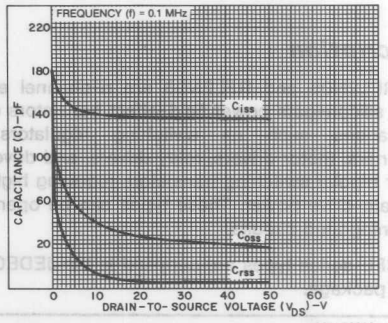


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

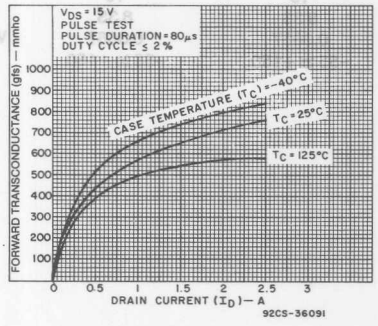


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

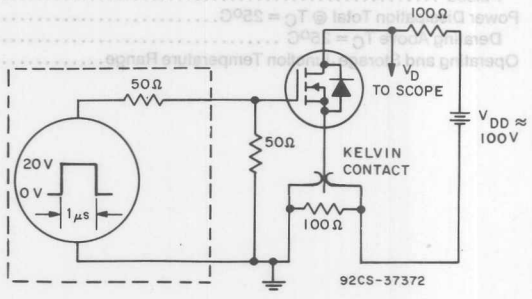


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFL2N05
RFL2N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 2A, 50V and 60V
- $R_{DS(on)} = 0.95\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

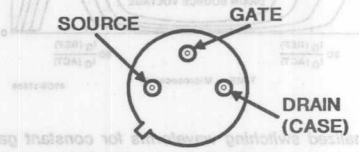
Description

The RFL2N05 and RFL2N06 are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package.

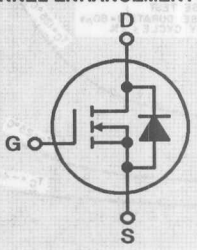
Package

TO-205AF



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFL2N05	RFL2N06	UNITS
Drain-Source Voltage	V_{DSS}	50	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	60	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Drain Current, RMS Continuous	I_D	2	2	A
Pulsed	I_{DM}	10	10	A
Power Dissipation Total @ T_C = 25°C	P_D	8.33	8.33	W
Derating Above T_C = 25°C		0.0667	0.0667	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

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File Number **1497.1**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL2N05 MIN	LIMITS RFL2N05 MAX	LIMITS RFL2N06 MIN	LIMITS RFL2N06 MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	50	–	60	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V	–	1	–	–	μA
		V_{DS} = 50V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 40V	–	50	–	–	μA
		V_{DS} = 50V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	0.95	–	0.95	V
		I_D = 2A, V_{GS} = 10V	–	2.0	–	2.0	V
		I_D = 4A, V_{GS} = 15V	–	4.8	–	4.8	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	0.95	–	0.95	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	85	–	85	pF
Reverse-Transfer Capacitance	C_{RSS}		–	30	–	30	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 30V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	6 (typ)	15	6 (typ)	15	ns
Rise Time	t_r		14 (typ)	30	14 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		16 (typ)	30	16 (typ)	30	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL2N05 MIN	LIMITS RFL2N05 MAX	LIMITS RFL2N06 MIN	LIMITS RFL2N06 MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulsed: Pulse duration ≤ 300μs max., duty cycle ≤ 2%.

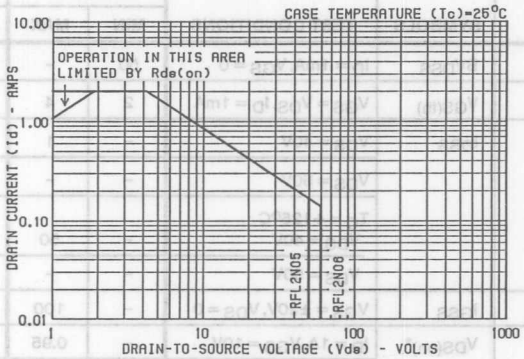


Fig. 1 — Maximum operating areas for all types.

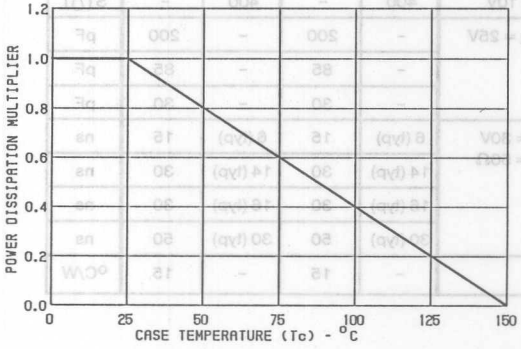


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

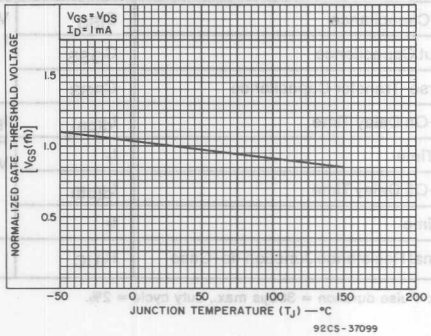


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

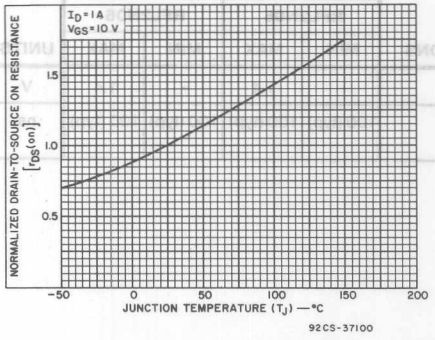


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

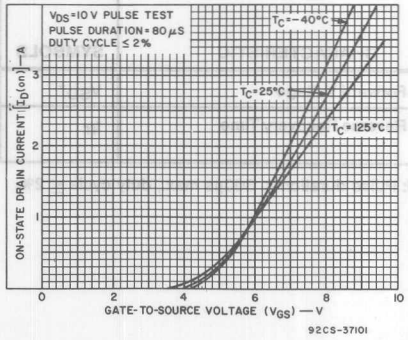


Fig. 5 — Typical transfer characteristics for all types.

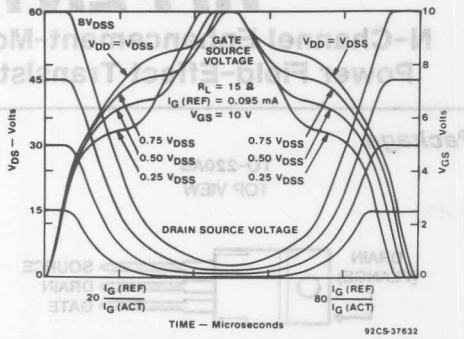


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

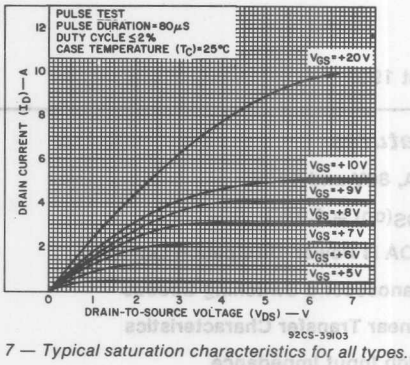


Fig. 7 — Typical saturation characteristics for all types.

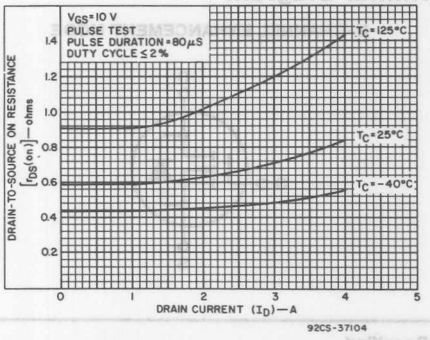


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

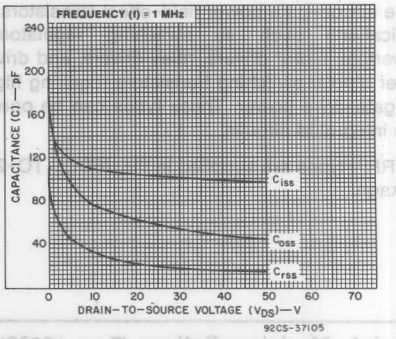


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

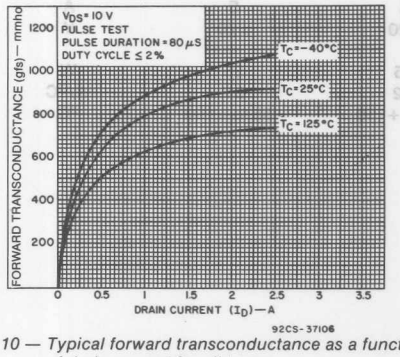


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

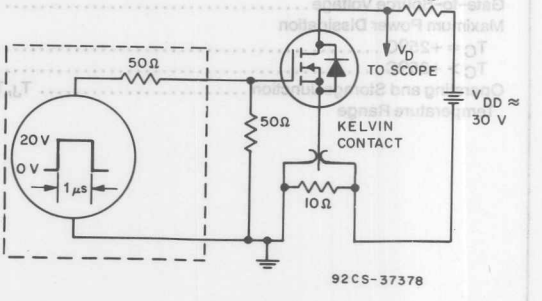


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFP2N08
RFP2N10

N-Channel Enhancement-Mode Power Field-Effect Transistors

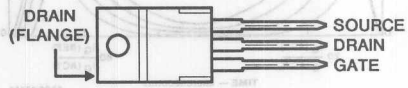
August 1991

Features

- 2A, 80V and 100V
- $r_{DS}(on) = 1.05\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-220AB
TOP VIEW



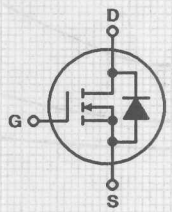
Description

The RFP2N08 and RFP2N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP-types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP2N08	RFP2N10	UNITS
Drain-Source Voltage	V_{DSS}	80	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	80	100	V
RMS Continuous Drain Current				
T_C = +25°C	I_D	2	2	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-to-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	25	25	W
T_C > +25°C		0.2	0.2	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2883

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP2N08 MIN	LIMITS RFP2N08 MAX	LIMITS RFP2N10 MIN	LIMITS RFP2N10 MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	80	–	100	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V	–	1	–	–	μA
		V_{DS} = 80V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 65V	–	50	–	–	μA
		V_{DS} = 80V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.05	–	1.05	V
		I_D = 2A, V_{GS} = 10V	–	3.0	–	3.0	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.05	–	1.05	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse Transfer Capacitance	C_{RSS}		–	25	–	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 50V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	17 (typ)	25	17 (typ)	25	ns
Rise Time	t_r		30 (typ)	45	30 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		30 (typ)	45	30 (typ)	45	ns
Fall Time	t_f		17 (typ)	25	17 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP2N08 MIN	LIMITS RFP2N08 MAX	LIMITS RFP2N10 MIN	LIMITS RFP2N10 MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

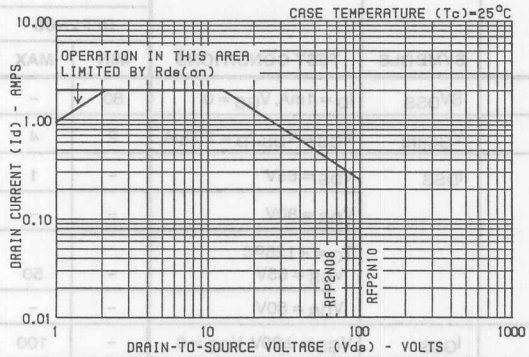


Fig. 1 - Maximum operating areas for all types.

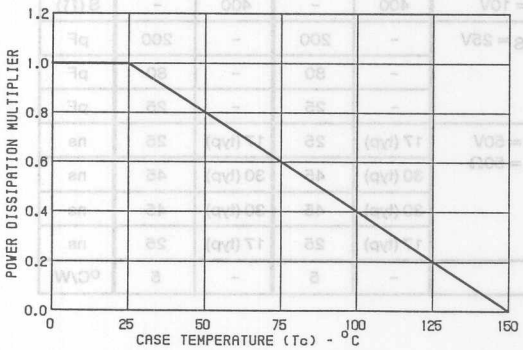


Fig. 2 - Normalized power dissipation vs. temperature derating curve

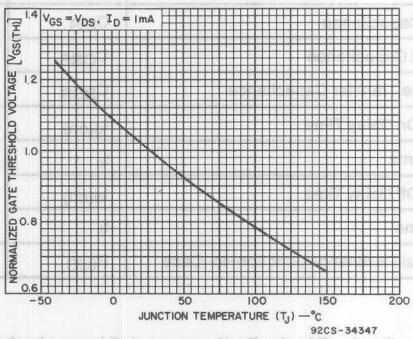


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

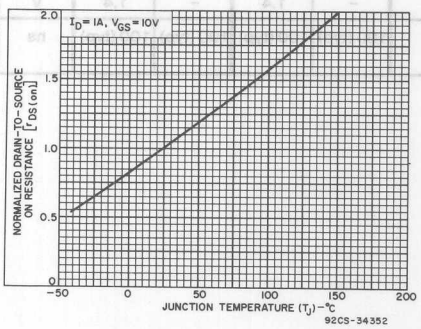


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

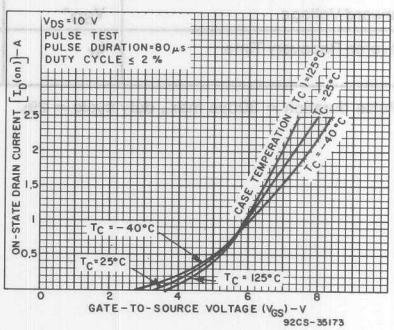


Fig. 5 - Typical transfer characteristics for all types.

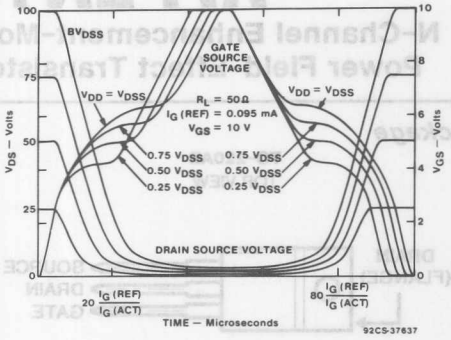


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

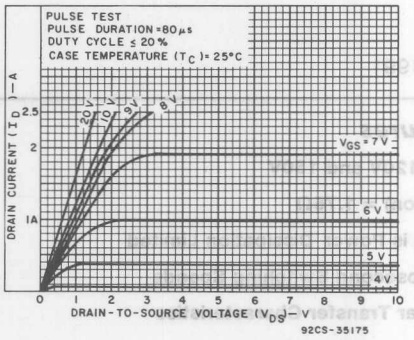


Fig. 7 - Typical saturation characteristics for all types.

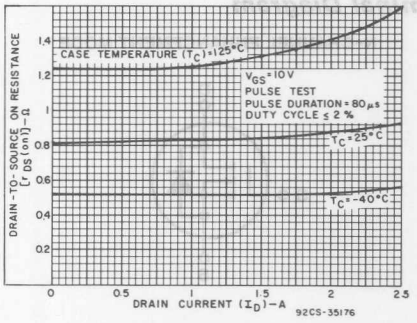


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

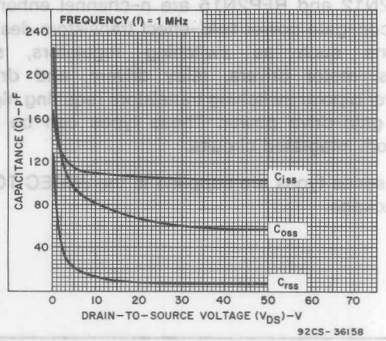


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

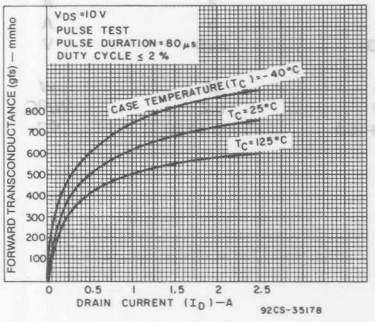


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

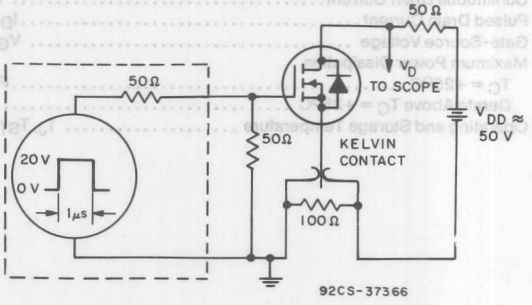


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFP2N12
RFP2N15

N-Channel Enhancement-Mode Power Field-Effect Transistors

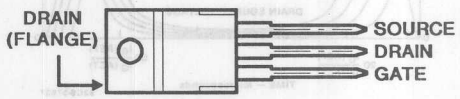
August 1991

Features

- 2A, 120V and 150V
- $r_{DS}(on) = 1.75\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-220AB
TOP VIEW



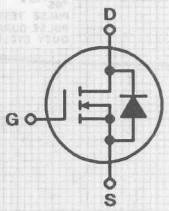
Description

The RFP2N12 and RFP2N15 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP2N12	RFP2N15	UNITS
Drain-Source Voltage	V_{DSS}	120	150	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	120	150	V
Continuous Drain Current	I_D	2	2	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	25	25	W
Derate Above T_C = +25°C		0.2	0.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2882

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP2N12 MIN	LIMITS RFP2N12 MAX	LIMITS RFP2N15 MIN	LIMITS RFP2N15 MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	120	–	150	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V	–	1	–	–	μA
		V_{DS} = 120V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 100V	–	50	–	–	μA
		V_{DS} = 120V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.75	–	1.75	V
		I_D = 2A, V_{GS} = 10V	–	6.0	–	6.0	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.75	–	1.75	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse-Transfer Capacitance	C_{RSS}		–	25	–	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 75V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	17 (typ)	25	17 (typ)	25	ns
Rise Time	t_r		30 (typ)	45	30 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		30 (typ)	45	30 (typ)	45	ns
Fall Time	t_f		17 (typ)	25	17 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP2N12 MIN	LIMITS RFP2N12 MAX	LIMITS RFP2N15 MIN	LIMITS RFP2N15 MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	150 (typ)	150 (typ)	150 (typ)	150 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

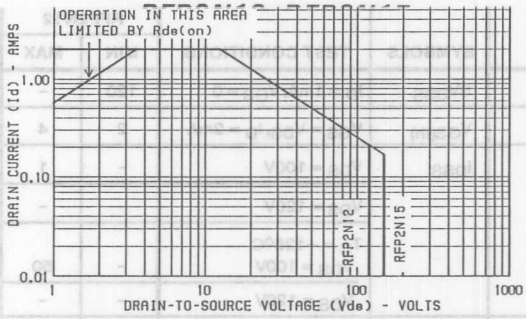


Fig. 1 — Maximum operating areas for all types.

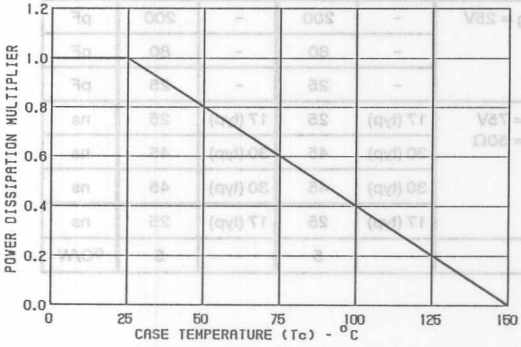


Fig. 2 – Normalized power dissipation vs temperature derating curve.

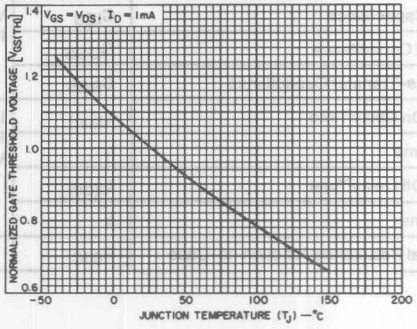


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

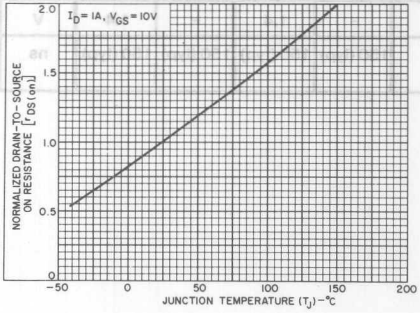


Fig. 4 – Normalized drain-to-source on resistance to junction temperature for all types.

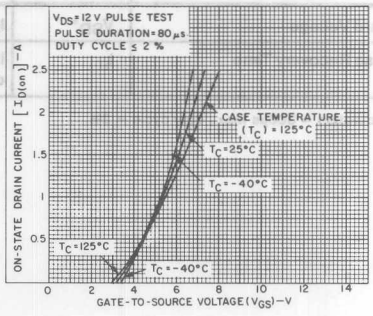


Fig. 5 — Typical transfer characteristics for all types.

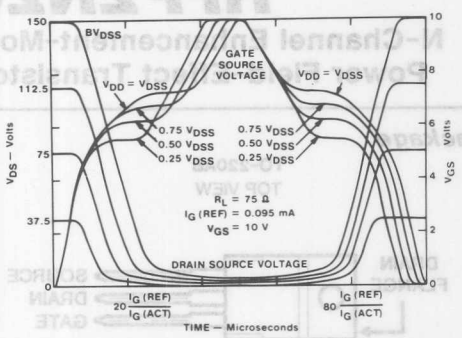


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

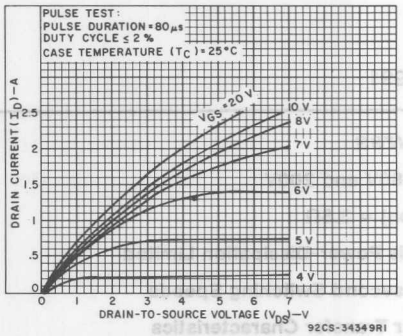


Fig. 7 — Typical saturation characteristics for all types.

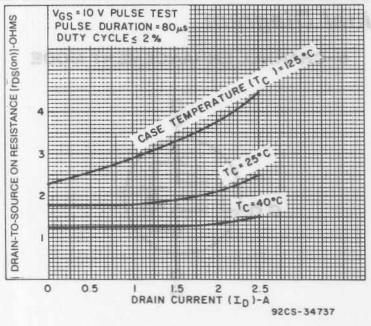


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

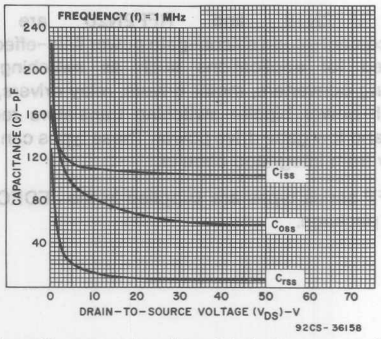


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

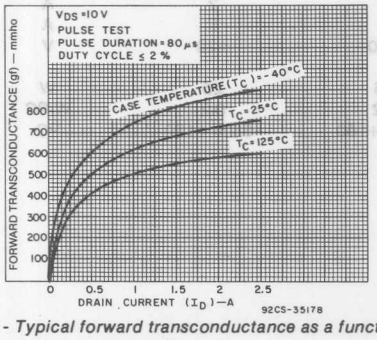


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

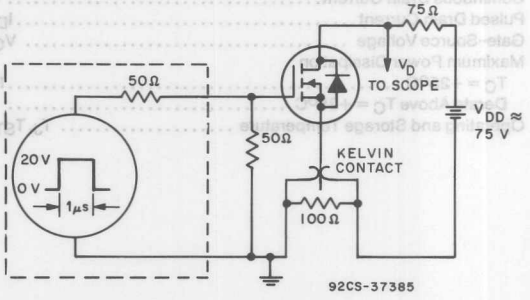


Fig. 11 — Switching Time Test Circuit.

4 N-CHANNEL POWER MOSFETs

HARRIS

RFP2N18
RFP2N20

N-Channel Enhancement-Mode Power Field-Effect Transistors

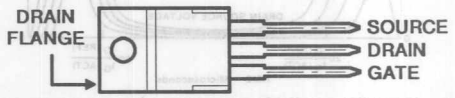
August 1991

Features

- 2A, 180V and 200V
- $r_{DS}(on) = 3.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-220AB
TOP VIEW



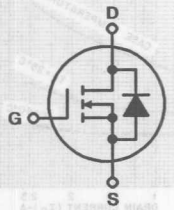
Description

The RFP2N18 and RFP2N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP2N18	RFP2N20	UNITS
Drain-Source Voltage	V_{DSS}	180	200	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	180	200	V
Continuous Drain Current	I_D	2	2	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	25	25	W
Derate Above T_C = +25°C		0.2	0.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2881

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP2N18 MIN	LIMITS RFP2N18 MAX	LIMITS RFP2N20 MIN	LIMITS RFP2N20 MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	180	–	200	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145V	–	1	–	–	μA
		V_{DS} = 160V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 145V	–	50	–	–	μA
		V_{DS} = 160V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	3.5	–	3.5	V
		I_D = 2A, V_{GS} = 10V	–	8.0	–	8.0	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	3.5	–	3.5	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	60	–	60	pF
Reverse-Transfer Capacitance	C_{RSS}		–	25	–	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 100V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	15 (typ)	25	15 (typ)	25	ns
Rise Time	t_r		20 (typ)	30	20 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		25 (typ)	40	25 (typ)	40	ns
Fall Time	t_f		15 (typ)	25	15 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP2N18 MIN	LIMITS RFP2N18 MAX	LIMITS RFP2N20 MIN	LIMITS RFP2N20 MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	200 (typ)	200 (typ)	200 (typ)	200 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

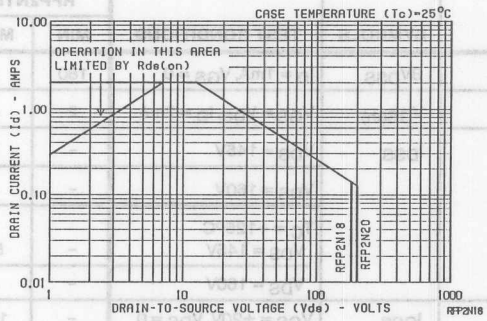


Fig. 1 - Maximum operating areas for all types.

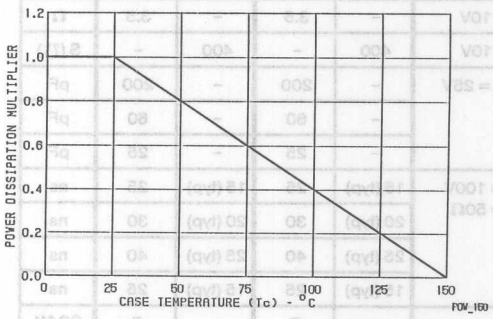


Fig. 2 – Normalized power dissipation vs temperature derating curve.

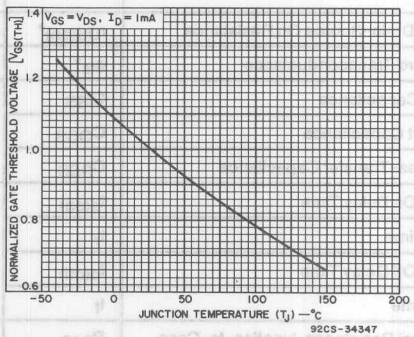


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

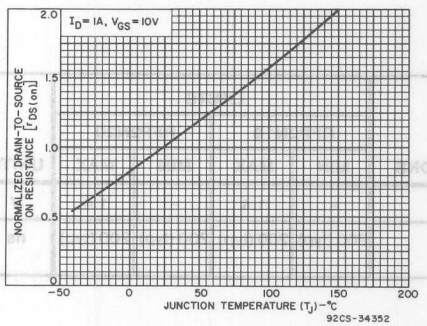


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

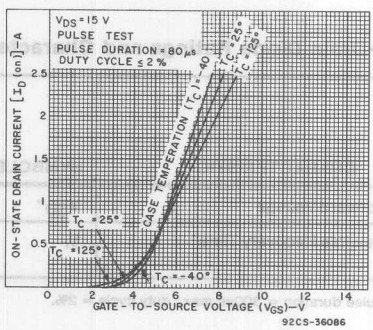


Fig. 5 - Typical transfer characteristics for all types.

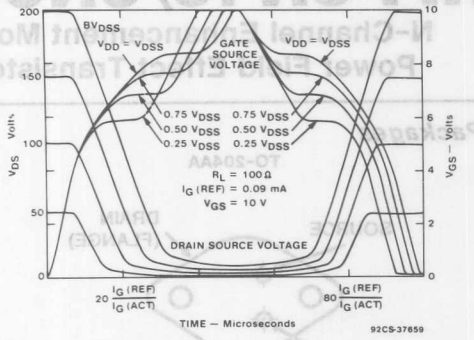


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

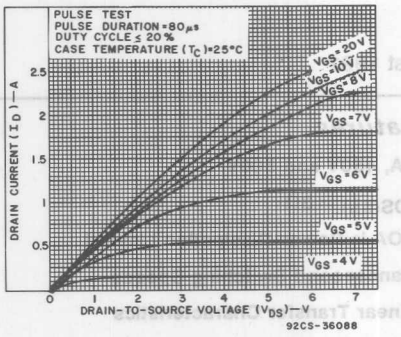


Fig. 7 - Typical saturation characteristics for all types.

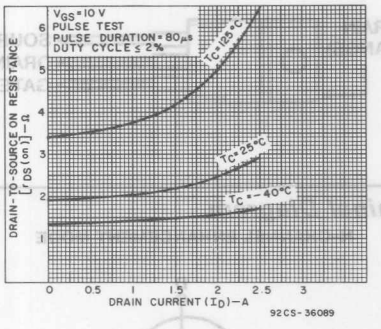


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

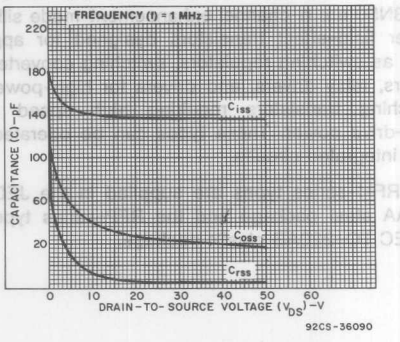


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

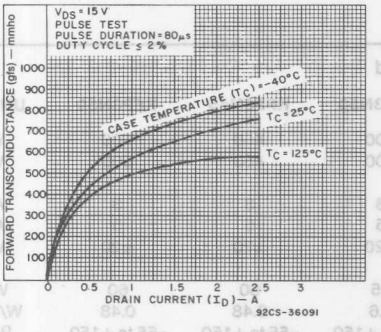


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

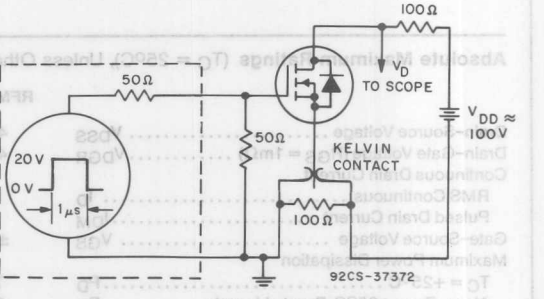


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFM3N45/3N50
RFP3N45/3N50

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 3A, 450V and 500V
- $r_{DS(on)} = 3\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

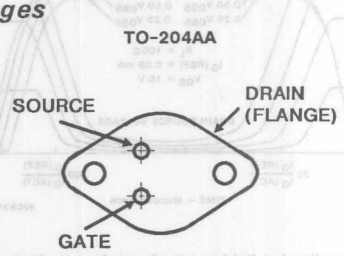
Description

The RFM3N45 and RFM3N50 and the RFP3N45 and RFP3N50 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

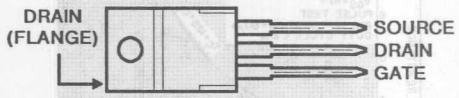
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA

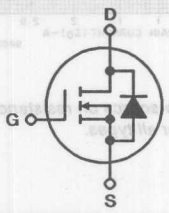


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM3N45	RFM3N50	RFP3N45	RFP3N50	UNITS
Drain-Source Voltage ..... V_{DSS}	450	500	450	500	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	450	500	450	500	V
Continuous Drain Current					
RMS Continuous ..... I_D	3	3	3	3	A
Pulsed Drain Current ..... I_{DM}	5	5	5	5	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly ..... P_D	0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1384.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM3N45 RFP3N45		RFM3N50 RFP3N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS}=0	450	—	500	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=360 V	—	10	—	—	μA
		V_{DS}=400 V	—	—	—	10	
		T_C=125°C V_{DS}=360 V	—	50	—	—	
		V_{DS}=400 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm$20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1.5 A V_{GS}=10 V	—	4.5	—	4.5	V
		I_D=3 A V_{GS}=10 V	—	10.5	—	10.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1.5 A V_{GS}=10 V	—	3	—	3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=1.5 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	750	—	750	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	150	—	150	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD}=250 V	30(Typ)	45	30(Typ)	45	ns
Rise Time	t_r	I_D=1.5 A	40(Typ)	60	40(Typ)	60	
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=R_{gs}$=50 Ω	90(Typ)	135	90(Typ)	135	
Fall Time	t_f	V_{GS}=10 V	50(Typ)	75	50(Typ)	75	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM3N45, RFM3N50	—	1.67	—	1.67	°C/W
		RFP3N45, RFP3N50	—	2.083	—	2.083	

[a] Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM3N45 RFP3N45		RFM3N50 RFP3N50		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=1.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	800(typ)		800(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

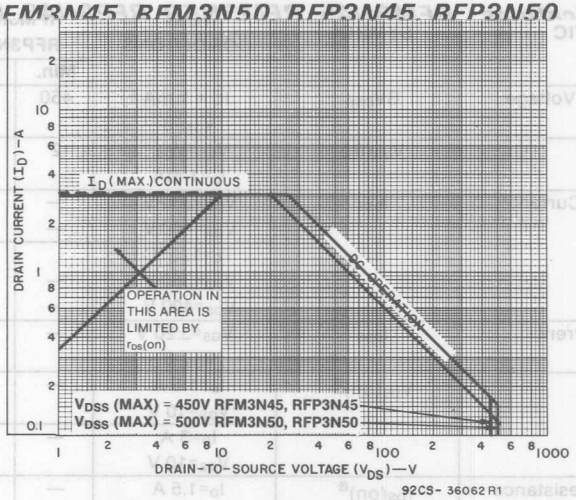


Fig. 1 - Maximum operating areas for all types.

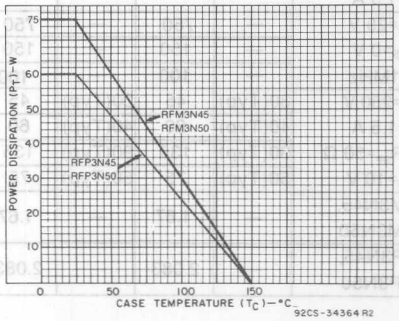


Fig. 2 - Power dissipation vs. temperature derating curve for all types.



Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

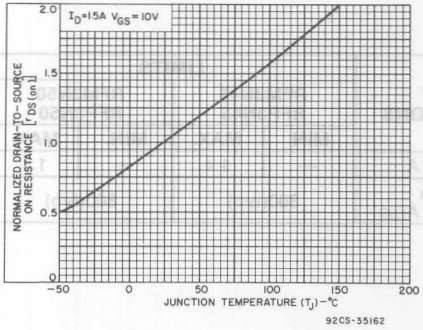


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

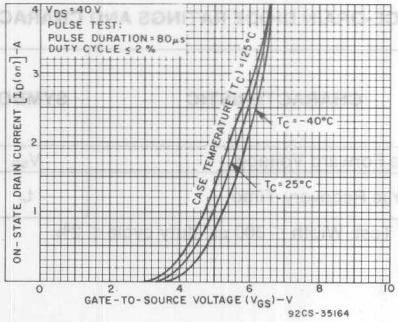


Fig. 5 - Typical transfer characteristics for all types

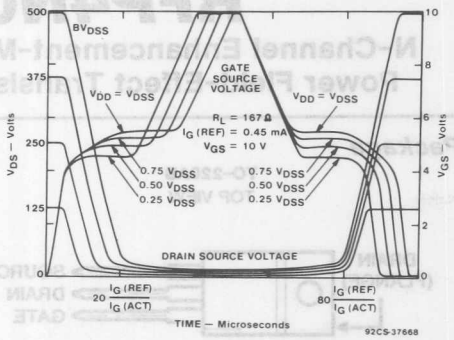


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

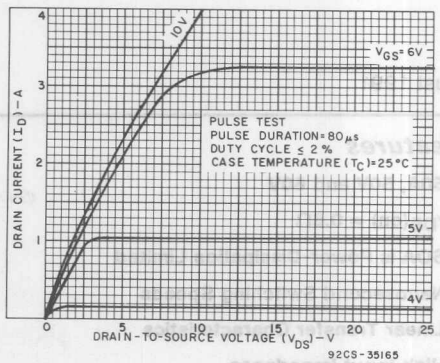


Fig. 7 - Typical saturation characteristics for all types.

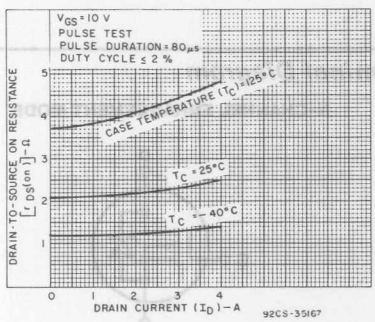


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

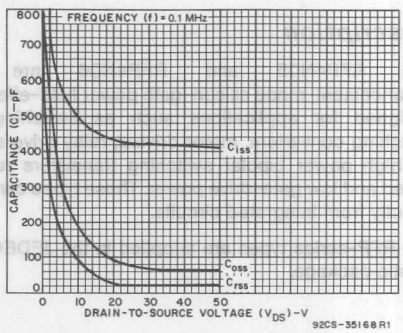


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

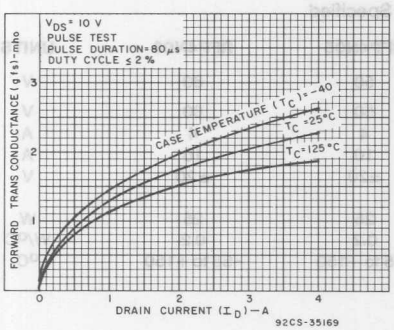


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

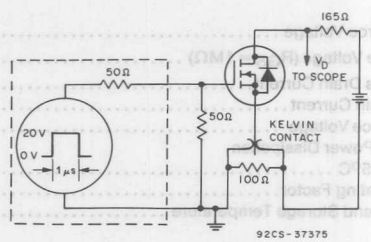


Fig. 11 — Switching Time Test Circuit

HARRIS

RFP4N05
RFP4N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

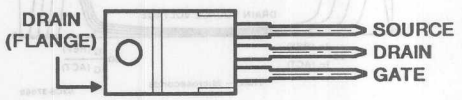
August 1991

Features

- 50A, 50V and 60V
- $r_{DS}(on) = 0.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-220AB
TOP VIEW



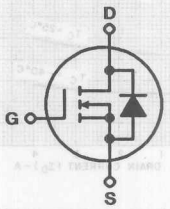
Description

The RFP4N05 and RFP4N06 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP-series types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP4N05	RFP4N06	UNITS
Drain-Source Voltage	V_{DSS}	50	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	60	V
Continuous Drain Current	I_D	4	4	A
Pulsed Drain Current	I_{DM}	10	10	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	25	25	W
Linear Derating Factor		0.2	0.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2880

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP4N05 MIN	LIMITS RFP4N05 MAX	LIMITS RFP4N06 MIN	LIMITS RFP4N06 MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	50	–	60	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V	–	1	–	–	μA
		V_{DS} = 50V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 40V	–	50	–	–	μA
		V_{DS} = 50V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	0.8	–	0.8	V
		I_D = 2A, V_{GS} = 10V	–	2.0	–	2.0	V
		I_D = 4A, V_{GS} = 10V	–	4.8	–	4.8	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	0.8	–	0.8	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	85	–	85	pF
Reverse-Transfer Capacitance	C_{RSS}		–	30	–	30	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 30V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	6 (typ)	15	6 (typ)	15	ns
Rise Time	t_r		14 (typ)	30	14 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		16 (typ)	30	16 (typ)	30	ns
Fall Time	t_f		14 (typ)	25	14 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP4N05 MIN	LIMITS RFP4N05 MAX	LIMITS RFP4N06 MIN	LIMITS RFP4N06 MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulsed: Pulse duration ≤ 300μs max., duty cycle ≤ 2%.

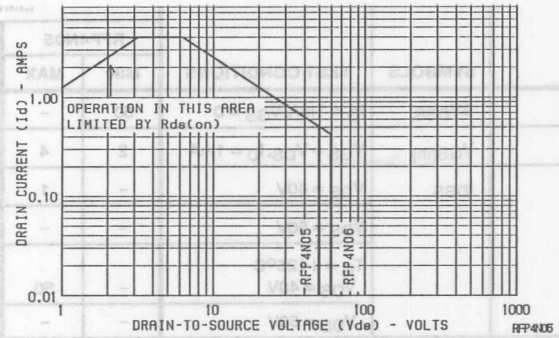


Fig. 1 — Maximum operating areas for all types.

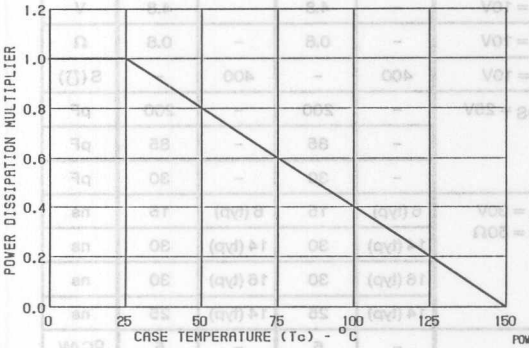


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

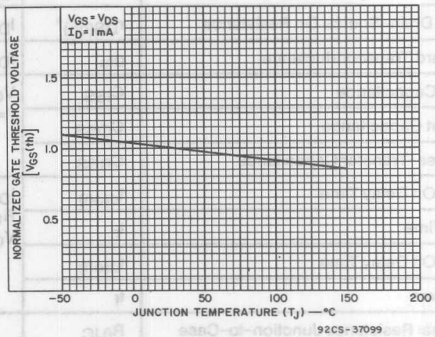


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

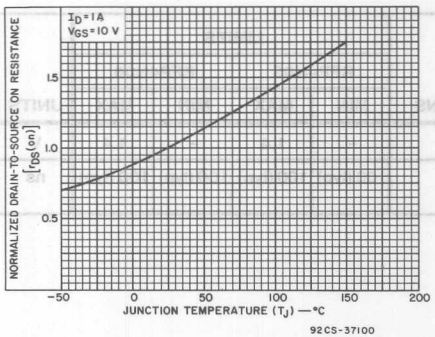


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

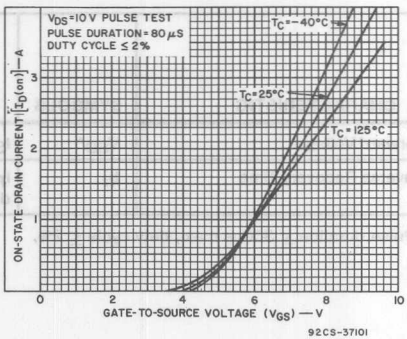


Fig. 5 — Typical transfer characteristics for all types.

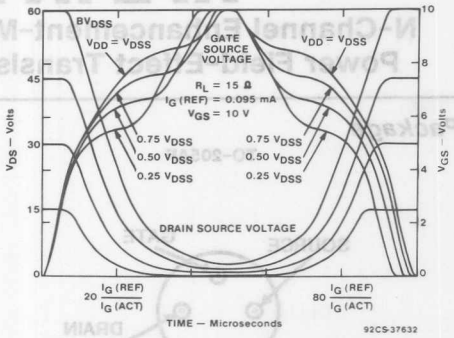


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

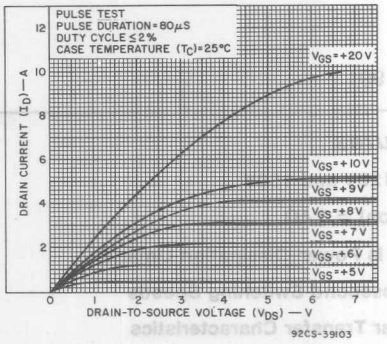


Fig. 7 — Typical saturation characteristics for all types.

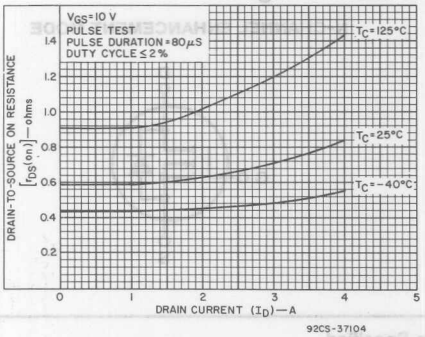


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

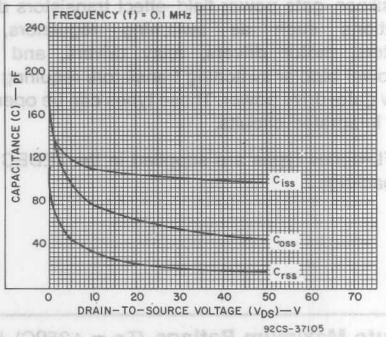


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types

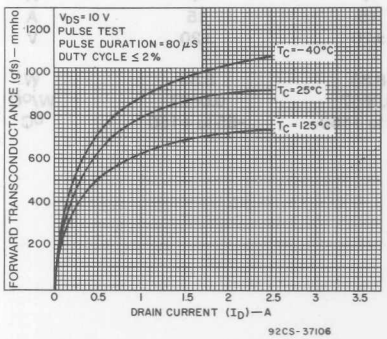


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

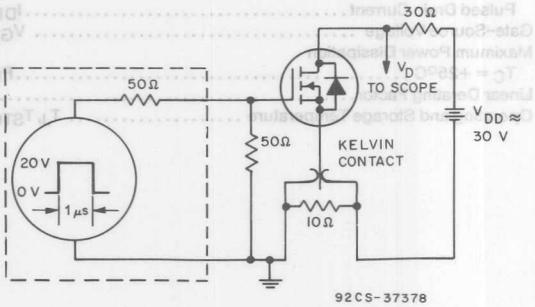


Fig. 11 — Switching Time Test Circuit

HARRIS

RFL4N12
RFL4N15

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 4A, 120V and 150V
- $r_{DS}(on) = 0.4\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

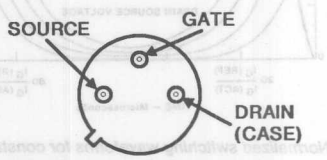
Description

The RFL4N12 and RFL4N15 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package.

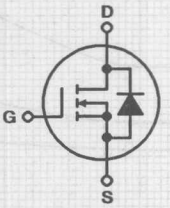
Package

TO-205AF



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFL4N12	RFL4N15	UNITS
Drain-Source Voltage	V_{DSS}	120	150	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	120	150	V
Continuous Drain Current				
T_C = +25°C	I_D	4	4	A
Pulsed Drain Current	I_{DM}	15	15	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	8.33	8.33	W
Linear Derating Factor		0.0667	0.0667	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1462.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL4N12		RFL4N15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	150	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V	—	1	—	—	μA
		V_{DS}=120 V	—	—	—	1	
		T_C=125°C V_{DS}=100 V	—	50	—	—	
		V_{DS}=120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	0.8	—	0.8	V
		I_D=4 A V_{GS}=10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	0.40	—	0.40	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=2 A	1.5	—	1.5	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	850	—	850	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	230	—	230	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 75 V	40(typ)	60	40(typ)	60	ns
Rise Time	t_r	I_D=2 A	165(typ)	250	165(typ)	250	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	90(typ)	135	90(typ)	135	
Fall Time	t_f	V_{GS}=10 V	90(typ)	135	90(typ)	135	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL4N12, RFL4N15	—	15	—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL4N12		RFL4N15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 2A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	200(typ.)		200(typ.)		ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

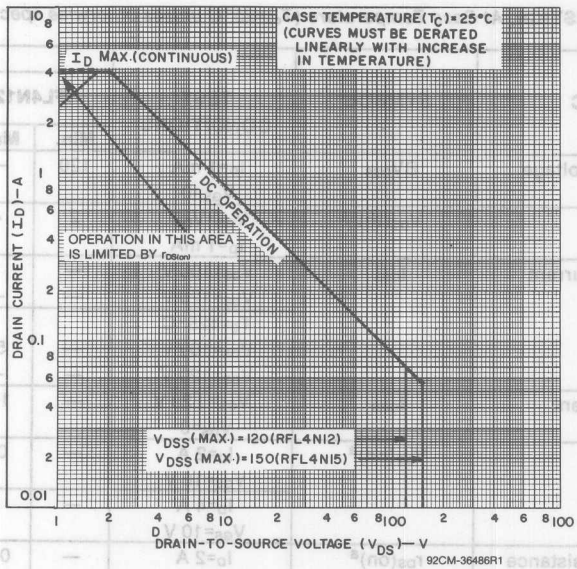


Fig. 1 - Maximum safe operating areas for all types.

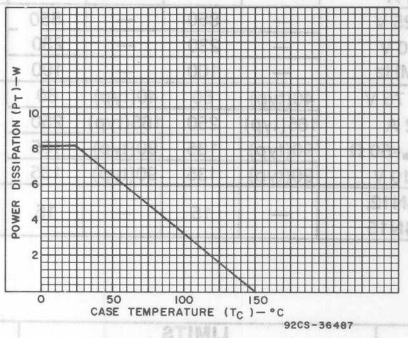


Fig. 2 - Power vs. temperature derating curve for all types.

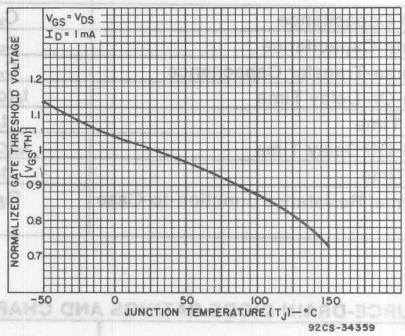


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

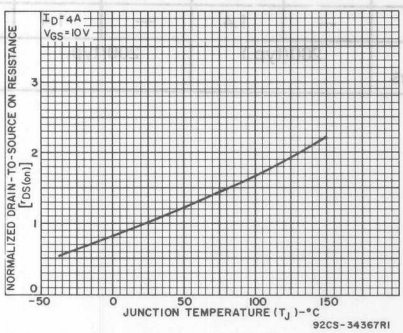


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

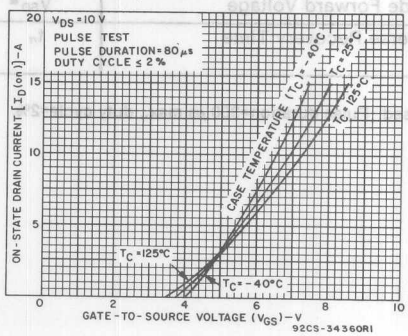


Fig. 5 - Typical transfer characteristics for all types.

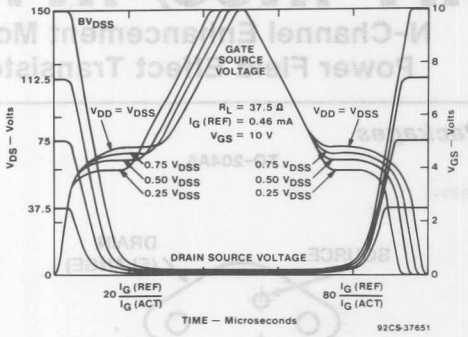


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

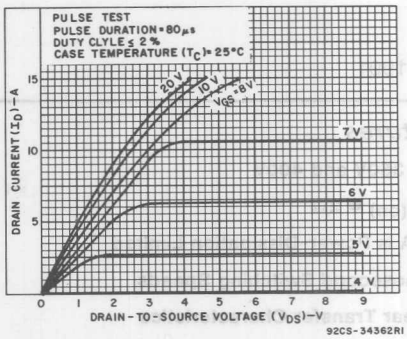


Fig. 7 - Typical saturation characteristics for all types.

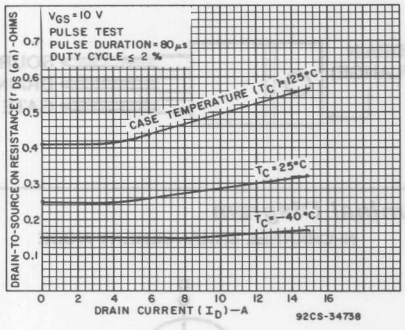


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

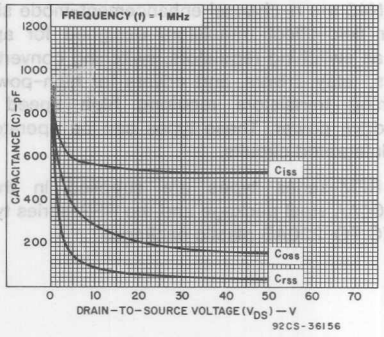


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

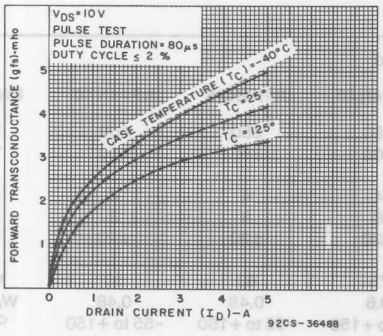


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

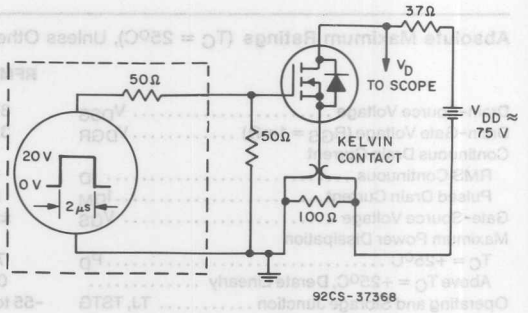


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFM4N35/4N40
RFP4N35/4N40

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 4A, 350V and 400V
- $r_{DS(on)} = 2\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

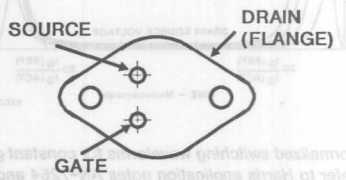
Description

The RFM4N35 and RFM4N40 and the RFP4N35 and RFP4N40 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

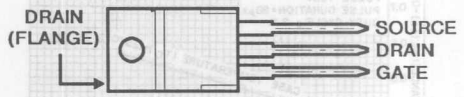
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA

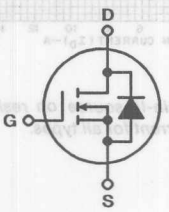


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM4N35	RFM4N40	RFP4N35	RFP4N40	UNITS
Drain-Source Voltage ..... V_{DSS}	350	400	350	400	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	350	400	350	400	V
Continuous Drain Current					
RMS Continuous ..... I_D	4	4	4	4	A
Pulsed Drain Current ..... I_{DM}	8	8	8	8	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1491.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) 25°C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM4N35 RFP4N35		RFM4N40 RFP4N40		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=280 V V_{DS}=320 V	— —	10 —	— —	— 10	μA
		T_C=125°C V_{DS}=280 V V_{DS}=320 V	— —	100 —	— —	— 100	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm$20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	4	—	4	V
		I_D=4 A V_{GS}=10 V	—	12	—	12	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	2	—	2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=2 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1 MHz	—	750	—	750	pF
Output Capacitance	C_{oss}		—	150	—	150	pF
Reverse Transfer Capacitance	C_{rss}		—	100	—	100	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=200 V I_D=2 A $R_{gen}=R_{gs}$=50 Ω V_{GS}=10 V	12(typ)	45	12(typ)	45	ns
Rise Time	t_r		42(typ)	60	42(typ)	60	ns
Turn-Off Delay Time	$t_d(off)$		130(typ)	200	130(typ)	200	ns
Fall Time	t_f		62(typ)	100	62(typ)	100	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM4N35, RFM4N40	—	1.67	—	1.67	°C/W
		RFP4N35, RFP4N40	—	2.083	—	2.083	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM4N35 RFP4N35		RFM4N40 RFP4N40		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD} [a]	I_{SD}=2 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	800(typ)		800(typ)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

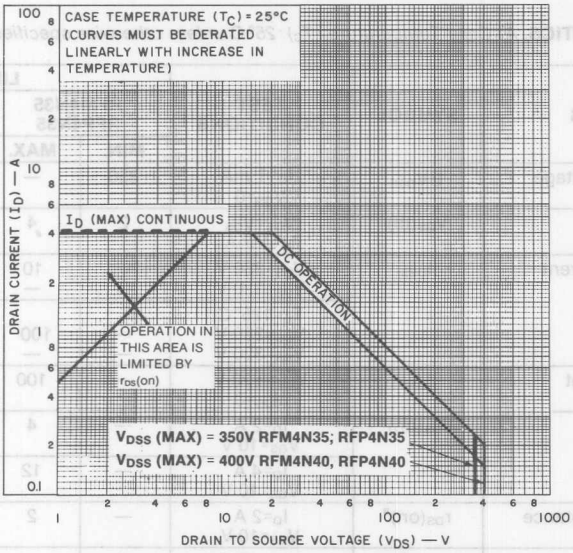


Fig. 1 — Maximum operating areas for all types.

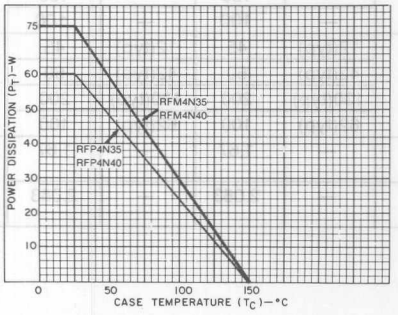


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

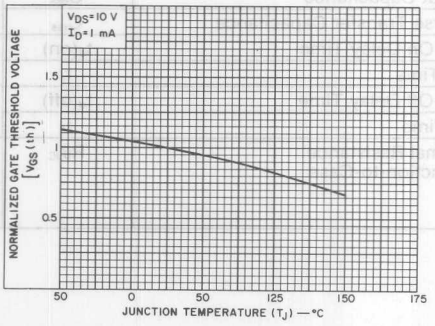


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

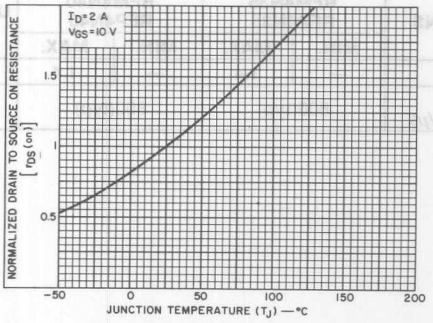


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

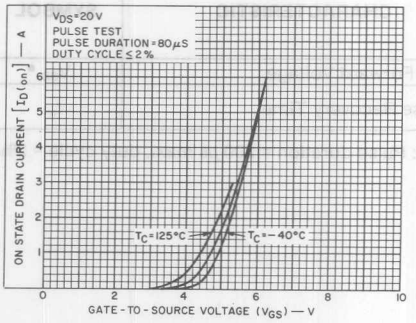


Fig. 5 — Typical transfer characteristics for all types.

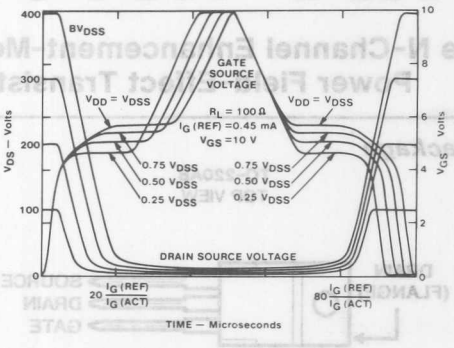


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

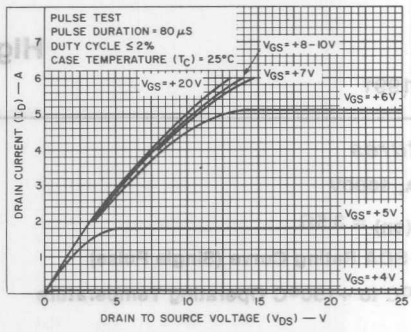


Fig. 7 — Typical saturation characteristics for all types.

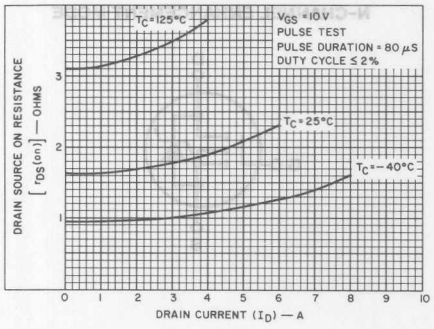


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

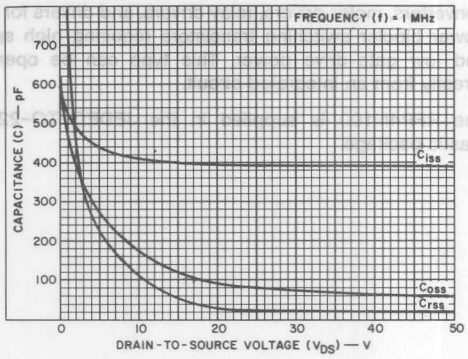


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

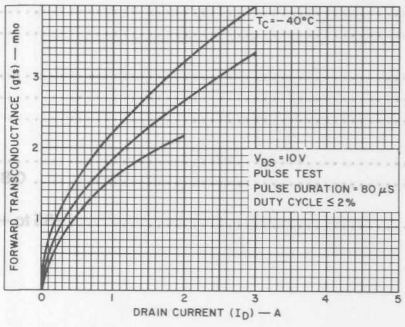


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

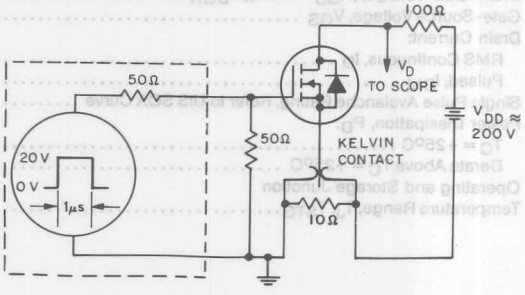


Fig. 11 — Switching Time Test Circuit

HARRIS

RFP4N100

High Voltage N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 4.3A, 1000V
- $r_{DS(on)} = 3.5\Omega$
- UIS SOA Rating Curve (Single Pulse)
- -55°C to +150°C Operating Temperature

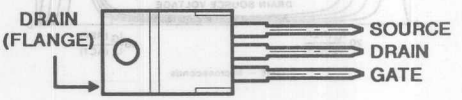
Description

The RFP4N100 is an n-channel enhancement mode silicon-gate power field effect transistor. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The RFP4N100 is supplied in the JEDEC TO-220AB plastic package.

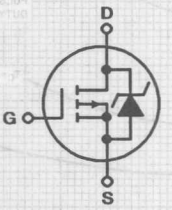
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS}	1000V
Drain-Gate Voltage, (R_{GS} = 1mΩ), V_{DGR}	1000V
Gate-Source Voltage, V_{GS}	±20V
Drain Current:	
RMS Continuous, I_D	4.3A
Pulsed, I_{DM}	17A
Single Pulse Avalanche Rating, Refer to UIS SOA Curve	490mJ
Power Dissipation, P_D:	
T_C = +25°C	150W
Derate Above T_C = +25°C	0.83W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55 to +150°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

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File Number **2457.1**

Electrical Characteristics (T_C = 25°C), Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V	1000	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA	2.0	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0V	–		μA
		V_{DS} = 1000V T_C = 25°C	–	250	μA
		V_{DS} = 800V T_C = 150°C	–	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V	–	±500	nA
On Resistance	$r_{DS(ON)}$	I_D = 2.5A, V_{GS} = 10V	–	3.5	Ω
Forward Transconductance	g_{fs}	I_D = 2.5A, V_{DS} = 100V	3.5	–	S (℧)
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 500V, I = 3.9A	–	30	ns
Rise Time	t_r	R_G = 9.1Ω	–	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$	R_D = 120Ω	–	170	ns
Fall Time	t_f	See Figure 14	–	50	ns
Total Gate Charge	Q_g	I_D = 3.9A, V_{DS} = 800V, V_{GS} = 10V	–	120	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		–	0.83	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$		–	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Forward Voltage	V_{SD}	I_{SD} = 4.3A	–	1.8	V
Reverse Recovery Time	t_{rr}	I_F = 3.9A, d_{IF}/dT = 100 A/μs	–	1000	ns

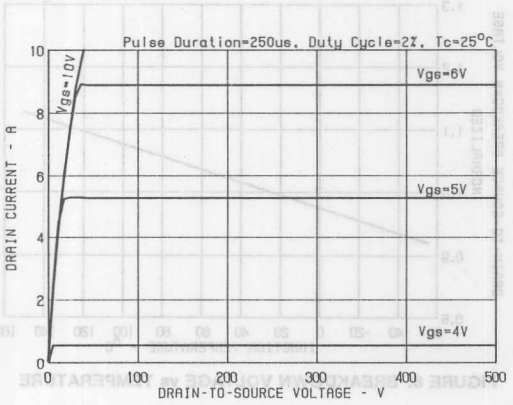


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

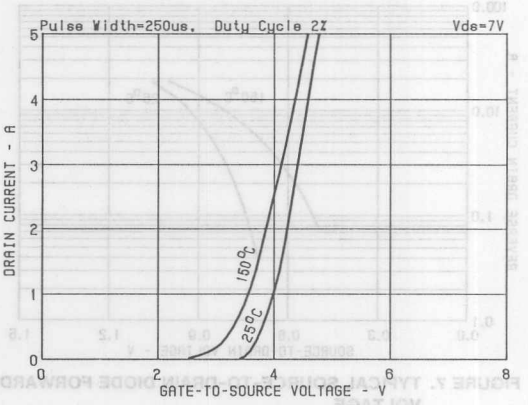


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

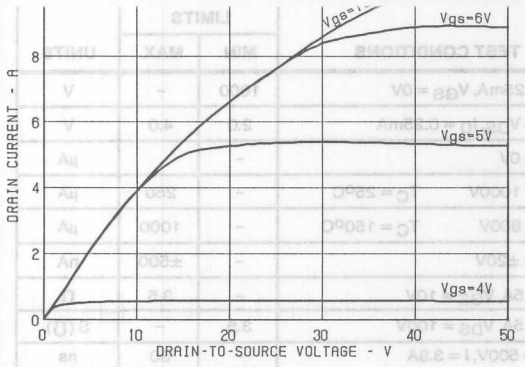


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

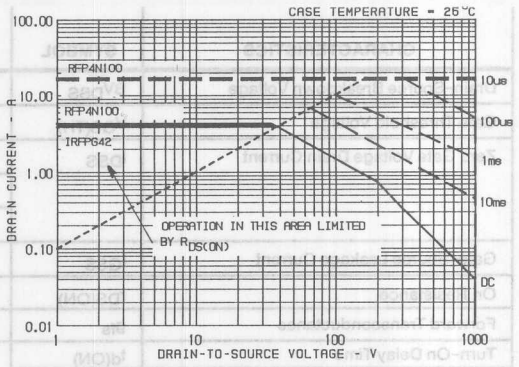


FIGURE 4. MAXIMUM SAFE OPERATING AREA

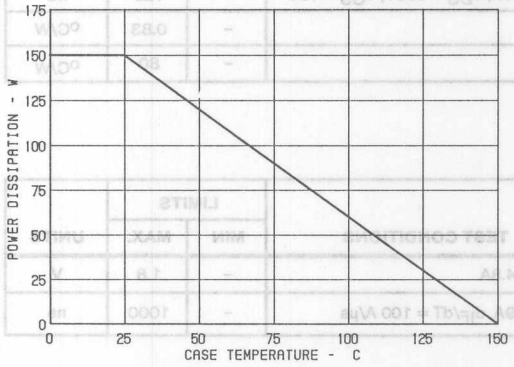


FIGURE 5. POWER vs. TEMPERATURE DERATING CURVE

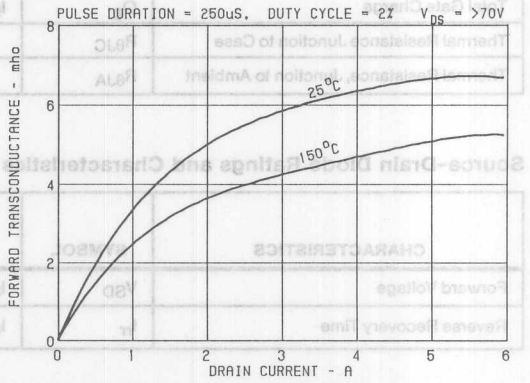


FIGURE 6. TYPICAL FORWARD TRANSCONDUCTANCE

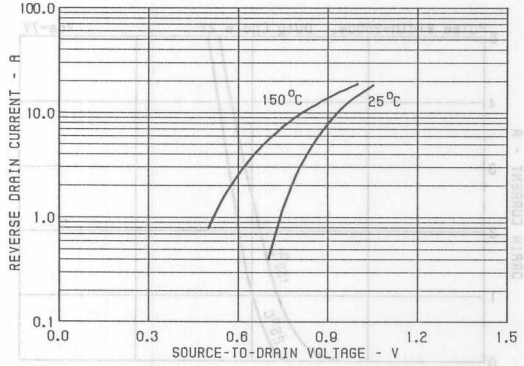


FIGURE 7. TYPICAL SOURCE-TO-DRAIN DIODE FORWARD VOLTAGE

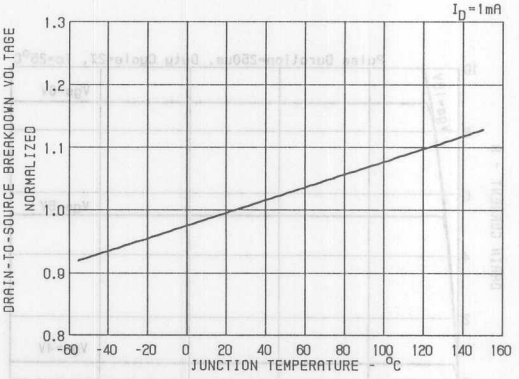


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

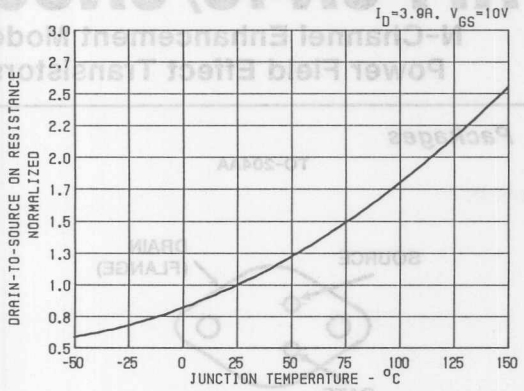


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE ON RESISTANCE

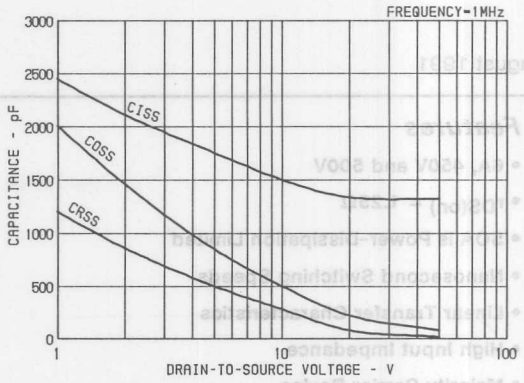


FIGURE 10. TYPICAL CAPACITANCE vs VOLTAGE

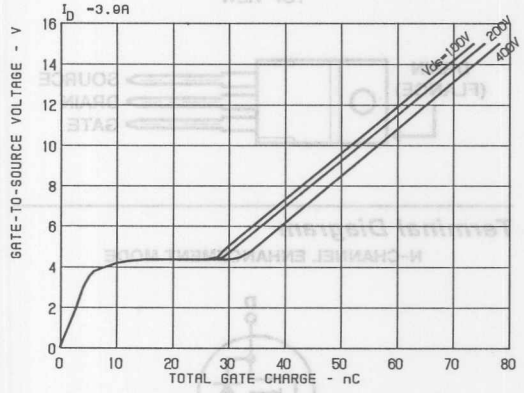


FIGURE 11. TYPICAL GATE CHARGE

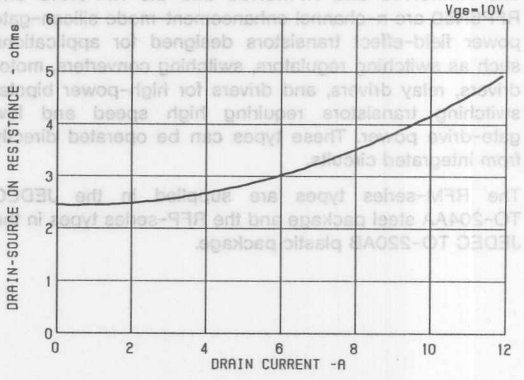


FIGURE 12. TYPICAL DRAIN-SOURCE ON RESISTANCE

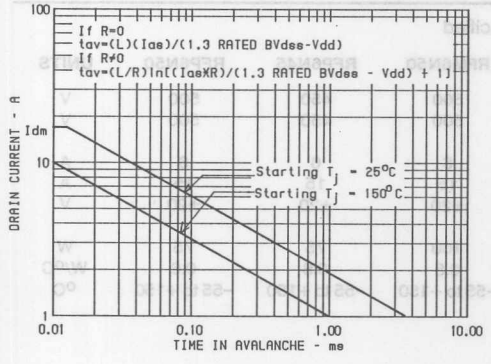


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING SOA

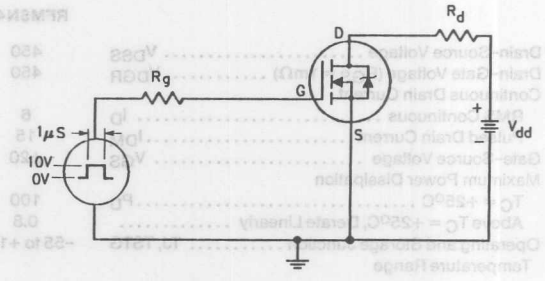


FIGURE 14. SWITCHING TIME TEST CIRCUIT

HARRIS

RFM6N45/6N50
RFP6N45/6N50

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 6A, 450V and 500V
- $r_{DS(on)} = 1.25\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

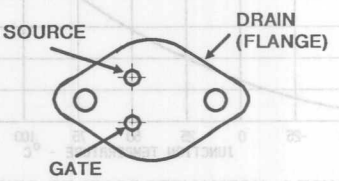
Description

The RFM6N45 and RFM6N50 and the RFP6N45 and RFP6N50 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

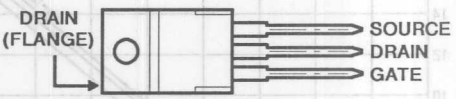
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA

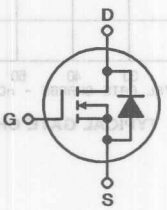


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM6N45	RFM6N50	RFP6N45	RFP6N50	UNITS
Drain-Source Voltage ..... V_{DSS}	450	500	450	500	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	450	500	450	500	V
Continuous Drain Current					
RMS Continuous ..... I_D	6	6	6	6	A
Pulsed Drain Current ..... I_{DM}	15	15	15	15	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	100	100	75	75	W
Above $T_C = +25^oC$, Derate Linearly	0.8	0.8	0.6	0.6	W/°C
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1494.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6N45 RFP6N45		RFM6N50 RFP6N50		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	450	—	500	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=360 V V_{DS}=400 V	— —	10 —	— —	— 10	μA
		T_C=125° C V_{DS}=360 V V_{DS}=400 V	— —	50 —	— —	— 50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=3 A V_{GS}=10 V	—	3.75	—	3.75	V
		I_D=6 A V_{GS}=10 V	—	12	—	12	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=3 A V_{GS}=10 V	—	1.25	—	1.25	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=3 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	1500	—	1500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	250	—	250	
Reverse Transfer Capacitance	C_{rss}	f=1 MHz	—	200	—	200	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 250 V	15(typ)	45	15(typ)	45	ns
Rise Time	t_r	I_D=3 A	40(typ)	80	40(typ)	80	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	190(typ)	300	190(typ)	300	
Fall Time	t_f	V_{GS}=10 V	60(typ)	100	60(typ)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM6N45, RFM6N50	—	1.25	—	1.25	°C/W
		RFP6N45, RFP6N50	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6N45 RFP6N45		RFM6N50 RFP6N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 3A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	800(typ.)		800(typ.)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

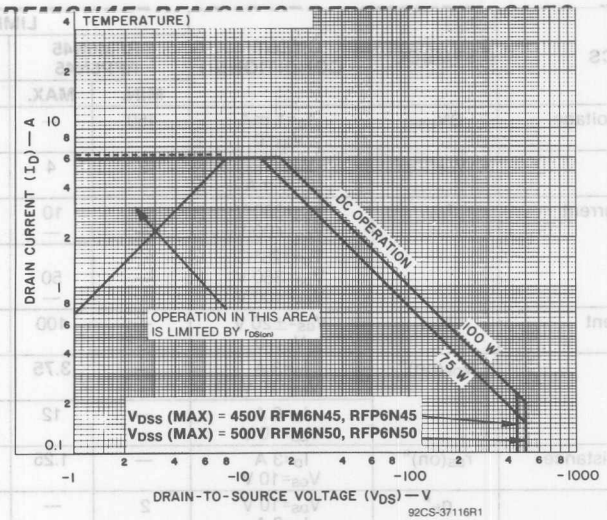


Fig. 1 — Maximum operating areas for all types.

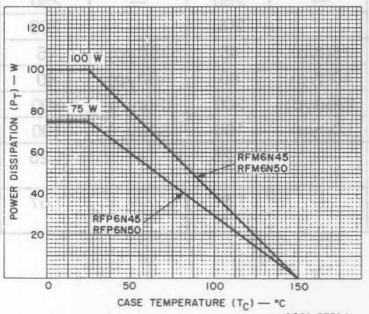


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

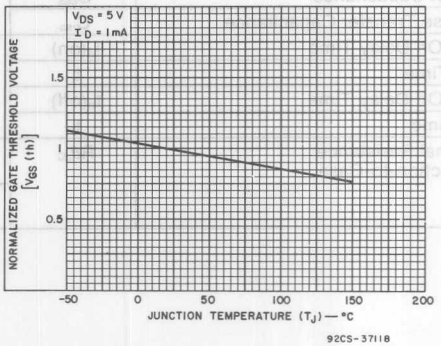


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

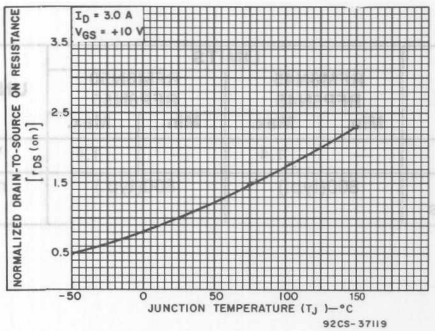


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

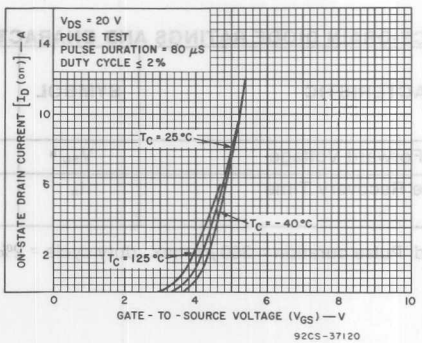


Fig. 5 — Typical transfer characteristics for all types.

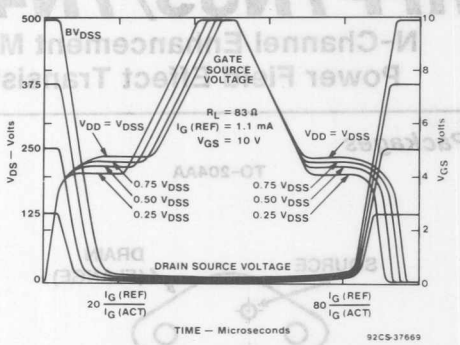


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

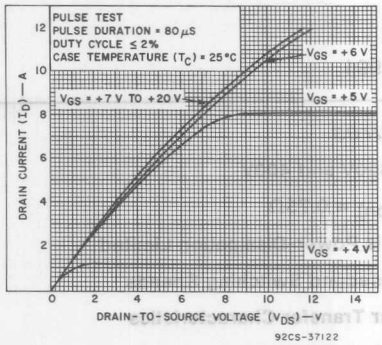


Fig. 7 — Typical saturation characteristics for all types.

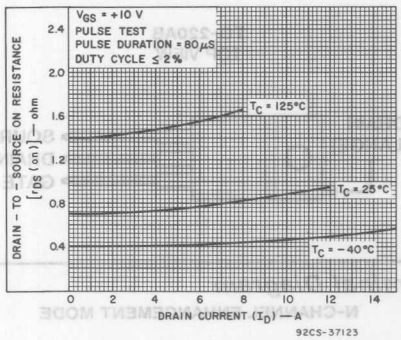


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

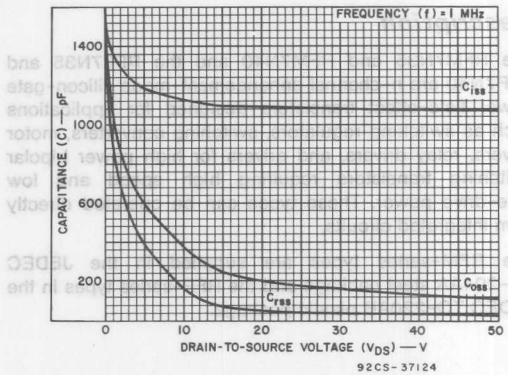


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

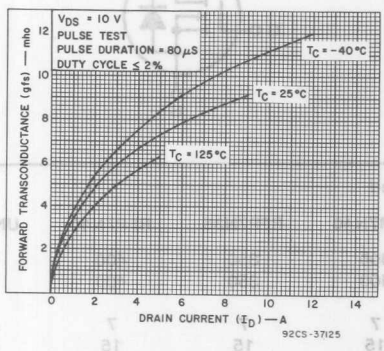


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

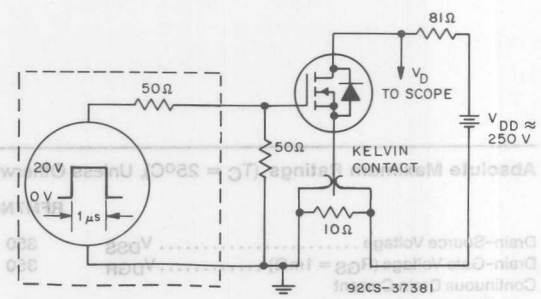


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFM7N35/7N40
RFP7N35/7N40

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 7A, 350V and 400V
- $r_{DS(on)} = 0.75\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

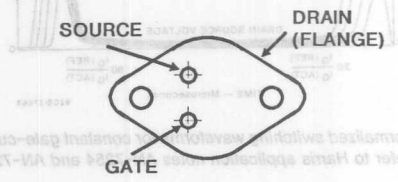
Description

The RFM7N35 and RFM7N40 and the RFP7N35 and RFP7N40 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

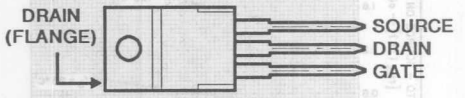
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA



TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM7N35	RFM7N40	RFP7N35	RFP7N40	UNITS
Drain-Source Voltage ..... V_{DSS}	350	400	350	400	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	350	400	350	400	V
Continuous Drain Current					
RMS Continuous ..... I_D	7	7	7	7	A
Pulsed Drain Current ..... I_{DM}	15	15	15	15	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	100	100	75	75	W
Above $T_C = +25^oC$, Derate Linearly	0.8	0.8	0.6	0.6	W/^{o}C
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1536.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM7N35 RFP7N35		RFM7N40 RFP7N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	350	—	400	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=280 V	—	1	—	—	μA
		V_{DS}=320 V	—	—	—	1	
		T_C=125° C V_{DS}=280 V	—	50	—	—	
		V_{DS}=320 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=3.5 A V_{GS}=10 V	—	2.63	—	2.63	V
		I_D=7 A V_{GS}=10 V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=3.5 A V_{GS}=10 V	—	0.75	—	0.75	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=3.5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f= 1 MHz	—	1600	—	1600	pF
Output Capacitance	C_{oss}		—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}		—	200	—	200	
Turn-On Delay Time	$t_d(on)$	V_{DS}=200 V I_D=3.5 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	16(typ)	45	16(typ)	45	ns
Rise Time	t_r		54(typ)	75	54(typ)	75	
Turn-Off Delay Time	$t_d(off)$		170(typ)	250	170(typ)	250	
Fall Time	t_f		62(typ)	100	62(typ)	100	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM7N35, RFM7N40	—	1.25	—	1.25	°C/W
		RFP7N35, RFP7N40	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM7N35 RFP7N35		RFM7N40 RFP7N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD}=3.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A di_F/dt=100 A/μs	870 (typ)				ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

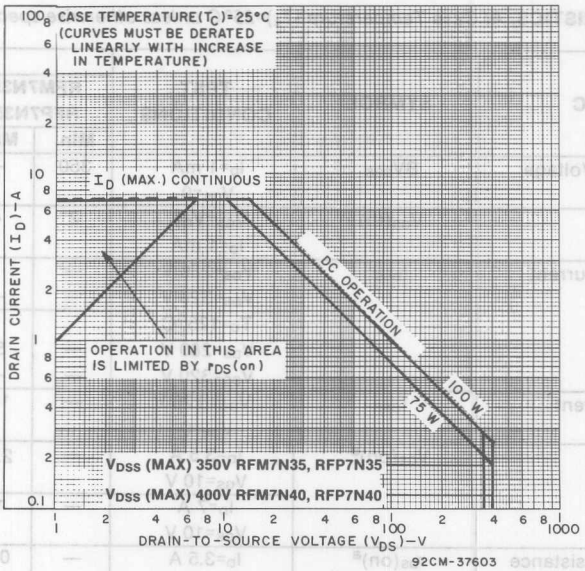


Fig. 1 - Maximum safe operating areas for all types.

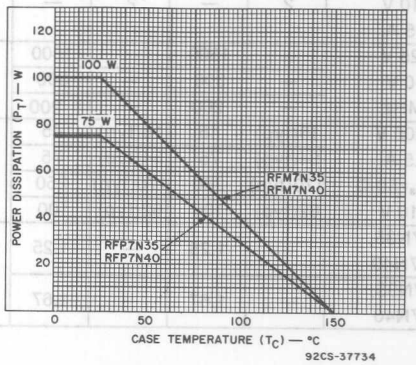


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

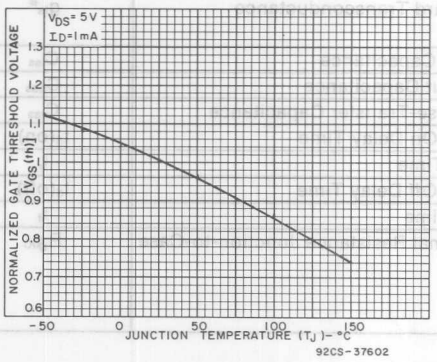


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

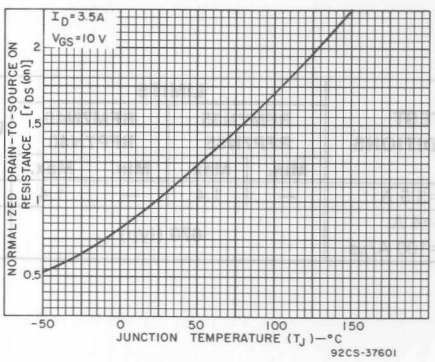


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

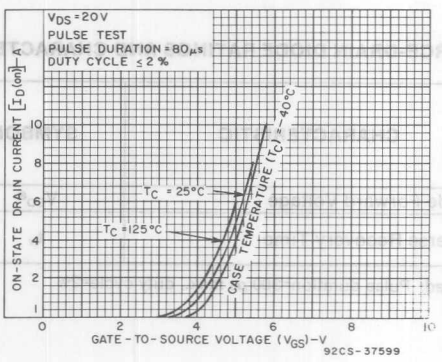


Fig. 5 - Typical transfer characteristics for all types.

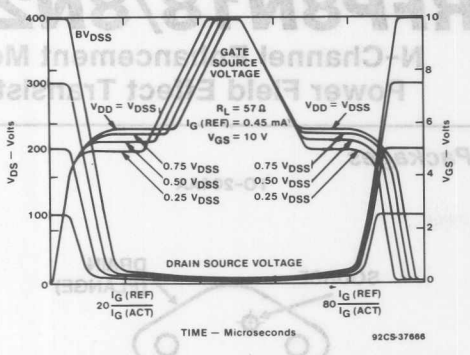


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

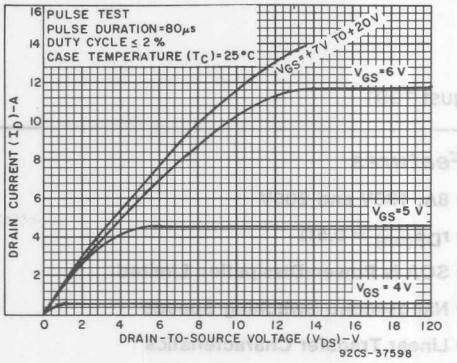


Fig. 7 - Typical saturation characteristics for all types.

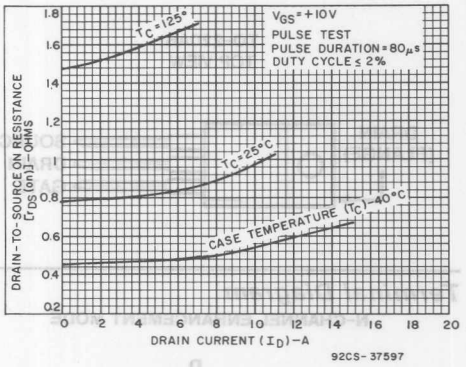


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

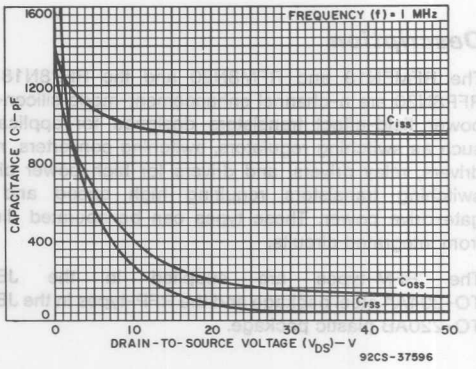


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

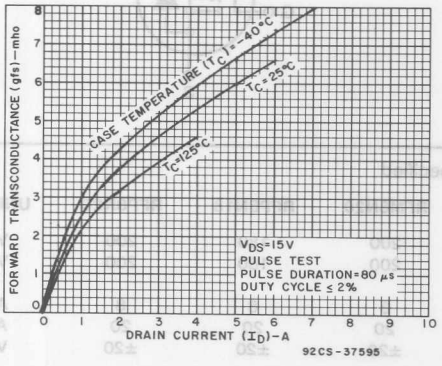


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

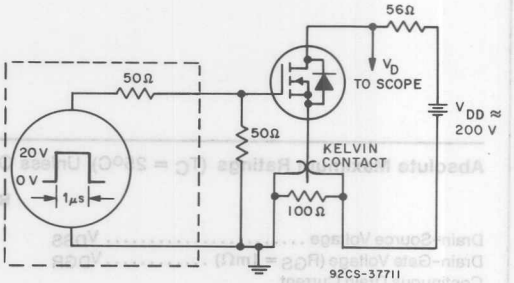


Fig. 11 - Switching time test circuit.

HARRIS

RFM8N18/8N20
RFP8N18/8N20

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 8A, 180V and 200V
- $r_{DS(on)} = 0.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

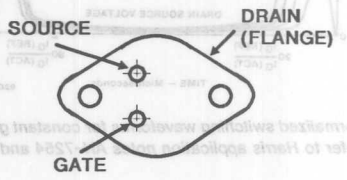
Description

The RFM8N18 and RFM8N20 and the RFP8N18 and RFP8N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

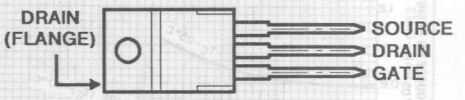
The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA



TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM8N18	RFM8N20	RFP8N18	RFP8N20	UNITS
Drain-Source Voltage ..... V_{DSS}	180	200	180	200	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	180	200	180	200	V
Continuous Drain Current					
RMS Continuous ..... I_D	8	8	8	8	A
Pulsed Drain Current ..... I_{DM}	20	20	20	20	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1447.1

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_c) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM8N18 RFP8N18 MIN.	LIMITS RFM8N18 RFP8N18 MAX.	LIMITS RFM8N20 RFP8N20 MIN.	LIMITS RFM8N20 RFP8N20 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145 V	—	1	—	—	μA
		V_{DS} = 160 V	—	—	—	1	
		T_C = 125° C, V_{DS} = 145 V	—	50	—	—	
		T_C = 125° C, V_{DS} = 160 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 4 A, V_{GS} = 10 V	—	2.0	—	2.0	V
		I_D = 8 A, V_{GS} = 10 V	—	5.5	—	5.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 4 A, V_{GS} = 10 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 4 A	1.5	—	1.5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz	—	750	—	750	pF
Output Capacitance	C_{oss}		—	250	—	250	
Reverse Transfer Capacitance	C_{rss}		—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V, I_D = 4 A, R_{gen} = R_{gs} = 50 Ω, V_{GS} = 10 V	30(typ.)	45	30(typ.)	45	ns
Rise Time	t_r		100(typ.)	150	100(typ.)	150	
Turn-Off Delay Time	$t_d(off)$		90(typ.)	135	90(typ.)	135	
Fall Time	t_f		70(typ.)	105	70(typ.)	105	
Thermal Resistance Junction-to-Case	RθJC	RFM8N18, RFM8N20	—	1.67	—	1.67	°C/W
		RFP8N18, RFP8N20	—	2.083	—	2.083	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM8N18 RFP8N18 Min.	LIMITS RFM8N18 RFP8N18 Max.	LIMITS RFM8N20 RFP8N20 Min.	LIMITS RFM8N20 RFP8N20 Max.	UNITS
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 4A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100A/μs	225(typ.)		225(typ.)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

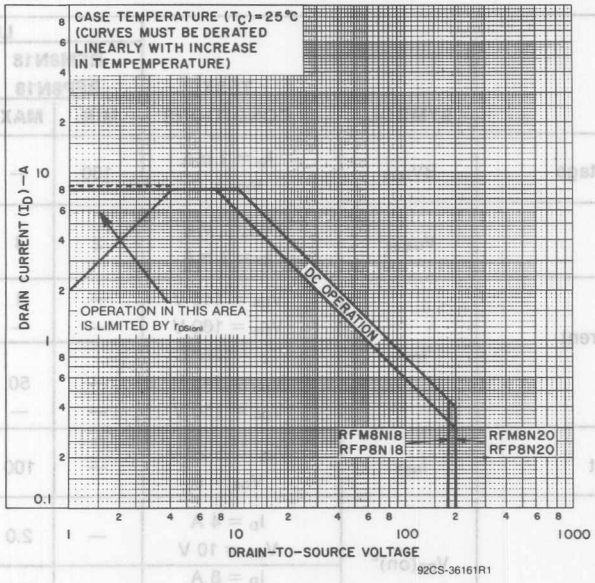


Fig. 1 — Maximum safe operating areas for all types.

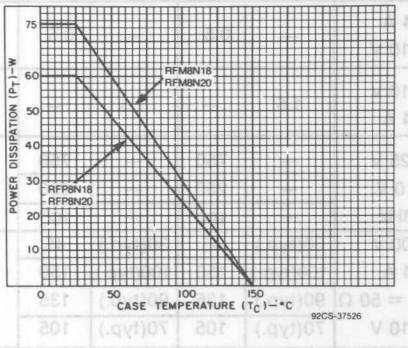


Fig. 2 — Power vs. temperature derating curve for all types.

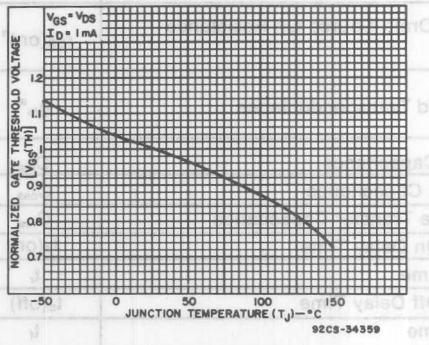


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

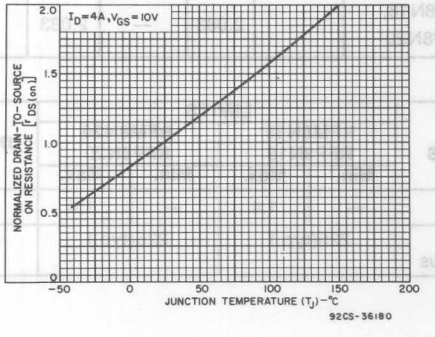


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

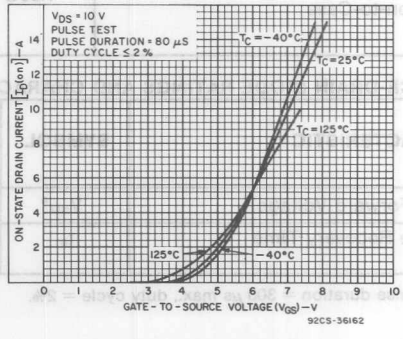


Fig. 5 — Typical transfer characteristics for all types.

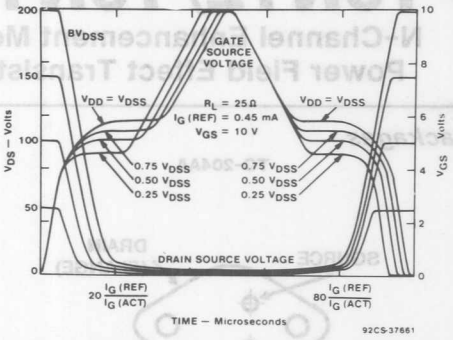


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

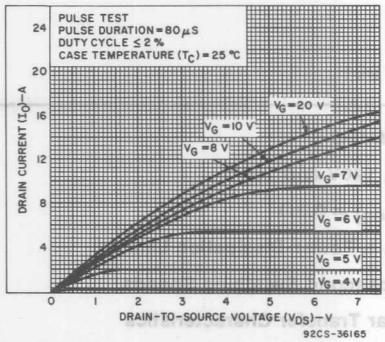


Fig. 7 — Typical saturation characteristics for all types.

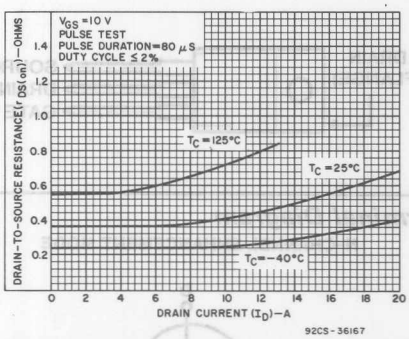


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

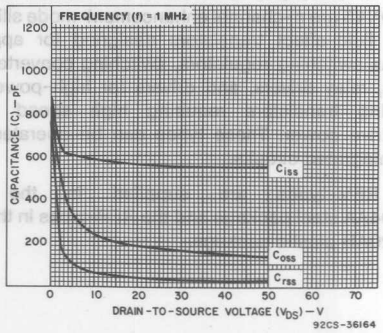


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

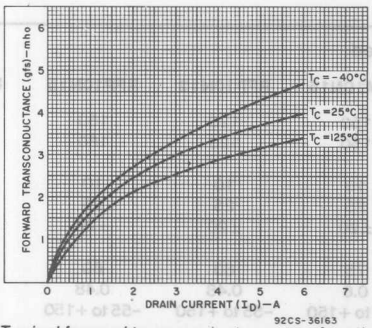


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

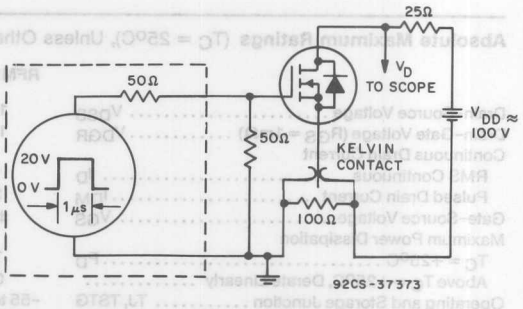


Fig. 11 — Switching Time Test Circuit.

RFM10N12/10N15
RFP10N12/10N15

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 10A, 120V and 150V
- $r_{DS(on)} = 0.3\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

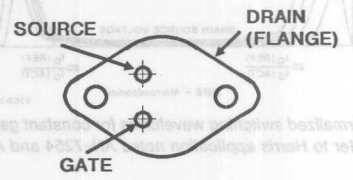
Description

The RFM10N12 and RFM10N15 and the RFP10N12 and RFP10N15 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

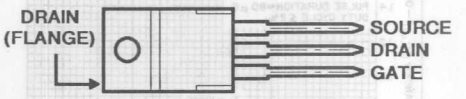
The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA

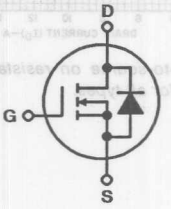


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM10N12	RFM10N15	RFP10N12	RFP10N15	UNITS
Drain-Source Voltage ..... V_{DSS}	120	150	120	150	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	120	150	120	150	V
Continuous Drain Current					
RMS Continuous ..... I_D	10	10	10	10	A
Pulsed Drain Current ..... I_{DM}	25	25	25	25	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1445.1

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_c) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM10N12 RFP10N12 MIN.	LIMITS RFM10N12 RFP10N12 MAX.	LIMITS RFM10N15 RFP10N15 MIN.	LIMITS RFM10N15 RFP10N15 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V	—	1	—	—	μA
		V_{DS} = 120 V	—	—	—	1	
		T_C = 125° C, V_{DS} = 100 V	—	50	—	—	
		T_C = 125° C, V_{DS} = 120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5 A, V_{GS} = 10 V	—	1.5	—	1.5	V
		I_D = 10 A, V_{GS} = 10 V	—	4	—	4	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5 A, V_{GS} = 10 V	—	0.3	—	0.3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	850	—	850	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	230	—	230	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75 V	40(typ.)	60	40(typ.)	60	ns
Rise Time	t_r	I_D = 5 A	165(typ.)	250	165(typ.)	250	
Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 50 Ω	90(typ.)	135	90(typ.)	135	
Fall Time	t_f	V_{GS} = 10 V	90(typ.)	135	90(typ.)	135	
Thermal Resistance Junction-to-Case	RθJC	RFM10N12, RFM10N15	—	1.67	—	1.67	°C/W
		RFP10N12, RFP10N15	—	2.083	—	2.083	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM10N12 RFP10N12 MIN.	LIMITS RFM10N12 RFP10N12 MAX.	LIMITS RFM10N15 RFP10N15 MIN.	LIMITS RFM10N15 RFP10N15 MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A, d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

[a] Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

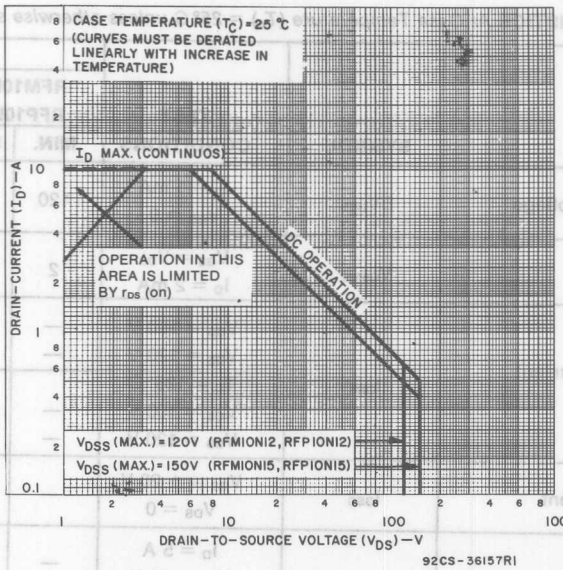


Fig. 1 — Maximum safe operating areas for all types.

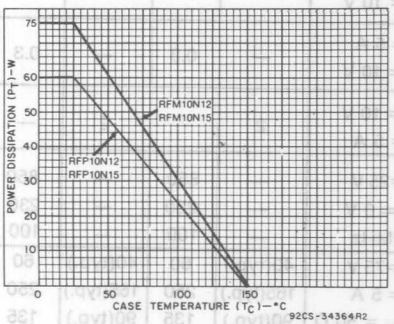


Fig. 2 — Power vs. temperature derating curve for all types.

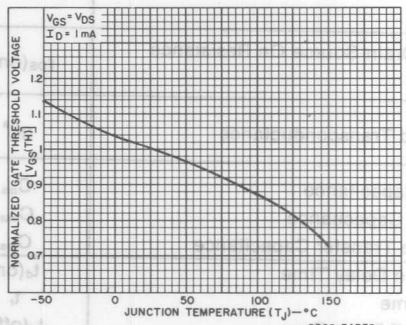


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

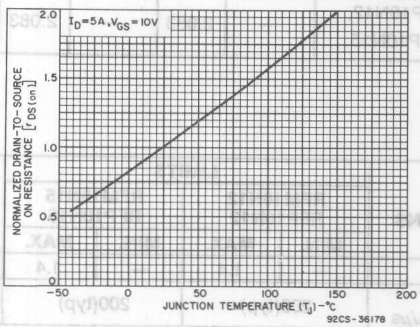


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

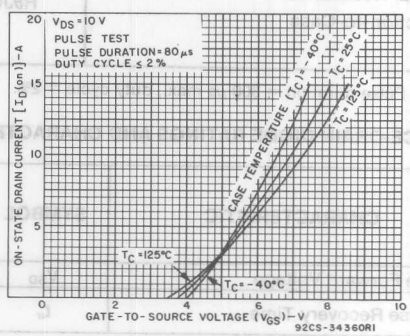


Fig. 5 — Typical transfer characteristics for all types.

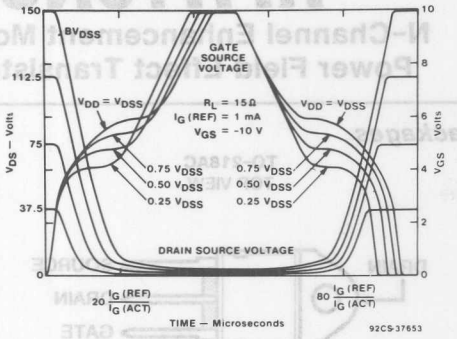


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

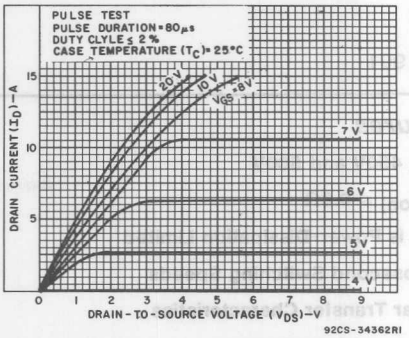


Fig. 7 — Typical saturation characteristics for all types.

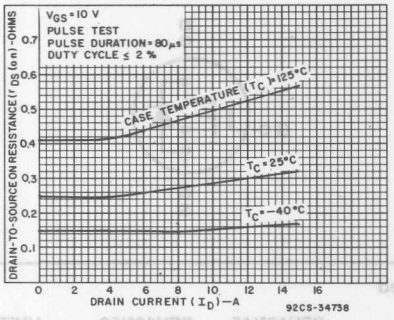


Fig. 8 – Typical drain-to-source on resistance as a function drain current for all types.

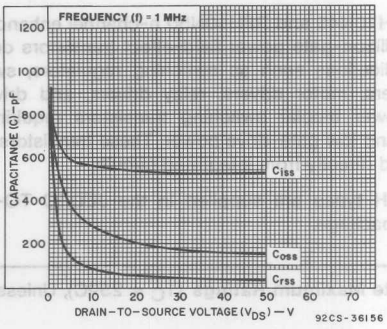


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

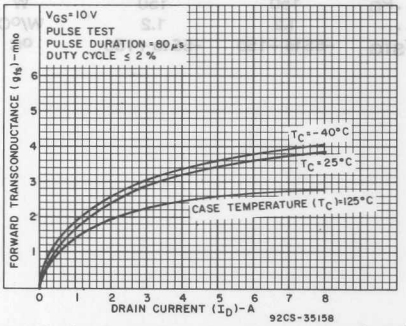


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

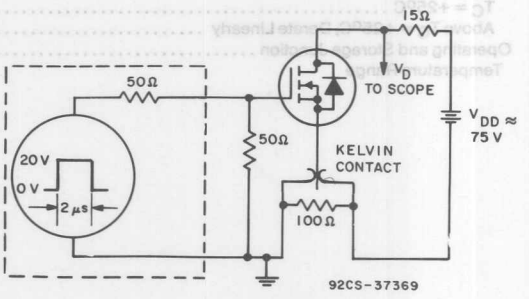


Fig. 11 — Switching Time Test Circuit

4 N-CHANNEL POWER MOSFETs

HARRIS

RFH10N45
RFH10N50

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 10A, 450V and 500V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Current, Low-Inductance Package

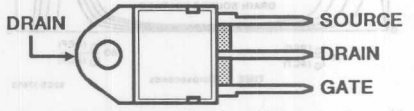
Description

The RFH10N45 and RFH10N50 n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

The RFH types are supplied in the JEDEC TO-218AC plastic package.

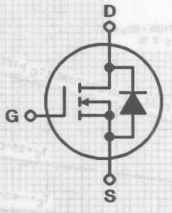
Packages

TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		RFH10N45	RFH10N50	UNITS
Drain-Source Voltage	V_{DSS}	450	500	V
Drain-Gate Voltage (R_{GS} = 1mΩ)	V_{DGR}	450	500	V
Continuous Drain Current				
RMS Continuous	I_D	10	10	A
Pulsed Drain Current	I_{DM}	20	20	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	150	150	W
Above T_C = +25°C, Derate Linearly		1.2	1.2	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1629.1

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH10N45		RFH10N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	450	—	500	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 360 V	—	1	—	—	μA
		V_{DS} = 400 V	—	—	—	1	
		T_C = 125° C V_{DS} = 360 V	—	50	—	—	
		V_{DS} = 400 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5 A V_{GS} = 10 V	—	3.0	—	3.0	V
		I_D = 10 A V_{GS} = 10 V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5A V_{GS} = 10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	600	—	600	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	200	—	200	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 250 V	26(typ)	60	26(typ)	60	ns
Rise Time	t_r	I_D = 5 A	50(typ)	100	50(typ)	100	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	525(typ)	900	525(typ)	900	
Fall Time	t_f	V_{GS} = 10 V	105(typ)	180	105(typ)	180	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH10N45, RFH10N50 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH10N45		RFH10N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 (typ.)		950 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

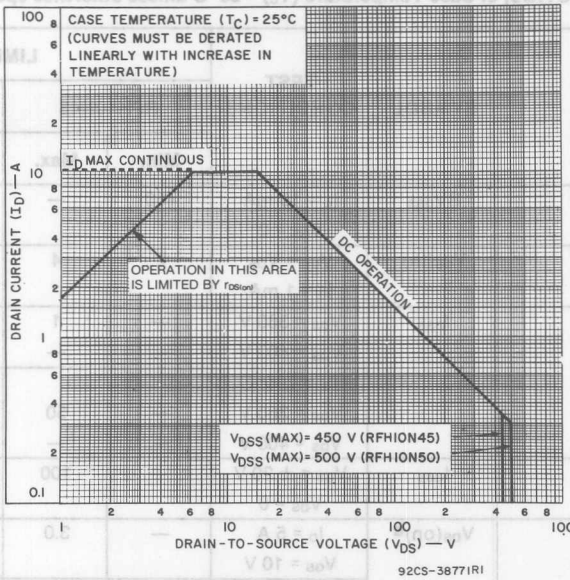


Fig. 1 - Maximum safe operating areas for all types.

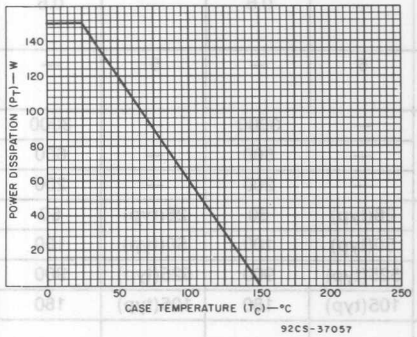


Fig. 2 - Power vs. temperature derating curve for all types.

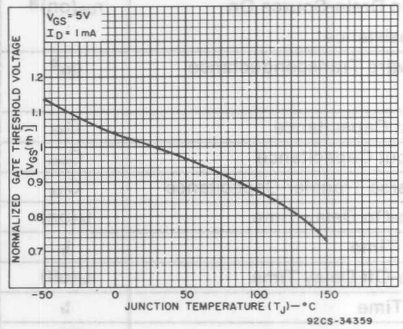


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

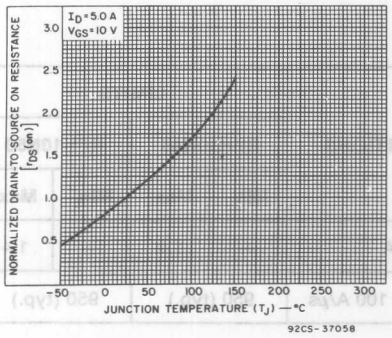


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

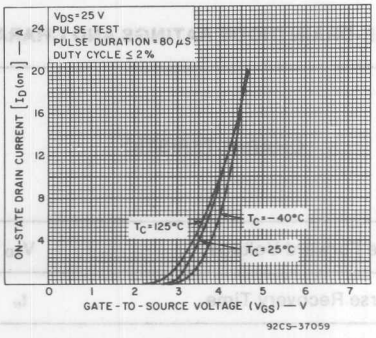


Fig. 5 - Typical transfer characteristics for all types.

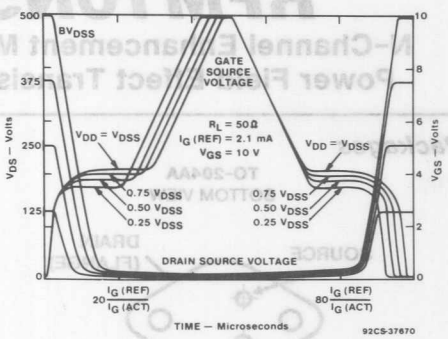


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

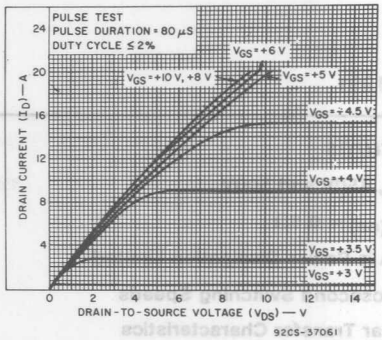


Fig. 7 - Typical saturation characteristics for all types.

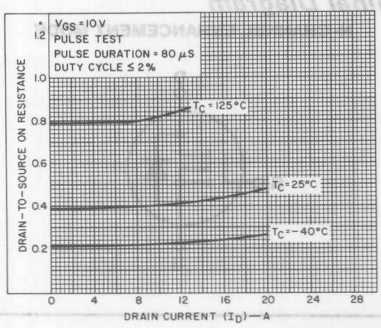


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

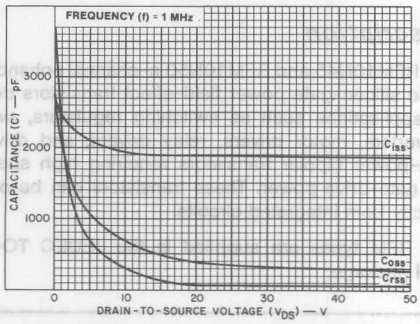


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

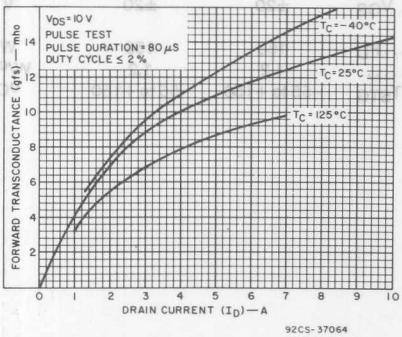


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

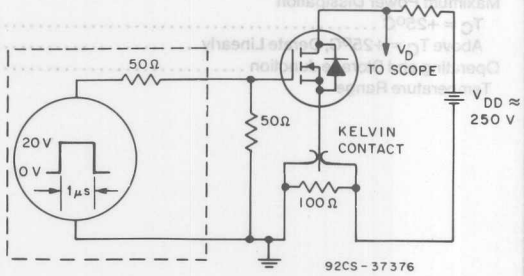


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFM10N45
RFM10N50

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 10A, 450V and 500V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Current, Low-Inductance Package

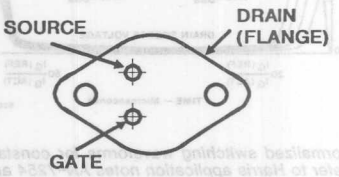
Description

The RFM10N45 and RFM10N50 n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

The RFM types are supplied in the JEDEC TO-204AA steel package.

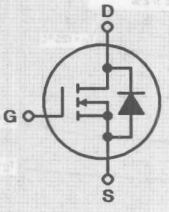
Packages

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

		RFM10N45	RFM10N50	UNITS
Drain-Source Voltage	V_{DSS}	450	500	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$)	V_{DGR}	450	500	V
Continuous Drain Current				
RMS Continuous	I_D	10	10	A
Pulsed Drain Current	I_{DM}	20	20	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	150	150	W
Above $T_C = +25^oC$, Derate Linearly		1.2	1.2	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1788

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N45		RFM10N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	450	—	500	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 360 V	—	1	—	—	μA
		V_{DS} = 400 V	—	—	—	1	
		T_C = 125° C V_{DS} = 360 V	—	50	—	—	
		V_{DS} = 400 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5 A V_{GS} = 10 V	—	3.0	—	3.0	V
		I_D = 10 A V_{GS} = 10 V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5A V_{GS} = 10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	600	—	600	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	200	—	200	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 250	26(typ)	60	26(typ)	60	ns
Rise Time	t_r	I_D = 5 A	50(typ)	100	50(typ)	100	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	525(typ)	900	525(typ)	900	
Fall Time	t_f	V_{GS} = 10 V	105(typ)	180	105(typ)	180	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10N45, RFM10N50 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFM10N45		RFM10N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 typ.		950 typ.		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

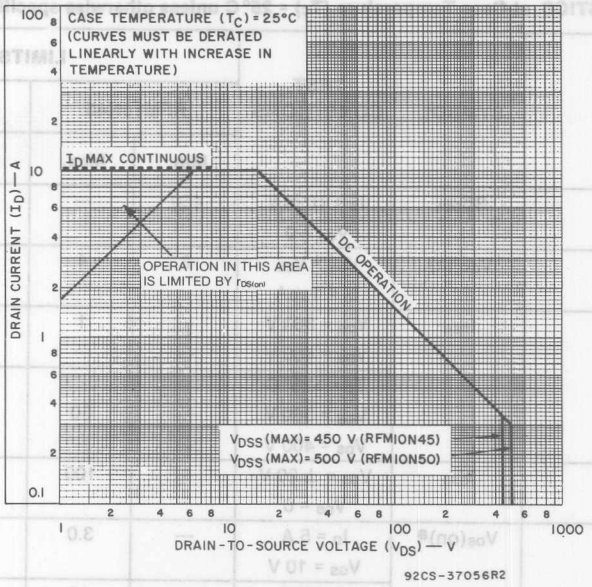


Fig. 1 - Maximum safe operating areas for all types.

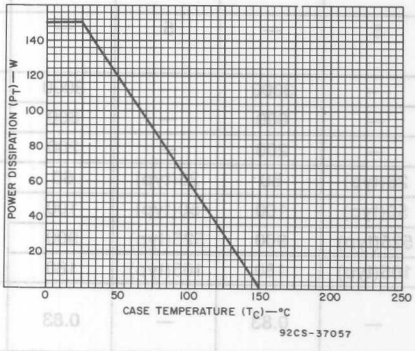


Fig. 2 - Power vs. temperature derating curve for all types.

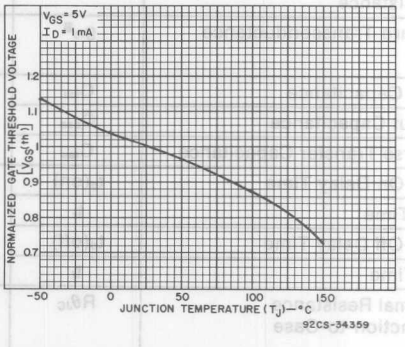


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

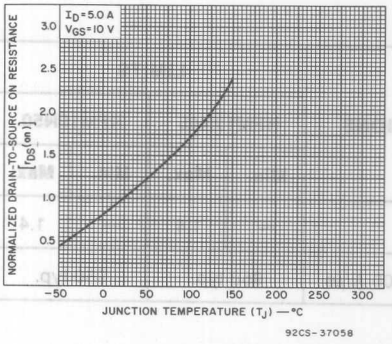


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

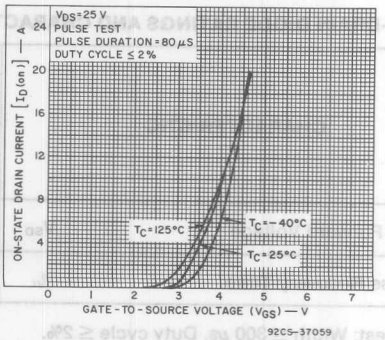


Fig. 5 - Typical transfer characteristics for all types.

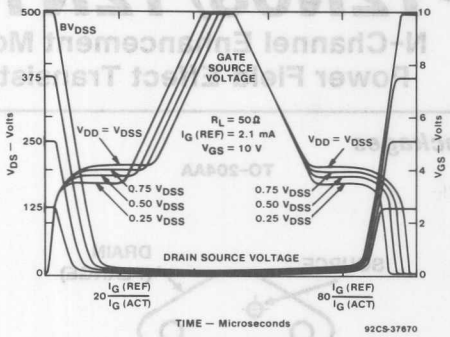


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

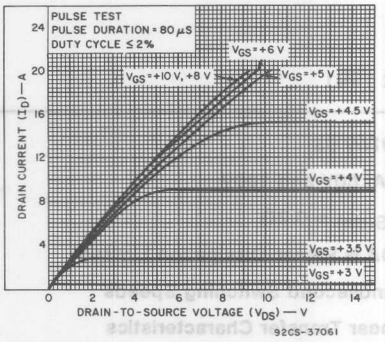


Fig. 7 - Typical saturation characteristics for all types.

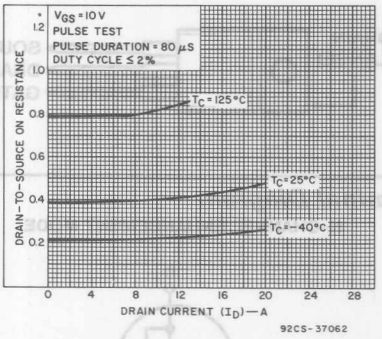


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

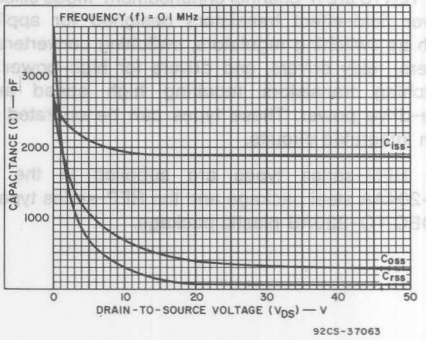


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

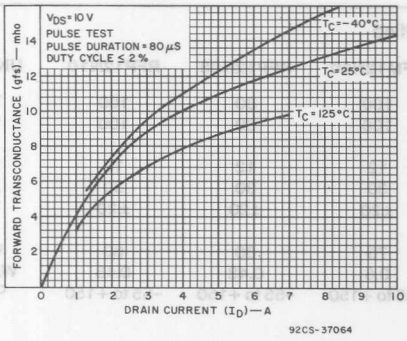


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

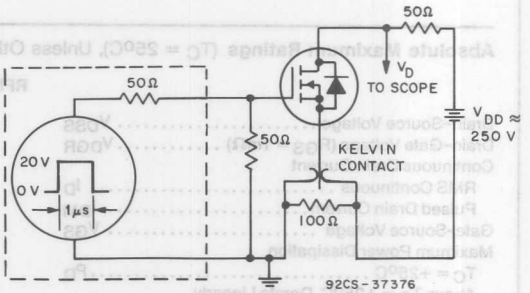


Fig. 11 - Switching Time Test Circuit.

RFM12N08/12N10
RFP12N08/12N10

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 12A, 80V and 100V
- $r_{DS(on)} = 0.2\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

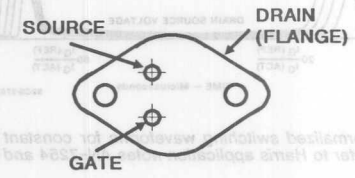
Description

The RFM12N08 and RFM12N10 and the RFP12N08 and RFP12N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

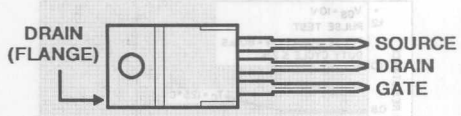
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA

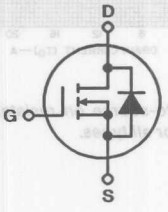


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM12N08	RFM12N10	RFP12N08	RFP12N10	UNITS
Drain-Source Voltage ..... V_{DSS}	80	100	80	100	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	80	100	80	100	V
Continuous Drain Current					
RMS Continuous ..... I_D	12	12	12	12	A
Pulsed Drain Current ..... I_{DM}	30	30	30	30	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1386.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08 RFP12N08		RFM12N10 RFP12N10		
			Min.	Max.	Min.	Max.	
Drain Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V	—	1	—	—	μA
		V_{DS}=80 V	—	—	—	1	
		T_C=125°C V_{DS}=65 V	—	50	—	—	
		V_{DS}=80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	1.2	—	1.2	V
		I_D=12 A V_{GS}=10 V	—	3.3	—	3.3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	0.2	—	0.2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	850	—	850	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	150	—	150	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	45(Typ)	70	45(Typ)	70	ns
Rise Time	t_r	I_D=6 A	250(Typ)	375	250(Typ)	375	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	85(Typ)	130	85(Typ)	130	
Fall Time	t_f	V_{GS}=10 V	100(Typ)	150	100(Typ)	150	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N08, RFM12N10	—	1.67	—	1.67	°C/W
		RFP12N08, RFP12N10	—	2.083	—	2.083	

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08 RFM12N10		RFP12N08 RFP12N10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

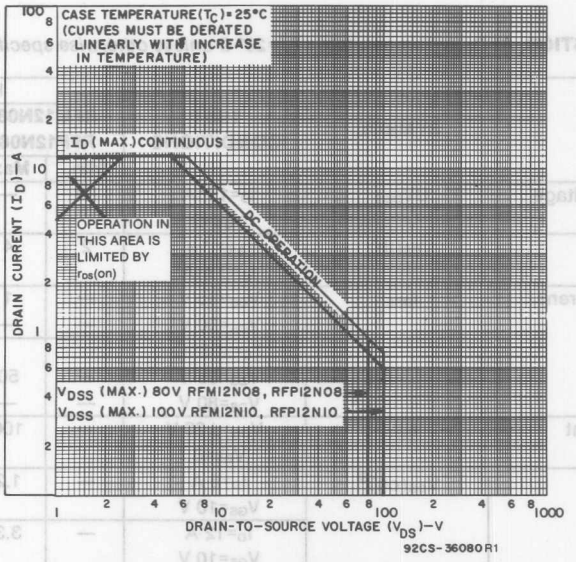


Fig. 1 - Maximum operating areas for all types.

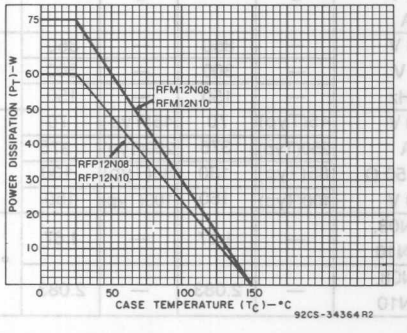


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

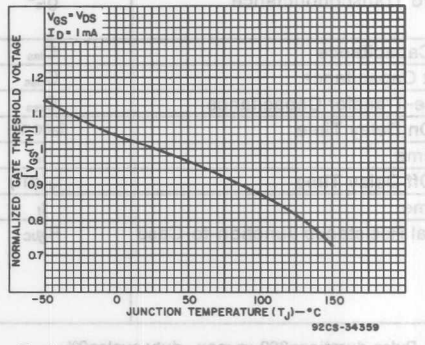


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

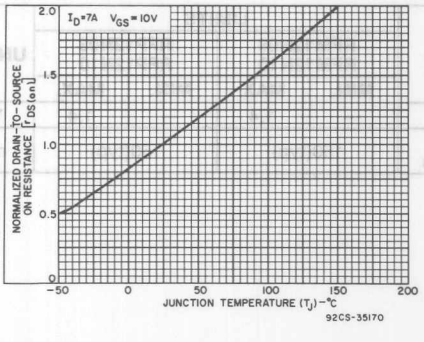


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

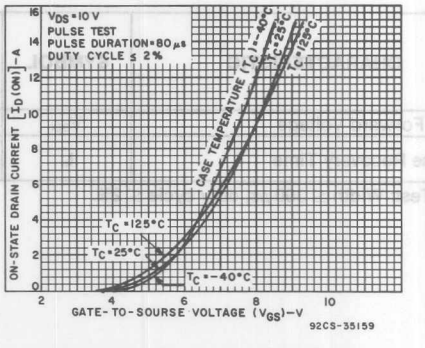


Fig. 5 - Typical transfer characteristics for all types.

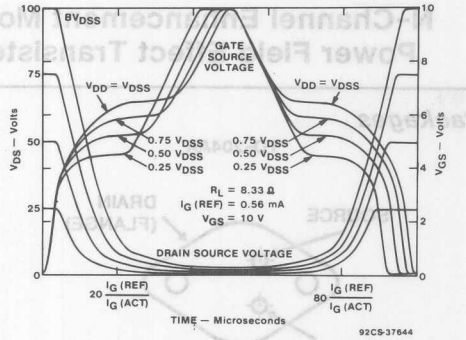


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

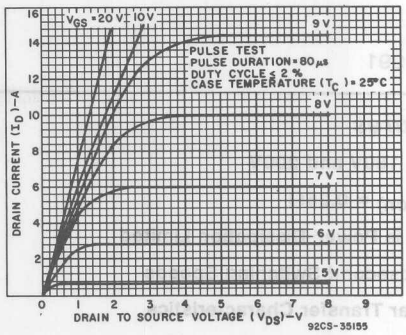


Fig. 7 - Typical saturation characteristics for all types.

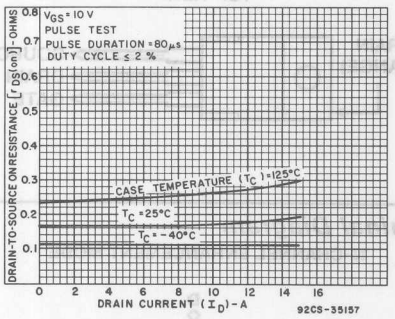


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

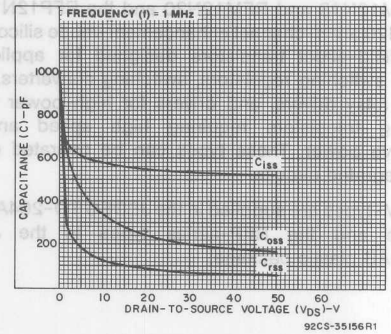


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

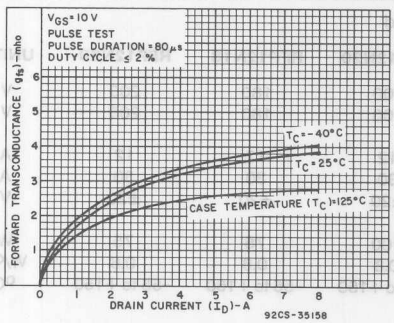


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

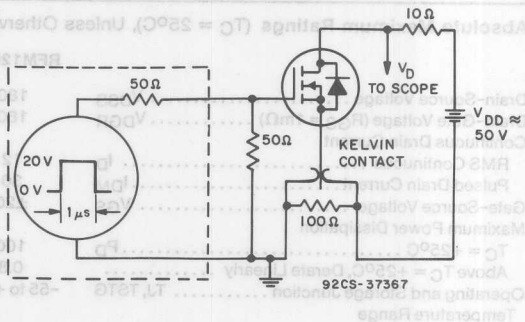


Fig. 11 — Switching Time Test Circuit

RFM12N18/12N20
RFP12N18/12N20

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 12A, 180V and 200V
- $r_{DS(on)} = 0.25\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

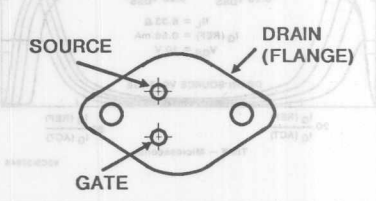
Description

The RFM12N18 and RFM12N20 and the RFP12N18 and RFP12N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

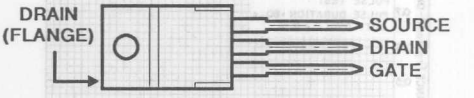
The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA

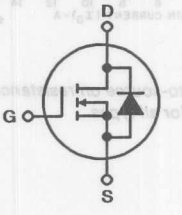


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM12N18	RFM12N20	RFP12N18	RFP12N20	UNITS
Drain-Source Voltage ..... V_{DSS}	180	200	180	200	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	180	200	180	200	V
Continuous Drain Current					
RMS Continuous ..... I_D	12	12	12	12	A
Pulsed Drain Current ..... I_{DM}	30	30	30	30	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	100	100	75	75	W
Above $T_C = +25^oC$, Derate Linearly	0.8	0.8	0.6	0.6	W/^{o}C
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1461.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N18 RFP12N18		RFM12N20 RFP12N20		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA, V_{GS}=0	180	—	200	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V	—	1	—	—	μA
		V_{DS}=160 V	—	—	—	1	
		T_C=125° C, V_{DS}=145 V	—	50	—	—	
		T_C=125° C, V_{DS}=160 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A, V_{GS}=10 V	—	1.5	—	1.5	V
		I_D=12 A, V_{GS}=10 V	—	3.6	—	3.6	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A, V_{GS}=10 V	—	0.25	—	0.25	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V, I_D=6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V, V_{GS}=0 V, f=1 MHz	—	1700	—	1700	pF
Output Capacitance	C_{oss}		—	600	—	600	
Reverse-Transfer Capacitance	C_{rss}		—	300	—	300	
Turn-On Delay Time	t_d(on)	V_{DD}=100 V, I_D=6 A, R_{gen}=R_{gs}=50 Ω, V_{GS}=10 V	35(typ)	50	35(typ)	50	ns
Rise Time	t_r		130(typ)	200	130(typ)	200	
Turn-Off Delay Time	t_d(off)		120(typ)	180	120(typ)	180	
Fall Time	t_f		105(typ)	160	105(typ)	160	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N18, RFM12N20	—	1.25	—	1.25	°C/W
		RFP12N18, RFP12N20	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N18 RFP12N18		RFM12N20 RFP12N20		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A, d_{IF}/d_t=100 A/μs	325(typ)		325(typ)		ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

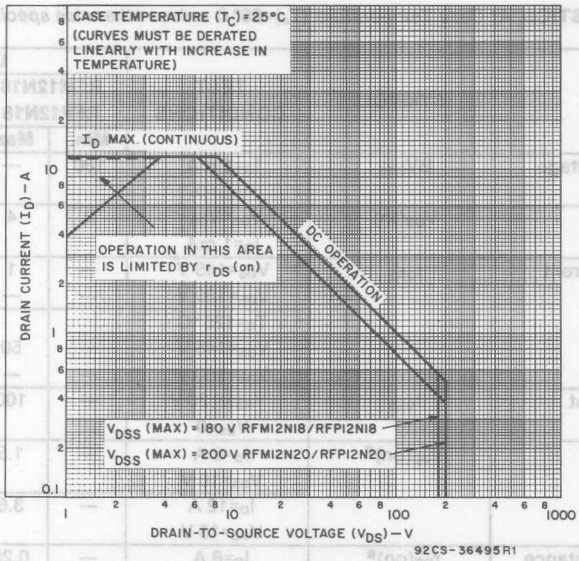


Fig. 1 - Maximum safe operating areas for all types.

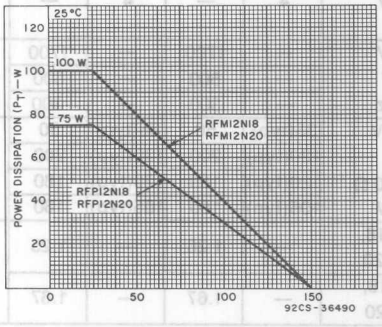


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

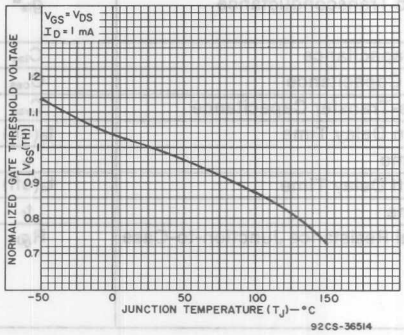


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

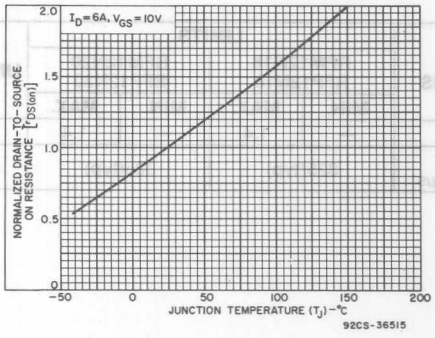


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

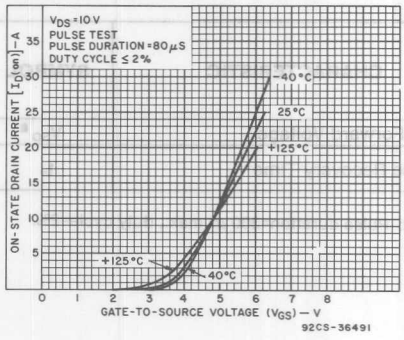


Fig. 5 - Typical transfer characteristics for all types.

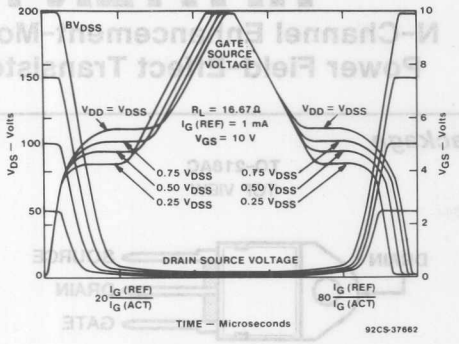


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

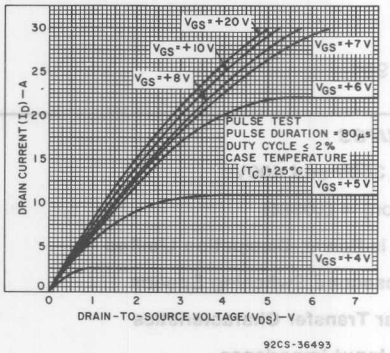


Fig. 7 - Typical saturation characteristics for all types.

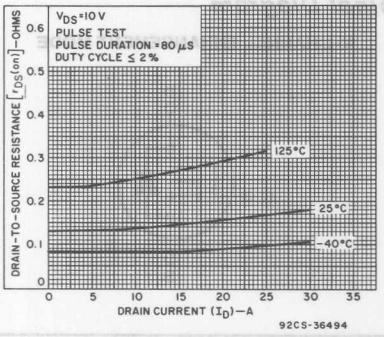


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

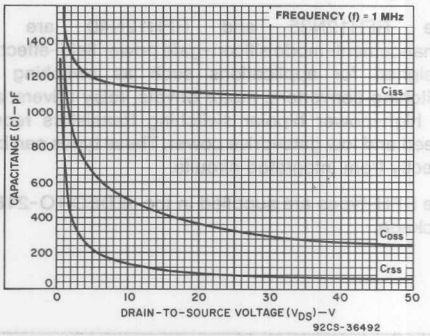


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

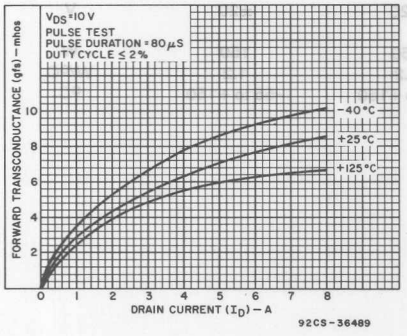


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

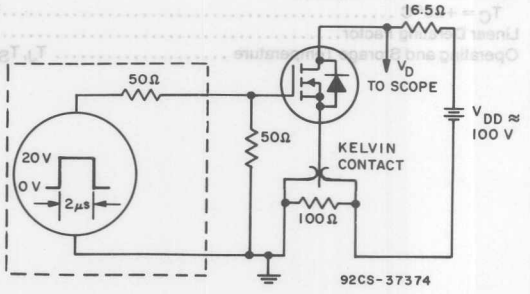


Fig. 11 — Switching Time Test Circuit

HARRIS

RFH12N35
RFH12N40

N-Channel Enhancement-Mode Power Field-Effect Transistors

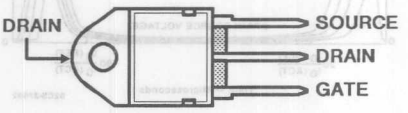
August 1991

Features

- 12A, 350V and 400V
- $r_{DS}(on) = 0.038\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Current, Low-Inductance Package

Package

TO-218AC
TOP VIEW



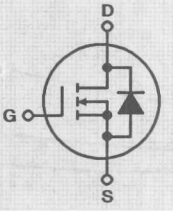
Description

The RFH12N35 and RFH12N40 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFH12N35	RFH12N40	UNITS
Drain-Source Voltage	V_{DSS}	350	400	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	350	400	V
Continuous Drain Current	I_D	12	12	A
Pulsed Drain Current	I_{DM}	24	24	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation, T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1630.1

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH12N35		RFH12N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 280 V	—	1	—	—	μA
		V_{DS} = 320 V	—	—	—	1	
		T_C = 125°C V_{DS} = 280 V	—	50	—	—	
		V_{DS} = 320 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	2.28	—	2.28	V
		I_D = 12 A V_{GS} = 10 V	—	6.75	—	6.75	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	0.38	—	0.38	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	900	—	900	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	400	—	400	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 200 V	30(typ)	50	30(typ)	50	ns
Rise Time	t_r	I_D = 6 A	105(typ)	150	105(typ)	150	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	480(typ)	750	480(typ)	750	
Fall Time	t_f	V_{GS} = 10 V	140(typ)	200	140(typ)	200	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH12N35, RFH12N40 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH12N35		RFH12N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 6A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 (typ.)		950 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

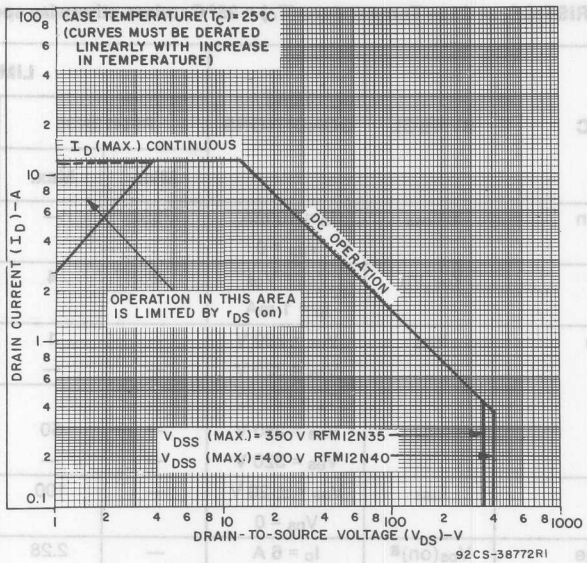


Fig. 1 - Maximum safe operating areas for all types.

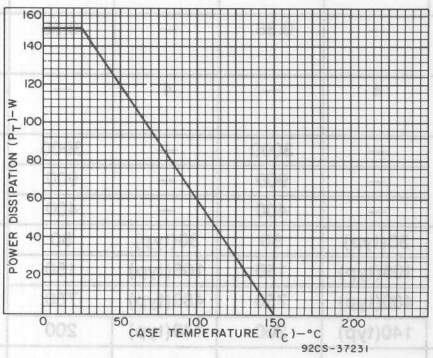


Fig. 2 - Power vs. temperature derating curve for all types.

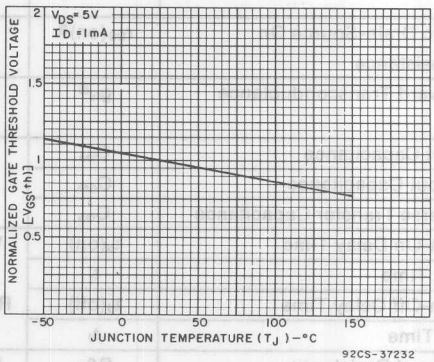


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

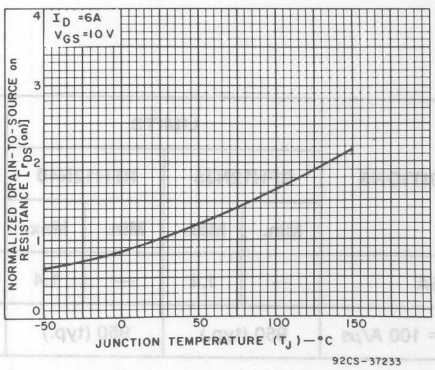


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

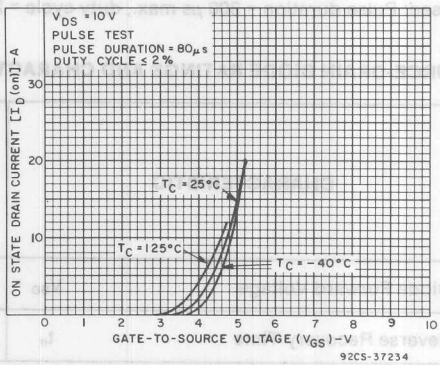


Fig. 5 - Typical transfer characteristics for all types.

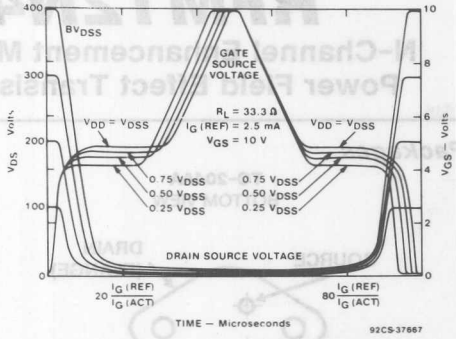


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

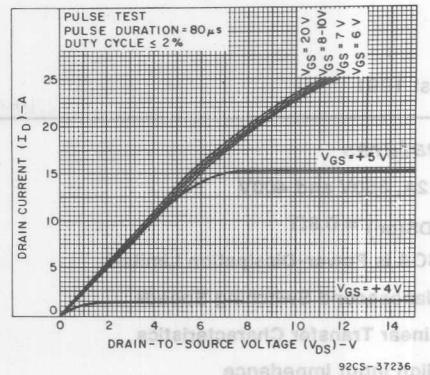


Fig. 7 - Typical saturation characteristics for all types.

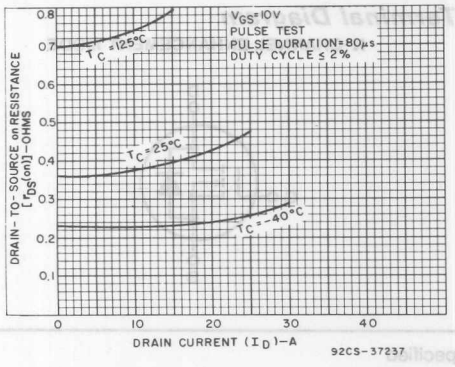


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

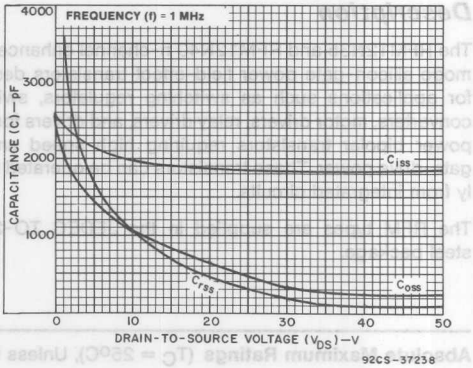


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

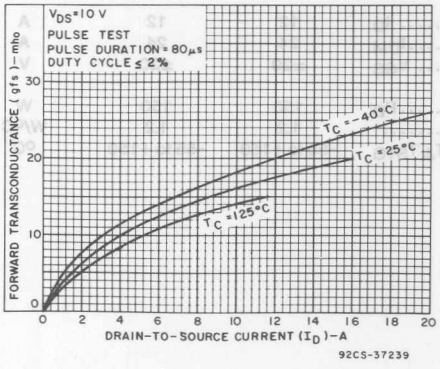


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

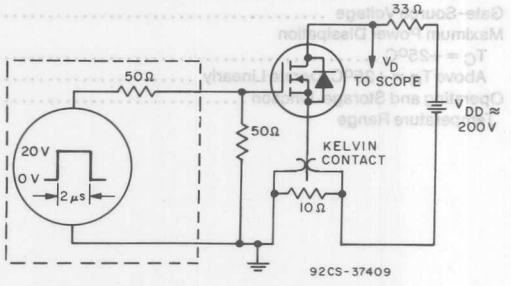


Fig. 11 - Switching Time Test Circuit.

Features

- 12A, 350V and 400V
- $r_{DS(on)} = 0.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

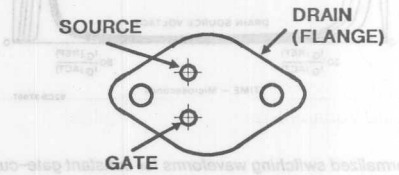
Description

The RFM12N35 and RFM12N40 n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

The RFM types are supplied in the JEDEC TO-204AA steel package.

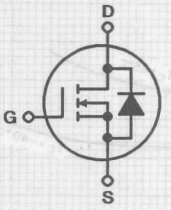
Packages

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

		RFM12N35	RFM12N40	UNITS
Drain-Source Voltage	V_{DSS}	350	400	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$)	V_{DGR}	350	400	V
Continuous Drain Current				
RMS Continuous	I_D	12	12	A
Pulsed Drain Current	I_{DM}	24	24	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	150	150	W
Above $T_C = +25^oC$, Derate Linearly		1.2	1.2	$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1787

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFM12N35		RFM12N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 280 V	—	1	—	—	μA
		V_{DS} = 320 V	—	—	—	1	
		T_C = 125° C V_{DS} = 280 V	—	50	—	—	
		V_{DS} = 320 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	3	—	3	V
		I_D = 12 A V_{GS} = 10 V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	900	—	900	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	400	—	400	
Turn-On Delay Time	$t_{d(on)}$	V_{DS} = 200	30(typ)	50	30(typ)	50	ns
Rise Time	t_r	I_D = 6 A	105(typ)	150	105(typ)	150	
Turn-Off Delay Time	$t_{d(off)}$	R_{gen}=R_{gs}=50Ω	480(typ)	750	480(typ)	750	
Fall Time	t_f	V_{GS} = 10 V	140(typ)	200	140(typ)	200	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N35, RFM12N40 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFM12N35		RFM12N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4 A, dI_F/d_t = 100 A/μs	950 typ.		950 typ.		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

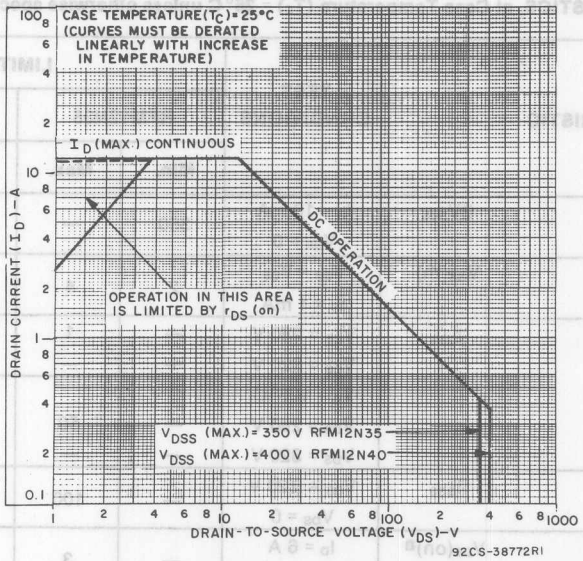


Fig. 1 - Maximum safe operating areas for all types.

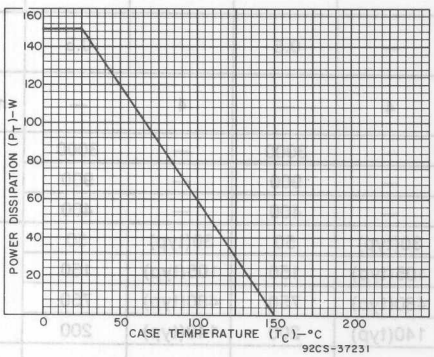


Fig. 2 - Power vs. temperature derating curve for all types.

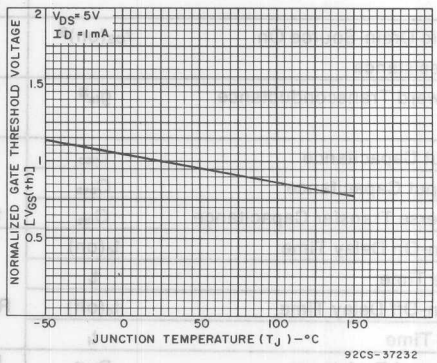


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

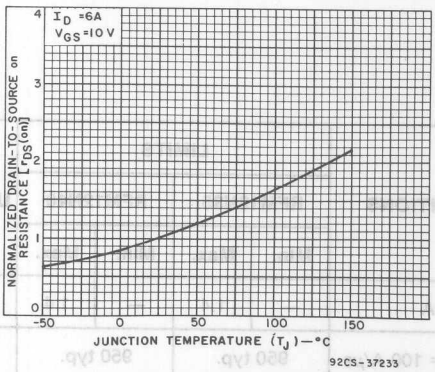


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

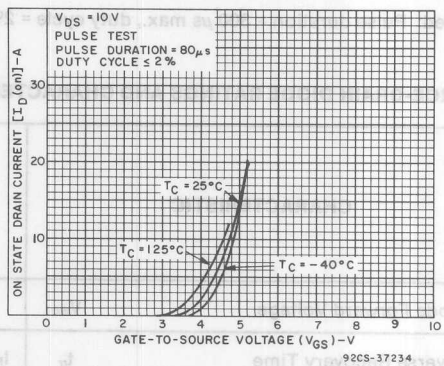


Fig. 5 - Typical transfer characteristics for all types.

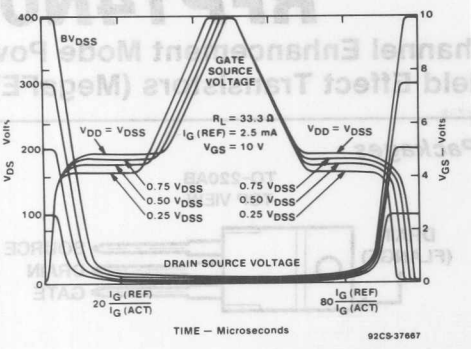


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

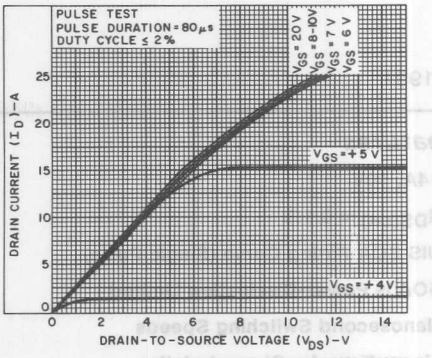


Fig. 7 - Typical saturation characteristics for all types.

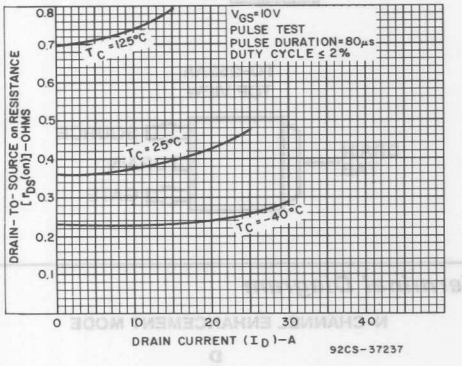


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

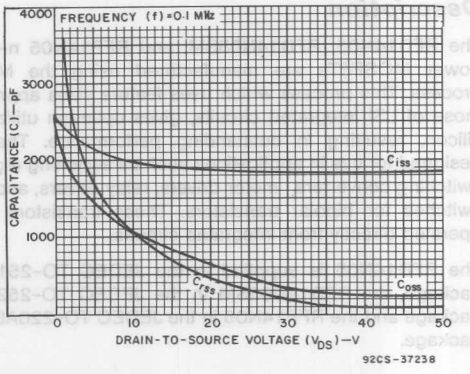


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

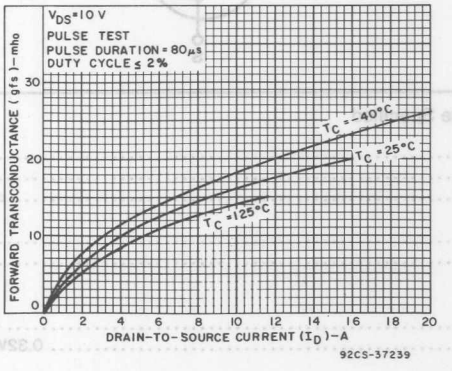


Fig. 10 - Typical forward transconductance as a function of drain for all types.

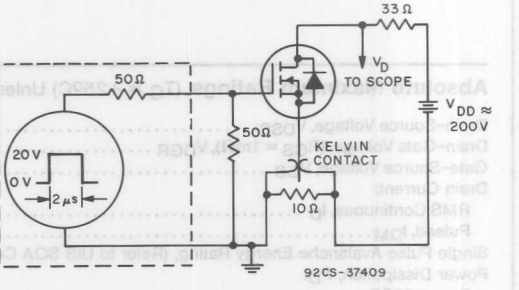


Fig. 11 - Switching Test Time Circuit.

May 1991

N-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

Features

- 14A, 50V
- $R_{DS(on)} = 0.1\Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature

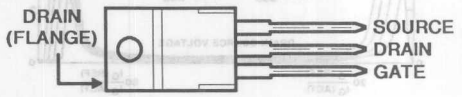
Description

The RFD14N05, RFD14N05SM, and RFP14N05 n-channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

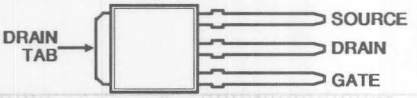
The RFD14N05 is supplied in the JEDEC TO-251 plastic package, the RFD14N05SM in the JEDEC TO-252 plastic package and the RFP14N05 in the JEDEC TO-220AB plastic package.

Packages

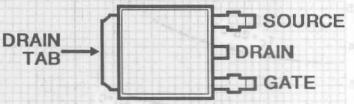
TO-220AB
TOP VIEW



TO-251AA
TOP VIEW

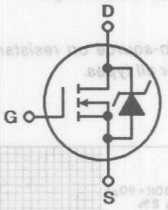


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

Drain-Source Voltage, V_{DSS} 50V
Drain-Gate Voltage, (R_{GS} = 1mΩ), V_{DGR} 50V
Gate-Source Voltage, V_{GS} ..... ±20V
Drain Current:
  RMS Continuous, I_D 14A
  Pulsed, I_{DM} 35A
Single Pulse Avalanche Energy Rating, (Refer to UIS SOA Curve)
Power Dissipation, P_D:
  T_C = +25°C 48W
  Derate Above T_C = +25°C ..... 0.32W/°C
Operating and Storage Junction
Temperature Range, T_J, T_{STG} ..... -55 to +175°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2268.1**

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V		—	1	μA
		T_C = 150° C		—	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V		—	100	nA
Static Drain-Source On-Resistance	$r_{DS}(on)$	I_D = 14 A, V_{GS} = 10 V		—	0.1	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 7 A, I_{g1} = I_{g2} = 0.2 A, V_{GS} (clamp) + 10 V, − 0.6 V, R_L = 3.57 Ω		—	60	ns
Turn-On Delay Time	$t_d(on)$			—	14 (typ.)	ns
Rise Time	t_r			—	26 (typ.)	ns
Turn-Off Delay Time	$t_d(off)$			—	45 (typ.)	ns
Fall Time	t_f			—	17 (typ.)	ns
Turn-Off Time	t(off)			—	100	ns
Total Gate Charge	$Q_g(total)$	V_{DD} = 40 V	V_{GS} = 0-20 V	—	40	nC
Gate Charge at 10 V	$Q_g(10)$	I_D = 14 A	V_{GS} = 0-10 V	—	25	nC
Threshold Gate Charge	$Q_g(th)$	R_L = 2.86 Ω	V_{GS} = 0-2 V	—	1.5	nC
Plateau Voltage	V(plateau)	I_D = 14 A, V_{DS} = 15 V		—	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 7 A, L = 0.2μH, R_L = 3.57 Ω, I_{g1} = I_{g2} = 0.2 A, V_{GS} (clamp) + 10 V, −0.6 V		—	14	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	3.125	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	TO-251 & TO-252		—	100	°C/W
		TO-220		—	80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 14 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, dI_F/dt = 100 A/μs	—	125	ns

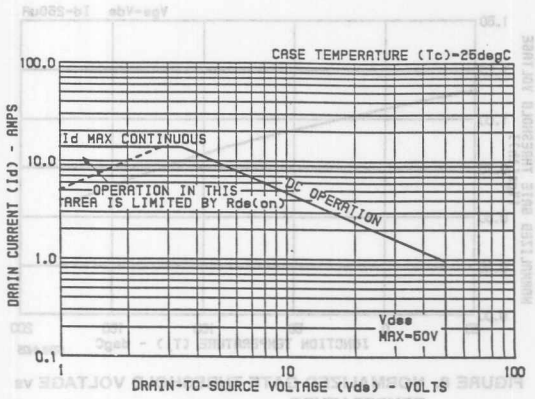


FIGURE 1. SAFE OPERATING AREA CURVE

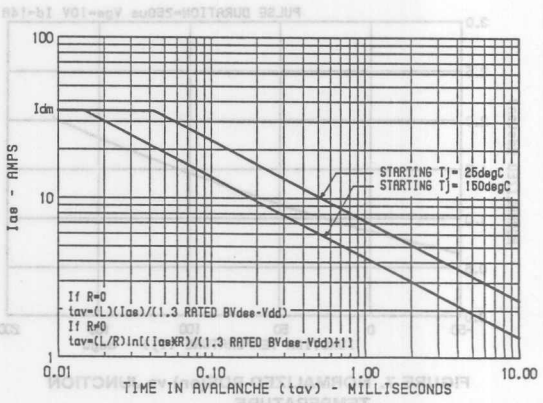


FIGURE 2. UNCLAMPED INDUCTIVE SWITCHING

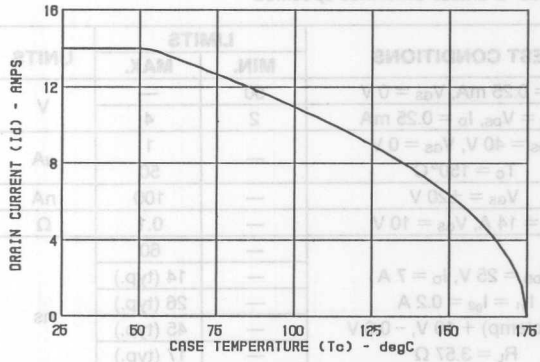


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

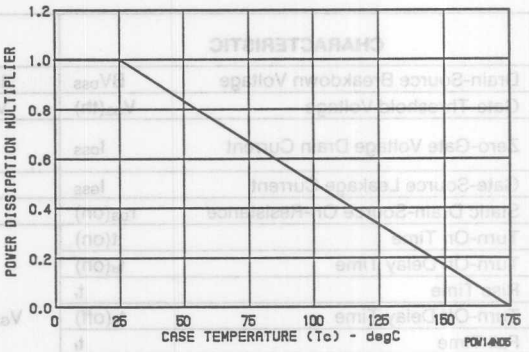


FIGURE 4. NORMALIZED POWER DISTRIBUTION vs TEMPERATURE DERATING

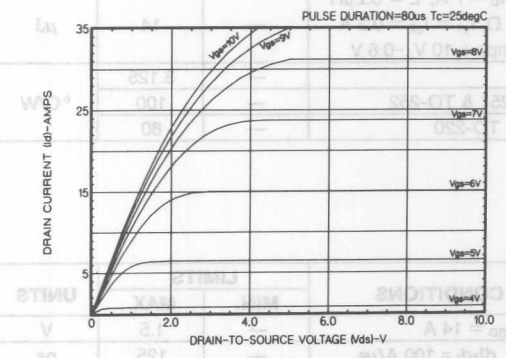


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

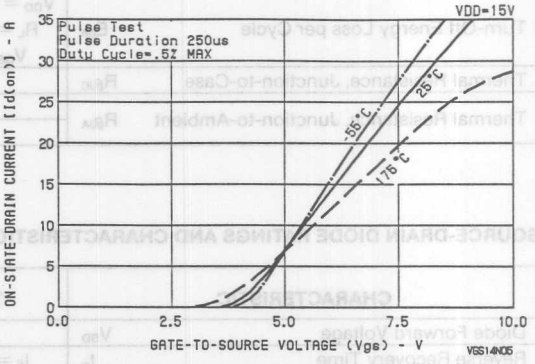


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

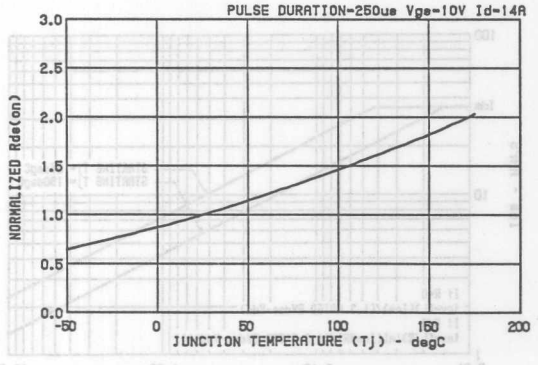


FIGURE 7. NORMALIZED RDS(on) vs JUNCTION TEMPERATURE

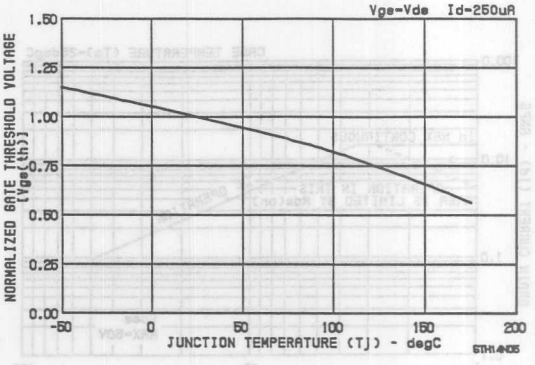


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

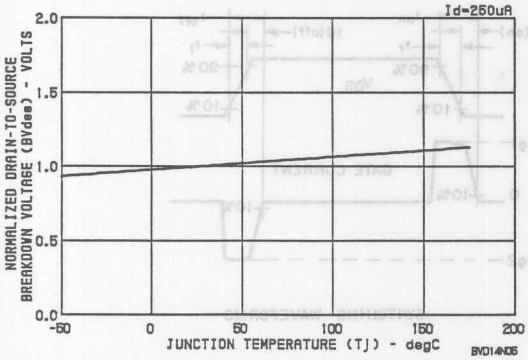


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

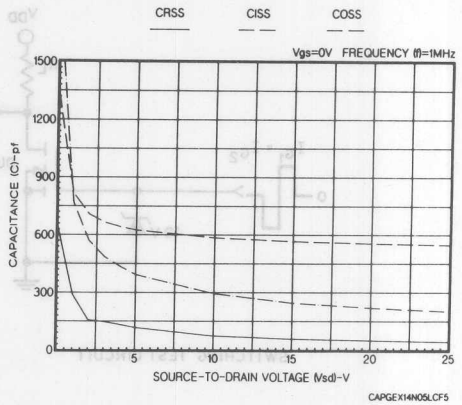


FIGURE 10. TYPICAL CAPACITANCE vs VOLTAGE

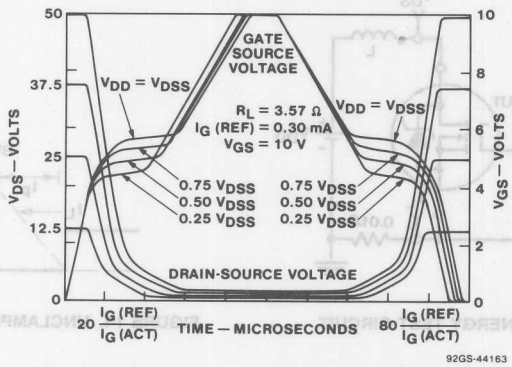


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

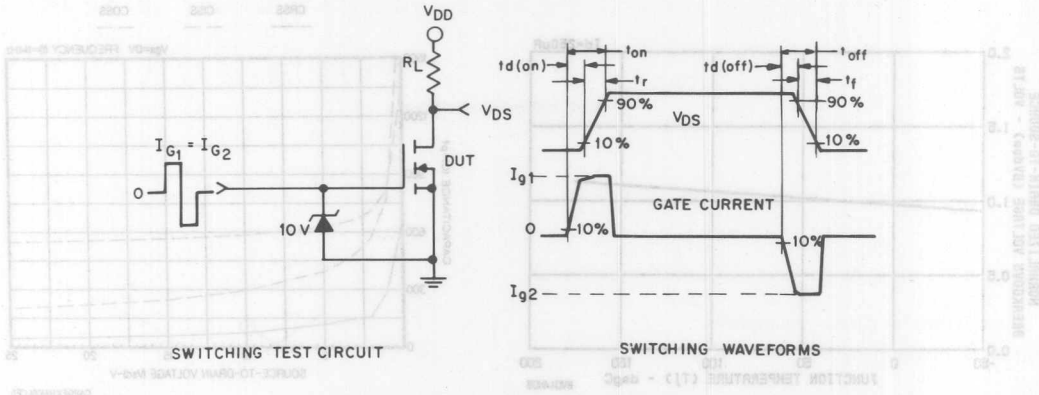


FIGURE 12. RESISTIVE SWITCHING

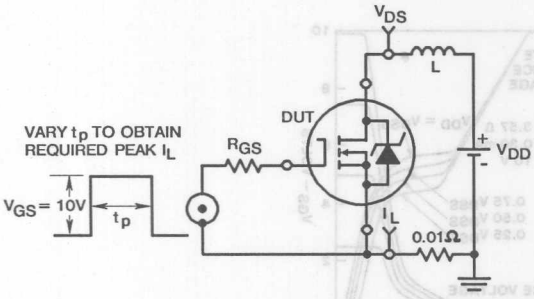


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

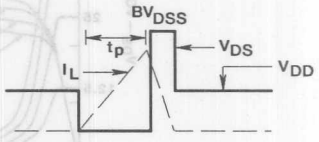


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

HARRIS RFM15N05/15N06 RFP15N05/15N06

N-Channel Enhancement Mode Power Field Effect Transistors

May 1992

Features

- 15A, 50V and 60V
- $r_{DS(on)} = 0.14\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Temperature Compensated SPICE Model Provided

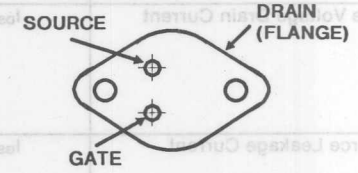
Description

The RFM15N05 and RFM15N06 and the RFP15N05 and RFP15N06 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

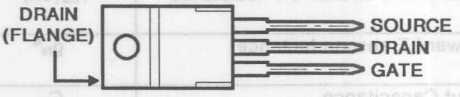
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

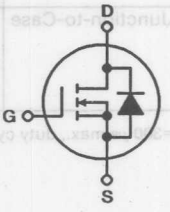


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

	RFM15N05	RFM15N06	RFP15N05	RFP15N06	UNITS
Drain-Source Voltage ..... V_{DSS}	50	60	50	60	V
Drain-Gate Voltage (R_{GS} = 1mΩ) ..... V_{DGR}	50	60	50	60	V
Continuous Drain Current					
RMS Continuous ..... I_D	15	15	15	15	A
Pulsed Drain Current ..... I_{DM}	40	40	40	40	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	90	90	90	90	W
Above T_C = +25°C, Derate Linearly	0.48	0.48	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1478.1**

		CONDITIONS	RFP15N05		RFP15N06		UNITS
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA, V_{GS}=0	50	—	60	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V	—	1	—	—	μA
		V_{DS}=50 V	—	—	—	1	
		T_C=125° C, V_{DS}=40 V	—	50	—	—	
		T_C=125° C, V_{DS}=50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=7.5 A, V_{GS}=10 V	—	1.05	—	1.05	V
		I_D=15 A, V_{GS}=10 V	—	2.5	—	2.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=7.5 A, V_{GS}=10 V	—	0.14	—	0.14	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V, I_D=7.5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V, V_{GS}=0 V, f = 1MHz	—	850	—	850	pF
Output Capacitance	C_{oss}		—	450	—	450	
Reverse-Transfer Capacitance	C_{rss}		—	180	—	180	
Turn-On Delay Time	$t_d(on)$	V_{DD}=30 V, I_D=7.5 A, R_{gen}=R_{gs}=50 Ω, V_{GS}=10 V	16(typ)	40	16(typ)	40	ns
Rise Time	t_r		100(typ)	175	100(typ)	175	
Turn-Off Delay Time	$t_d(off)$		72(typ)	175	72(typ)	175	
Fall Time	t_f		66(typ)	140	66(typ)	140	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM15N05, RFM15N06	—	1.67	—	1.67	°C/W
		RFP15N05, RFP15N06	—	1.67	—	1.67	

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05 RFP15N05		RFM15N06 RFP15N06		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD} = 15A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A, d_{IF}/d_t=100 A/μs	100 (typ)		100(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

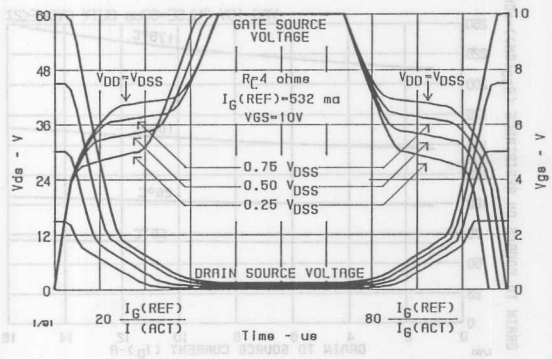


FIGURE 1. NORMALIZED SWITCHING WAVEFORMS

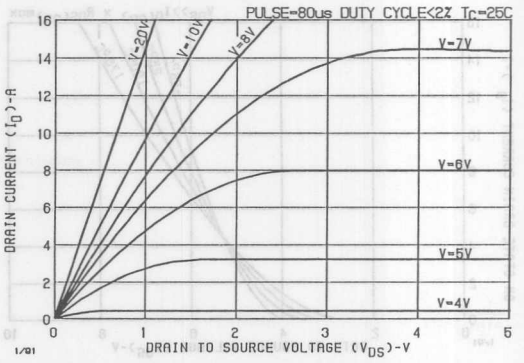


FIGURE 2. TYPICAL SATURATION CHARACTERISTICS

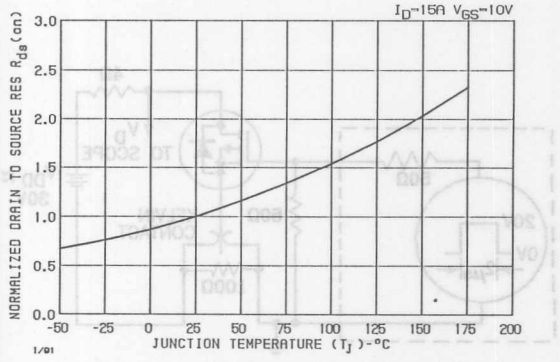


FIGURE 3. NORMALIZED $r_{DS(ON)}$ vs TEMPERATURE

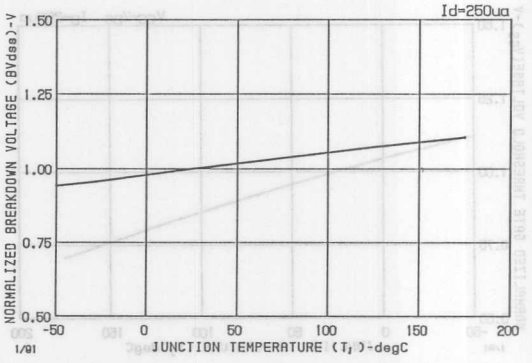


FIGURE 4. BREAKDOWN VOLTAGE vs TEMPERATURE

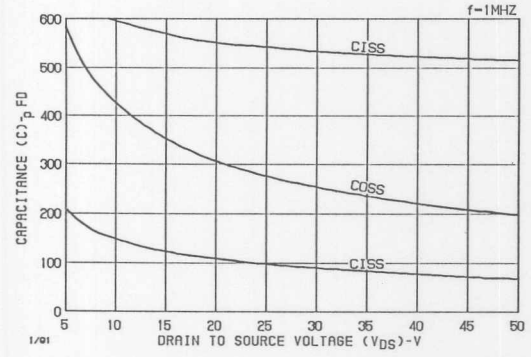


FIGURE 5. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

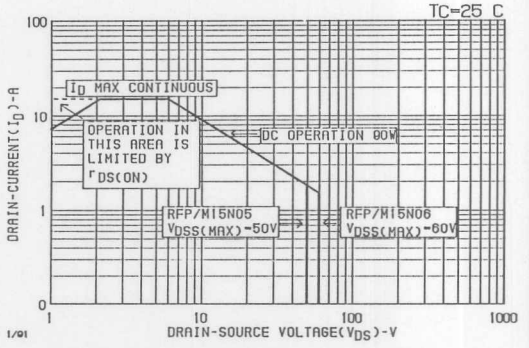


FIGURE 6. MAXIMUM SAFE OPERATING AREA

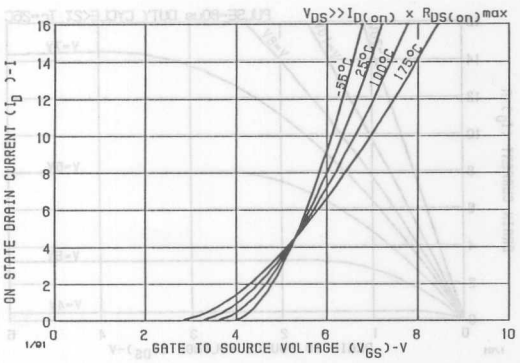


FIGURE 7. TYPICAL TRANSFER CHARACTERISTICS

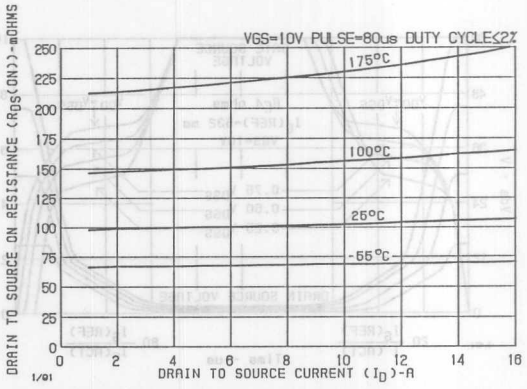


FIGURE 8. $r_{DS(ON)}$ vs DRAIN CURRENT

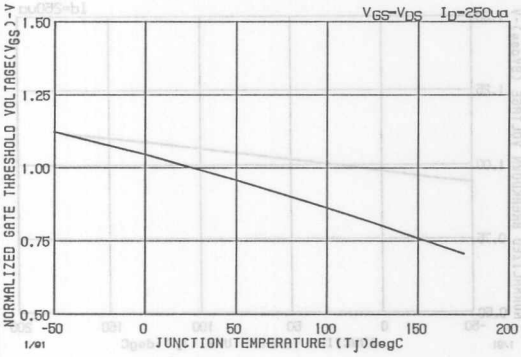


FIGURE 9. THRESHOLD VOLTAGE vs TEMPERATURE (T_J)

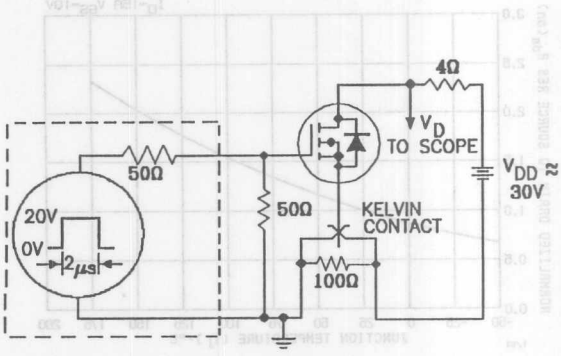
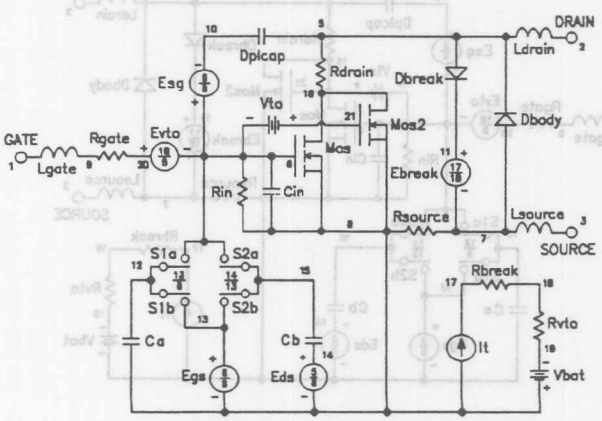


FIGURE 10. SWITCHING TIME TEST CIRCUIT

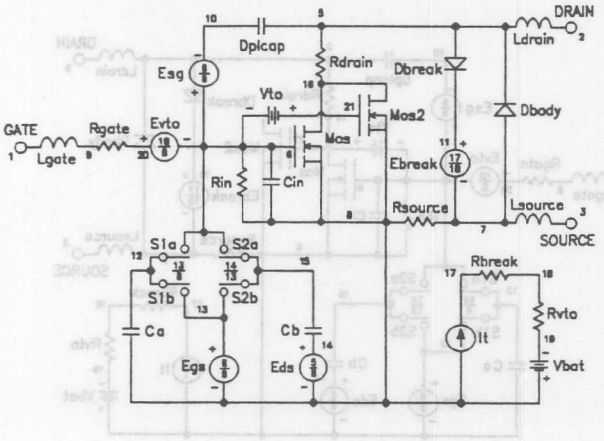
Spice Model (RFM15N06)

```
.SUBCKT RFM15N06  2  1  3;  rev 01/07/91
*Nominal Temperature = 25°C
.MODEL MOSMOD NMOS (VTO=3.46  KP=3.09  IS=1e-30  N=10  TOS=1  L=1u  W=1u)
Vto  21  6  .74
Rsource  8  7  RDSMOD  34.82e-3
Rdrain  5  16  RDSMOD  13.3e-3
.MODEL RDSMOD RES (TCl=6.5e-3  TC2=3.28e-5)
.MODEL RVTOMOD RES (TCl=-4.30e-3  TC2=-3.77e-6)
.MODEL RVTOMOD2 RES (TCl=0  TC2=0)
Ebreak  11  7  17  18  102.35
.MODEL RBKMOD RES (TCl=8.33e-1  TRS1=7.81e-4  TRS2=-9.28e-6)
.MODEL DBKMOD D (RS=3.83e-1  TRS1=7.81e-4  TRS2=-9.28e-6)
.MODEL DBDMOD D (IS=8.16e-13  RS=1.54e-2  TRS1=1.77e-3  TRS2=1.85e-5)
+CJO=9.16e-10  TT=7e-8
Cin  6  8  4.44e-10
Ca  12  8  9.14e-10
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-3.66  VOFF=-1.66)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-1.66  VOFF=-3.66)
.MODEL DPLCAPMOD D (CJO=4.90e-10  IS=1e-30  N=10)
Cb  12  14  5.81e-10
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=3.07  VOFF=8.07)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON8.07  VOFF=3.07)
Rgate  9  20  20.43
Lgate  1  9  1.32e-8
Ldrain  2  5  1.0e-10
Lsource  3  7  1.68e-8
Dbody  7  5  DBDMOD
Dbreak  5  11  DBKMOD
Dplcap  10  5  DPLCAPMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Evto  20  6  18  8  1
It  8  17  1
Mos  16  6  8  8  MOSMOD  M=0.99
MOS2  16  21  8  8  MOSMOD  M=0.01
Rbreak  17  18  RBKMOD  1
Rin  6  8  1e9
Rvto  18  19  RVTOMOD  1
Sla  6  12  13  8  S1AMOD
Slb  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
.ENDS
```



Spice Model (RFM15N06)

```
.SUBCKT RFM15N06  2  1  3;  rev 01/07/91
*Nominal Temperature = 25°C
.MODEL MOSMOD NMOS (VTO=3.46  KP=3.09  IS=1e-30  N=10  TOS=1  L=1u  W=1u)
Vto  21  6  .74
Rsource  8  7  RDSMOD  34.82e-3
Rdrain  5  16  RDSMOD  13.3e-3
.MODEL RDSMOD RES (TCI=6.5e-3  TC2=3.28e-5)
.MODEL RVTOMOD RES (TCI=-4.30e-3  TC2=-3.77e-6)
.MODEL RVTOMOD2 RES (TCI=0  TC2=0)
Ebreak  11  7  17  18  102.35
.MODEL RBKMOD RES (TCI=8.33e-1  TRS1=7.81e-4  TRS2=-9.28e-6)
.MODEL DBKMOD D (RS=3.83e-1  TRS1=7.81e-4  TRS2=-9.28e-6)
.MODEL DBDMOD D (IS=8.16e-13  RS=1.54e-2  TRS1=1.77e-3  TRS2=1.85e-5 +CJO=9.16e-10  TT=7e-8)
Cin  6  8  4.44e-10
Ca  12  8  9.14e-10
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-3.66  VOFF=-1.66)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-1.66  VOFF=-3.66)
.MODEL DPLCAPMOD D (CJO=4.90e-10  IS=1e-30  N=10)
Cb  12  14  5.81e-10
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=3.07  VOFF=8.07)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=8.07  VOFF=3.07)
Rgate  9  20  20.43
Lgate  1  9  1.32e-8
Ldrain  2  5  1.0e-10
Lsource  3  7  1.68e-8
Dbody  7  5  DBDMOD
Dbreak  5  11  DBKMOD
Dplcap  10  5  DPLCAPMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Evto  20  6  18  8  1
It  8  17  1
Mos  16  6  8  8  MOSMOD  M=0.99
MOS2  16  21  8  8  MOSMOD  M=0.01
Rbreak  17  18  RBKMOD  1
Rin  6  8  1e9
Rvto  18  19  RVTOMOD  1
S1a  6  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
.ENDS
```



RFM15N12/15N15
RFP15N12/15N15

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 15A, 120V and 150V
- $r_{DS(on)} = 0.15\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

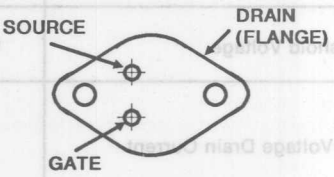
Description

The RFM15N12 and RFM15N15 and the RFP15N12 and RFP15N15 are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

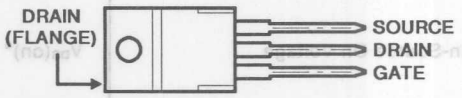
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW



TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

	RFM15N12	RFM15N15	RFP15N12	RFP15N15	UNITS
Drain-Source Voltage ..... V_{DSS}	120	150	120	150	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	120	150	120	150	V
Continuous Drain Current					
RMS Continuous ..... I_D	15	15	15	15	A
Pulsed Drain Current ..... I_{DM}	40	40	40	40	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	100	100	75	75	W
Above $T_C = +25^oC$, Derate Linearly	0.8	0.8	0.6	0.6	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1443**

Specifications RFM15N12, RFM15N15, RFP15N12, RFP15N15

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	RFM15N12 RFP15N12		RFM15N15 RFP15N15		UNITS
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1$ mA, $V_{GS} = 0$	120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 1$ mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100$ V	—	1	—	—	μA
		$V_{DS} = 120$ V	—	—	—	1	
		$V_{DS} = 100$ V, $T_C = 125°C$	—	50	—	—	
		$V_{DS} = 120$ V, $T_C = 125°C$	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20$ V, $V_{DS} = 0$	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	$I_D = 7.5$ A, $V_{GS} = 10$ V	—	1.125	—	1.125	V
		$I_D = 15$ A, $V_{GS} = 10$ V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	$I_D = 7.5$ A, $V_{GS} = 10$ V	—	0.15	—	0.15	Ω
Forward Transconductance	g_{fs}[a]	$V_{DS} = 10$ V, $I_D = 7.5$ A	5	—	5	—	mho
Input Capacitance	C_{iss}	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1MHz	—	1700	—	1700	pF
Output Capacitance	C_{oss}		—	750	—	750	
Reverse Transfer Capacitance	C_{rss}		—	350	—	350	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75 V, $I_D = 7.5$ A, $R_{gen} = R_{gs} = 50\ \Omega$, $V_{GS} = 10$ V	50(typ.)	75	50(typ.)	75	ns
Rise Time	t_r		150(typ.)	225	150(typ.)	225	
Turn-Off Delay Time	$t_d(off)$		185(typ.)	280	185(typ.)	280	
Fall Time	t_f		125(typ.)	190	125(typ.)	190	
Thermal Resistance Junction-to-Case	$R\theta JC$	RFM15N12, RFM15N15	—	1.25	—	1.25	°C/W
		RFP15N12, RFP15N15	—	1.67	—	1.67	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM15N12 RFP15N12		LIMITS RFM15N15 RFP15N15		UNITS
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=7.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A, d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

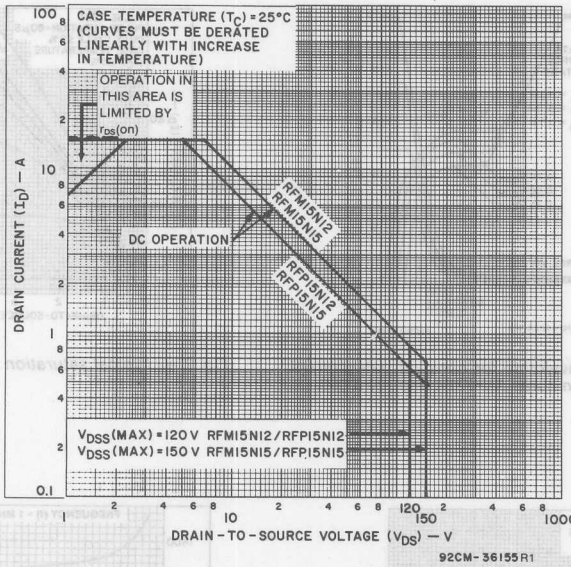


Fig. 1 — Maximum operating areas for all types.

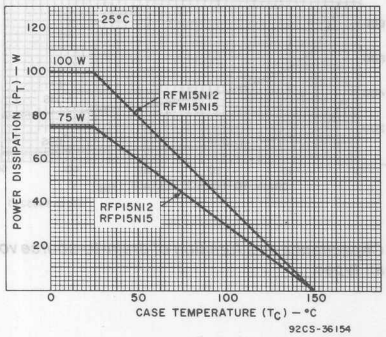


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

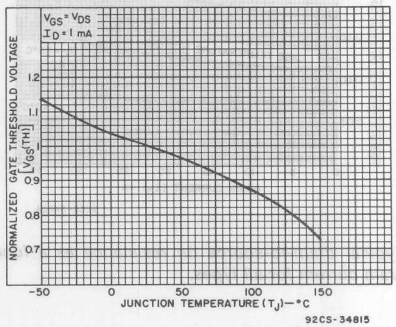


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

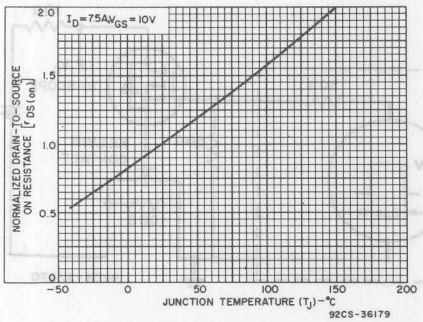


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

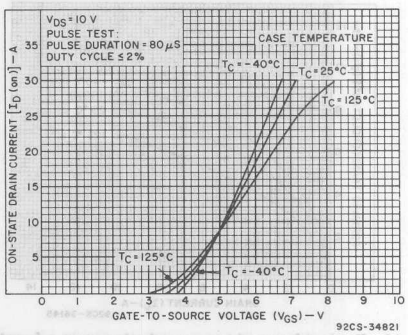


Fig. 5 — Typical transfer characteristics for all types.

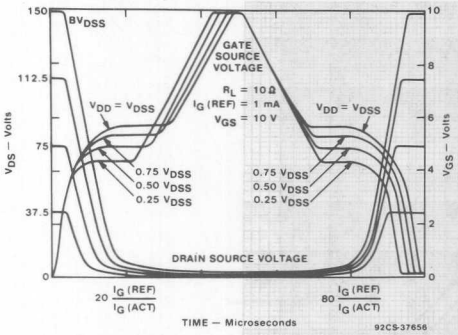


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

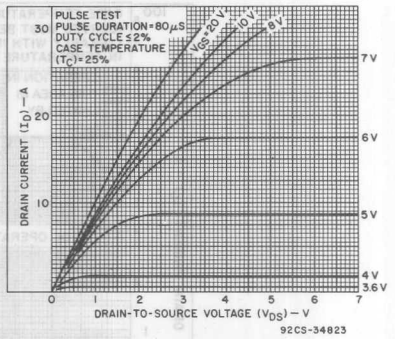


Fig. 7 — Typical saturation characteristics for all types.

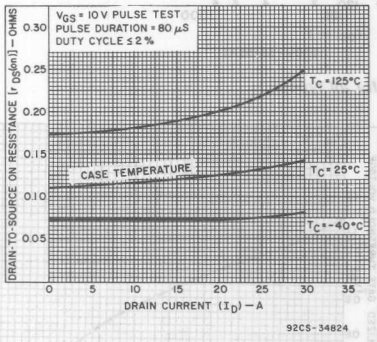


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

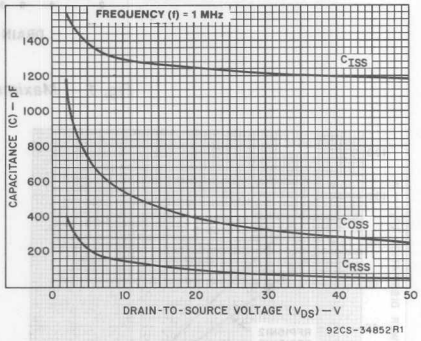


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

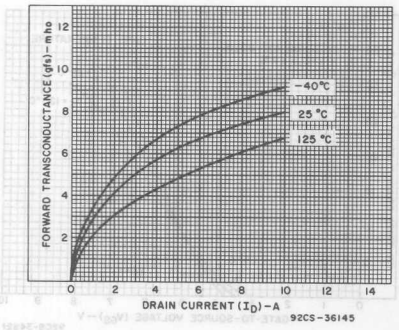


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

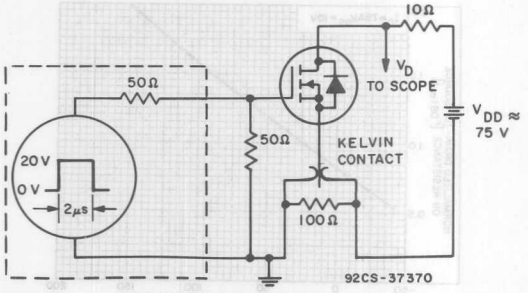


Fig. 11 — Switching Time Test Circuit

RFD16N05
RFD16N05SM

N-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

May 1992

Features

- 16A, 50V
- $r_{DS(on)} = 0.047\ \Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature

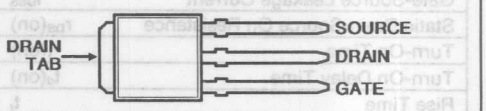
Description

The RFD16N05 and RFD16N05SM n-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFD16N05 is supplied in the JEDEC TO-251AA plastic package and the RFD16N05SM in the TO-252AA plastic package.

Packages

TO-251AA
TOP VIEW

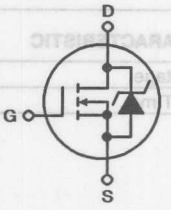


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25°C$), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS}	50V
Drain-Gate Voltage, ($R_{GS} = 1m\Omega$), V_{DGR}	50V
Gate-Source Voltage, V_{GS}	±20V
Drain Current:	
RMS Continuous, I_D	16A
Pulsed, I_{DM}	45A
Single Pulse Avalanche Rating, Refer to UIS SOA	
Power Dissipation, P_D:	
$T_C = +25°C$	72W
Derate Above $T_C = +25°C$	0.48W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55 to +175°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2267.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified:*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V		—	1	μA
		T_C = 150° C			50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D = 16 A, V_{GS} = 10 V		—	0.047	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 8 A, I_{g1} = I_{g2} = 0.4 A, V_{GS} (clamp) + 10 V, − 0.6 V, R_L = 3.125 Ω		—	60	ns
Turn-On Delay Time	$t_d(on)$			—	14 (typ.)	ns
Rise Time	t_r			—	30 (typ.)	ns
Turn-Off Delay Time	$t_d(off)$			—	52 (typ.)	ns
Fall Time	t_f			—	16 (typ.)	ns
Turn-Off Time	t(off)			—	100	ns
Total Gate Charge	Q_g(total)	V_{GS} = 0-20 V	V_{DD} = 40 V	—	80	nC
Gate Charge at 10 V	$Q_g(10)$	V_{GS} = 0-10 V	I_D = 16 A	—	45	nC
Threshold Gate Charge	$Q_g(th)$	V_{GS} = 0-2 V	R_L = 2.5 Ω	—	3	nC
Plateau Voltage	V(plateau)	I_D = 16 A, V_{DS} = 15 V		—	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 8 A, R_L = 3.125 Ω, L = 0.2 μH, I_{g1} = I_{g2} = 0.4 A, V_{GS} (clamp) + 10 V, −0.6 V		—	19	μJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$			—	2.083	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			—	100	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 16 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 16 A, dI_F/d_t = 100 A/μs	—	125	ns

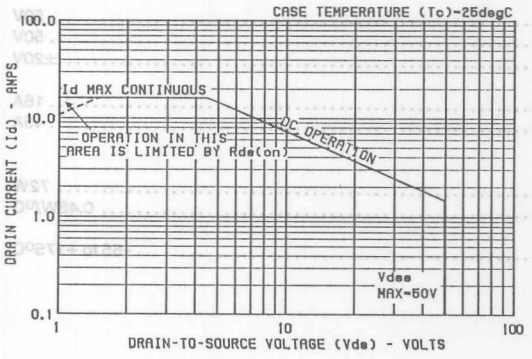


Fig. 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

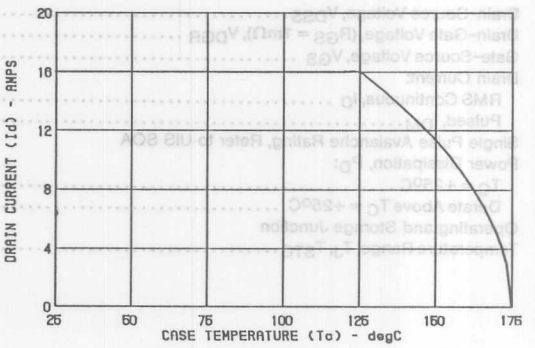


Fig. 2 - Maximum continuous drain current vs. temperature.

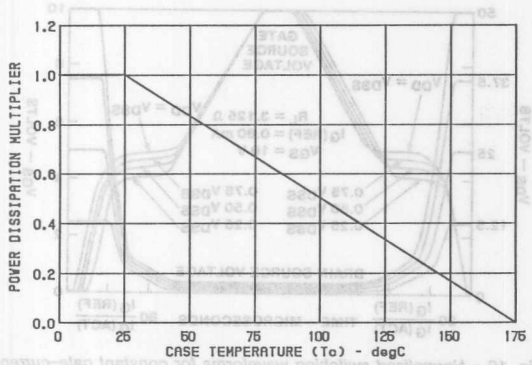


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

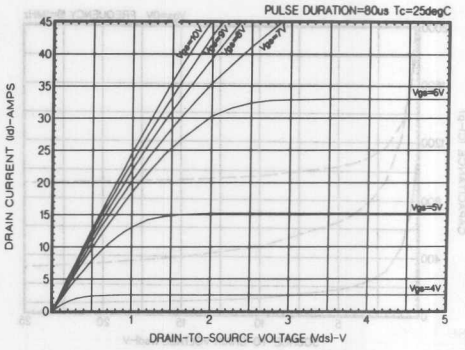


Fig. 4 - Typical saturation characteristics.

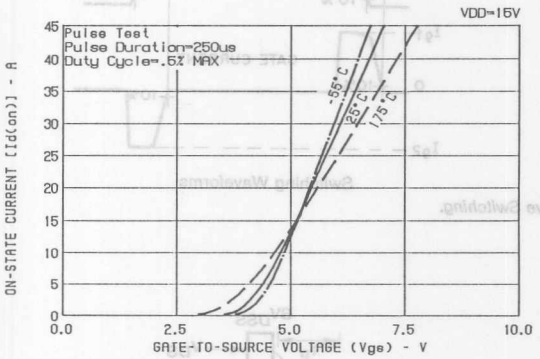


Fig 5 - Typical transfer characteristics.

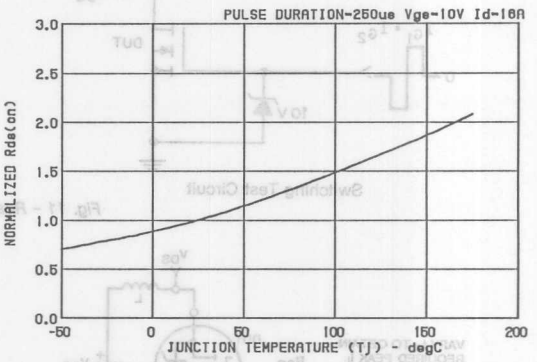


Fig 6 - Normalized $R_{ds}(on)$ vs. junction temperature.

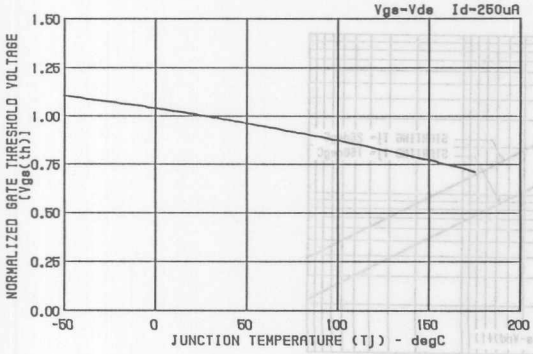


Fig. 7 - Normalized gate threshold voltage.

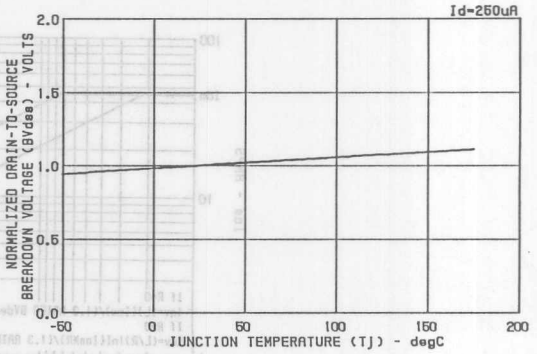


Fig. 8 - Normalized drain source breakdown voltage vs. temperature.

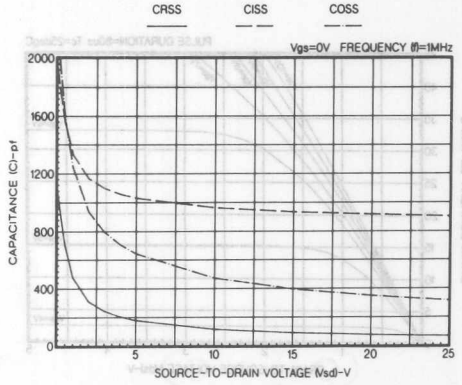


Fig. 9 – Typical capacitance vs. voltage.

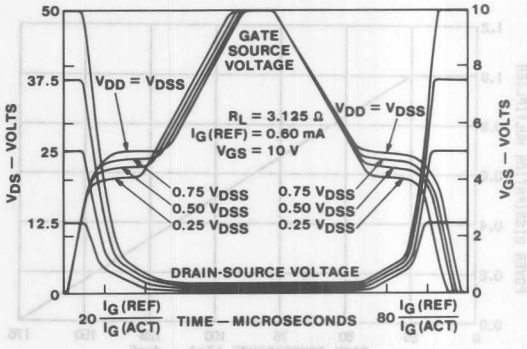
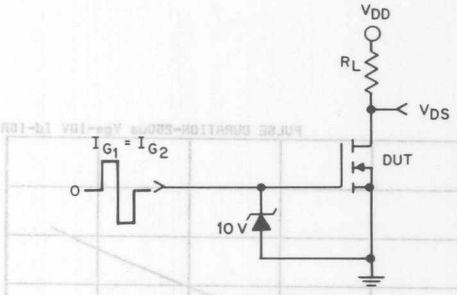


Fig. 10 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.



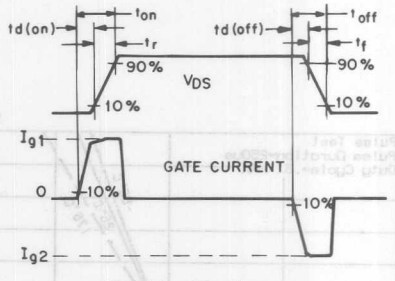


Fig. 11 – Resistive Switching.

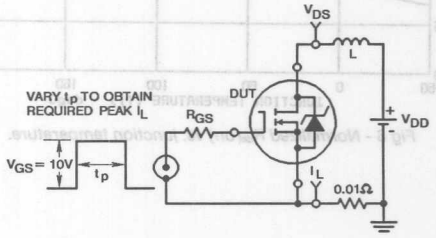


Fig. 12 – Unclamped energy test circuit.

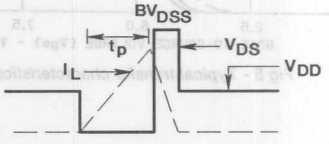


Fig. 13 – Unclamped energy waveforms.

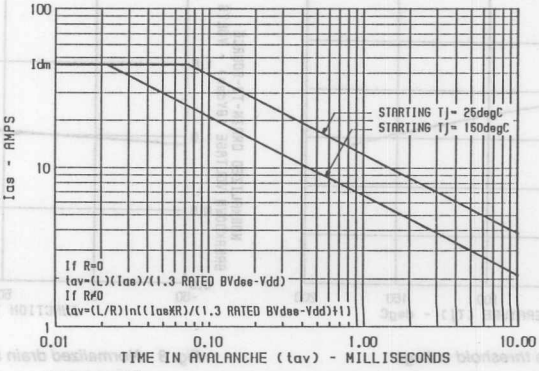


Fig. 14 – Unclamped-Inductive-Switching SOA. (Single Pulse UIS SOA)

RFM18N08/18N10
RFP18N08/18N10

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 18A, 80V and 100V
- $r_{DS(on)} = 0.1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

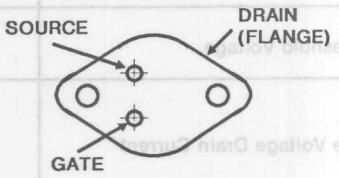
Description

The RFM18N08 and RFM18N10 and the RFP18N08 and RFP18N10 are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

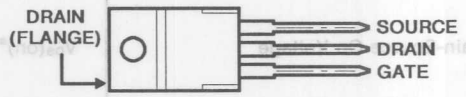
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

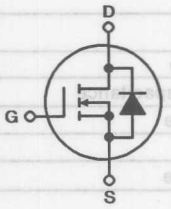


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

	RFM18N08	RFM18N10	RFP18N08	RFP18N10	UNITS
Drain-Source Voltage ..... V_{DSS}	80	100	80	100	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	80	100	80	100	V
Continuous Drain Current					
RMS Continuous ..... I_D	18	18	18	18	A
Pulsed Drain Current ..... I_{DM}	45	45	45	45	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	100	100	75	75	W
Above $T_C = +25^oC$, Derate Linearly	0.8	0.8	0.6	0.6	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1446**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM18N08 RFP18N08 MIN.	LIMITS RFM18N08 RFP18N08 MAX.	LIMITS RFM18N10 RFP18N10 MIN.	LIMITS RFM18N10 RFP18N10 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1$ mA, $V_{GS} = 0$	80	—	100	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 1$ mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 65$ V	—	1	—	—	μA
		$V_{DS} = 80$ V	—	—	—	1	
		$T_C = 125°C$, $V_{DS} = 65$ V	—	50	—	—	
		$T_C = 125°C$, $V_{DS} = 80$ V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20$ V, $V_{DS} = 0$	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	$I_D = 9$ A, $V_{GS} = 10$ V	—	0.9	—	0.9	V
		$I_D = 18$ A, $V_{GS} = 10$ V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	$I_D = 9$ A, $V_{GS} = 10$ V	—	0.10	—	0.10	Ω
Forward Transconductance	g_{fs}[a]	$V_{DS} = 10$ V, $I_D = 9$ A	5	—	5	—	mho
Input Capacitance	C_{iss}	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1MHz	—	1700	—	1700	pF
Output Capacitance	C_{oss}		—	750	—	750	
Reverse Transfer Capacitance	C_{rss}		—	300	—	300	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V, $I_D = 9$ A, $R_{gen} = R_{gs} = 50\ \Omega$, $V_{GS} = 10$ V	60(typ.)	90	60(typ.)	90	ns
Rise Time	t_r		300(typ.)	450	300(typ.)	450	
Turn-Off Delay Time	$t_d(off)$		150(typ.)	225	150(typ.)	225	
Fall Time	t_f		150(typ.)	225	150(typ.)	225	
Thermal Resistance Junction-to-Case	$R\theta JC$	RFM18N08, RFM18N10	—	1.25	—	1.25	°C/W
		RFP18N08, RFP18N10	—	1.67	—	1.67	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM18N08 RFM18N10 MIN.	LIMITS RFM18N08 RFM18N10 MAX.	LIMITS RFP18N08 RFP18N10 MIN.	LIMITS RFP18N08 RFP18N10 MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=9 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A, d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

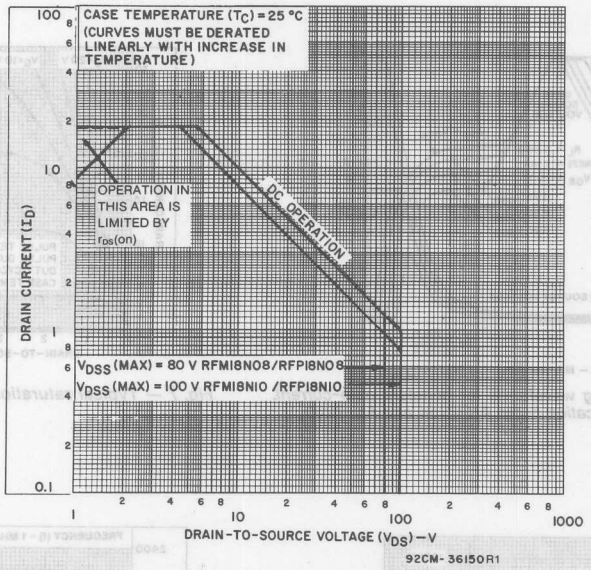


Fig. 1 — Maximum operating areas for all types.

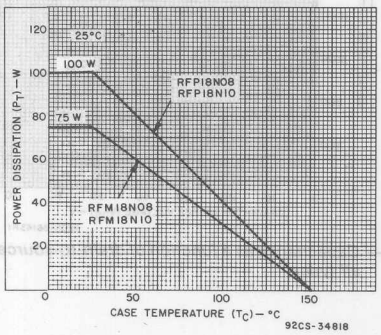


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

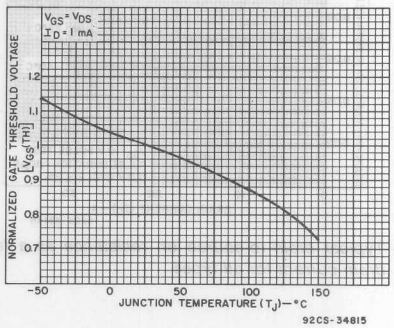


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

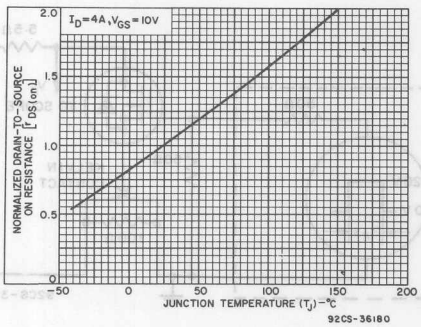


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

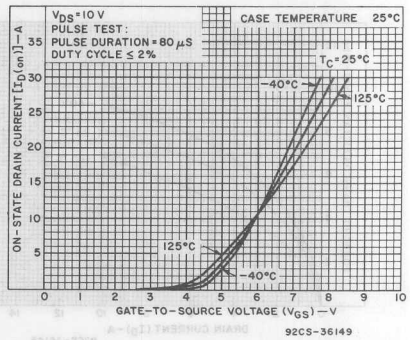


Fig. 5 — Typical transfer characteristics for all types.

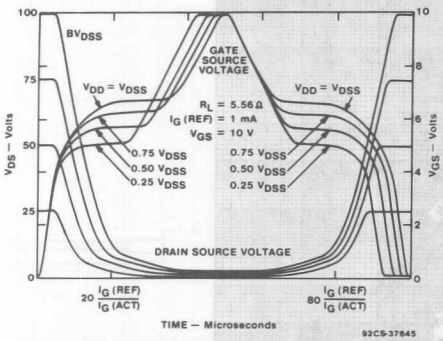


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

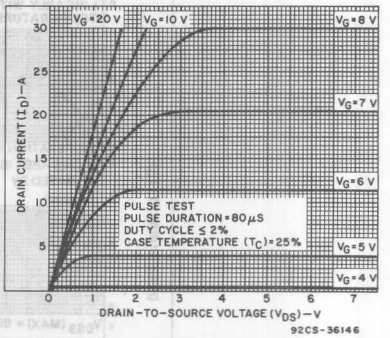


Fig. 7 — Typical saturation characteristics for all types.

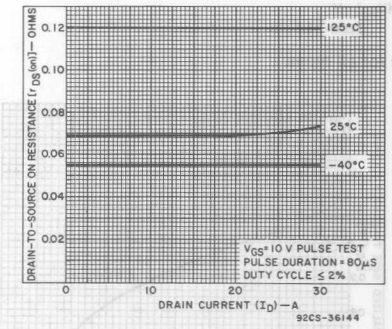


Fig. 8 – Typical drain-to-source on resistance as a function of drain current for all types.

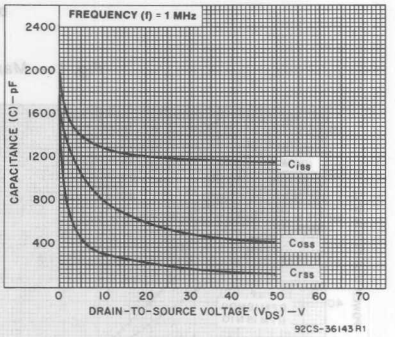


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

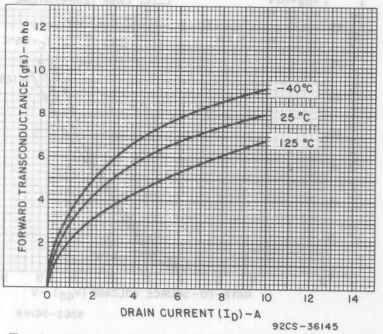


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

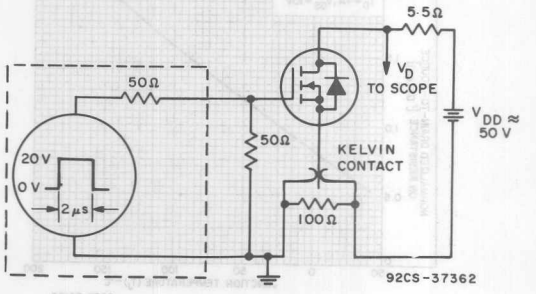


Fig. 11 — Switching Time Test Circuit

HARRIS

RFP22N10

August 1991

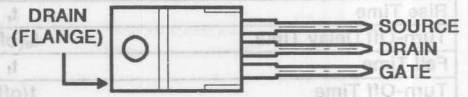
N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

Features

- 22A, 100V
- $r_{DS(on)} = 0.080\Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 175°C Operating Temperature

Package

TO-220AB
TOP VIEW



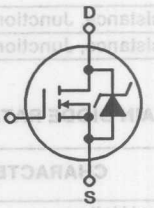
Description

The RFP22N10 n-channel power MOSFETs is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. The RFP22N10 was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. This transistor can be operated directly from integrated circuits.

The RFP22N10 is supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP22N10	UNITS
Drain-Source Voltage	V_{DSS}	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	100	V
Continuous Drain Current	I_D	22	A
Pulsed Drain Current	I_{DM}	50	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	100	W
Derated Above T_C = 25°C		0.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	°C
Single Pulse Avalanche Rating, Refer to UIS SOA Curve			

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2385.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified:*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=0.25 mA, V_{GS}=0 V		100	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$, I_D=0.25 mA		2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=80 V, V_{GS}=0 V		—	1	μA
		T_C=150°C			50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D=22 A, V_{GS}=10 V		—	0.080	Ω
Turn-On Time	t(on)	V_{DD}=50 V, I_D=11 A, $I_{g1}=I_{g2}$=0.6 A, V_{GS} (clamp): +10 V, -0.6 V, R_L=4.55 Ω, (See Fig. 12)		—	60	ns
Turn-On Delay Time	$t_d(on)$			13 (typ.)	—	ns
Rise Time	t_r			24 (typ.)	—	ns
Turn-Off Delay Time	$t_d(off)$			65 (typ.)	—	ns
Fall Time	t_f			18 (typ.)	—	ns
Turn-Off Time	t(off)			—	120	ns
Total Gate Charge	Q_g(total)	V_{GS}=0 to 20V	V_{DD}=80 V	—	150	nC
Gate Charge at 10 V	$Q_g(10)$	V_{GS}=0 to 10V	I_D=22 A	—	75	nC
Threshold Gate Charge	$Q_g(th)$	V_{GS}=0 to 2V	R_L=3.64 Ω	—	3.5	nC
Plateau Voltage	V(plateau)	I_D=22 A, V_{DS}=15 V		—	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD}=50V, I_D=11A, R_L=4.55Ω, L=0.2 μH, $I_{g1}=I_{g2}$=0.6 A, V_{GS} (clamp): +10 V, -0.6 V		—	80	μJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$			—	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			—	80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=22 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F=22 A, dI_F/d_t=100 A/μs	—	200	ns

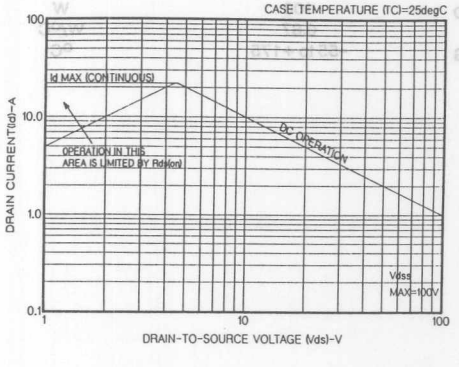


Fig. 1 - Safe-operating-area curve. (Curves must be derated linearly with increase in temperature.)

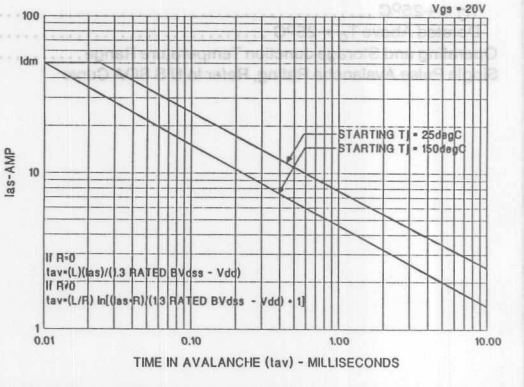


Fig. 2 - Unclamped-inductive-switching safe-operating-area curve. (Single pulse UIS SOA). See Fig. 13 for test circuit.

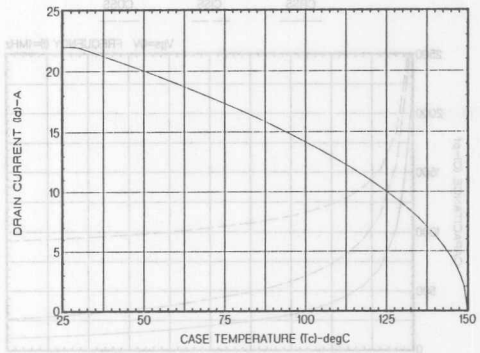


Fig. 3 - Maximum continuous drain current vs. temperature.

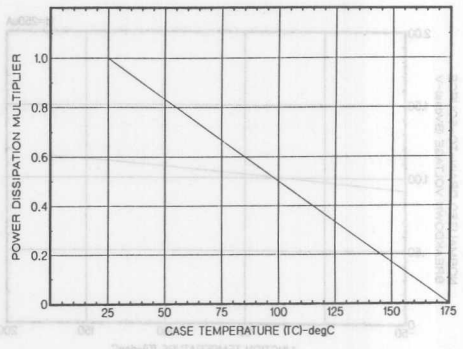


Fig. 4 - Normalized power dissipation vs. temperature derating curve.

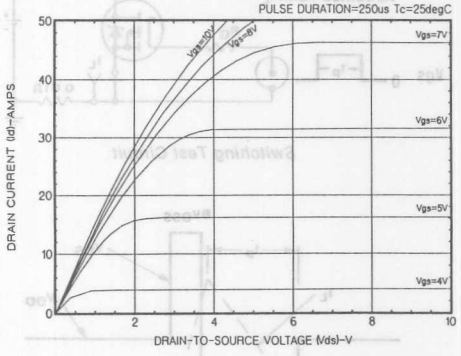


Fig. 5 - Typical saturation characteristics.

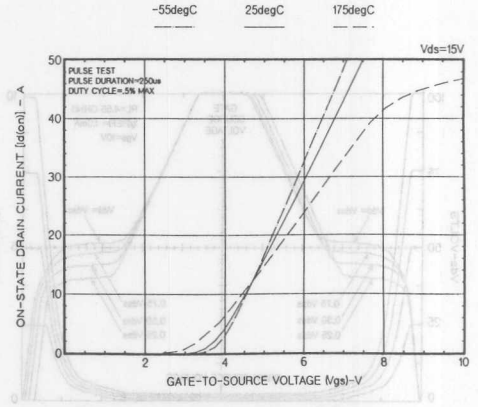


Fig. 6 - Typical transfer characteristics.

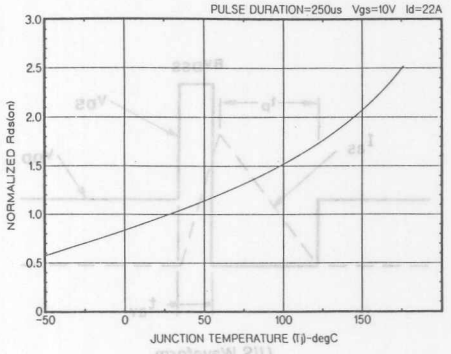


Fig. 7 - Normalized $r_{DS}(on)$ vs. junction temperature.

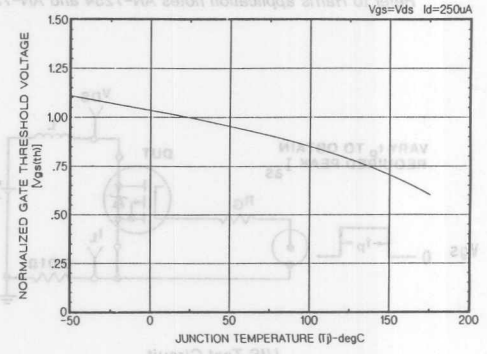


Fig. 8 - Normalized gate threshold voltage.

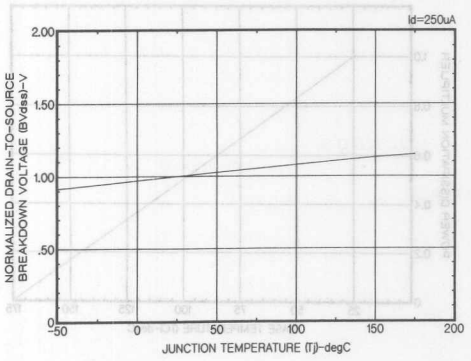


Fig. 9 - Normalized drain source breakdown voltage vs. temperature.

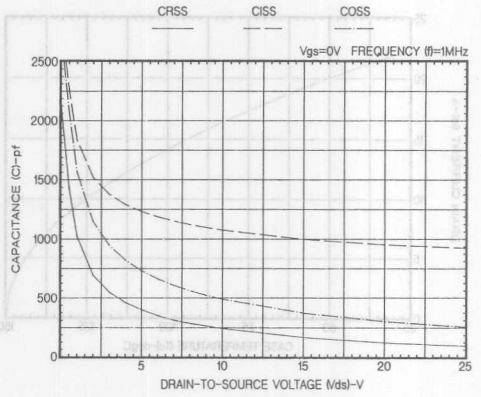


Fig. 10 - Typical capacitance vs. voltage.

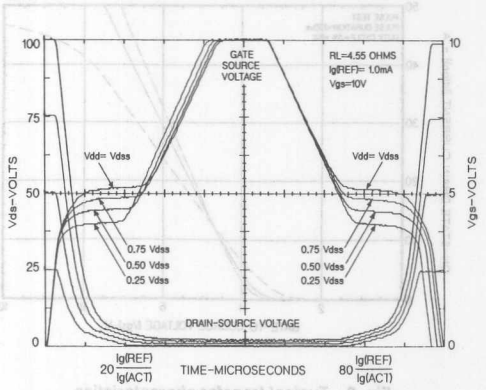


Fig. 11 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

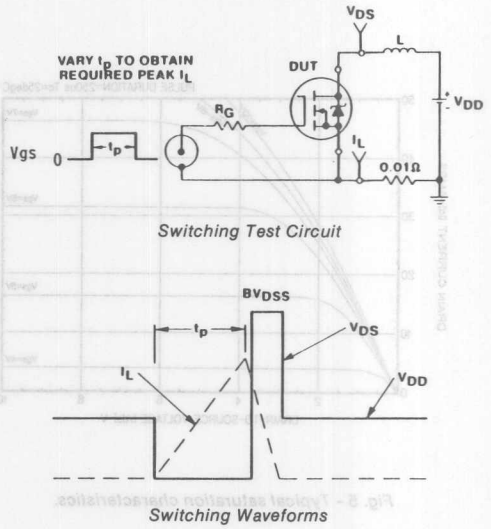
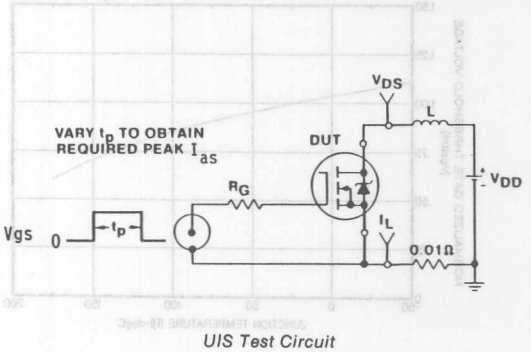


Fig. 12 - Resistive switching.



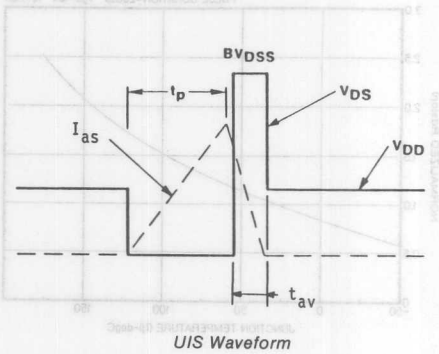


Fig. 13 - Unclamped-inductive-switching test.

HARRIS

RFP25N05

August 1991

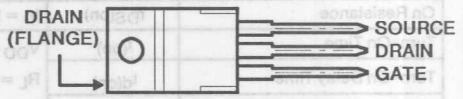
N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

Features

- 25A, 50V
- $r_{DS(on)} = 0.047\Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 175°C Operating Temperature

Package

TO-220AB
TOP VIEW



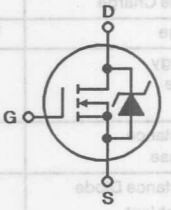
Description

The RFP25N05 n-channel power MOSFETs is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. The RFP25N05 was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. This transistor can be operated directly from integrated circuits.

The RFP25N05 is supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP25N05	UNITS
Drain-Source Voltage	V_{DSS}	50	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	V
Continuous Drain Current	I_D	25	A
Pulsed Drain Current	I_{DM}	65	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	72	W
Derated Above T_C = 25°C		0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	°C
Single Pulse Avalanche Rating, Refer to UIS SOA Curve			

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2112.1

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D =0.25mA, V_{GS} = 0V		50	–	–	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25mA		2	–	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =80V, V_{GS} = 0V		–	–	1	μA
		T_C =+150°C		–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		–	–	100	nA
On Resistance	$r_{DS(on)}$	I_D = 25A, V_{GS} = 10V		–	–	0.047	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = 25V, I_D = 12.5A, R_L = 2Ω, $I_{G1} = I_{G2}$ = 0.5A, $V_{GS(clamp)}$ = +10V, -0.6V		–	–	60	ns
Turn-On Delay Time	$t_{d(on)}$			–	14	–	ns
Rise Time	t_r			–	30	–	ns
Turn-Off Delay Time	$t_{d(off)}$			–	45	–	ns
Fall Time	t_f			–	14	–	ns
Turn-Off Time	$t_{(off)}$			–	–	100	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0 - 20V	V_{DD} = 40V	–	–	80	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0 - 10V	I_D = 25A	–	–	45	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} =0 - 2V	R_L = 1.6Ω	–	–	3	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 25A, V_{DS} = 15V		–	–	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 12.5A, $I_{G1} = I_{G2}$ = 0.5A, $V_{GS(clamp)}$ = +10V, -0.6V, L = 0.2μH, R_L = 2Ω		–	–	30	μJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			–	–	2.083	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{\theta JA}$			–	–	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 25A	–	–	1.5	V
Reverse Recovery Time	t_{rr}	I_f = 25A, dI_f/dt = 100A/μs	–	–	125	ns

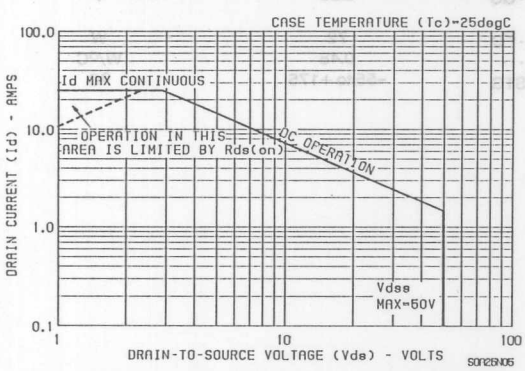


FIGURE 1. SAFE-OPERATING-AREA CURVE (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN CASE TEMPERATURE)

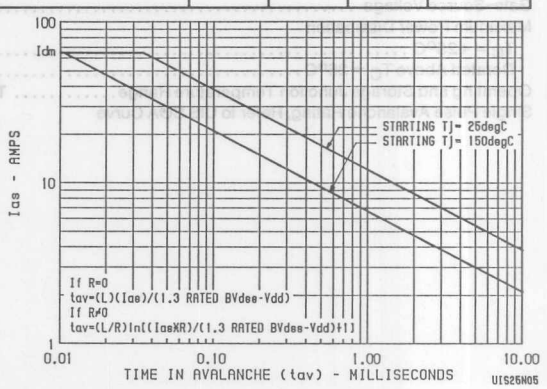


FIGURE 2. UNCLAMPED -INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

Performance Curves

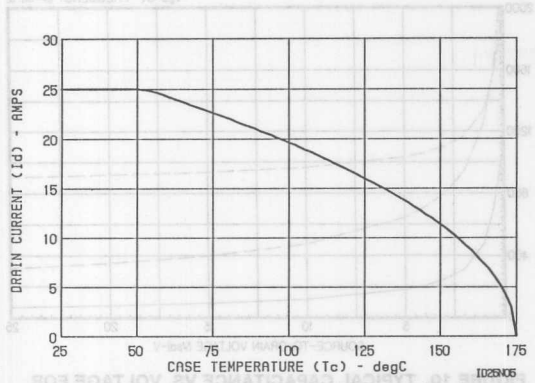


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT VS. TEMPERATURE

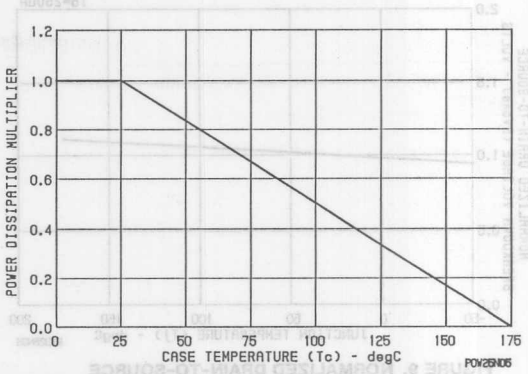


FIGURE 4. NORMALIZED POWER DISSIPTION VS. TEMPERATURE DERATING CURVE

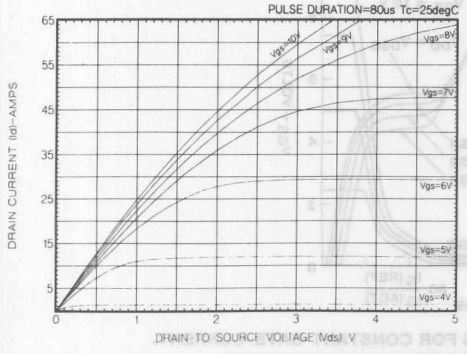


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

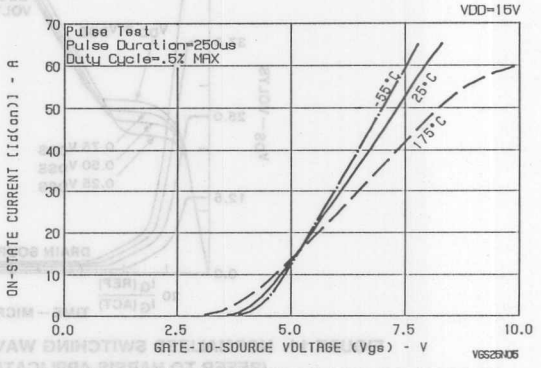


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

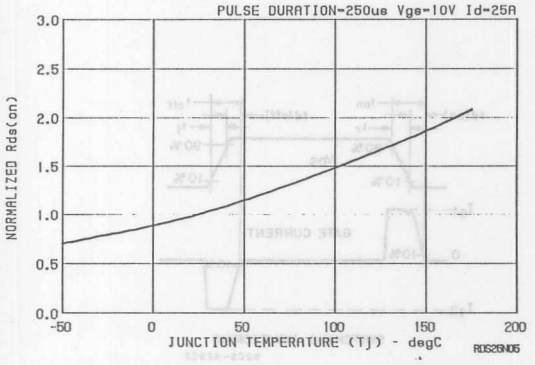


FIGURE 7. NORMALIZED $r_{DS(on)}$ VS. JUNCTION TEMPERATURE

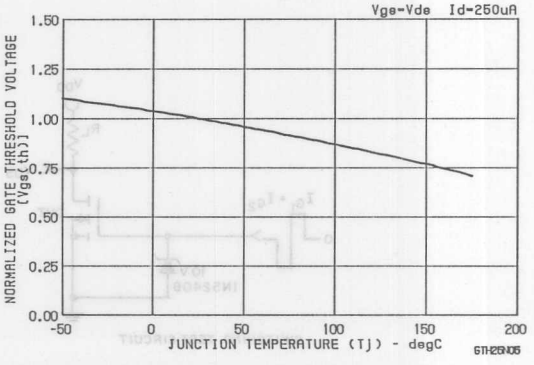


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE

4 N-CHANNEL POWER MOSFETs

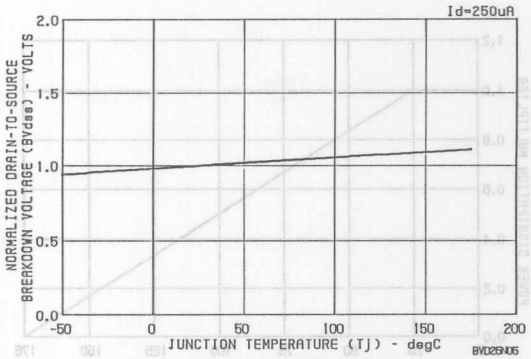


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE BREAKDOWN VOLTAGE VS. TEMPERATURE

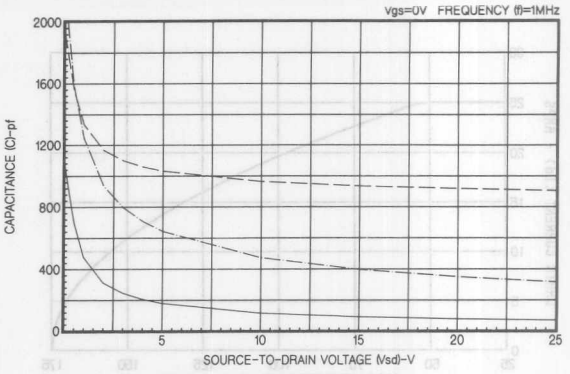


FIGURE 10. TYPICAL CAPACITANCE VS. VOLTAGE FOR ALL TYPES

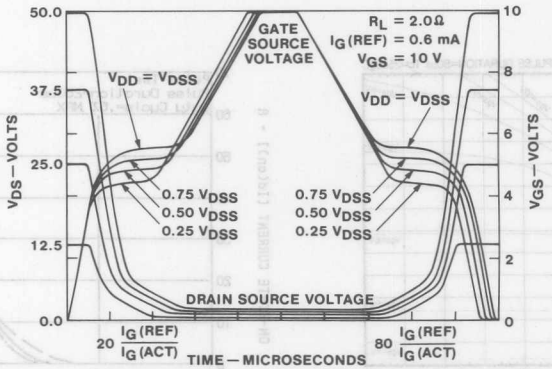
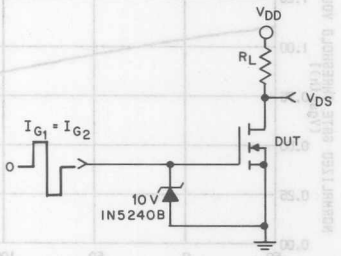
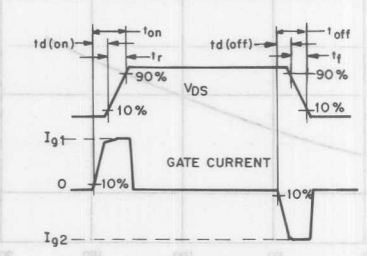


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. (REFER TO HARRIS APPLICATION NOTES AN-7254 AND AN-7260)



SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS

92CS-42922

FIGURE 12. RESISTIVE SWITCHING

Performance Curves (Continued)

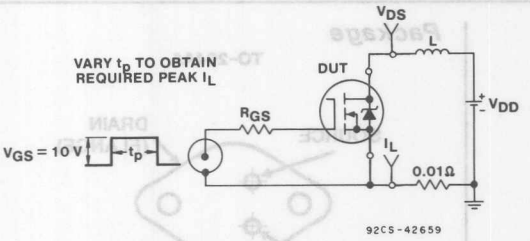


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

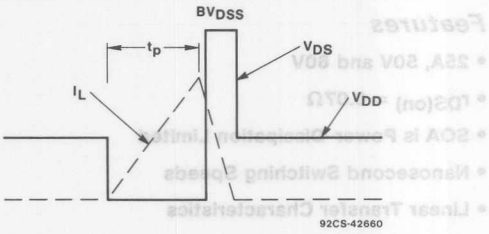


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

HARRIS

RFM25N06
RFP25N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 25A, 50V and 60V
- $r_{DS(on)} = 0.07\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

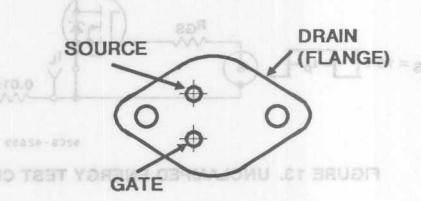
Description

The RFM25N06 and RFP25N06 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

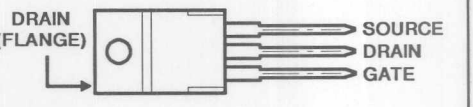
The RFM-type is supplied in the JEDEC TO-204AA steel package and the RFP-type in the JEDEC TO-220AB plastic package.

Package

TO-204AA

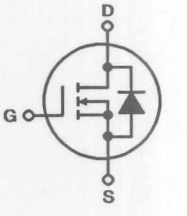


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFM25N06	RFP25N06	UNITS
Drain-Source Voltage	V_{DSS}	60	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	60	60	V
Continuous Drain Current	I_D	25	25	A
Pulsed Drain Current	I_{DM}	60	60	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	100	75	W
Linear Derating Factor		0.8	0.6	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

Caution: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1492.1**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM25N06 RFP25N06 MIN.	LIMITS RFM25N06 RFP25N06 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1$ mA, $V_{GS} = 0$	60	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 1$ mA	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40$ V	—	—	μA
		$V_{DS} = 50$ V	—	1	
		$T_c = 125$ °C, $V_{DS} = 40$ V	—	—	
		$T_c = 125$ °C, $V_{DS} = 50$ V	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20$ V, $V_{DS} = 0$	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	$I_D = 12.5$ A, $V_{GS} = 10$ V	—	0.875	V
		$I_D = 25$ A, $V_{GS} = 10$ V	—	2.5	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	$I_D = 12.5$ A, $V_{GS} = 10$ V	—	0.07	Ω
Forward Transconductance	g_{fs}[a]	$V_{DS} = 10$ V, $I_D = 12.5$ A	5	—	mho
Input Capacitance	C_{iss}	$V_{DS} = 25$ V	—	1700	pF
Output Capacitance	C_{oss}	$V_{GS} = 0$ V	—	900	
Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	—	400	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30$ V	18 (typ.)	60	ns
Rise Time	t_r	$I_D = 12.5$ A	120 (typ.)	225	
Turn-Off Delay Time	$t_{d(off)}$	$R_{gen} = R_{gs} = 50\ \Omega$	123 (typ.)	225	
Fall Time	t_f	$V_{GS} = 10$ V	123 (typ.)	200	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM25N06	—	1.25	°C/W
		RFP25N06	—	1.67	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM25N06 RFP25N06 MIN.	LIMITS RFM25N06 RFP25N06 MAX.	UNITS
Diode Forward Voltage	V_{SD}	$I_{SD} = 12.5$ A	—	1.4	V
Reverse Recovery Time	t_{rr}	$I_F = 4$ A, $dI_F/dt = 100$ A/μs	150(typ.)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

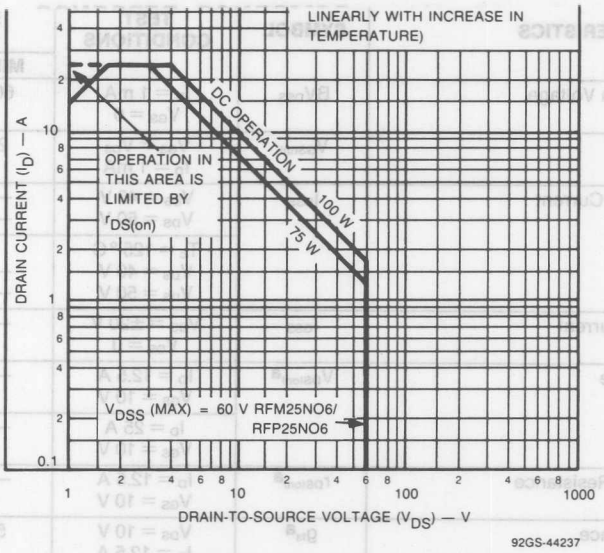


Fig. 1 — Maximum operating areas for all types.

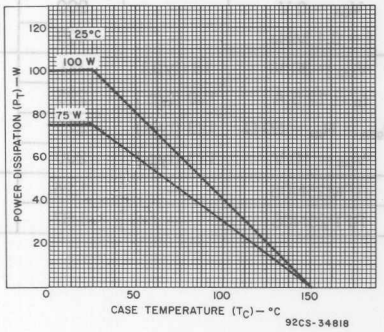


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

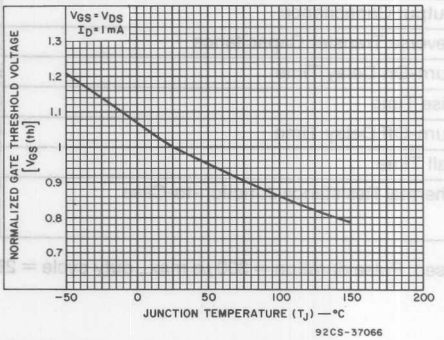


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

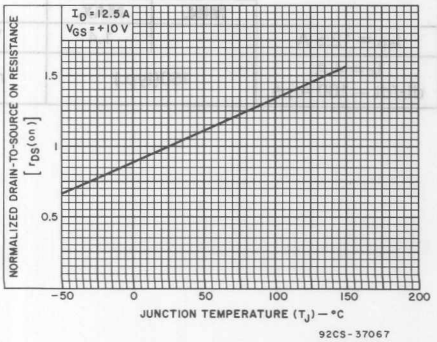


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

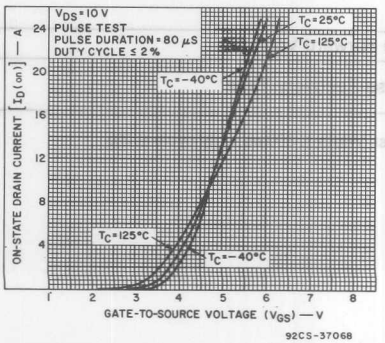


Fig. 5 — Typical transfer characteristics for all types.

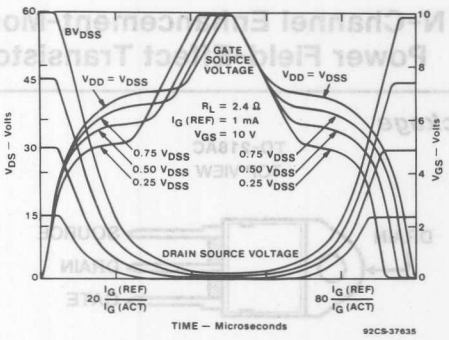


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

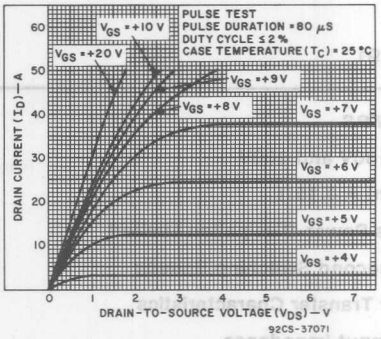


Fig. 7 — Typical saturation characteristics for all types.

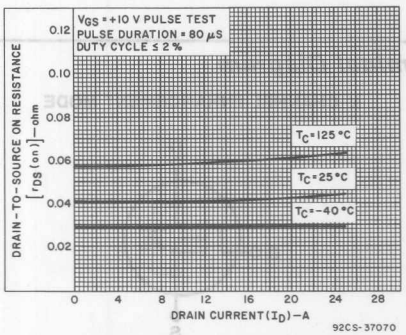


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

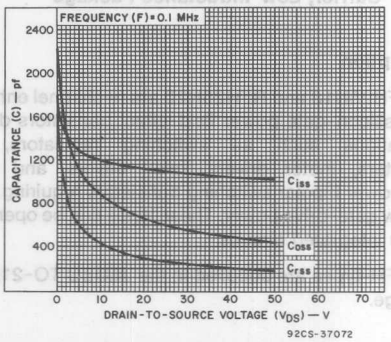


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

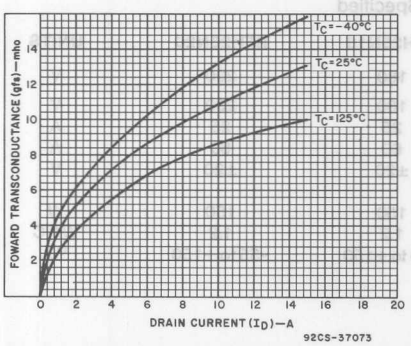


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

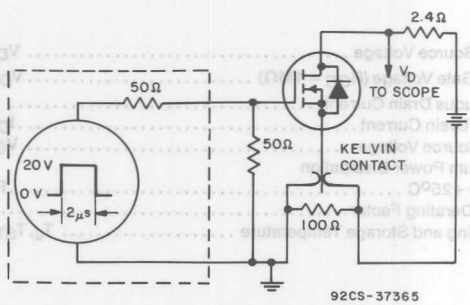


Fig. 11 — Switching Time Test Circuit

HARRIS

RFH25N18
RFH25N20

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 25A, 180V and 200V
- $r_{DS}(on) = 0.15\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Carrier, Low-Inductance Package

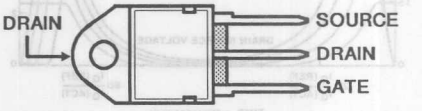
Description

The RFH25N18 and RFH25N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

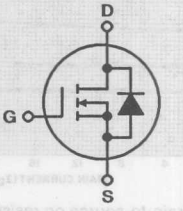
Package

TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFH25N18	RFH25N20	UNITS
Drain-Source Voltage	V_{DSS}	180	200	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	180	200	V
Continuous Drain Current	I_D	25	25	A
Pulsed Drain Current	I_{DM}	60	60	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1631.1

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH25N18		RFH25N20		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145 V V_{DS} = 160 V	— —	1 —	— —	— 1	μA
		T_C = 125° C V_{DS} = 145 V V_{DS} = 160 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 12.5 A V_{GS} = 10 V	—	1.875	—	1.875	V
		I_D = 25 A V_{GS} = 10 V	—	5	—	5	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 12.5 A V_{GS} = 10 V	—	.15	—	.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 12.5 A	7	—	7	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	3500	—	3500	pF
Output Capacitance	C_{oss}		—	900	—	900	pF
Reverse Transfer Capacitance	C_{rss}		—	400	—	400	pF
Turn-On Delay Time	$t_d(on)$	V_{DS} = 100 V I_D = 12.5 A R_{gen}=R_{gs}=50Ω V_{GS} = 10 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r		150(typ)	225	150(typ)	225	ns
Turn-Off Delay Time	$t_d(off)$		300(typ)	400	300(typ)	400	ns
Fall Time	t_f		120(typ)	200	120(typ)	200	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH25N18, RFH25N20 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH25N18		RFH25N20		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 12.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	300 (typ.)		300 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

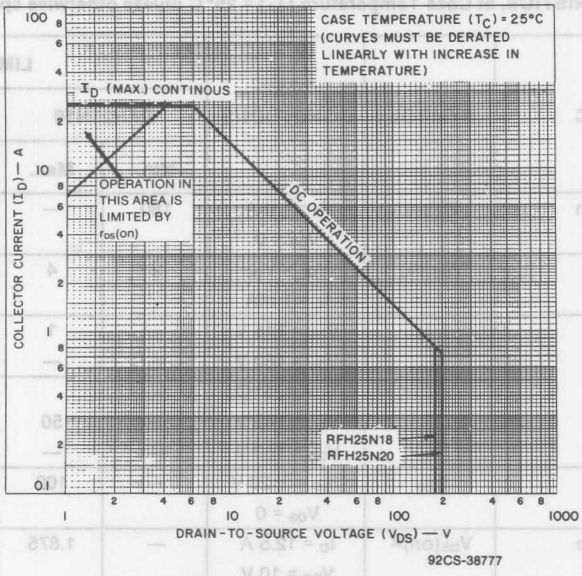


Fig. 1 - Maximum safe operating areas for all types.

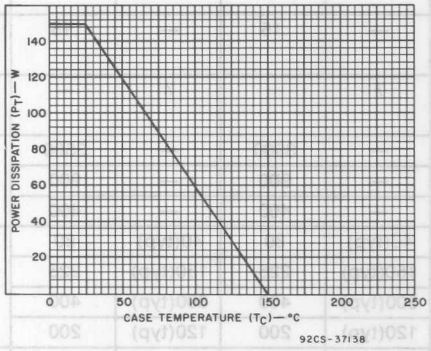


Fig. 2 - Power vs. temperature derating curve for all types.

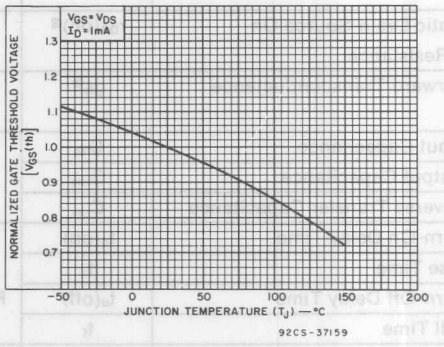


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

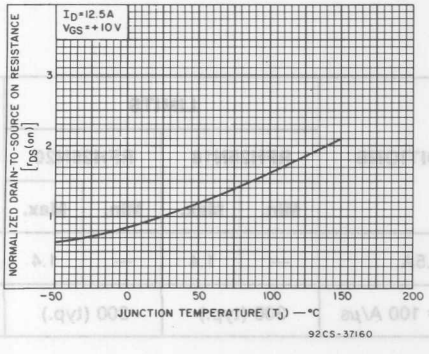


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

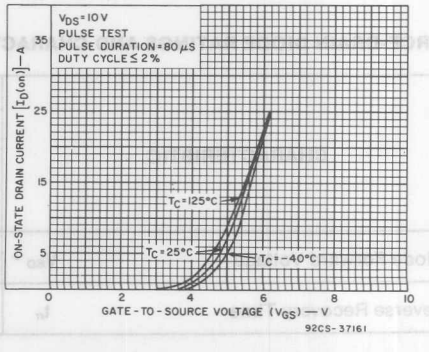


Fig. 5 - Typical transfer characteristics for all types.

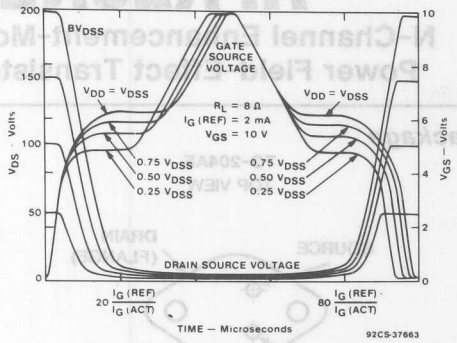


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

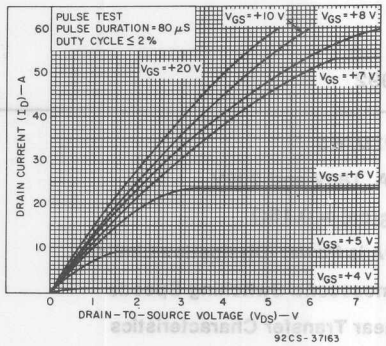


Fig. 7 - Typical saturation characteristics for all types.

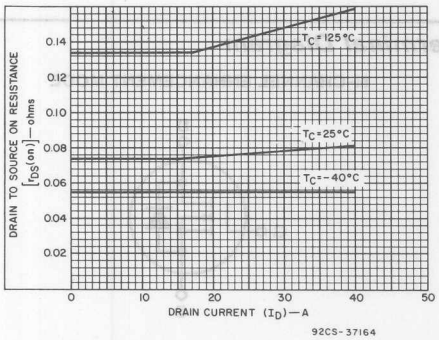


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

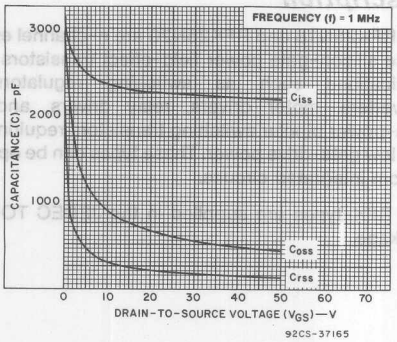


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

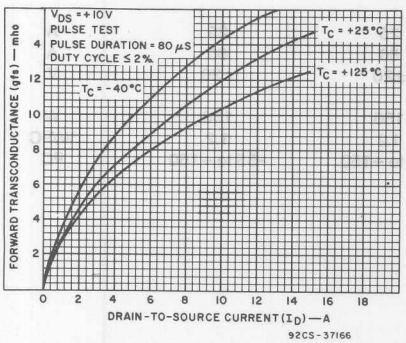


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

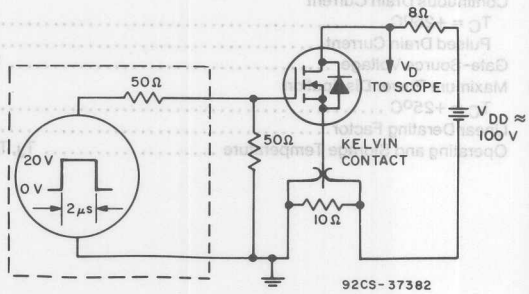


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFK25N18
RFK25N20

N-Channel Enhancement-Mode Power Field-Effect Transistors

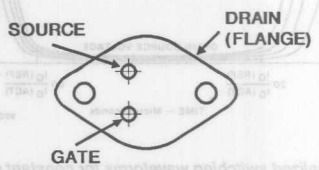
May 1992

Features

- 25A, 180V and 200V
- $r_{DS}(on) = 0.15\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AE
TOP VIEW



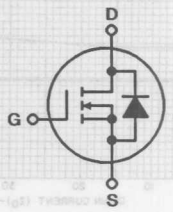
Description

The RFK25N18 and RFK25N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFK25N18	RFK25N20	UNITS
Drain-Source Voltage	V_{DSS}	180	200	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	180	200	V
Continuous Drain Current				
T_C = +25°C	I_D	25	25	A
Pulsed Drain Current	I_{DM}	60	60	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1500.2

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25N18		RFK25N20		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V V_{DS}=160 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=145 V V_{DS}=160 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=12.5 A V_{GS}=10 V	—	1.875	—	1.875	V
		I_D=25 A V_{GS}=10 V	—	5	—	5	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=12.5 A V_{GS}=10 V	—	.15	—	.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=12.5 A	7	—	7	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3500	—	3500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	900	—	900	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	400	—	400	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r	I_D=12.5 A	150(typ)	225	150(typ)	225	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	300(typ)	400	300(typ)	400	ns
Fall Time	t_f	V_{GS}=10 V	120(typ)	200	120(typ)	200	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK25N18, RFK25N20 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25N18		RFK25N20		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=12.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	300(typ)		300(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

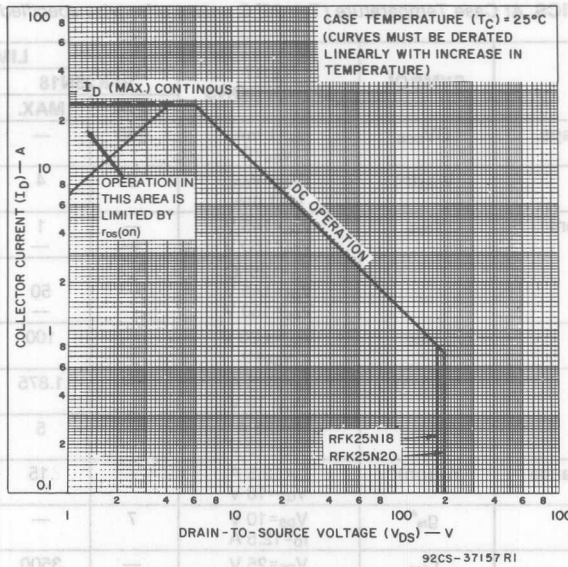


Fig. 1 — Maximum safe operating areas for all types.

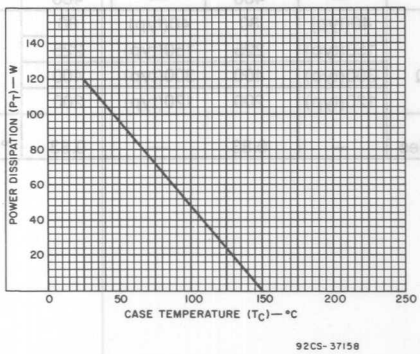


Fig. 2 — Power vs. temperature derating curve for all types.

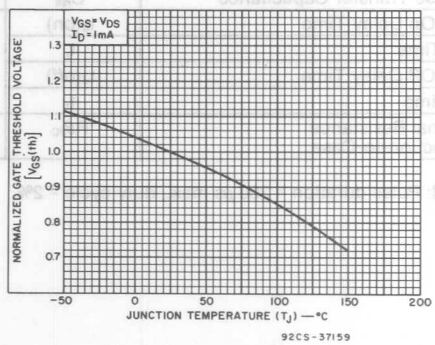


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

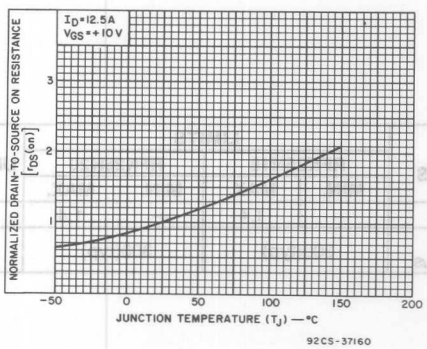


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

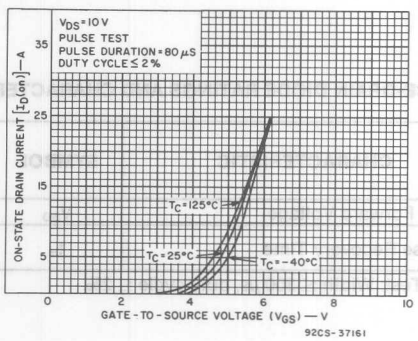


Fig. 5 — Typical transfer characteristics for all types.

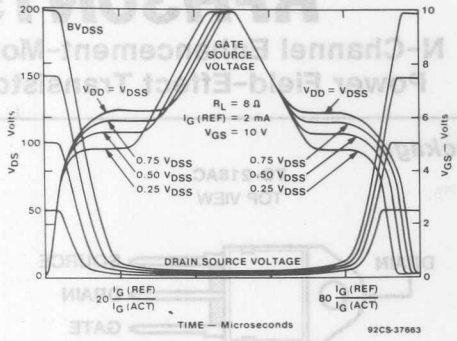


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

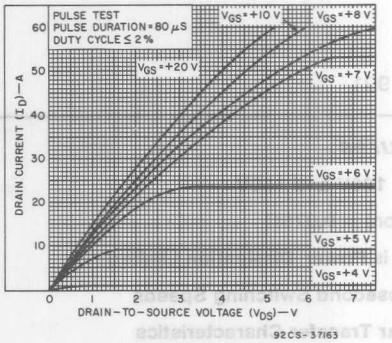


Fig. 7 — Typical saturation characteristics for all types.

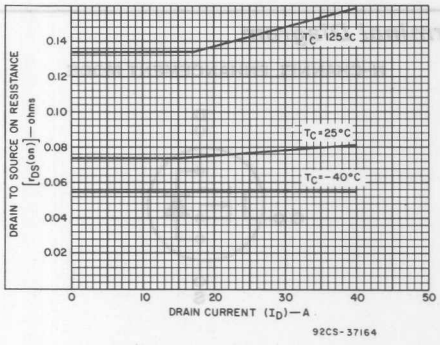


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

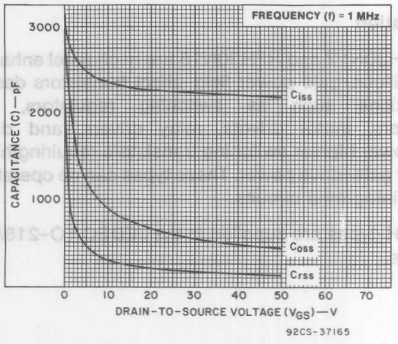


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

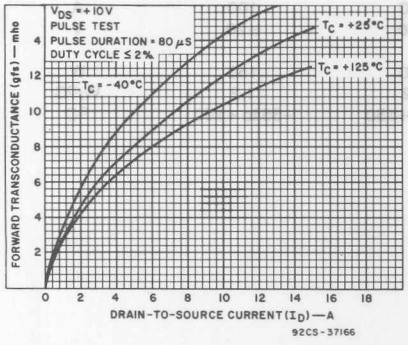


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

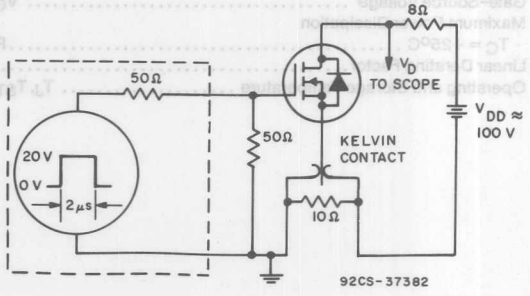


Fig. 11 — Switching Time Test Circuit

HARRIS

RFH30N12
RFH30N15

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 30A, 120V and 150V
- $r_{DS}(on) = 0.075\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Carrier, Low-Inductance Package

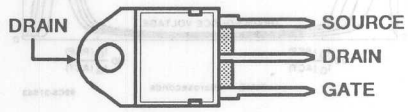
Description

The RFH30N12 and RFH30N15 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

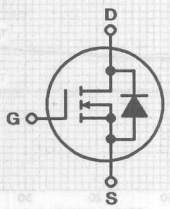
Package

TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFH30N12	RFH30N15	UNITS
Drain-Source Voltage	V_{DSS}	120	150	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	120	150	V
Continuous Drain Current	I_D	30	30	A
Pulsed Drain Current	I_{DM}	100	100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1633.1

Specifications RFH30N12, RFH30N15

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH30N12		RFH30N15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V	—	1	—	—	μA
		V_{DS} = 120 V	—	—	—	1	
		T_C = 125° C V_{DS} = 100 V	—	50	—	—	
		V_{DS} = 120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
On-State Gate Voltage	$V_{GS}(on)$[a]	V_{DS} = 5 V I_D = 15 A	—	8	—	8	V
		V_{DS} = 10 V I_D = 30 A	—	10	—	10	
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 15 A V_{GS} = 10 V	—	1.125	—	1.125	V
		I_D = 30 A V_{GS} = 10 V	—	2.65	—	2.65	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 15 A V_{GS} = 10 V	—	0.075	—	0.075	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 15 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1200	—	1200	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	500	—	500	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 75 V	75(typ)	115	75(typ)	115	ns
Rise Time	t_r	I_D = 15 A	420(typ)	630	420(typ)	630	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	300(typ)	450	300(typ)	450	
Fall Time	t_f	V_{GS} = 10 V	250(typ)	375	250(typ)	375	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH30N12, RFH30N15 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH30N12		RFH30N15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 15A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	200 (typ.)		200 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

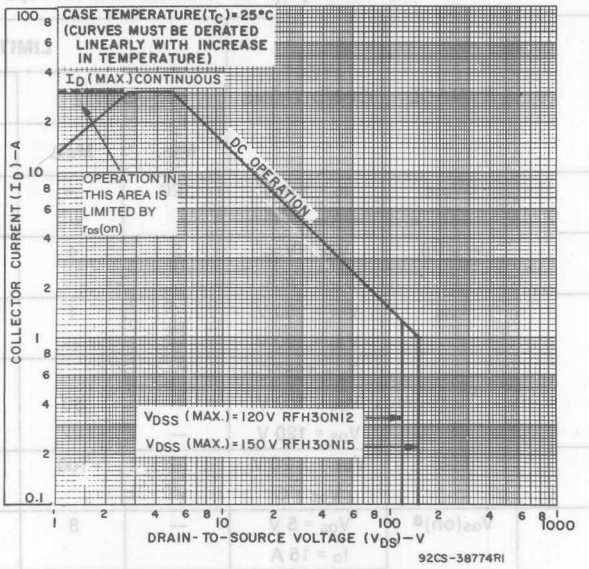


Fig. 1 - Maximum safe operating areas for all types.

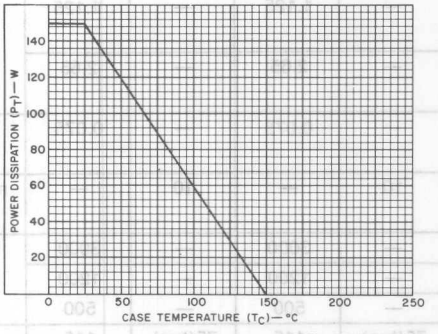


Fig. 2 - Power vs. temperature derating curve for all types.

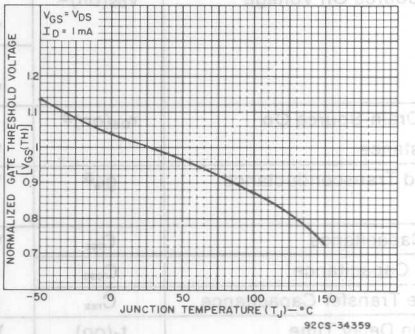


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

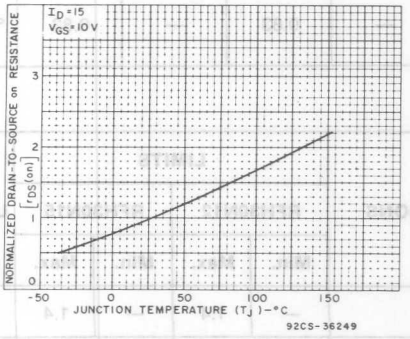


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

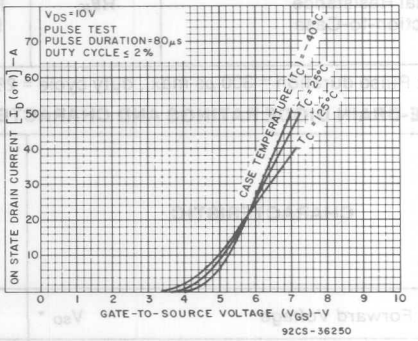


Fig. 5 - Typical transfer characteristics for all types.

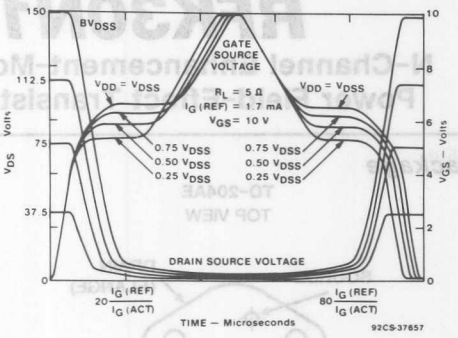


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

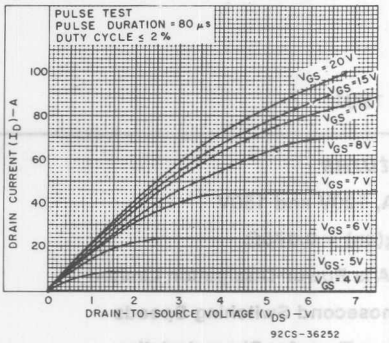


Fig. 7 - Typical saturation characteristics for all types.

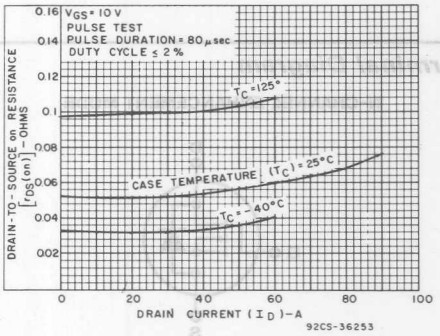


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

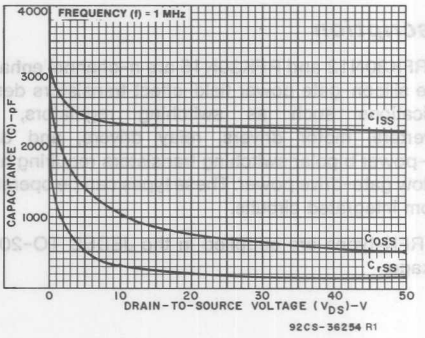


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

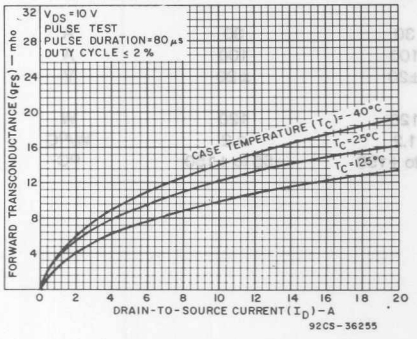


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

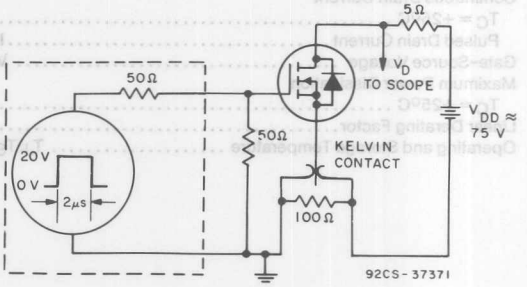


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFK30N12
RFK30N15

N-Channel Enhancement-Mode Power Field-Effect Transistors

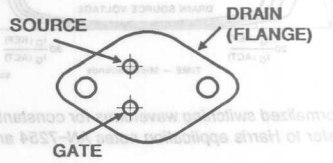
August 1991

Features

- 30A, 120V and 150V
- $r_{DS}(on) = 0.075\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AE
TOP VIEW



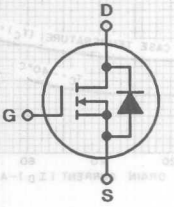
Description

The RFK30N12 and RFK30N15 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFK30N12	RFK30N15	UNITS
Drain-Source Voltage	V_{DSS}	120	150	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	120	150	V
Continuous Drain Current				
T_C = +25°C	I_D	30	30	A
Pulsed Drain Current	I_{DM}	100	100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	120	120	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1455.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK30N12		RFK30N15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V	—	1	—	—	μA
		V_{DS}=120 V	—	—	—	1	
		T_C=125° C V_{DS}=100 V	—	50	—	—	
		V_{DS}=120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}= ± 20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=15 A V_{GS}=10 V	—	1.125	—	1.125	V
		I_D=30 A V_{GS}=10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=15 A V_{GS}=10 V	—	0.075	—	0.075	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=15 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1200	—	1200	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	500	—	500	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75V	75(typ)	115	75(typ)	115	ns
Rise Time	t_r	I_D=15 A	420(typ)	630	420(typ)	630	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	300(typ)	450	300(typ)	450	
Fall Time	t_f	V_{GS}=10 V	250(typ)	375	250(typ)	375	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFK30N12, RFK30N15 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK30N12		RFK30N15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=15 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

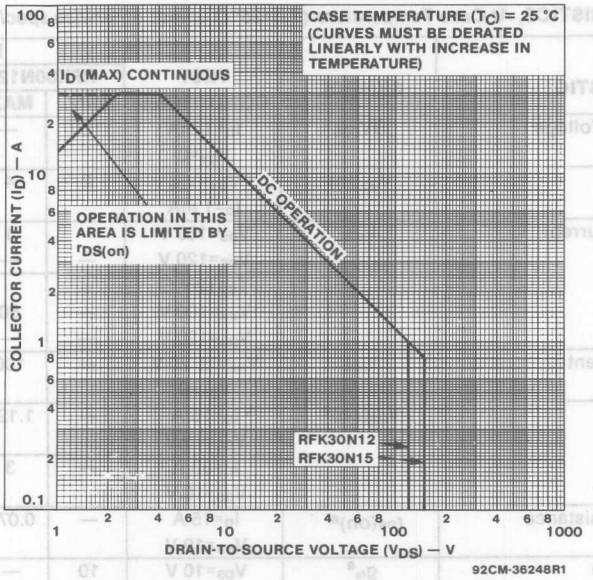


Fig. 1 - Maximum safe operating areas for all types.

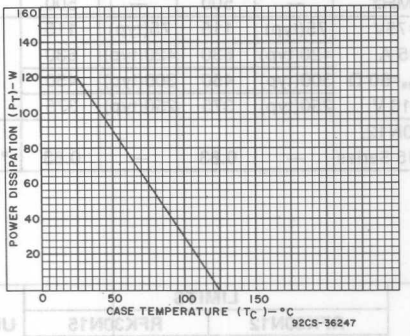


Fig. 2 - Power vs. temperature derating curve for all types.

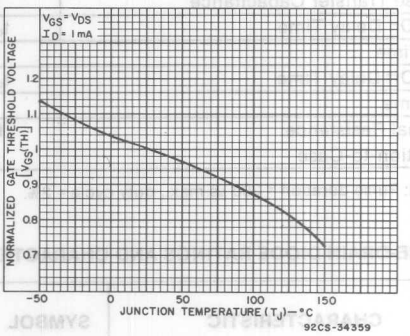


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

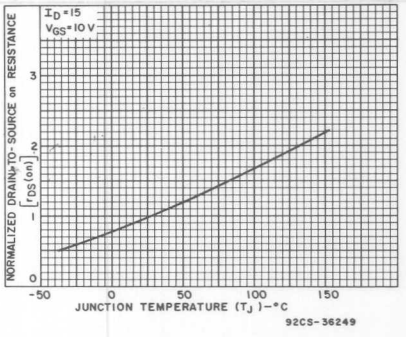


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

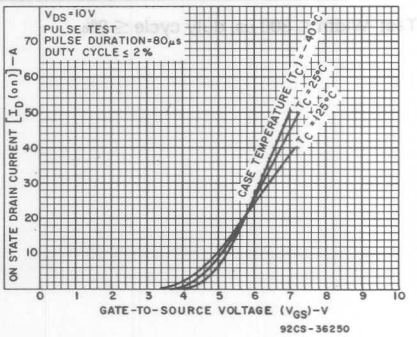


Fig. 5 - Typical transfer characteristics for all types.

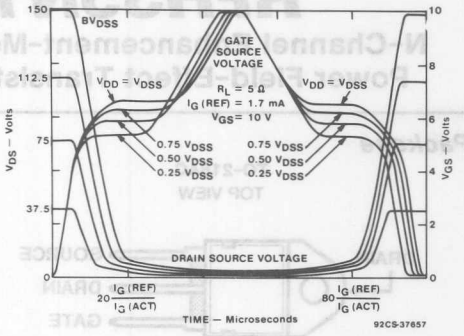


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

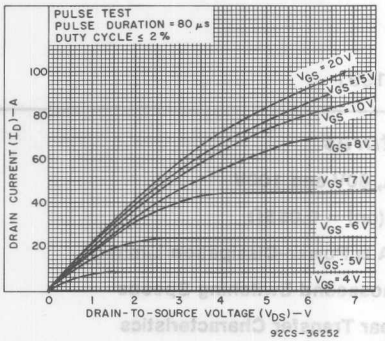


Fig. 7 - Typical saturation characteristics for all types.

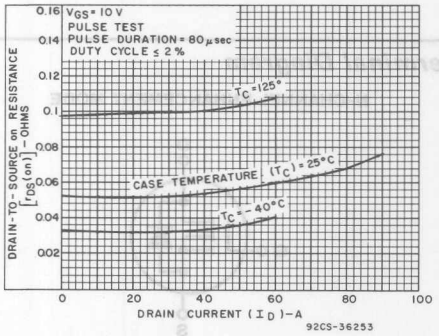


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

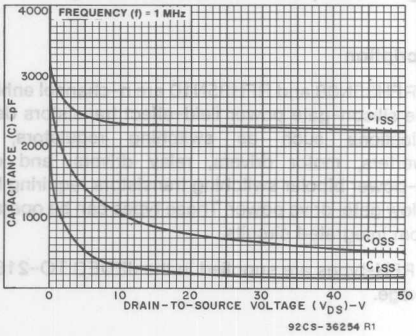


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

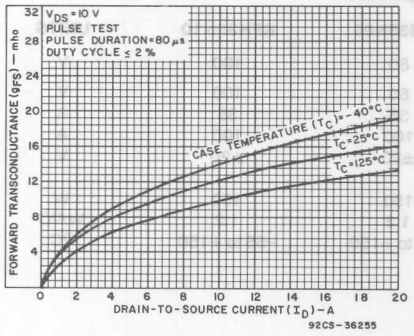


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

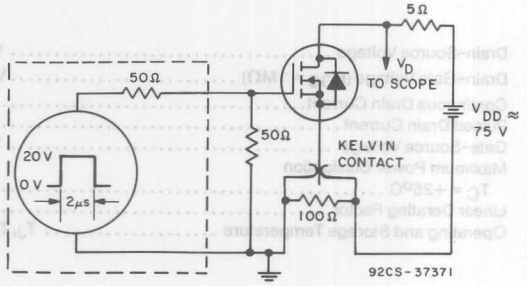


Fig. 11 — Switching Time Test Circuit

HARRIS

RFH35N08
RFH35N10

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 35A, 80V and 100V
- $r_{DS}(on) = 0.055\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Carrier, Low-Inductance Package

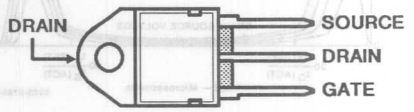
Description

The RFH35N08 and RFH35N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

Package

TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFH35N08	RFH35N10	UNITS
Drain-Source Voltage	V_{DSS}	80	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	80	100	V
Continuous Drain Current	I_D	35	35	A
Pulsed Drain Current	I_{DM}	100	100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1634.1**

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH35N08		RFH35N10		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65 V	—	1	—	—	μA
		V_{DS} = 80 V	—	—	—	1	
		T_C = 125°C					
		V_{DS} = 65 V	—	50	—	—	
		V_{DS} = 80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 17.5 A V_{GS} = 10 V	—	0.963	—	0.963	V
		I_D = 35 A V_{GS} = 10 V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 17.5 A V_{GS} = 10 V	—	0.055	—	0.055	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 17.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1500	—	1500	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	600	—	600	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	45(typ)	100	45(typ)	100	ns
Rise Time	t_r	I_D = 17.5 A	225(typ)	450	225(typ)	450	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	240(typ)	450	240(typ)	450	
Fall Time	t_f	V_{GS} = 10 V	165(typ)	350	165(typ)	350	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH35N08, RFH35N10 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH35N08		RFH35N10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}*	I_{SD} = 17.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	200 (typ.)		200 (typ.)		ns

* Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

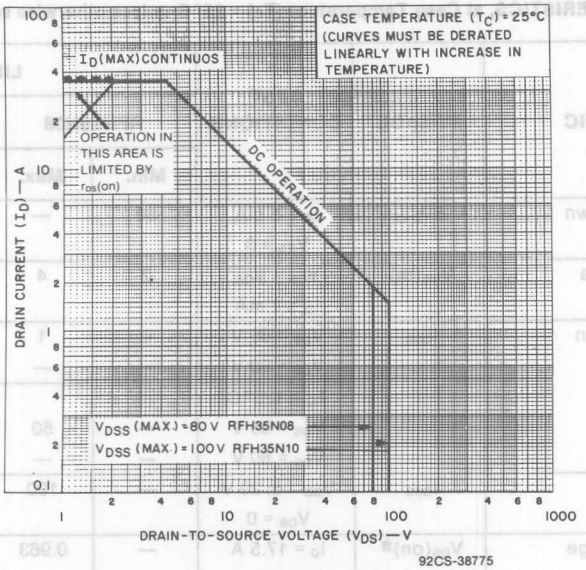


Fig. 1 - Maximum safe operating areas for all types.

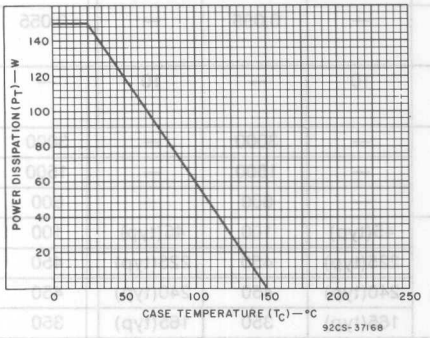


Fig. 2 - Power vs. temperature derating curve for all types.

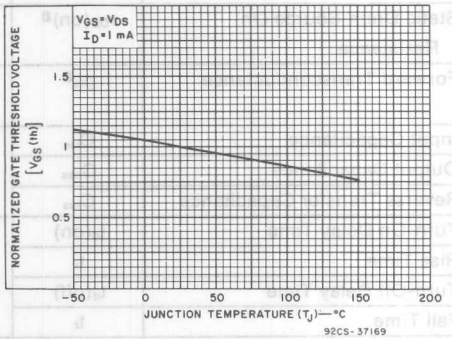


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

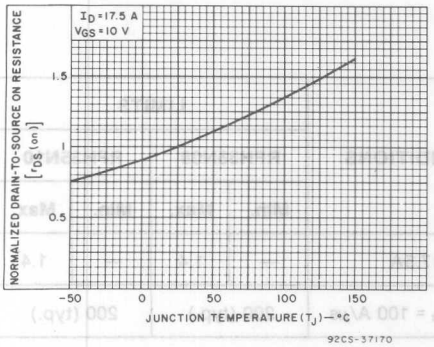


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

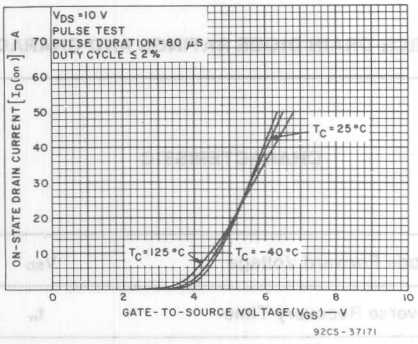


Fig. 5 - Typical transfer characteristics for all types.

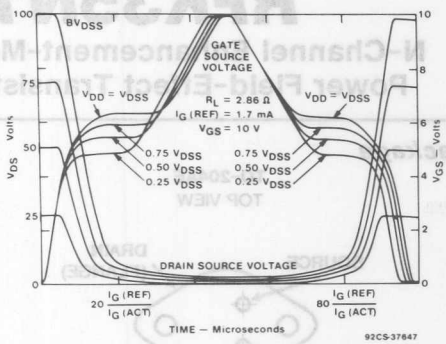


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

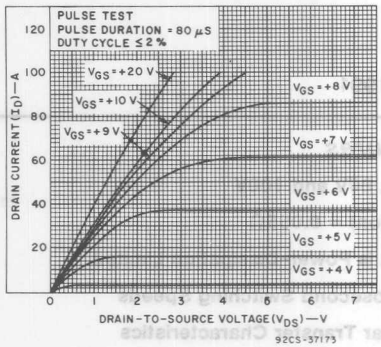


Fig. 7 - Typical saturation characteristics for all types.

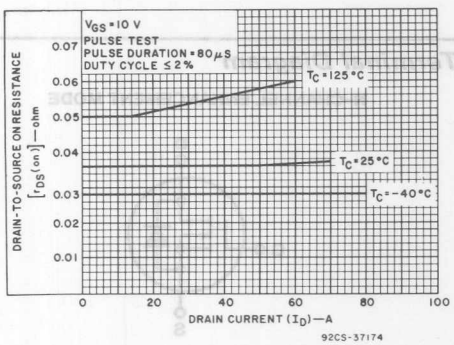


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

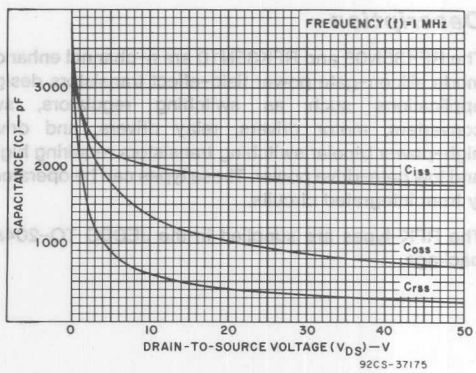


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

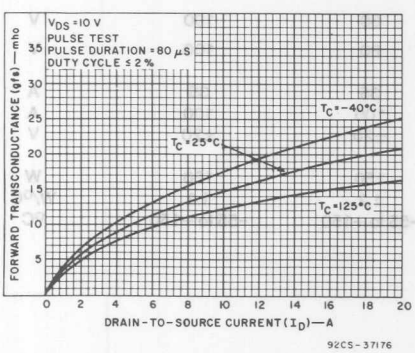


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

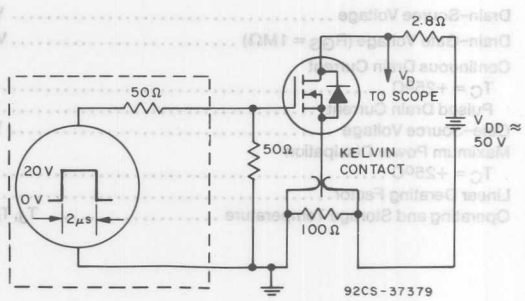


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFK35N08
RFK35N10

N-Channel Enhancement-Mode Power Field-Effect Transistors

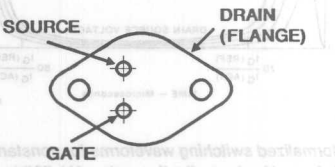
August 1991

Features

- 35A, 80V and 100V
- $r_{DS}(on) = 0.055\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AE
TOP VIEW



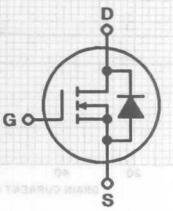
Description

The RFK35N08 and RFK35N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFK35N08	RFK35N10	UNITS
Drain-Source Voltage	V_{DSS}	80	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	80	100	V
Continuous Drain Current T_C = +25°C	I_D	35	35	A
Pulsed Drain Current	I_{DM}	100	100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1499.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK35N08		RFK35N10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V V_{DS}=80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=65 V V_{DS}=80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=17.5 A V_{GS}=10 V	—	0.9625	—	0.9625	V
		I_D=35 A V_{GS}=10 V	—	3.5	—	3.5	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=17.5 A V_{GS}=10 V	—	0.055	—	0.055	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=17.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1500	—	1500	pF
Reverse Transfer Capacitance	C_{rss}	f=1 MHz	—	600	—	600	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	45(typ)	100	45(typ)	100	ns
Rise Time	t_r	I_D=17.5 A	225(typ)	450	225(typ)	450	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	240(typ)	450	240(typ)	450	ns
Fall Time	t_f	V_{GS}=10 V	165(typ)	350	165(typ)	350	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK35N08, RFK35N10 Series	—	0.83	—	0.83	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK35N08		RFK35N10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD} [a]	I_{SD}=17.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

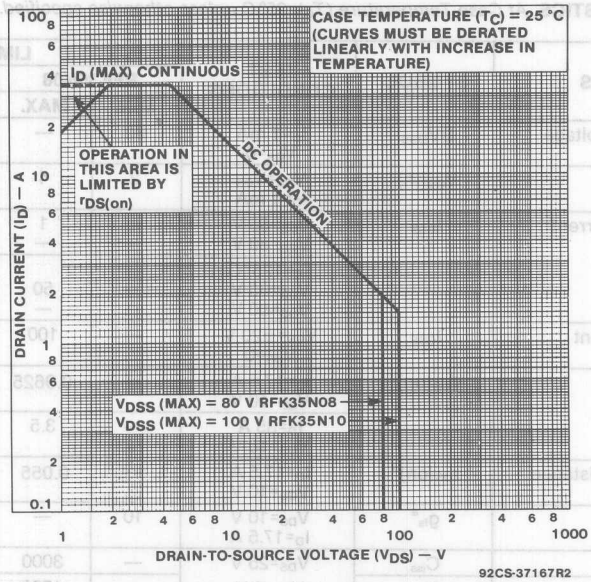


Fig. 1 — Maximum safe operating areas for all types.

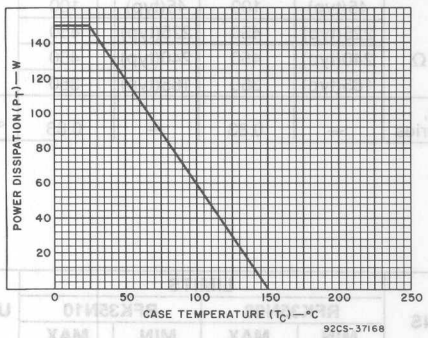


Fig. 2 — Power vs. temperature derating curve for all types.

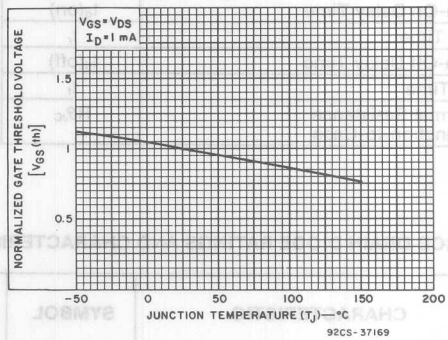


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

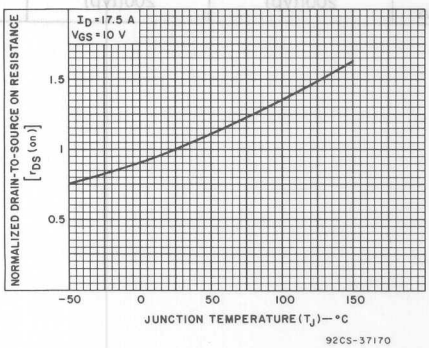


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

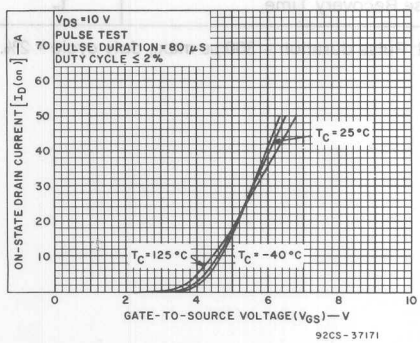


Fig. 5 — Typical transfer characteristics for all types.

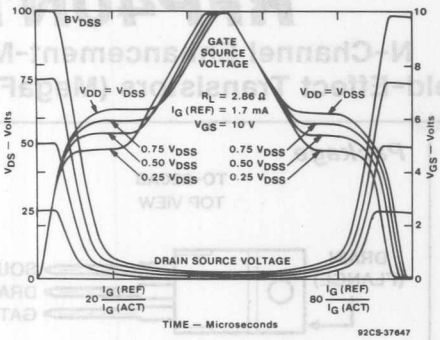


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

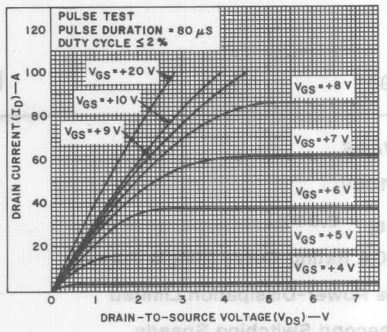


Fig. 7 — Typical saturation characteristics for all types.

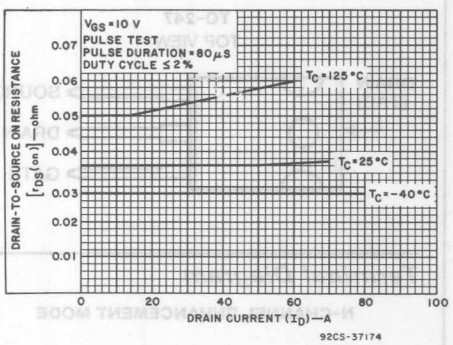


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

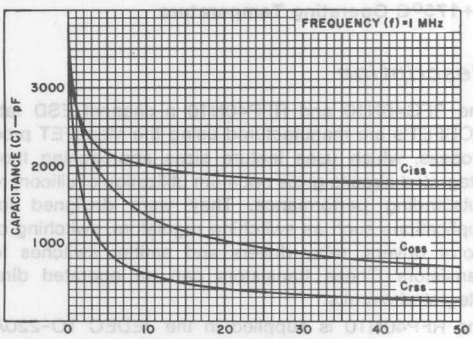


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

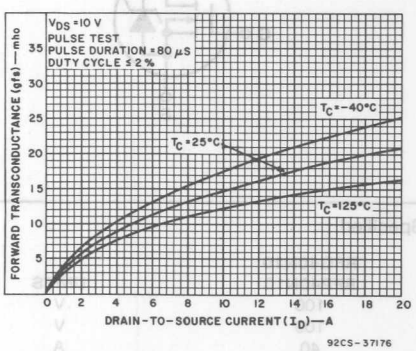


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

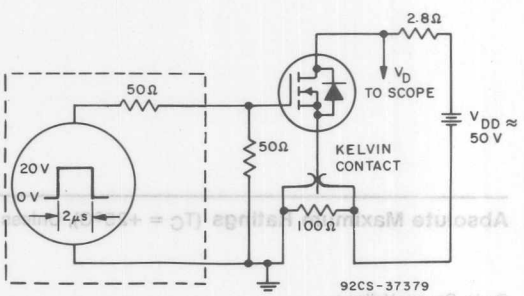


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFG40N10
RFP40N10

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

August 1991

Features

- 40A, 100V
- $r_{DS(on)} = 0.040\Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature

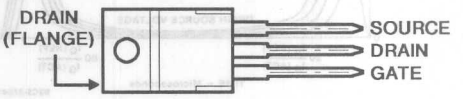
Description

The RFG40N10 and RFP40N10 n-channel ESD rated power MOSFET's are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

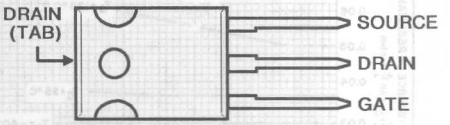
The RFP40N10 is supplied in the JEDEC TO-220AB plastic package and the RFG40N10 is supplied in the TO-247 plastic package.

Package

TO-220AB
TOP VIEW

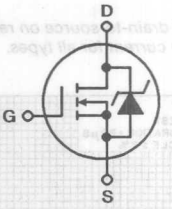


TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFG40N10 RFP40N10	UNITS
Drain-Source Voltage	V_{DSS}	100	V
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	V
Continuous Drain Current	I_D	40	A
Pulsed Drain Current	I_{DM}	100	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	160	W
Derated Above +25°C		1.07	W/°C
Operating and Storage Junction Temperature Range	T_{JC}, T_{STG}	-55 to +175	°C

Caution: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2431.1

ELECTRICAL CHARACTERISTICS *At Case Temperature (Tc) = 25°C unless otherwise specified.*

CHARACTERISTICS		TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	ID = 0.25 mA, VGS = 0 V		100	–	V
Gate Threshold Voltage	VGS(th)	VGS = VDS, ID = 0.25 mA		2	4	V
Zero Gate Voltage Drain Current	IDSS	VDS = 80 V, VGS = 0 V Tc = 150°C		–	1 50	µA
Gate-Source Leakage Current	IGSS	VGS = ±20 V, VDS = 0 V		–	100	nA
Static Drain-Source on Resistance	rDS(on)	ID = 40 A, VGS = 10 V		–	0.040	Ω
Turn-On Time	t(on)	VDD = 50 V, ID = 20 A Ig1 = Ig2 = 1.2 A VGS (clamp): +10 V, -0.6 V RL = 2.5 Ω		–	80	ns
Turn-On Delay Time	td(on)			17 (typ)	–	
Rise Time	tr			30 (typ)	–	
Turn-Off Delay Time	td(off)			42 (typ)	–	
Fall Time	tr			20 (typ)	–	
Turn-Off Time	t(off)			–	100	
Total Gate Charge	Qg(total)	VGS = 0 to 20 V	VDD = 80 V	–	300	nC
Gate Charge at 10V	Qg(10)	VGS = 0 to 10 V	ID = 40 A	–	150	
Threshold Gate Charge	Qg(th)	VGS = 0 to 2 V	RL = 2 Ω	–	7.5	
Plateau Voltage	V(plateau)	ID = 40 A, VDS = 15 V		–	7.5	V
Turn-Off Energy Loss per Cycle	Eoff	VDD = 50 V, ID = 20 A, RL = 2.5 Ω L = 0.8 µH, Ig1 = Ig2 = 1.2 A VGS (clamp): +10 V, -0.6 V		–	300	µJ
Thermal Resistance, Junction to Case	RθJC			–	0.94	°C/W
Thermal Resistance, Junction to Ambient	RθJA			–	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	VSD	ISD = 40 A	–	1.5	V
Reverse Recovery Time	trr	ISD = 40 A, dISD/dt = 100 A/µs	–	200	ns

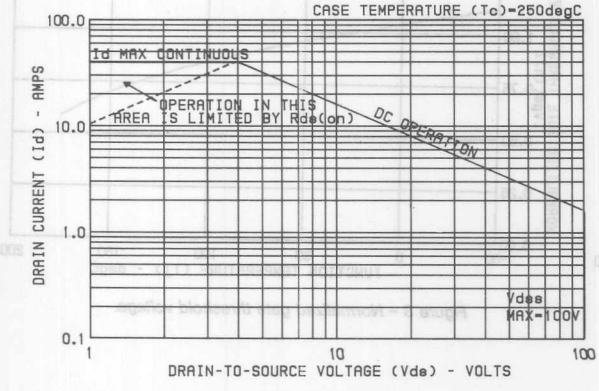


Figure 1 – Safe operating area curve.
(Curves must be derated linearly with increase in temperature.)

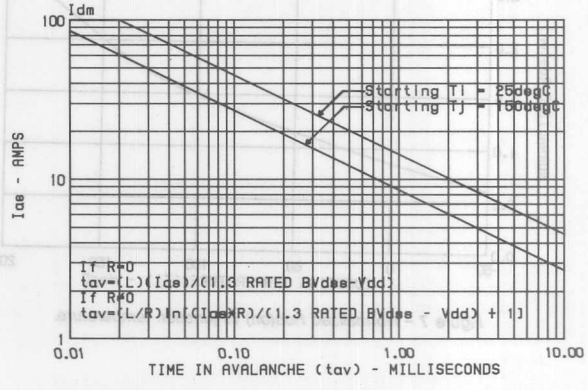


Figure 2 – Unclamped-inductive-switching safe-operating-area (single pulse UIS SOA). See Figure 13 for test circuit.

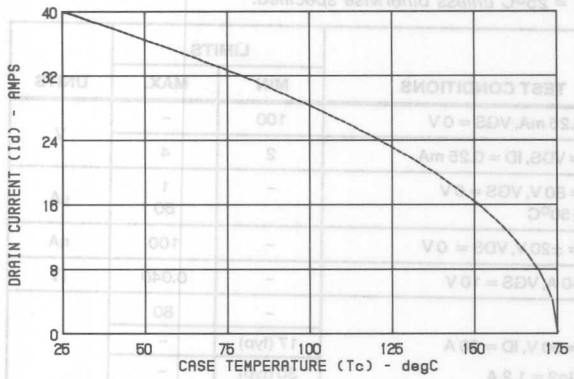


Figure 3 – Maximum continuous drain current vs. temperature.

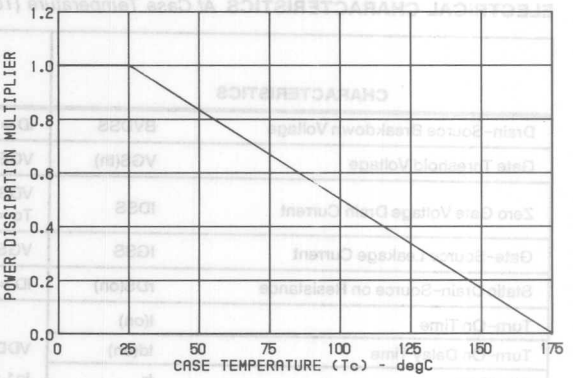


Figure 4 – Normalized power dissipation vs temperature derating curve.

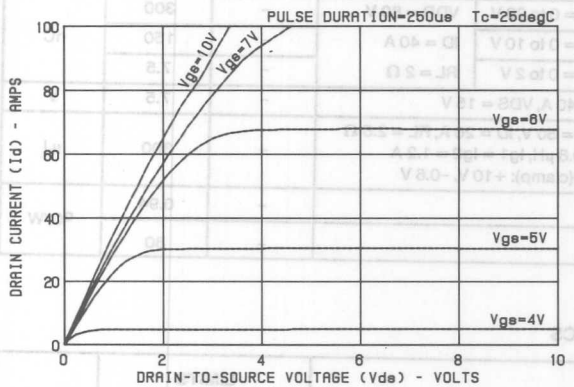


Figure 5 – Typical saturation characteristics.

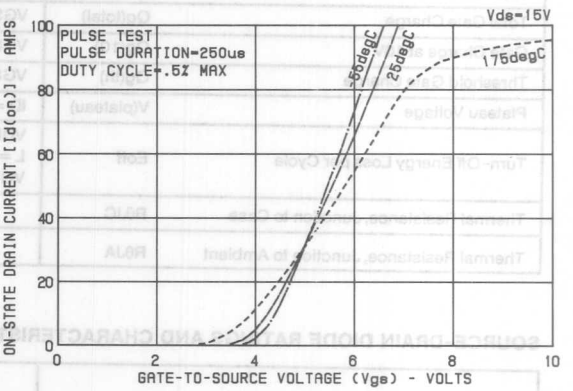


Figure 6 – Typical transfer characteristics.

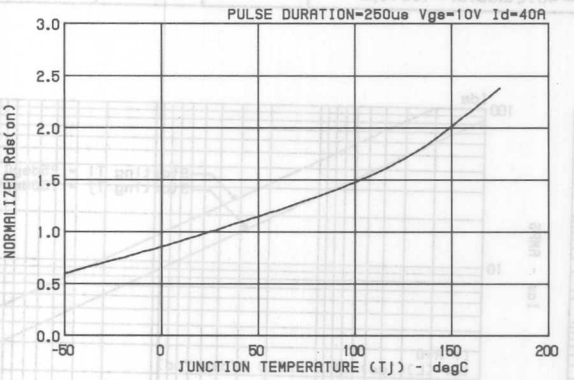


Figure 7 – Normalized Rds(on) vs junction temperature.

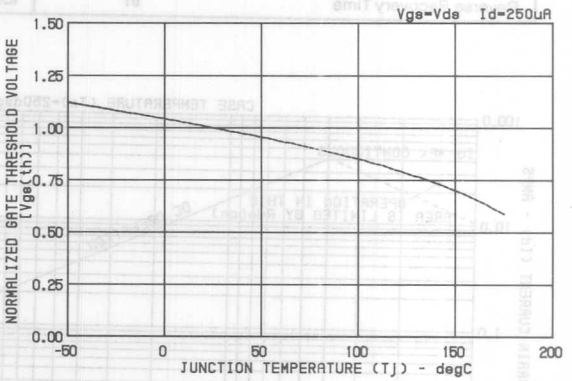


Figure 8 – Normalized gate threshold voltage.

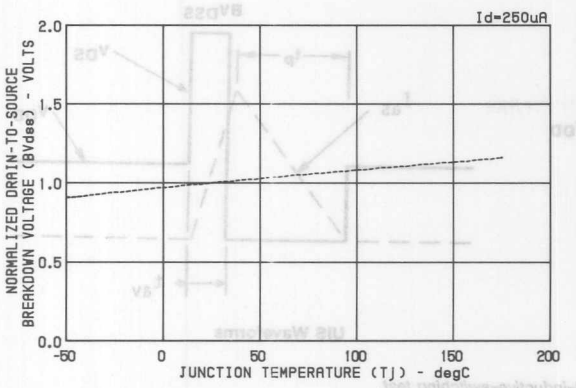


Figure 9 – Normalized drain source breakdown voltage vs temperature.

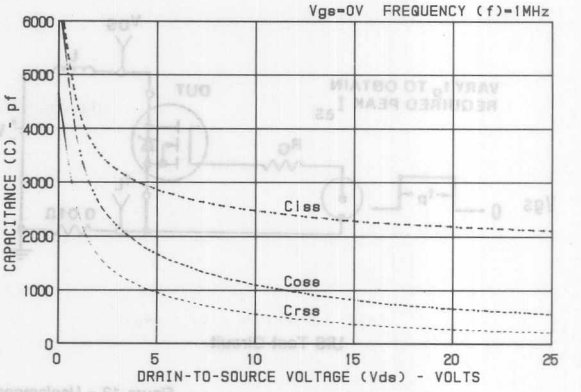


Figure 10 – Typical capacitance vs voltage.

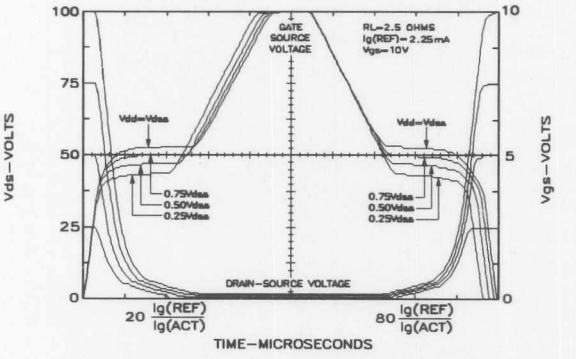


Figure 11 – Normalized switching waveforms for constant gate-current.
Refer to Harris application notes AN-7254 and AN-7260

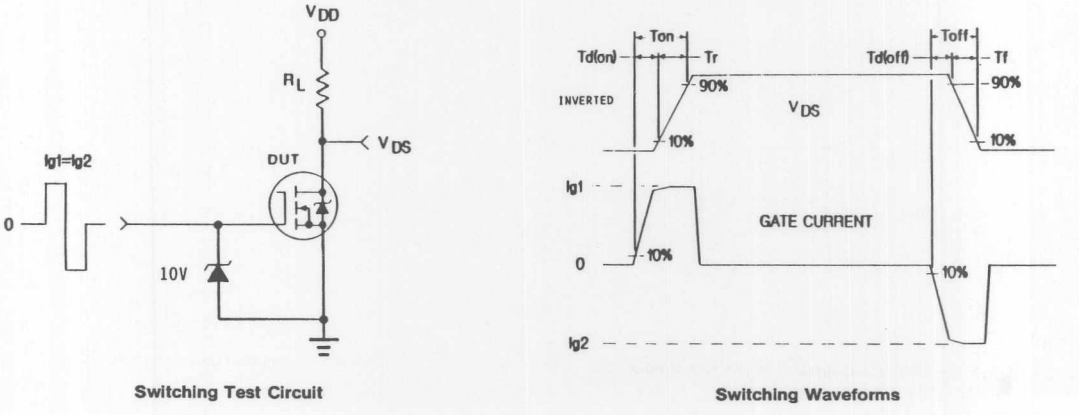


Figure 12 – Resistive switching.

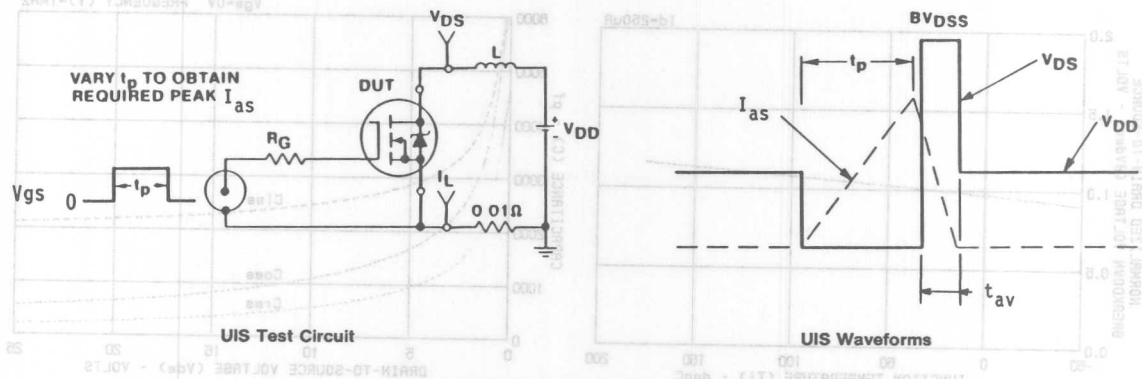


Figure 13 – Unclamped-inductive-switching test.

RFH45N05
RFH45N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

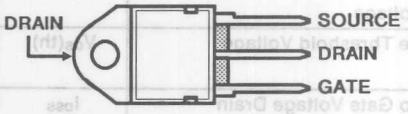
August 1991

Features

- 45A, 50V and 60V
- $r_{DS}(on) = 0.040\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Current, Low-Inductance Package

Package

TO-218AC
TOP VIEW



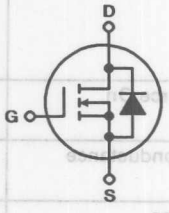
Description

The RFH45N05 and RFH45N06 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFH45N05	RFH45N06	UNITS
Drain-Source Voltage	V_{DSS}	50	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	60	V
Continuous Drain Current	I_D	45	45	A
Pulsed Drain Current	I_{DM}	100	100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1635.1**

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH45N05		RFH45N06		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V	—	1	—	—	μA
		V_{DS} = 50 V	—	—	—	1	
		T_C = 125° C V_{DS} = 40 V	—	50	—	—	
		V_{DS} = 50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 22.5 A V_{GS} = 10 V	—	0.9	—	0.9	V
		I_D = 45 A V_{GS} = 10 V	—	3.6	—	3.6	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 22.5 A V_{GS} = 10 V	—	.04	—	.04	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 22.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1800	—	1800	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	750	—	750	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 30 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r	I_D = 22.5 A	310(typ)	475	310(typ)	475	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	220(typ)	350	220(typ)	350	
Fall Time	t_f	V_{GS} = 10 V	240(typ)	375	240(typ)	375	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH45N05, RFH45N06 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH45N05		RFH45N06		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 22.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	150 (typ.)		150 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

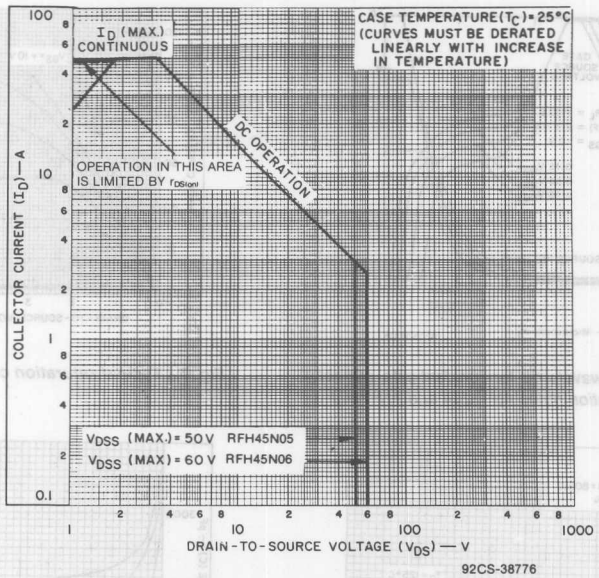


Fig. 1 - Maximum safe operating areas for all types.

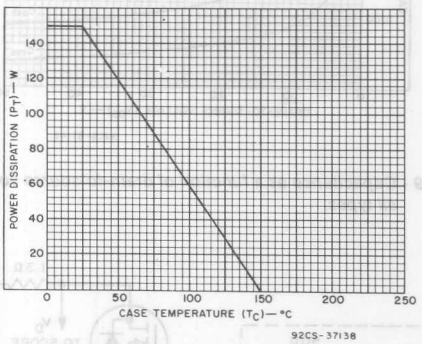


Fig. 2 - Power vs. temperature derating curve for all types.

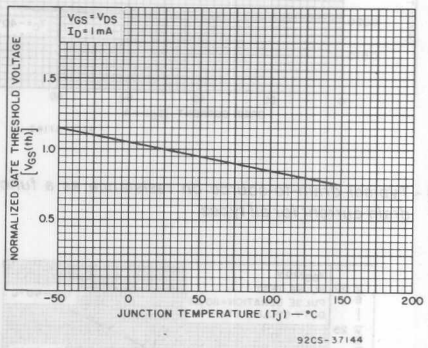


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

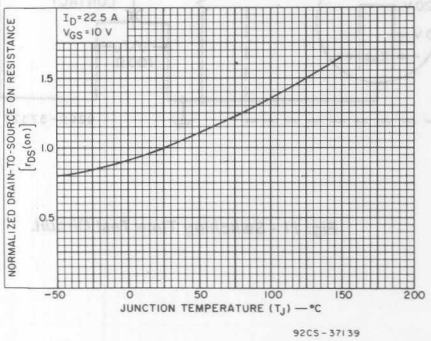


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

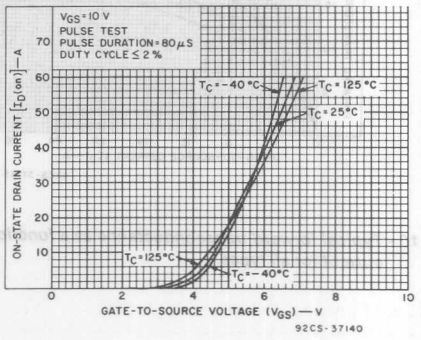


Fig. 5 - Typical transfer characteristics for all types.

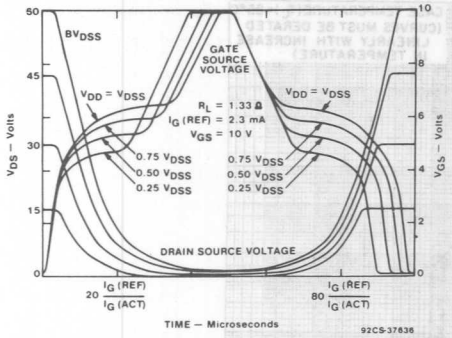


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

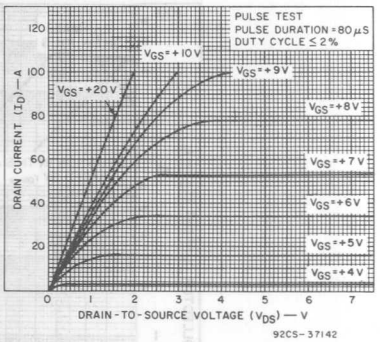


Fig. 7 - Typical saturation characteristics for all types.

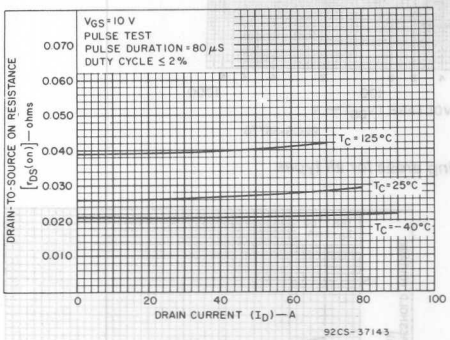


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

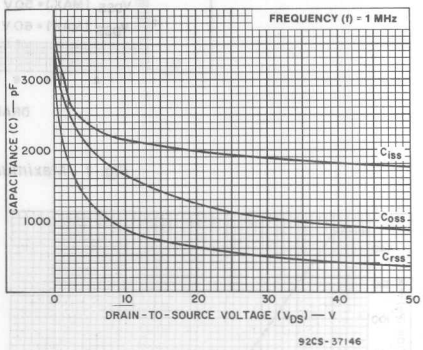


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

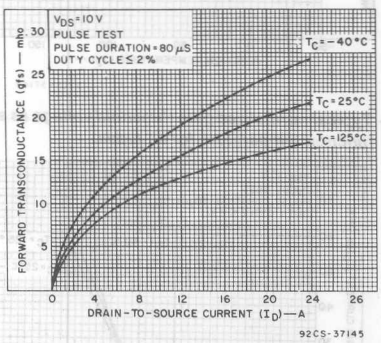


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

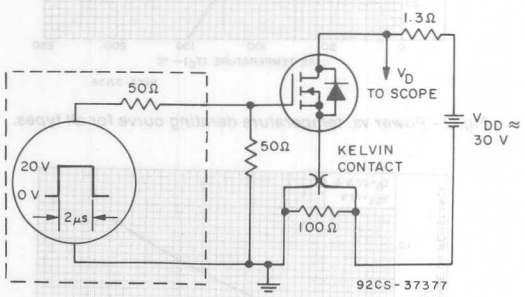


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFK45N05
RFK45N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

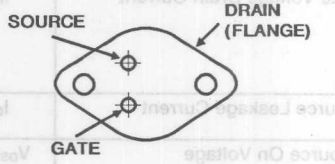
August 1991

Features

- 45A, 50V and 60V
- $r_{DS}(on) = 0.040\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AE



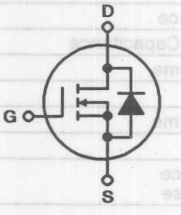
Description

The RFK45N05 and RFK45N06 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFK45N05	RFK45N06	UNITS
Drain-Source Voltage	V_{DSS}	50	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	60	V
Continuous Drain Current T_C = +25°C	I_D	45	45	A
Pulsed Drain Current	I_{DM}	100	100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1498.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK45N05		RFK45N06		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V V_{DS}=50 V	— —	1 —	— —	— 1	μA
		T_C=125° c V_{DS}=40 V V_{DS}=50 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=22.5 A V_{GS}=10 V	—	0.9	—	0.9	V
		I_D=45 A V_{GS}=10 V	—	3.6	—	3.6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=22.5 A V_{GS}=10 V	—	.04	—	.04	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=22.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1800	—	1800	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	750	—	750	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 30 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r	I_D=22.5 A	310(typ)	475	310(typ)	475	ns
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=R_{gs}$=50 Ω	220(typ)	350	220(typ)	350	ns
Fall Time	t_f	V_{GS}=10 V	240(typ)	375	240(typ)	375	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK45N05, RFK45N06 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK45N05		RFK45N06		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 22.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	150(typ.)		150(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

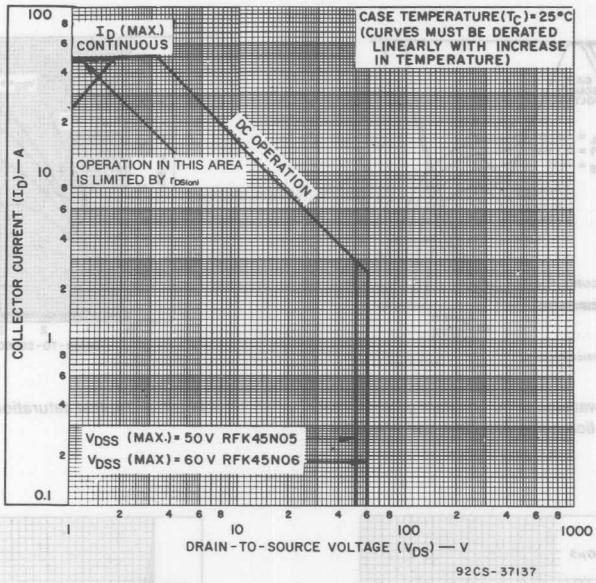


Fig. 1 — Maximum safe operating areas for all types.

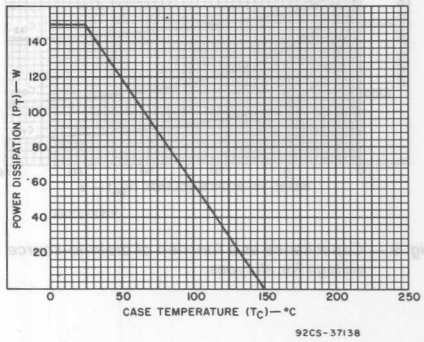


Fig. 2 — Power vs. temperature derating curve for all types.

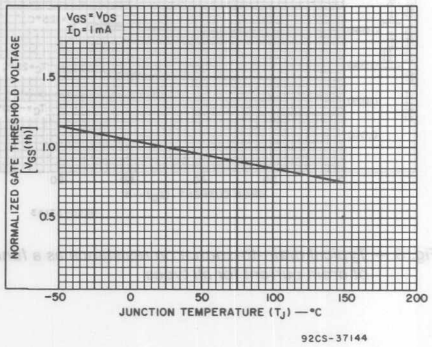


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

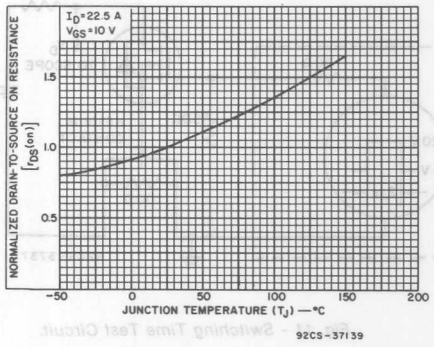


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

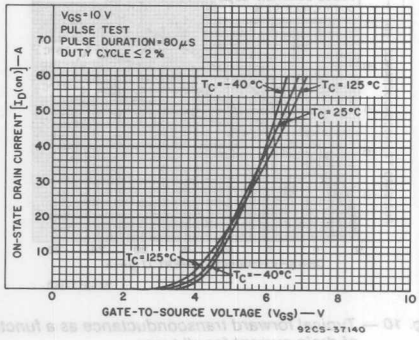


Fig. 5 — Typical transfer characteristics for all types.

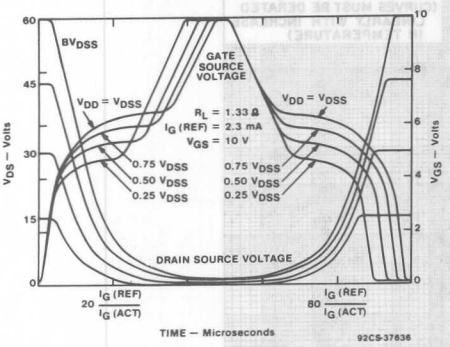


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

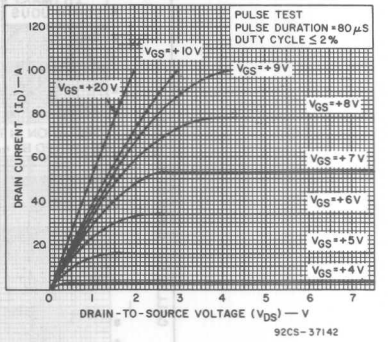


Fig. 7 — Typical saturation characteristics for all types.

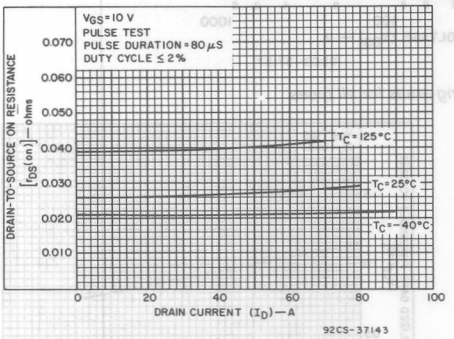


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

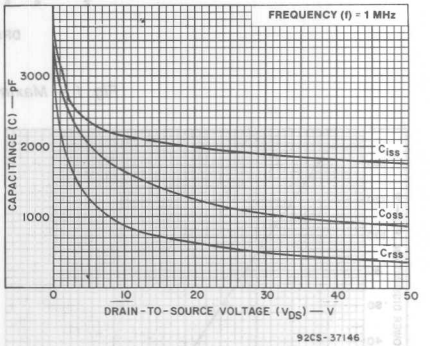


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

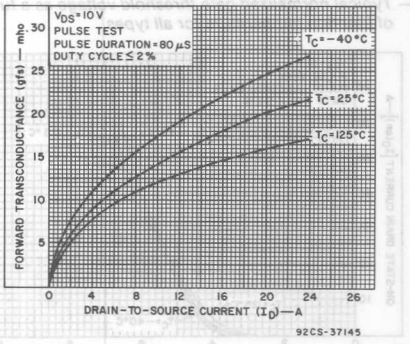


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

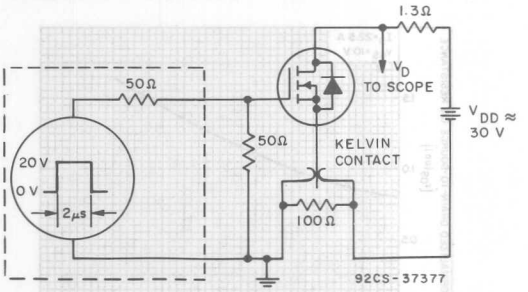


Fig. 11 - Switching Time Test Circuit.

RFP50N05
RFG50N05

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

May 1992

Features

- 50A, 50V
- $r_{DS(on)} = 0.022\Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature

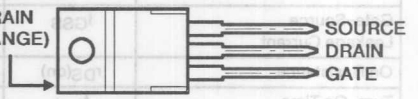
Description

The RFP50N05 and RFG50N05 n-channel power MOSFET's are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors.

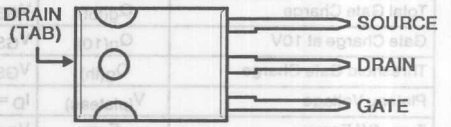
The RFP50N05 is supplied in the JEDEC TO-220AB plastic package and the RFG50N05 is supplied in the TO-247 plastic package.

Package

TO-220AB
TOP VIEW

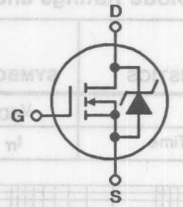


TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	RFP50N05 RFG50N05	UNITS
Drain-Source Voltage ..... V_{DSS}	50	V
Drain-Gate Voltage (R_{GS} = 1 MΩ) ..... V_{DGR}	50	V
Continuous Drain Current ..... I_D	50	A
Pulsed Drain Current ..... I_{DM}	120	A
Gate-Source Voltage ..... V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	132	W
Derated Above +25°C	0.88	W/°C
Operating and Storage Junction Temperature Range ..... T_{JC}, T_{STG}	-55 to +175	°C
Single-Pulse Avalanche Ratings	Refer to UIS SOA Curve	

Caution: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2873.1**

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D =0.25mA, V_{GS} = 0V		50	–	–	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25mA		2	–	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =40V, V_{GS} = 0V		–	–	1	µA
		T_C =+150°C		–	–	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		–	–	100	nA
On Resistance	$r_{DS(on)}$	I_D = 50A, V_{GS} = 10V		–	–	0.022	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = 25V, I_D = 25A		–	–	100	ns
Turn-On Delay Time	$t_{d(on)}$	R_L = 1.0Ω		–	15	–	ns
Rise Time	t_r	$I_{G1} = I_{G2}$ = 1.5A		–	55	–	ns
Turn-Off Delay Time	$t_{d(off)}$	$V_{GS(clamp)}$ = +10V, -0.6V		–	60	–	ns
Fall Time	t_f			–	15	–	ns
Turn-Off Time	$t_{(off)}$			–	–	100	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0-20V	V_{DD} = 40V	–	–	160	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0-10V	I_D = 50A	–	–	80	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} =0-2V	R_L = 0.8Ω	–	–	6	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 50A, V_{DS} = 15V		–	–	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 25A, $I_{G1} = I_{G2}$ = 1.5A, $V_{GS(clamp)}$ = +10V, -0.6V, L = 0.2µH, R_L = 1.0Ω		–	–	150	µJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			–	–	1.14	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{\theta JA}$			–	–	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 50A	–	–	1.5	V
Reverse Recovery Time	t_{rr}	I_f = 50A, dI_f/dt = 100A/µs	–	–	125	ns

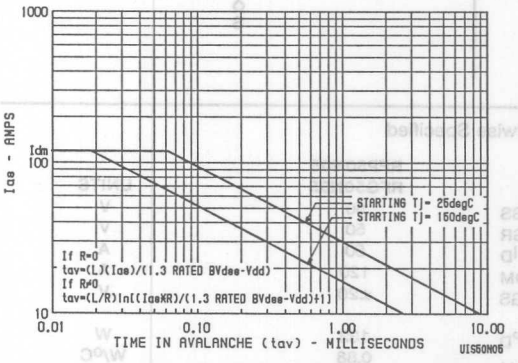


FIGURE 1. UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

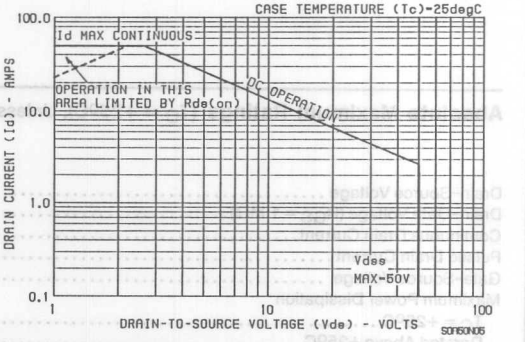


FIGURE 2. SAFE-OPERATING-AREA CURVE. (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN CASE TEMPERATURE)

Performance Curves

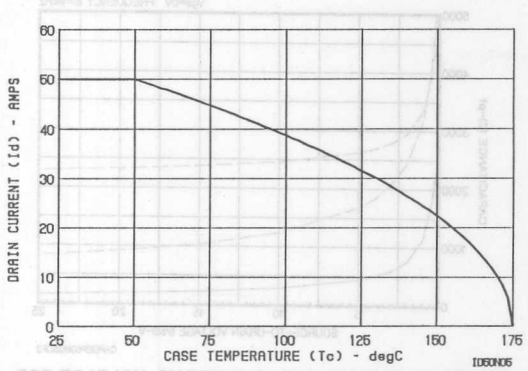


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT VS. TEMPERATURE

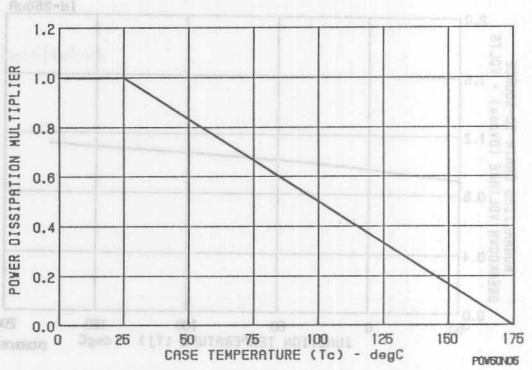


FIGURE 4. NORMALIZED POWER DISSIPTION VS. TEMPERATURE DERATING CURVE

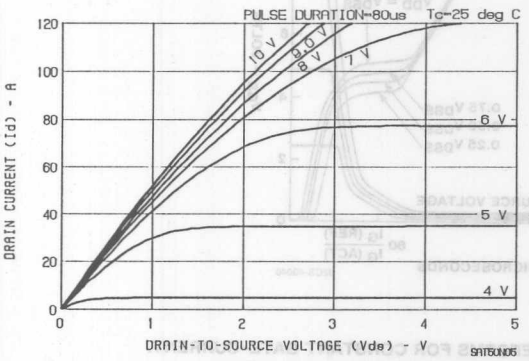


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

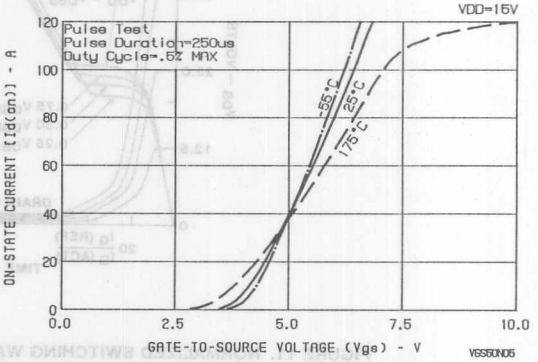


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

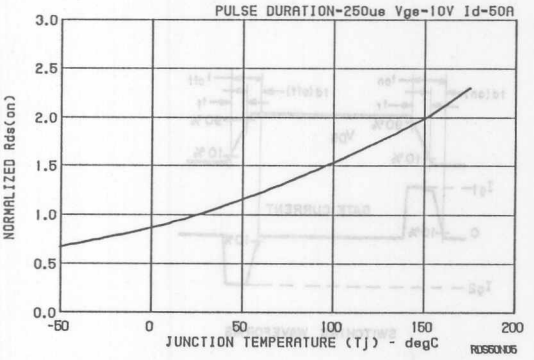


FIGURE 7. NORMALIZED $r_{DS(on)}$ VS. JUNCTION TEMPERATURE

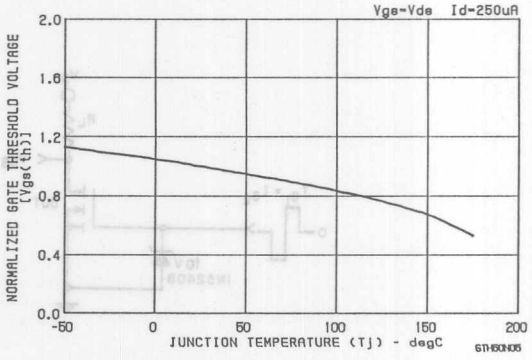


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE

Performance Curves (Continued)

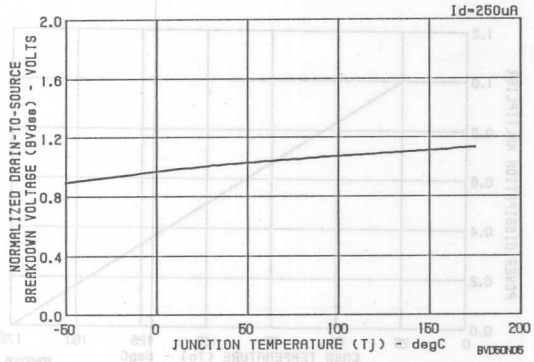


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE BREAKDOWN VOLTAGE VS. TEMPERATURE

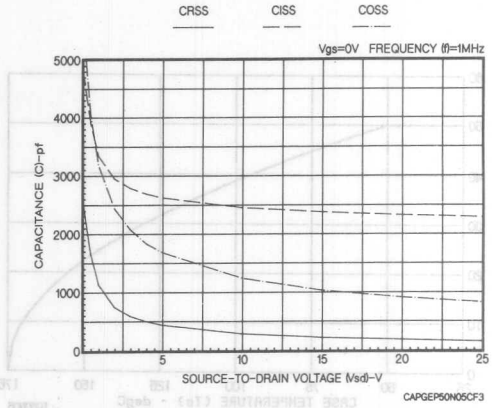


FIGURE 10. TYPICAL CAPACITANCE VS. VOLTAGE FOR ALL TYPES

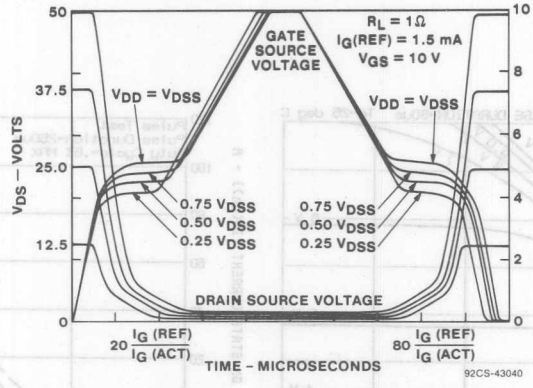
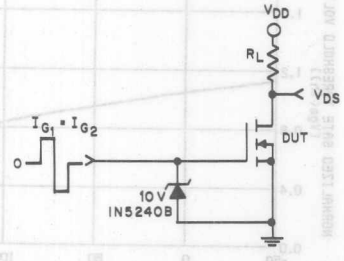


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. (REFER TO HARRIS APPLICATION NOTES AN-7254 AND AN-7260)



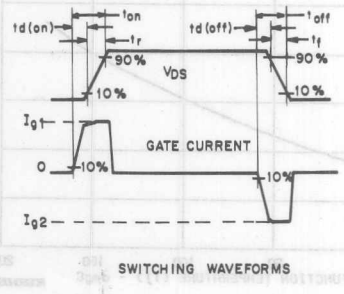


FIGURE 12. RESISTIVE SWITCHING

Performance Curves (Continued)

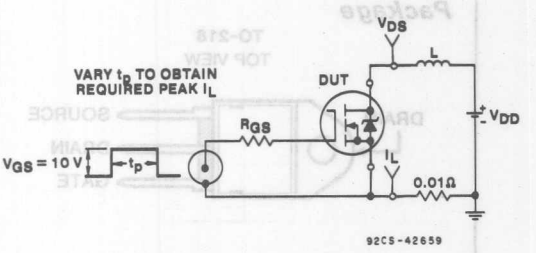


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

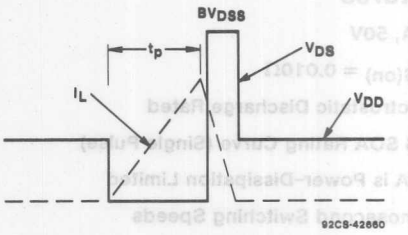


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

Power Field-Effect Transistors (MegaFETs)

Features

- 75A, 50V
- $r_{DS(on)} = 0.010\Omega$
- Electrostatic Discharge Rated
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature
- Temperature Compensated SPICE Model Provided

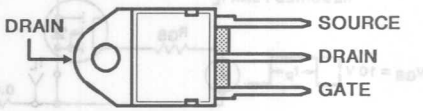
Description

The RFG75N05E and RFH75N05E n-channel ESD rated power MOSFET's are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

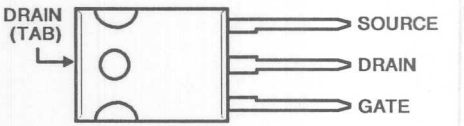
The RFG75N05E is supplied in the TO-247 style (3 lead) plastic package and the RFH75N05E is supplied in the TO-218 (3 lead) plastic package.

Package

TO-218
TOP VIEW

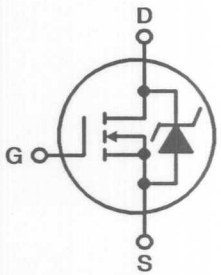


TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFG75N05E RFH75N05E	UNITS
Drain-Source Voltage	V_{DSS}	50	V
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	V
Continuous Drain Current	I_D	75*	A
Pulsed Drain Current	I_{DM}	200	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	240	W
Derated Above +25°C		1.6	W/°C
Operating and Storage Junction Temperature Range	T_{JC}, T_{STG}	-55 to +175	°C
Electrostatic Discharge Rating			
MIL-STD-883, Category B(2)	E_{SD}	2	kV
Single-Pulse Avalanche Rating		Refer to UIS SOA Curves	

*I_D Current Limited by Package

Caution: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2275.2**

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D =0.25mA, V_{GS} = 0V		50	–	–	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25mA		2	–	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =40V, V_{GS} = 0V		–	–	1	µA
		T_C =+150°C		–	–	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		–	–	100	nA
On Resistance	$r_{DS(on)}$	I_D = 75A, V_{GS} = 10V		–	–	0.010	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = 25V, I_D = 37.5A		–	–	125	ns
Turn-On Delay Time	$t_{d(on)}$	R_L = 0.67Ω		–	17	–	ns
Rise Time	t_r	$I_{G1} = I_{G2}$ = 3A		–	75	–	ns
Turn-Off Delay Time	$t_{d(off)}$	$V_{GS(clamp)}$ = +10V, -0.6V		–	70	–	ns
Fall Time	t_f			–	17	–	ns
Turn-Off Time	$t_{(off)}$			–	–	125	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0, 20V	V_{DD} = 40V	–	–	400	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0, 10V	I_D = 75A	–	–	220	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} =0, 2V	R_L = 0.53Ω	–	–	15	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 75A, V_{DS} = 15V		–	–	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 37.5A, $I_{G1} = I_{G2}$ = 3A, $V_{GS(clamp)}$ = +10V, -0.6V, L = 0.2µH, R_L = 0.67Ω		–	–	300	µJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			–	–	0.625	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{\theta JA}$			–	–	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 75A	–	–	1.5	V
Reverse Recovery Time	t_{rr}	I_f = 75A, dI_f/dt = 100A/µs	–	–	125	ns

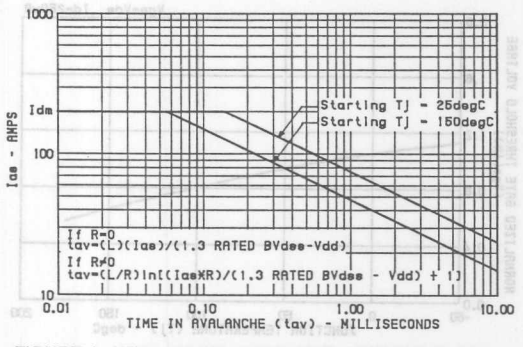


FIGURE 1. UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

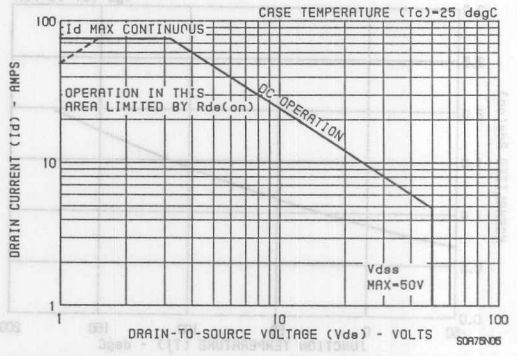


FIGURE 2. SAFE-OPERATING-AREA CURVE. (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN CASE TEMPERATURE)

Performance Curves

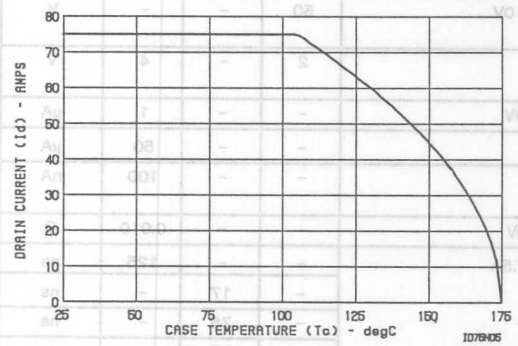


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT VS. TEMPERATURE

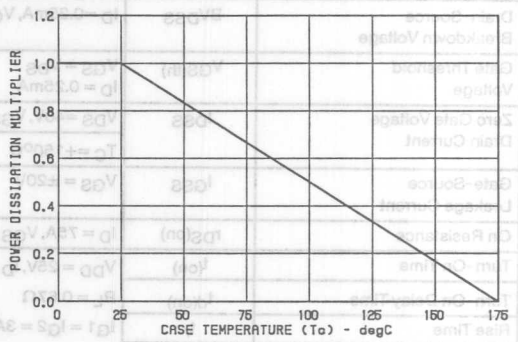


FIGURE 4. NORMALIZED POWER DISSIPTION VS. TEMPERATURE DERATING CURVE

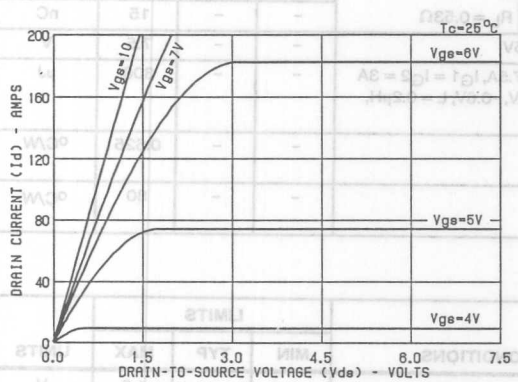


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

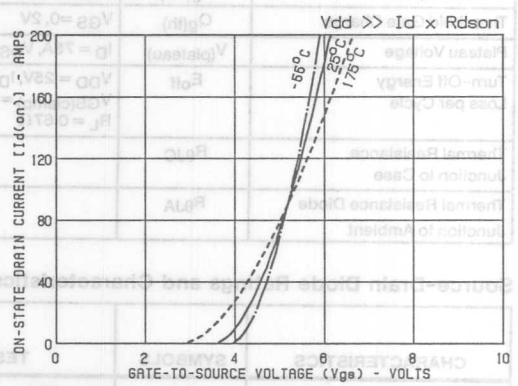


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

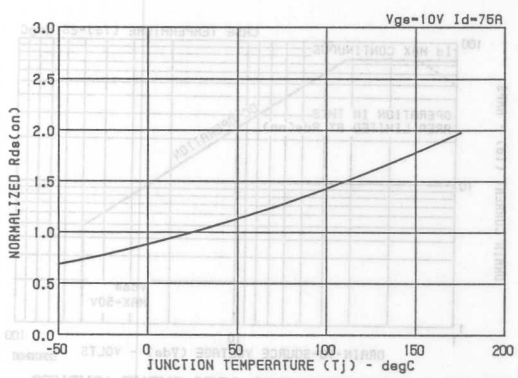


FIGURE 7. NORMALIZED $r_{DS(on)}$ VS. JUNCTION TEMPERATURE

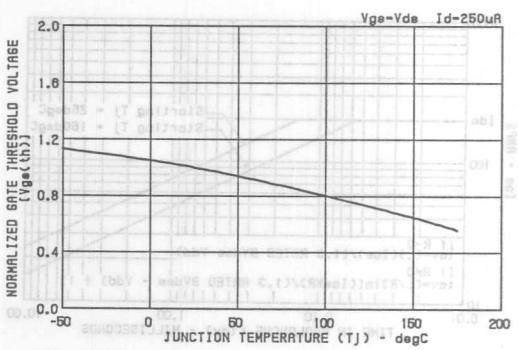


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE

Performance Curves (Continued)

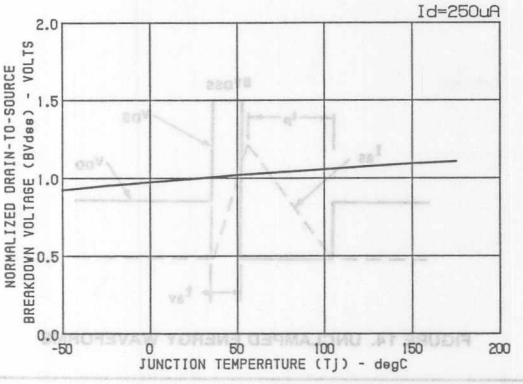


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE BREAKDOWN VOLTAGE VS. TEMPERATURE

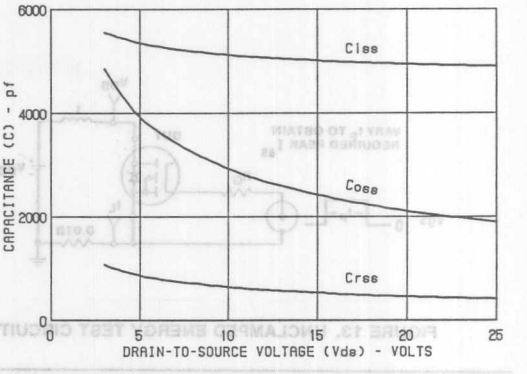


FIGURE 10. TYPICAL CAPACITANCE VS. VOLTAGE FOR ALL TYPES

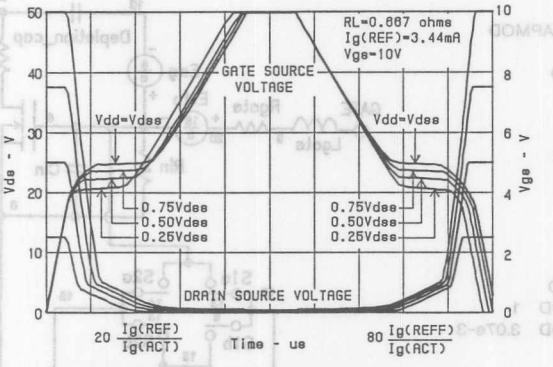


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. (REFER TO HARRIS APPLICATION NOTES AN-7254 AND AN-7260)

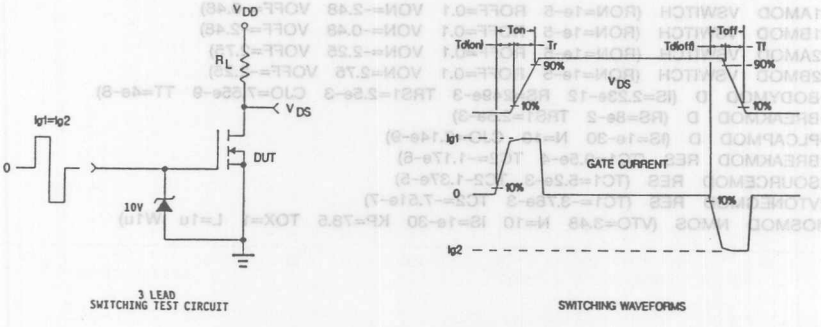


FIGURE 12. RESISTIVE SWITCHING

Performance Curves (Continued)

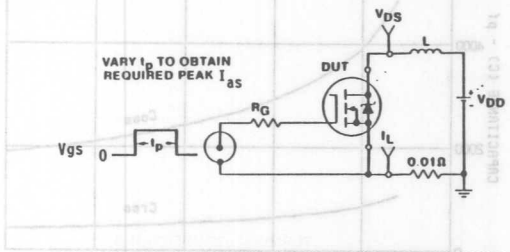


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

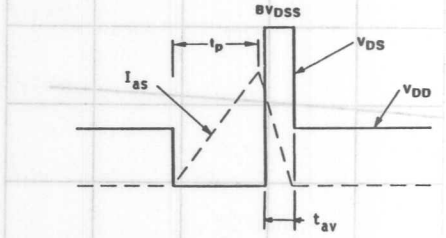
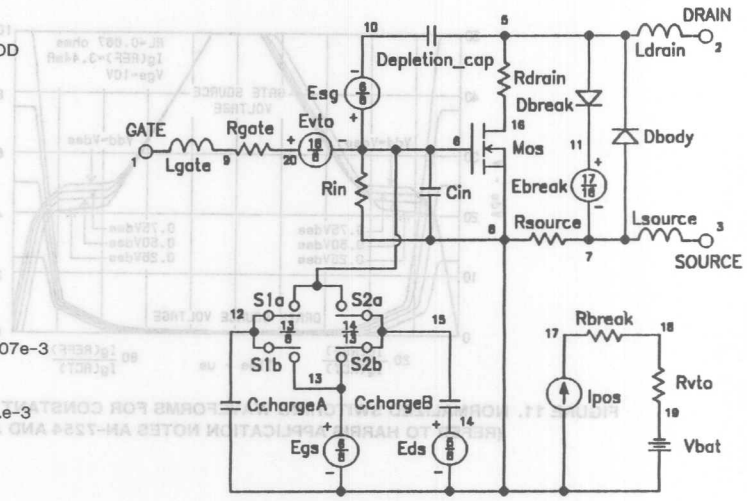


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

Spice Model

```
.SUBCKT RFH75N05  2  1  3  ;  rev 10/30/90
*Nominal Temperature = 25°C
CchargeA  12  8  8.98e-9
CchargeB  15  14  8.81e-9
Cin  6  8  4.48e-9
Depletion_cap  10  5  DPLCAPMOD
Dbody  7  5  DBODYMOD
Dbreak  5  11  DBREAKMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Ebreak  11  7  17  18  58.4
Evto  20  6  18  8  1
Ipos  8  17  1
Ldrain  2  5  e-10
Lgate  1  9  5e-9
Lsource  3  7  3e-9
Mos  16  6  8  8  MOSMOD
Rbreak  17  18  RBREAKMOD  1
Rdrain  5  16  RSOURCEMOD  3.07e-3
Rgate  9  20  1.2
Rin  6  8  1e9
Rsource  8  7  RSOURCEMOD  2.e-3
Rvto  18  19  RVTONEGMOD  1
S1a  6  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
.MODEL  S1AMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-2.48  VOFF=-0.48)
.MODEL  S1BMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-0.48  VOFF=-2.48)
.MODEL  S2AMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-2.25  VOFF=2.75)
.MODEL  S2BMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=2.75  VOFF=-2.25)
.MODEL  DBODYMOD  D  (IS=2.23e-12  RS=249e-3  TRS1=2.5e-3  CJO=7.55e-9  TT=4e-8)
.MODEL  DBREAKMOD  D  (RS=8e-2  TRS1=2.5e-3)
.MODEL  DPLCAPMOD  D  (IS=1e-30  N=10  CJO=2.14e-9)
.MODEL  RBREAKMOD  RES  (TC1=9.5e-4  TC2=-1.17e-6)
.MODEL  RSOURCEMOD  RES  (TC1=5.2e-3  TC2-1.37e-5)
.MODEL  RVTONEGMOD  RES  (TC1=-3.78e-3  TC2=-7.51e-7)
.MODEL  MOSMOD  NMOS  (VTO=3.48  N=10  IS=1e-30  KP=78.5  TOX=1  L=1u  W1u)
.ENDS
```



HARRIS RFA100N05E

May 1992

N-Channel Enhancement-Mode Power Field-Effect Transistor (MegaFET)

Features

- 100A, 50V
- $r_{DS(on)} = 0.010\Omega$
- Electrostatic Discharge Rated
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature
- Temperature Compensated SPICE Model Provided

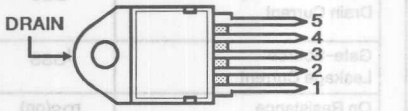
Description

The RFA100N05E n-channel ESD rated power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFA100N05E is supplied in the MO-093 plastic package.

Package

MO-093
TOP VIEW

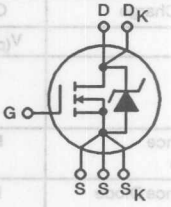


TERMINAL CONNECTIONS

1 - Gate
2 - Source Kelvin
3 - Drain Kelvin
4 - Source Current
5 - Source Current

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFA100N05E	UNITS
Drain-Source Voltage	V_{DSS}	50	V
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	V
Continuous Drain Current	I_D	100	A
Pulsed Drain Current	I_{DM}	300	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	240	W
Derated Above 25°C		1.6	W/°C
Operating and Storage Junction Temperature Range	T_{JC}, T_{STG}	-55 to +175	°C
Electrostatic Discharge Rating			
MIL-STD-883, Category B(2)	E_{SD}	2	kV
Single-Pulse Avalanche Rating		Refer to UIS SOA Curves	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2869.1

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D =0.25mA, V_{GS} = 0V		50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =40V, V_{GS} = 0V		-	-	1	µA
		T_C =+150°C		-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(on)}$	I_D = 100A, V_{GS} = 10V		-	-	0.010	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = 25V, I_D = 50A, R_L = 0.50Ω, $I_{G1} = I_{G2}$ = 3A, $V_{GS(clamp)}$ = +10V, -0.6V		-	-	60	ns
Turn-On Delay Time	$t_{d(on)}$			-	17	-	ns
Rise Time	t_r			-	8	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	50	-	ns
Fall Time	t_f			-	10	-	ns
Turn-Off Time	$t_{(off)}$			-	-	100	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0, 20V	V_{DD} = 40V	-	-	430	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0, 10V	I_D = 100A	-	-	230	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} =0, 2V	R_L = 0.40Ω	-	-	15	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 100A, V_{DS} = 15V		-	-	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 50A, $I_{G1} = I_{G2}$ = 3A, $V_{GS(clamp)}$ = +10V, -0.6V, L = 0.2µH, R_L = 0.50Ω		-	-	500	µJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.625	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 100A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_f = 100A, dI_f/dt = 100A/µs	-	-	125	ns

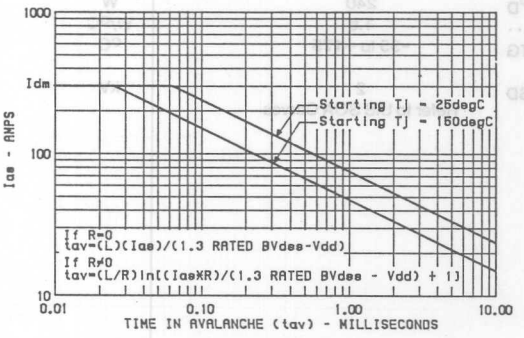


FIGURE 1. UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

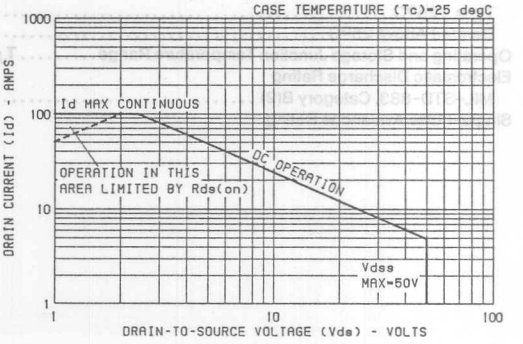


FIGURE 2. SAFE-OPERATING-AREA CURVE. (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN CASE TEMPERATURE)

Performance Curves

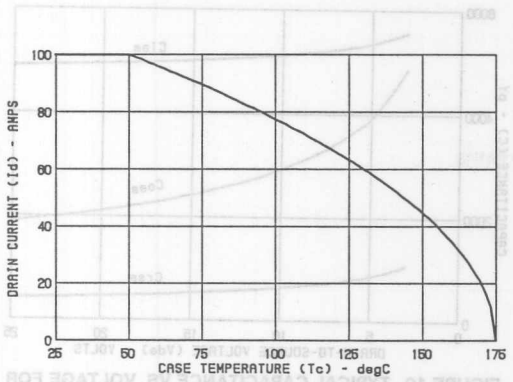


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT VS. TEMPERATURE

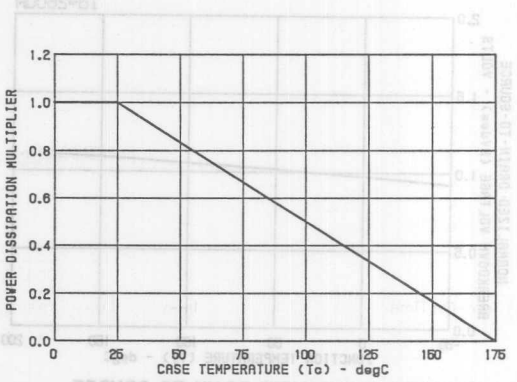


FIGURE 4. NORMALIZED POWER DISSIPTION VS. TEMPERATURE DERATING CURVE

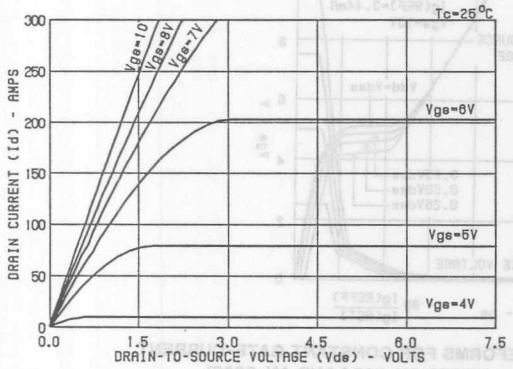


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

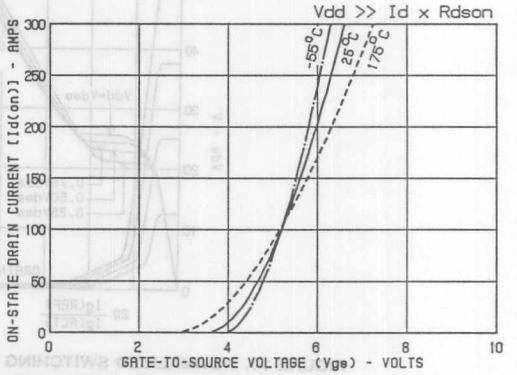


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

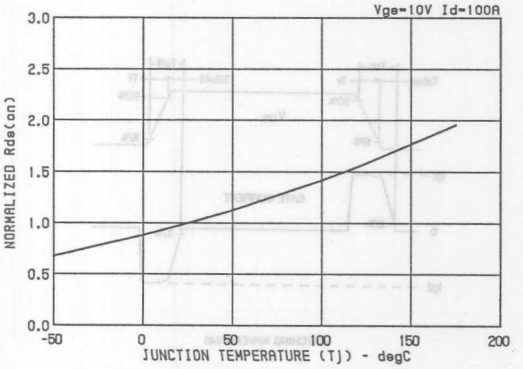


FIGURE 7. NORMALIZED $r_{DS(on)}$ VS. JUNCTION TEMPERATURE

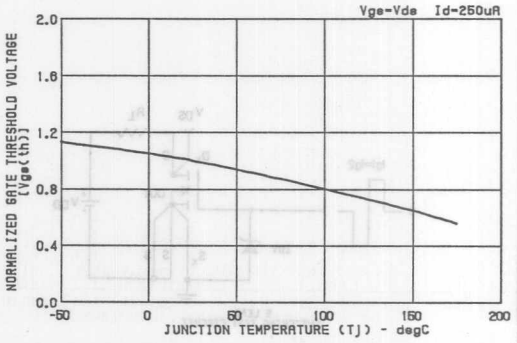


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE

Performance Curves (Continued)

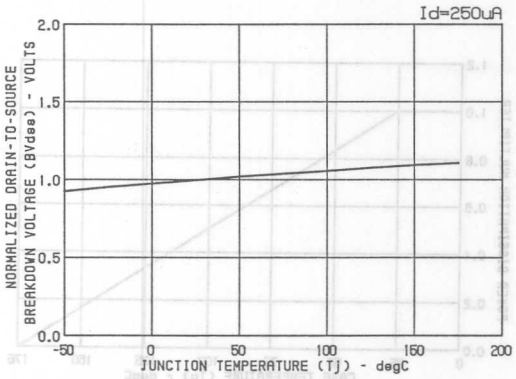


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE BREAKDOWN VOLTAGE VS. TEMPERATURE

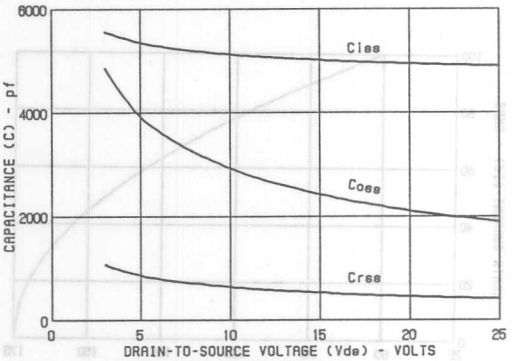


FIGURE 10. TYPICAL CAPACITANCE VS. VOLTAGE FOR ALL TYPES

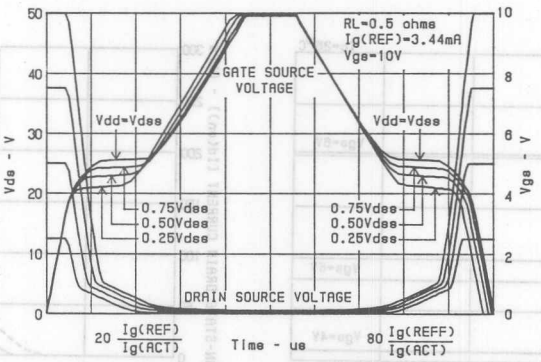
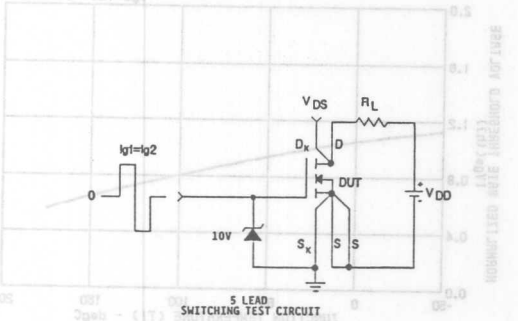


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. (REFER TO HARRIS APPLICATION NOTES AN-7254 AND AN-7260)



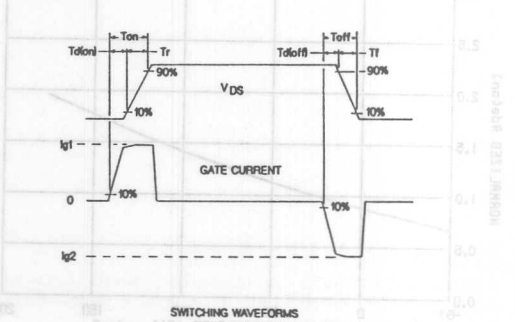
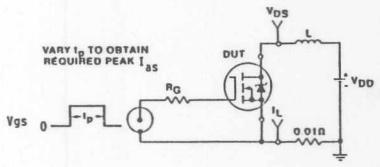
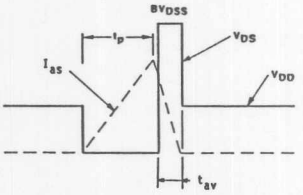


FIGURE 12. RESISTIVE SWITCHING

Performance Curves (Continued)



UIS TEST CIRCUIT.



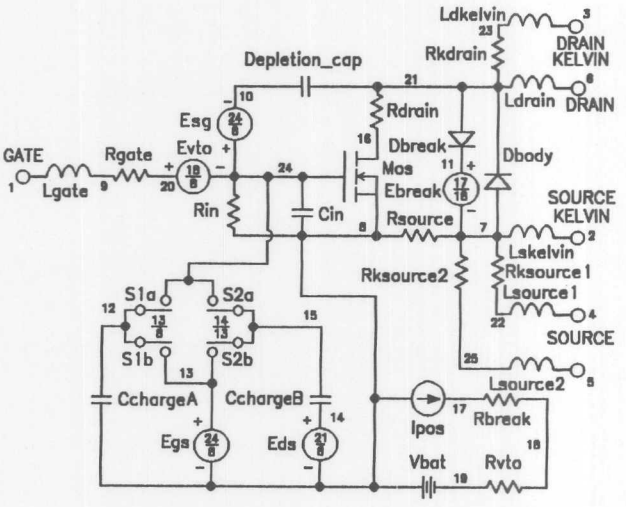
UIS WAVEFORMS.

FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

Spice Model

```
.SUBCKT RFA100N05  6  1  4  5  3  2  ;  rev 10/30/90
*Nominal Temperature = 25°C
CchargeA  12  8  8.98e-9
CchargeB  15  14  8.8e-9
Cin  24  8  4.48e-009
Depletion_cap  10  21  DPLCAPMOD
Dbody  7  21  DBODYMOD
Dbreak  21  11  DBREAKMOD
Eds  14  8  21  8  1
Egs  13  8  24  8  1
Esg  24  10  24  8  1
Ebreak  11  7  17  18  58.4
Evto  20  24  18  8  1
Ipos  8  17  1
Ldkelvin  3  23  1e-9
Ldrain  6  21  2e-10
Lgate  1  9  5e-9
Lskelvin  2  7  5e-9
Lsource1  4  22  6e-9
Lsource2  5  25  6e-9
Mos  16  24  8  8  MOSMOD
Rbreak  17  18  RBREAKMOD  1
Rdrain  21  16  RSOURCEMOD  2.74e-3
Rgate  9  20  1.2
Rkdrain  23  21  0.33e-3
Rksource1  7  22  1.6e-3
Rksource2  7  25  1.6e-3
Rin  24  8  1e+9
Rsource  8  7  RSOURCEMOD  1.2e-3
Rvto  18  19  RVTONEGMOD  1
S1a  24  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  24  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  88  19  DC  1
.MODEL  S1AMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-2.48  VOFF=-0.48)
.MODEL  S1BMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-0.48  VOFF=-2.48)
.MODEL  S2AMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-2.25  VOFF=2.75)
.MODEL  S2BMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=2.75  VOFF=-2.25)
.MODEL  DBODYMOD  D  (IS=2.23e-12  RS=2.5e-3  TRS1=2.5e-3  CJO=7.55e-9  TT=4e-8)
.MODEL  DBREAKMOD  D  (RS=8e-2  TRS1=2.5e-3)
.MODEL  DPLCAPMOD  D  (IS=1e-030  N=10  CJO=2.14e-9)
.MODEL  RBREAKMOD  RES  (TC1=9.5e-4  TC2=-1.17e-6)
.MODEL  RSOURCEMOD  RES  (TC1=5.2e-3  TC2=1.37e-5)
.MODEL  RVTONEGMOD  RES  (TC1=-3.78e-3  TC2=-7.5e-7)
.MODEL  MOSMOD  NMOS  (VTO=3.48  N=10  IS=1e-030  KP=78.5  TOX=1  L=1u  W1u)
.ENDS
```



Performance Curves (Continued)

UIS TEST CIRCUIT.

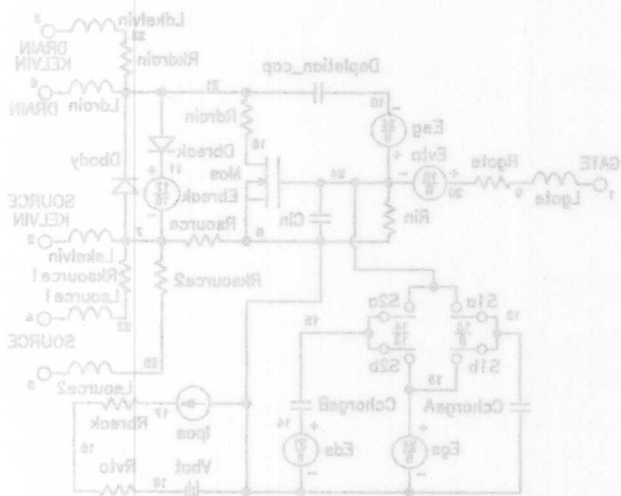
FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

UIS WAVEFORMS.

FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

Spice Model

```
.SUBCKT RFA100N05 6 1 4 5 3 2 ; rev 10/30/90
*Nominal Temperature = 25°C
Cbargea 12 8 8.98e-9
Cbargeb 15 14 8.8e-9
Cin 24 6 4.48e-009
Depletion_cap 10 21 DPLCAPMOD
Dbody 7 21 DBODYMOD
Dbreak 21 11 DBREAKMOD
Ede 14 6 21 6 1
Egs 13 6 24 6 1
Esg 24 10 24 6 1
Ebreak 11 7 17 18 58.4
Evio 20 24 18 6 1
Ipos 6 17 1
Ldrain 8 21 2e-10
Lgate 1 9 5e-9
Lsalvin 2 7 5e-9
Lsource1 4 22 6e-9
Lsource2 5 25 6e-9
Mos 16 24 6 6 MOSMOD
Rbreak 17 18 RBREAKMOD 1
Rdrain 21 16 RSOURCEMOD 2.74e-3
Rgate 9 20 1.2
Rkdrain 23 21 0.23e-3
Rksource1 7 22 1.6e-3
Rksource2 7 25 1.8e-3
Rin 24 6 1e+9
Rsource 6 7 RSOURCEMOD 1.2e-3
Rvio 18 19 RVTONEMOD 1
S1a 24 12 13 6 S1AMOD
S1b 13 12 13 6 S1BMOD
S2a 24 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD
Vbat 6 19 DC 1
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.48 VOFF=-0.48)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.48 VOFF=-2.48)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.25 VOFF=-2.75)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.75 VOFF=-2.25)
.MODEL DBODYMOD D (IS=2.23e-12 RS=2.23e-3 TRS1=2.59e-3 CJO=7.85e-9 TT=4e-8)
.MODEL DBREAKMOD D (RS=8e-2 TRS1=2.5e-3)
.MODEL DPLCAPMOD D (IS=1e-030 N=10 CJO=2.14e-9)
.MODEL RBREAKMOD RES (TC1=9.5e-4 TC2=-1.17e-6)
.MODEL RSOURCEMOD RES (TC1=5.2e-3 TC2=-1.37e-5)
.MODEL RVTONEMOD RES (TC1=-3.78e-3 TC2=-7.5e-7)
.MODEL MOSMOD NMOS (VTO=3.48 N=10 IS=1e-030 KP=78.5 TOX=1 L=1u W=1u)
.ENDS
```



POWER MOSFETs 5

P-CHANNEL POWER MOSFETs

DATA SHEETS		PAGE
2N6804	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-3
2N6849	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-8
2N6851	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-13
2N6895	P-Channel Enhancement-Mode Power MOS Field-Effect Transistors	5-18
2N6896	P-Channel Enhancement-Mode Power MOS Field-Effect Transistors	5-22
2N6897	P-Channel Enhancement-Mode Power MOS Field-Effect Transistors	5-26
2N6898	P-Channel Enhancement-Mode Power MOS Field-Effect Transistors	5-30
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IRF9150, IRF9151	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-44
IRF9230, IRF9231, IRF9232, IRF9233	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-50
IRF9240, IRF9241, IRF9242, IRF9243	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-55
IRF9510, IRF9511, IRF9512, IRF9513	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-60
IRF9520, IRF9521, IRF9522, IRF9523	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-65
IRF9530, IRF9531, IRF9532, IRF9533	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-70
IRF9540, IRF9541, IRF9542, IRF9543	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-75
IRF9620, IRF9621, IRF9622, IRF9623	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-80
IRF9630, IRF9631, IRF9632, IRF9633	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-85
IRF9640, IRF9641, IRF9642, IRF9643	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-90
IRFD9110, IRFD9113	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-95
IRFD9120, IRFD9123	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-100
IRFD9220, IRFD9223	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-105
IRFF9120, IRFF9121, IRFF9122, IRFF9123	Avalanche-Energy-Rated P-Channel Power MOSFETs	5-110

IRFF9130, IRFF9131, IRFF9132, IRFF9133	Avalanche Energy-Rated P-Channel Power MOSFETs	5-115
IRFF9220, IRFF9221, IRFF9222, IRFF9223	Avalanche Energy-Rated P-Channel Power MOSFETs	5-120
IRFF9230, IRFF9231, IRFF9232, IRFF9233	Avalanche Energy-Rated P-Channel Power MOSFETs	5-125
IRFP9140/P9141, IRFP9142/P9143	Avalanche Energy-Rated P-Channel Power MOSFETs	5-130
IRFP9150, IRFP9151	Avalanche Energy-Rated P-Channel Power MOSFETs	5-135
IRFP9240/P9241, IRFP9242/P9243	Avalanche Energy-Rated P-Channel Power MOSFETs	5-140
RFL1P08, RFL1P10	P-Channel Enhancement-Mode Power Field-Effect Transistors	5-145
RFP2P08, RFP2P10	P-Channel Enhancement-Mode Power Field-Effect Transistors	5-149
RFM5P12, RFM5P15, RFP5P12, RFP5P15	P-Channel Enhancement-Mode Power Field-Effect Transistors	5-153
RFM6P08, RFM6P10, RFP6P08, RFP6P10	P-Channel Enhancement-Mode Power Field-Effect Transistors	5-157
RFD8P05/05SM, RFP8P05	P-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)	5-161
RFM8P08, RFM8P10, RFP8P08, RFP8P10	P-Channel Enhancement-Mode Power Field-Effect Transistors	5-166
RFM10P12/M10P15, RFP10P12/P10P15	P-Channel Enhancement-Mode Power Field-Effect Transistors	5-170
RFM12P08/M12P10, RFP12P08/P12P10	P-Channel Enhancement-Mode Power Field-Effect Transistors	5-174
RFD15P05/05SM, RFP15P05	P-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)	5-178
RFH25P08/H25P10, RFK25P08/K25P10	P-Channel Enhancement-Mode Power Field-Effect Transistors	5-183
RFG30P05, RFP30P05	P-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)	5-187
RFG30P06, RFP30P06	P-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)	5-192
RFG60P05E, RFG60P06E	P-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)	5-197

HARRIS

2N6804

Avalanche-Energy-Rated P-Channel Power MOSFETs

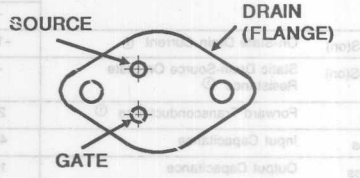
August 1991

Features

- -11A, -100V
- $r_{DS(on)} = 0.30\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AA
BOTTOM VIEW



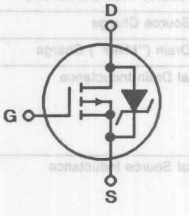
Description

The 2N6804 is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. This is a p-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6804 is supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



5
P-CHANNEL POWER MOSFETs

Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		2N6804	UNITS
Drain-Source Voltage	V_{DS}	-100*	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$)	V_{DGR}	-100*	V
Continuous Drain Current			
$T_C = +25^oC$	I_D	-11*	A
$T_C = +100^oC$	I_D	-7.0*	A
Pulsed Drain Current (Note 2)	I_{DM}	-50*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
$T_C = +25^oC$ (See Figure 14)	P_D	75*	W
Above $T_C = +25^oC$, Derate Linearly (See Figure 14)		0.6*	$W/^oC$
Single Pulse Avalanche Energy (Note 3)	E_{AS}	500	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	^oC
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	^oC

NOTES:

*JEDEC registered values

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
2. Repetitive Rating: Pulse width limited by maximum junction temperature, See Transient Thermal Impedance Curve (Figure 5).
3. $V_{DD} = 25V$, Starting $T_J = 25^oC$, L = 6.2mH, $R_G = 25\Omega$, Peak $I_L = 11A$, (See Figure 15 and 16).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

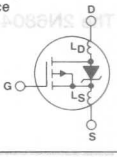
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File Number 2217

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	−100*	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0*	—	−4.0*	V	V_{DS} = V_{GS}, I_D = −0.25mA
I_{GSS}	Gate-Source Leakage Forward	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	−0.25*	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Drain Current ①	−11*	—	—	A	V_{DS} > $I_{D(on)}$ × $R_{DS(on)}$ max., V_{GS} = −10V
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	—	—	0.30	Ω	V_{GS} = −10V, I_D = −6.5A
g_{fs}	Forward Transconductance ①	2.0	3.7	—	S(℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = −6.5A
C_{iss}	Input Capacitance	400	500	—	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100	300	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	50	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	30	60	ns	V_{DD} ≃ −35V, I_D = −7.0A, Z_o = 50Ω
t_r	Rise Time	—	70	140	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	—	70	140	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	25	45	nC	V_{GS} = −15V, I_D = −15A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	13	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	12	22	nC	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

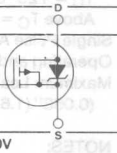


Thermal Resistance

$R_{\theta JC}$	Junction-to-Case	—	—	1.67*	°C/W	
$R_{\theta CS}$	Case-to-Sink	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
$R_{\theta JA}$	Junction-to-Ambient	—	—	30	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	−11*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	−50	A	
V_{SD}	Diode Forward Voltage ①	—	—	−1.5	V	T_C = 25°C, I_S = −11A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	—	250	ns	T_J = 25°C, I_F = −11A, dI_F/dt = −100 A/μs
Q_{RR}	Reverse Recovered Charge	—	1.8	—	μC	T_J = 25°C, I_F = −11A, dI_F/dt = −100 A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



*JEDEC Registered Value

① Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by max. junction temperature, See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 25V, Starting T_J = 25°C, L = 6.2 mH, R_G = 25Ω, Peak I_L = 11 A, (See Fig. 15 and 16).

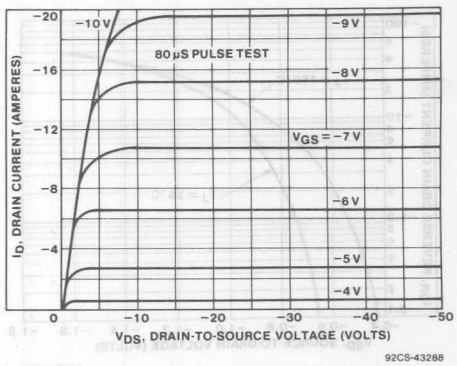


Fig. 1 - Typical Output Characteristics

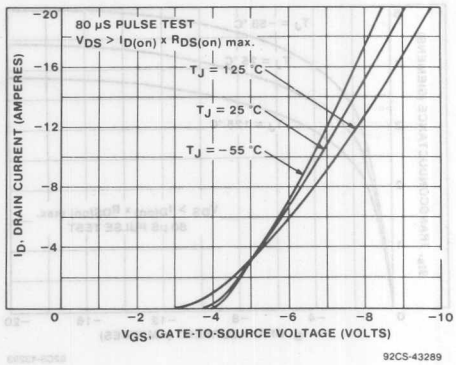


Fig. 2 - Typical Transfer Characteristics

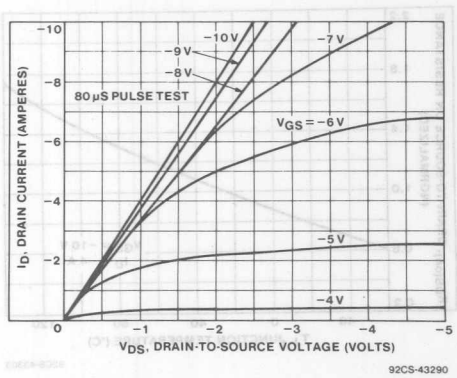


Fig. 3 - Typical saturation characteristic.

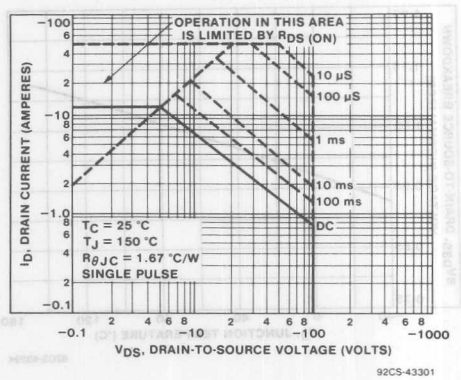


Fig. 4 - Maximum safe operating area.

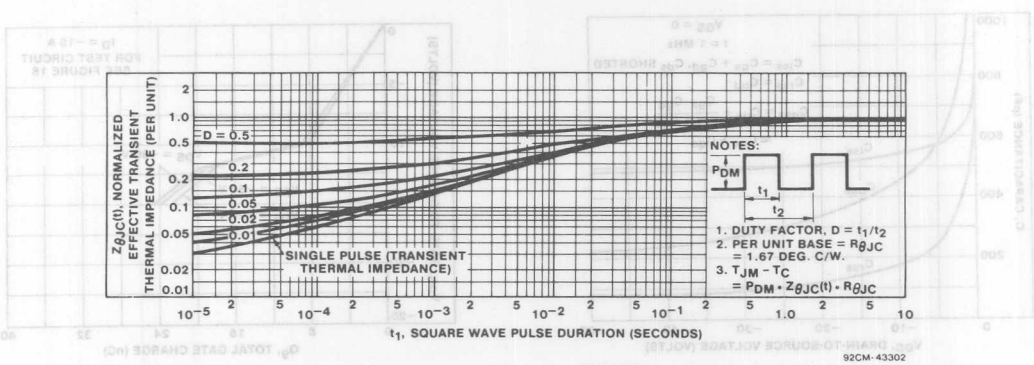


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

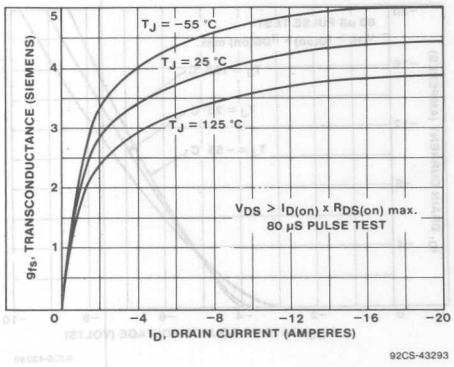


Fig. 6 - Typical transconductance vs. drain current.

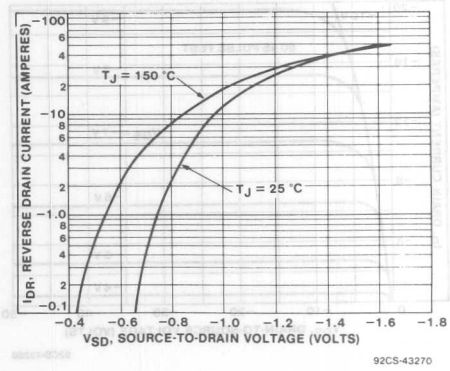


Fig. 7 - Typical source-drain diode forward voltage.

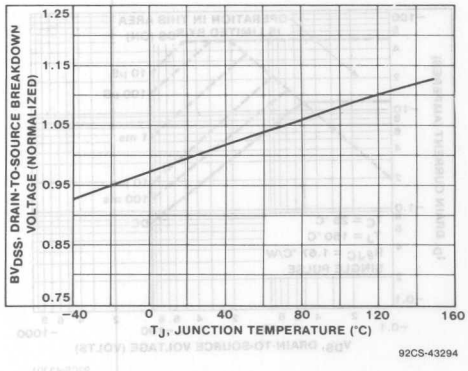


Fig. 8 - Breakdown voltage vs. temperature.

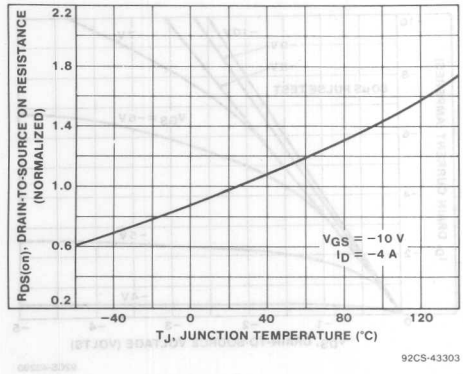


Fig. 9 - Normalized on-resistance vs. temperature.

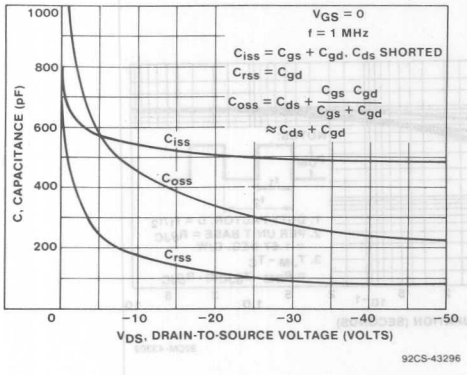


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

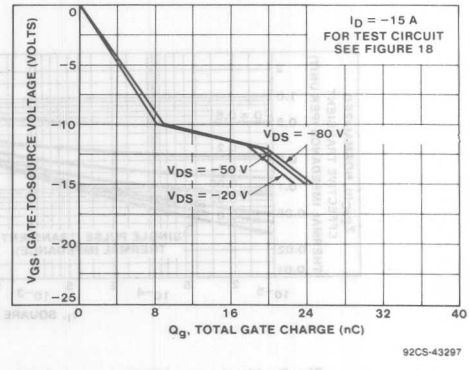


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

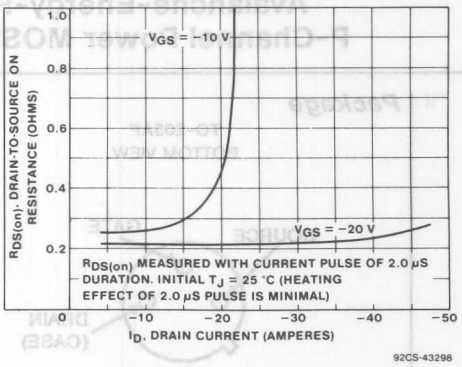


Fig. 12 - Typical on-resistance vs. drain current.

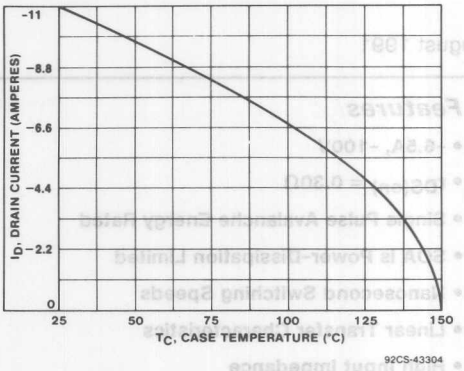


Fig. 13 - Maximum drain current vs. case temperature.

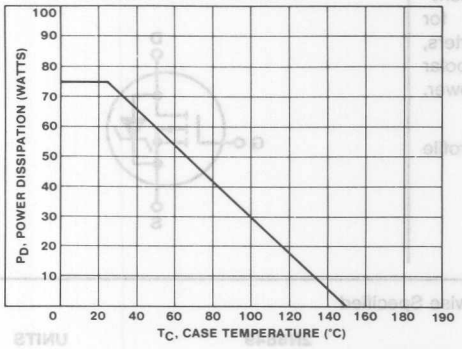


Fig. 14 - Power vs. temperature derating curve.

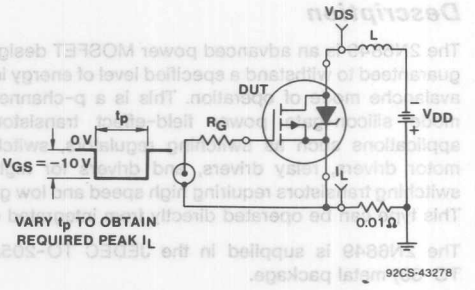


Fig. 15 - Unclamped inductive test circuit.

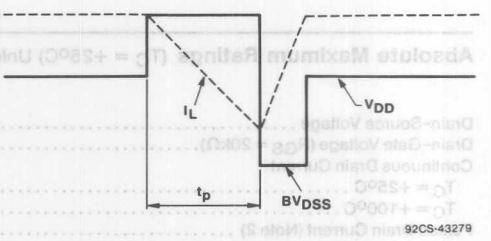


Fig. 16 - Unclamped inductive waveforms.

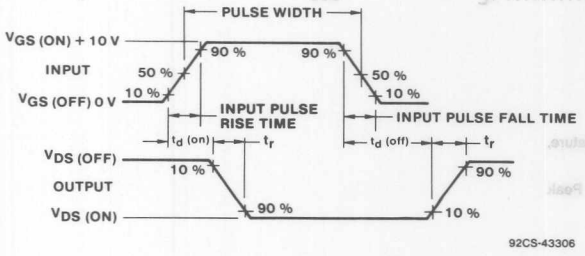


Fig. 17 - Switching time test circuit.

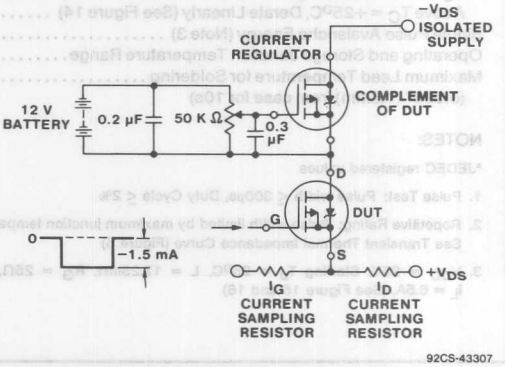


Fig. 18 - Gate charge test circuit.

HARRIS

2N6849

Avalanche-Energy-Rated P-Channel Power MOSFETs

August 1991

Features

- -6.5A, -100V
- $r_{DS(on)} = 0.30\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

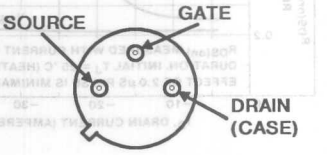
Description

The 2N6849 is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. This is a p-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6849 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6849	UNITS
Drain-Source Voltage	V_{DS}	-100*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	-100*	V
Continuous Drain Current			
T_C = +25°C	I_D	-6.5*	A
T_C = +100°C	I_D	-4.1*	A
Pulsed Drain Current (Note 2)	I_{DM}	-25*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	25*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.2*	W/°C
Single Pulse Avalanche Energy (Note 3)	E_{AS}	500	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	°C

NOTES:

*JEDEC registered values

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. Repetitive Rating: Pulse width limited by maximum junction temperature, See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 25V, Starting T_J = 25°C, L = 17.25mH, R_G = 25Ω, Peak I_L = 6.5A, (See Figure 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

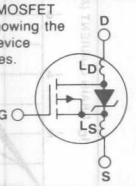
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File Number 2219

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	−100*	—	—	V	V_{GS} = 0V, I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0*	—	−4.0*	V	V_{DS} = V_{GS}, I_D = −0.25mA
I_{GSS}	Gate-Source Leakage Forward	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	−0.25*	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Drain Voltage ①	—	—	−2.1	V	V_{DS} > $I_{D(on)}R_{DS(on)}$max., V_{GS} = −10V, I_D = 6.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	—	—	0.30*	Ω	V_{GS} = −10V, I_D = −4.1A
g_{fs}	Forward Transconductance ①	2.5	3.5	7.5	S(℧)	V_{DS} = −5V, $I_{D(on)}$ × $R_{DS(on)}$ max., I_D = −4.1A
C_{iss}	Input Capacitance	—	500	—	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz
C_{oss}	Output Capacitance	—	300	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	30	60	ns	V_{DD} ≅ −42V, I_D = −4.1A, Z_o = 50Ω
t_r	Rise Time	—	70	140	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	—	70	140	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	25	45	nC	V_{GS} = −15V, I_D = −15A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	13	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	12	22	nC	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

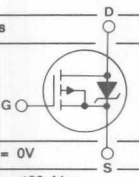


Thermal Resistance

$R\theta_{JC}$	Junction-to-Case	—	—	5.0*	°C/W	
$R\theta_{JA}$	Junction-to-Ambient	—	—	175	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	−6.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	−25	A	
V_{SD}	Diode Forward Voltage ①	—	—	-1.5	V	T_C = 25°C, I_S = −6.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	—	250	ns	T_J = 25°C, I_F = −6.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	—	1.8	—	μC	T_J = 25°C, I_F = −6.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



*JEDEC Registered Value

① Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 25V, starting T_J = 25°C, L = 17.25 mH, R_G = 25Ω, Peak I_L = 6.5A. (See Fig. 15 and 16)

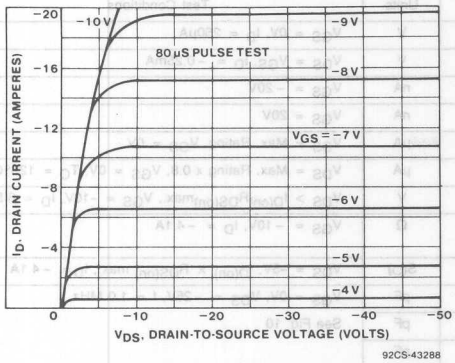


Fig. 1 - Typical Output Characteristics

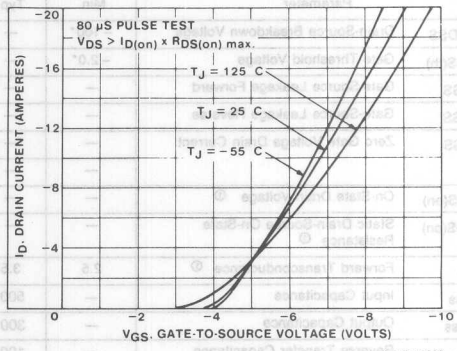


Fig. 2 - Typical Transfer Characteristics

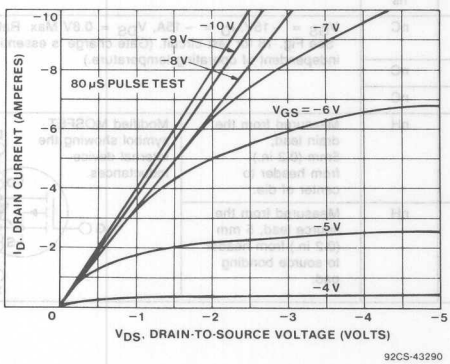


Fig. 3 - Typical Saturation Characteristics

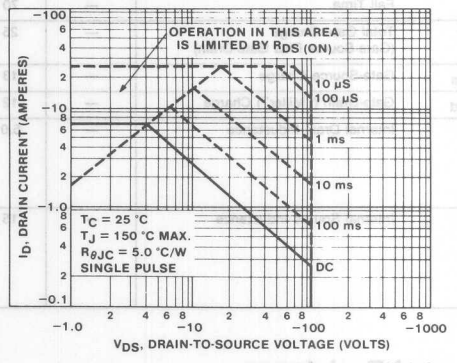


Fig. 4 - Maximum Safe Operating Area

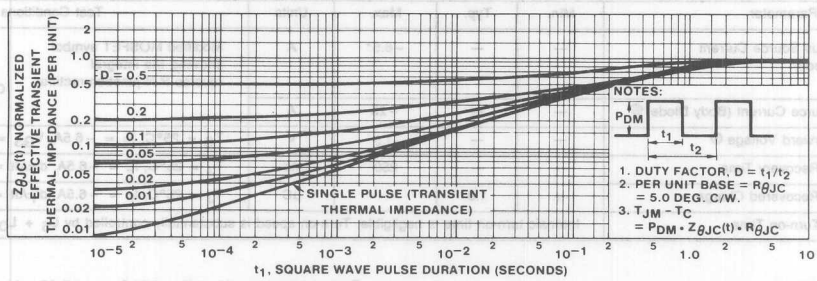


Fig. 5 - Maximum Effective Transient Thermal Impedance,
Junction-to-Case Vs. Pulse Duration

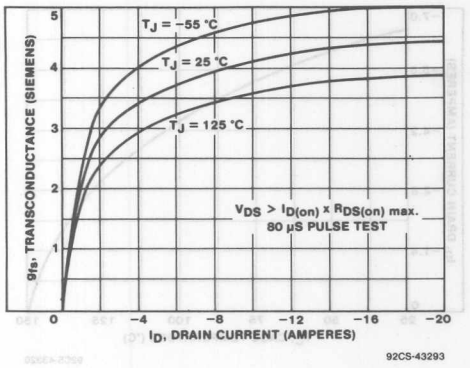


Fig. 6 - Typical Transconductance Vs. Drain Current

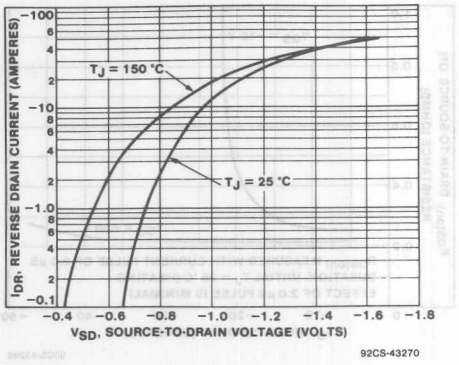


Fig. 7 - Typical Source-Drain Diode Forward Voltage

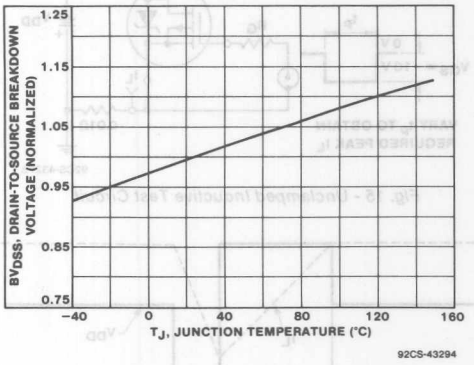


Fig. 8 - Breakdown Voltage Vs. Temperature

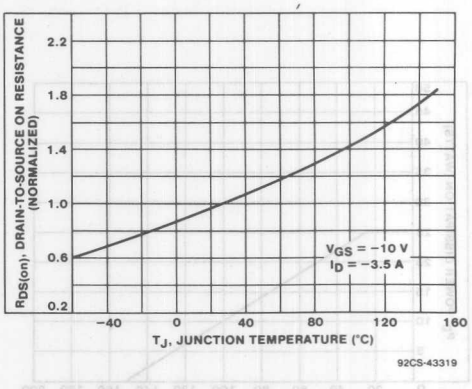


Fig. 9 - Normalized On-Resistance Vs. Temperature

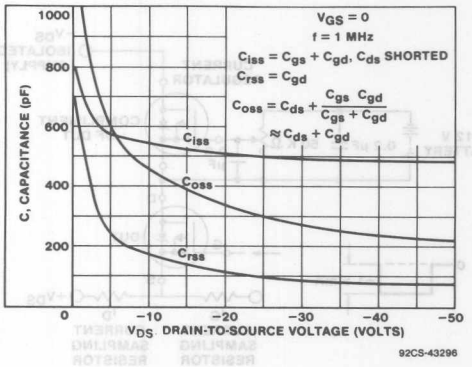


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

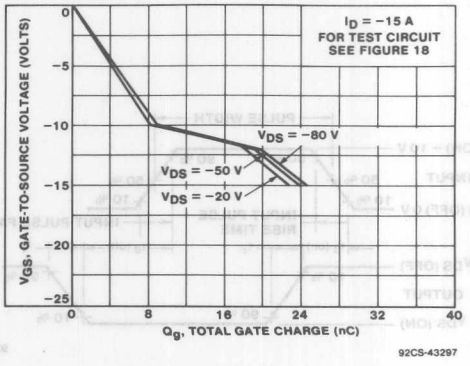


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

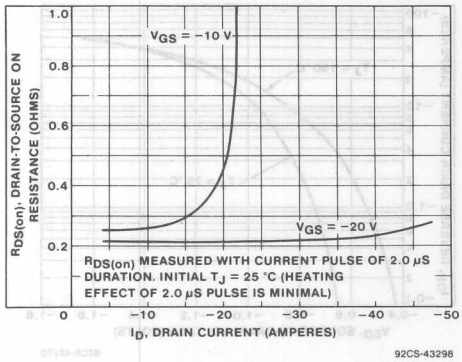


Fig. 12 - Typical On-Resistance Vs. Drain Current

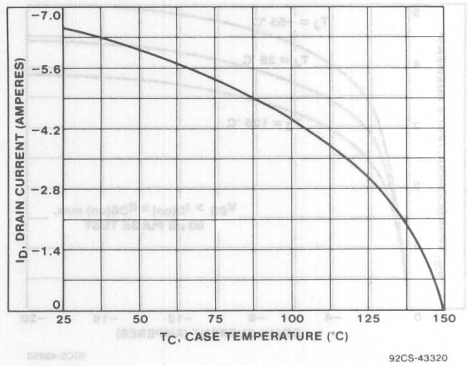


Fig. 13 - Maximum Drain Current Vs. Case Temperature

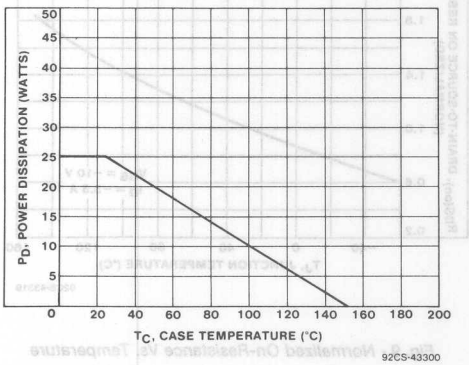


Fig. 14 - Power Vs. Temperature Derating Curve

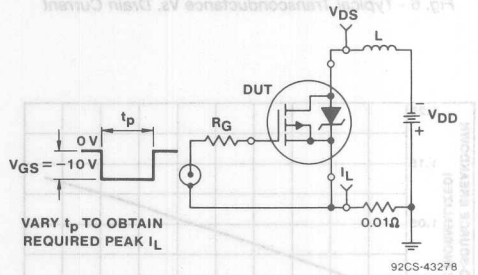


Fig. 15 - Unclamped Inductive Test Circuit

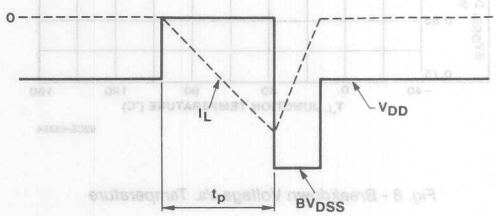


Fig. 16 - Unclamped Inductive Waveforms

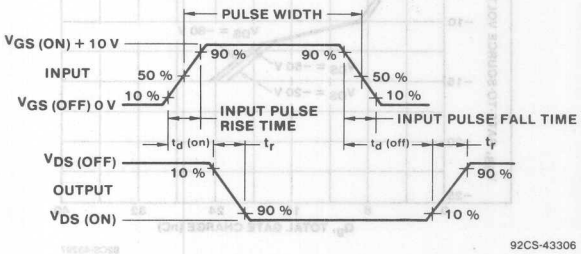


Fig. 17 - Switching Time Test Circuit

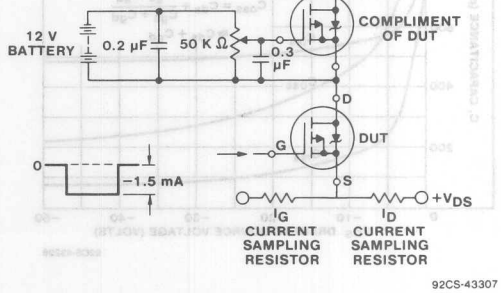


Fig. 18 - Gate Charge Test Circuit

HARRIS

2N6851

Avalanche-Energy-Rated P-Channel Power MOSFETs

August 1991

Features

- -4.0A, -200V
- $r_{DS(on)} = 0.80\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

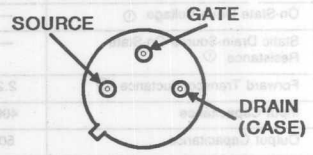
Description

The 2N6851 is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. This is a p-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6851 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

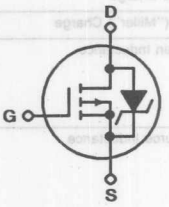
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



5 P-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6851	UNITS
Drain-Source Voltage	V_{DS}	-200*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	-200*	V
Continuous Drain Current			
T_C = +25°C	I_D	-4.0*	A
T_C = +100°C	I_D	-2.4*	A
Pulsed Drain Current (Note 2)	I_{DM}	-20*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	25*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.2*	W/°C
Single Pulse Avalanche Energy (Note 3)	E_{AS}	500	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	°C

NOTES:

*JEDEC registered values

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
2. Repetitive Rating: Pulse width limited by maximum junction temperature, See Transient Thermal Impedance Curve (Figure 5).
3. V_{DD} = 50V, Starting T_J = 25°C, L = 46.9mH, R_G = 25Ω, Peak I_L = 4.0A, (See Figure 15 and 16).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

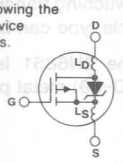
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File Number 2218

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	−200*	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0*	—	−4.0*	V	V_{DS} = V_{GS}, I_D = −0.25mA
I_{GSS}	Gate-Source Leakage Forward	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	−0.25*	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Drain Voltage ①	—	—	−3.3	V	V_{DS} > $I_{D(on)}$ × $R_{DS(on)}$ max., V_{GS} = −10V, I_D = −4.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	—	—	0.80*	Ω	V_{GS} = −10V, I_D = −2.4A
g_{fs}	Forward Transconductance ①	2.2	3.5	−6.6	S(℧)	V_{DS} = −5V × $R_{DS(on)max.}$, I_D = −2.4A
C_{iss}	Input Capacitance	400	550	—	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz
C_{oss}	Output Capacitance	50	170	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	40	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	30	50	ns	V_{DD} ≅ −95V, I_D = −2.4A, Z_o = 50Ω
t_r	Rise Time	—	50	100	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	—	50	80	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	40	80	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	31	45	nC	V_{GS} = −15V, I_D = −8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	18	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	13	22	nC	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

$R\theta_{JC}$	Junction-to-Case	—	—	5.0*	°C/W	
$R\theta_{JA}$	Junction-to-Ambient	—	—	175	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	−4.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	−20	A	
V_{SD}	Diode Forward Voltage ①	—	—	-1.5	V	T_C = 25°C, I_S = −4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	—	400	ns	T_J = 25°C, I_F = −4.0A, dI_F/dt = −100 A/μs
Q_{RR}	Reverse Recovered Charge	—	2.6	—	μC	T_J = 25°C, I_F = −4.0A, dI_F/dt = −100 A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



*JEDEC Registered Value

① Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 50V, starting T_J = 25°C, L = 46.9 mH, R_G = 25Ω, Peak I_L = 4.0A. (See Fig. 15 and 16)

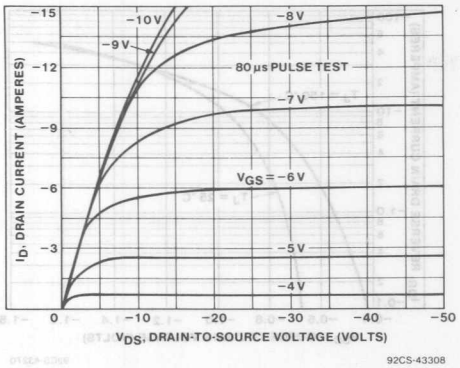


Fig. 1 - Typical Output Characteristics

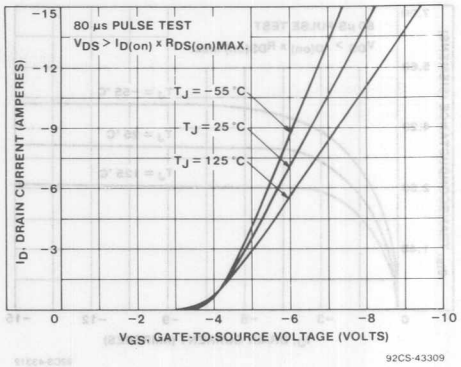


Fig. 2 - Typical Transfer Characteristics

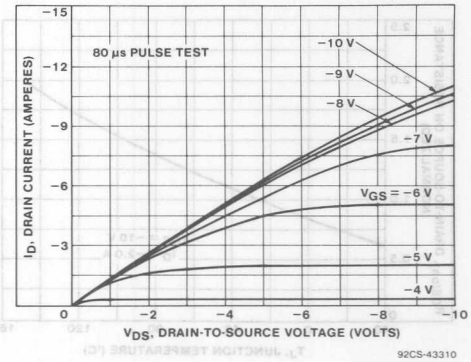


Fig. 3 - Typical Saturation Characteristics

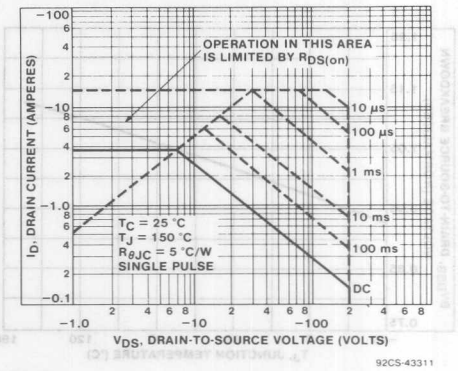


Fig. 4 - Maximum Safe Operating Area

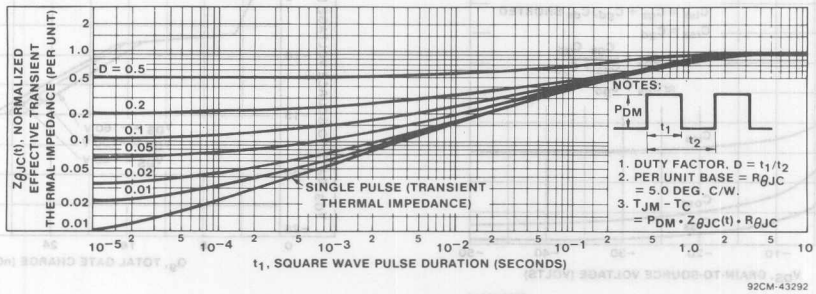


Fig. 5 - Maximum Effective Transient Thermal Impedance,
Junction-to-Case Vs. Pulse Duration

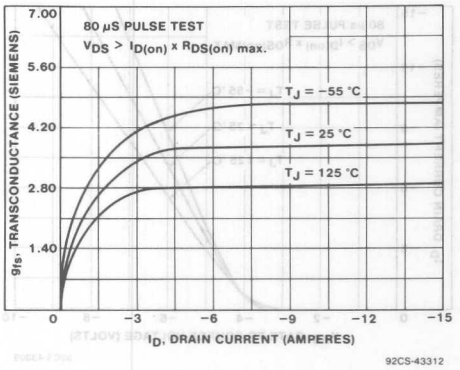


Fig. 6 - Typical Transconductance Vs. Drain Current

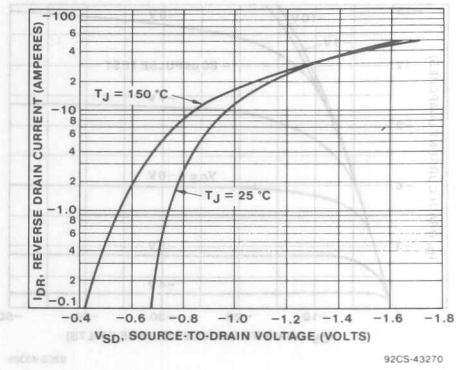


Fig. 7 - Typical Source-Drain Diode Forward Voltage

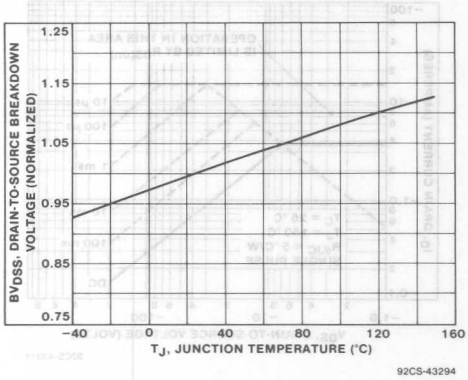


Fig. 8 - Breakdown Voltage Vs. Temperature

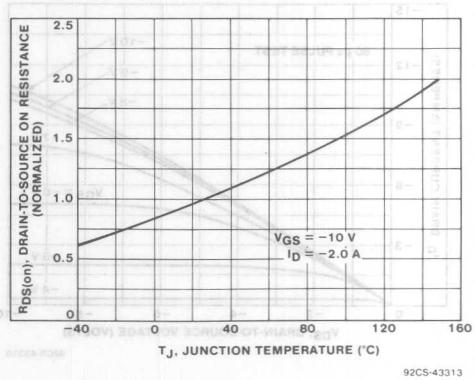


Fig. 9 - Normalized On-Resistance Vs. Temperature

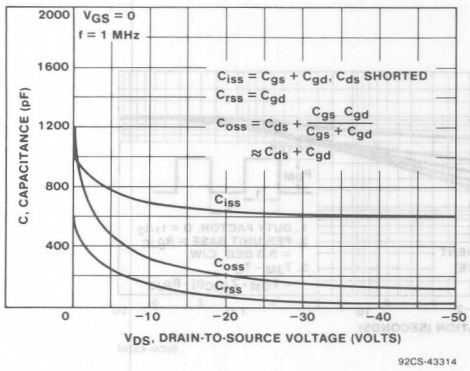


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

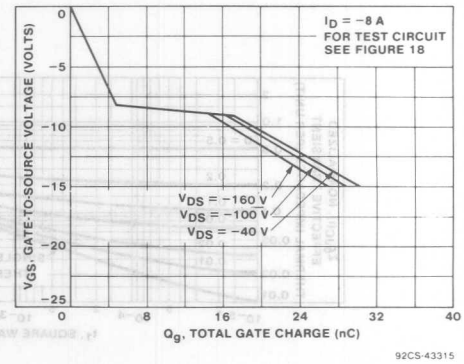


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

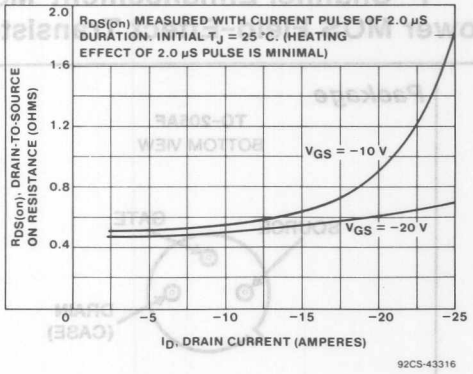


Fig. 12 - Typical On-Resistance Vs. Drain Current

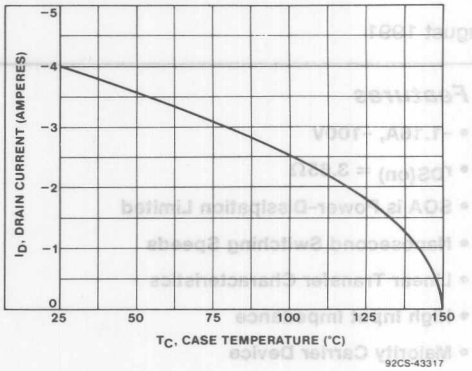


Fig. 13 - Maximum Drain Current Vs. Case Temperature

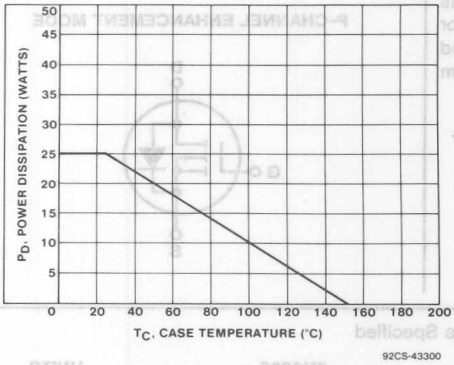


Fig. 14 - Power Vs. Temperature Derating Curve

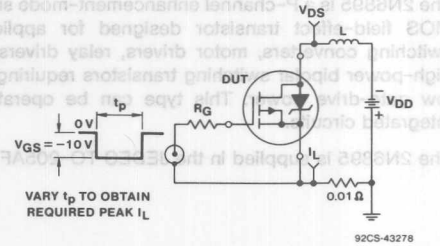


Fig. 15 - Unclamped Inductive Test Circuit

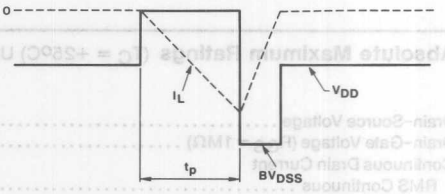


Fig. 16 - Unclamped Inductive Waveforms

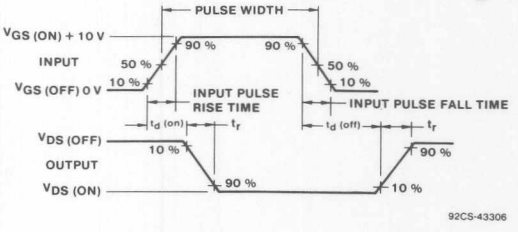


Fig. 17 - Switching Time Test Circuit

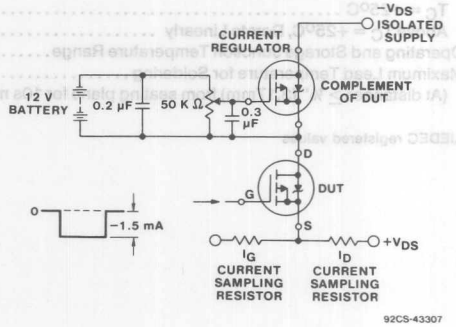


Fig. 18 - Gate Charge Test Circuit

5 P-CHANNEL POWER MOSFETs

Power MOS Field-Effect Transistors

Features

- -1.16A, -100V
- $r_{DS(on)} = 3.65\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

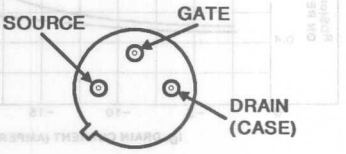
Description

The 2N6895 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6895 is supplied in the JEDEC TO-205AF metal package.

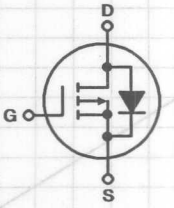
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6895	UNITS
Drain-Source Voltage	V_{DSS}	-100*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	-100*	V
Continuous Drain Current			
RMS Continuous	I_D	-1.16*	A
Pulsed Drain Current	I_{DM}	-5*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	8.33*	W
Above T_C = +25°C, Derate Linearly		0.0667*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (At distances ≥ ⅛" (3.17mm) from seating plane for 10s max)	T_L	260	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number **1873**

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 0.74 A, V_{GS} = -10 V	—	2.7	V
			I_D = 1.16 A, V_{GS} = -10 V	—	6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 0.74 A, V_{GS} = -10 V	—	3.65	Ω
			T_C = 125°C, I_D = 0.74 A, V_{GS} = 10 V	—	5.66	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 0.74 A	200	800	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	40	150	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	20	80	
*	Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	7.5	30	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	25	ns
*	Rise Time	t_r	I_D = 0.74 A	—	45	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	45	
*	Fall Time	t_f	V_{GS} = -10 V	—	50	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1.16 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 50 A/μs	—	340	ns

*In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

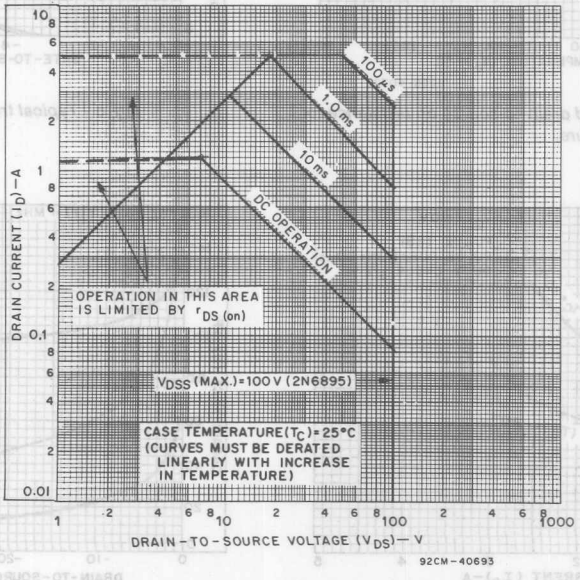


Fig. 1 - Maximum operating areas.

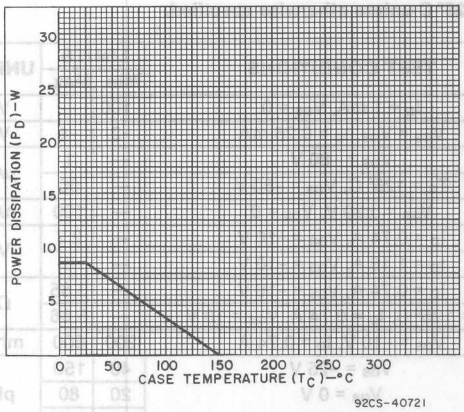


Fig. 2 - Power dissipation vs. temperature derating curve.

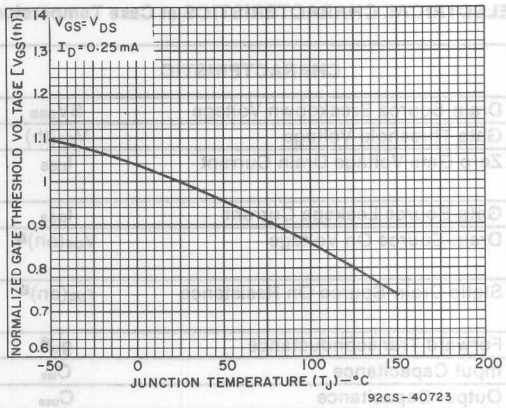


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

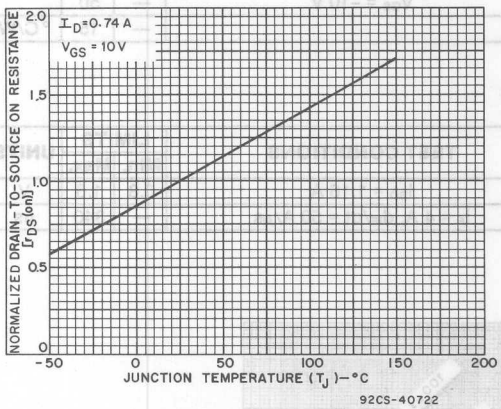


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

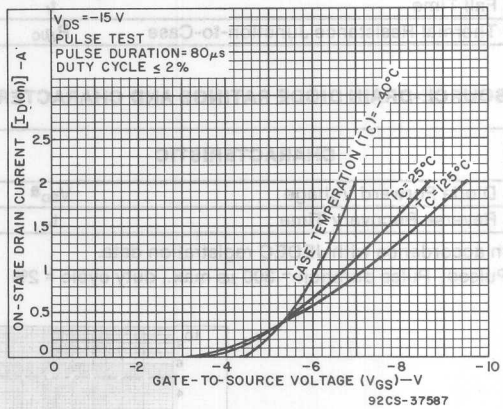


Fig. 5 - Typical transfer characteristics.

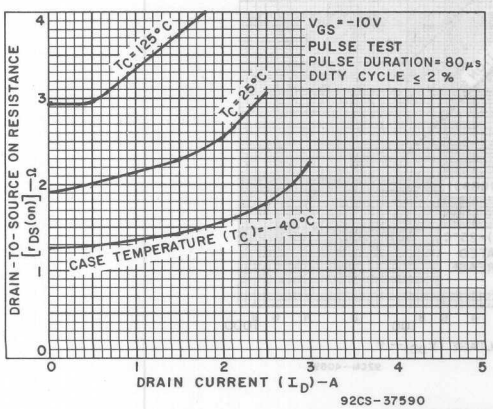


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

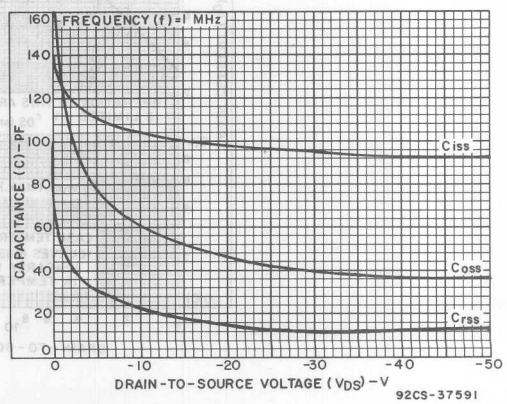


Fig. 7 - Capacitance as a function of drain-to-source voltage.

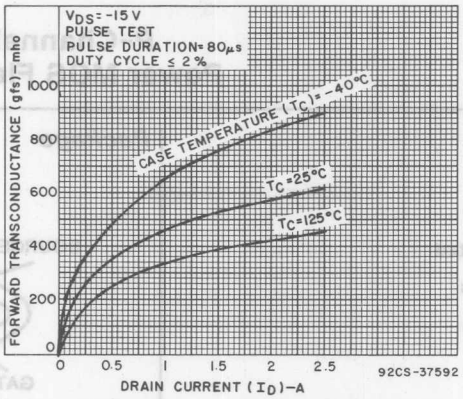


Fig. 8 - Typical forward transconductance as a function of drain current.

HARRIS

2N6896

August 1991

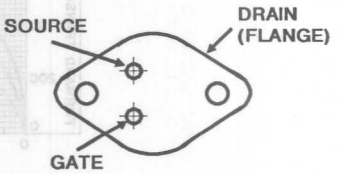
P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

Features

- -6A, -100V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AA
BOTTOM VIEW



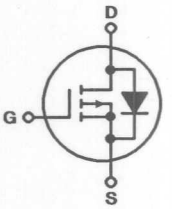
Description

The 2N6896 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

The 2N6896 is supplied in the JEDEC TO-204AA metal package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6896	UNITS
Drain-Source Voltage	V_{DSS}	-100*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	-100*	V
Continuous Drain Current			
RMS Continuous	I_D	-6*	A
Pulsed Drain Current	I_{DM}	-20*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	60*	W
Above T_C = +25°C, Derate Linearly		0.48*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (At distances ≥ ⅛" (3.17mm) from seating plane for 10s max)	T_L	260	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1874

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 3.8 A, V_{GS} = -10 V	—	2.28	V
			I_D = 6 A, V_{GS} = -10 V	—	-6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 3.8 A, V_{GS} = -10 V	—	0.6	Ω
			T_C = 125°C, I_D = 3.8 A, V_{GS} = 10 V	—	0.96	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 3.8 A	1	4	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	200	800	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	100	350	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	40	150	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	60	ns
*	Rise Time	t_r	I_D = 3.8 A	—	100	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	150	
*	Fall Time	t_f	V_{GS} = -10 V	—	100	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	2.083	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 12 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 50 A/μs	—	375	ns

*In accordance with JEDEC registration data.
[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

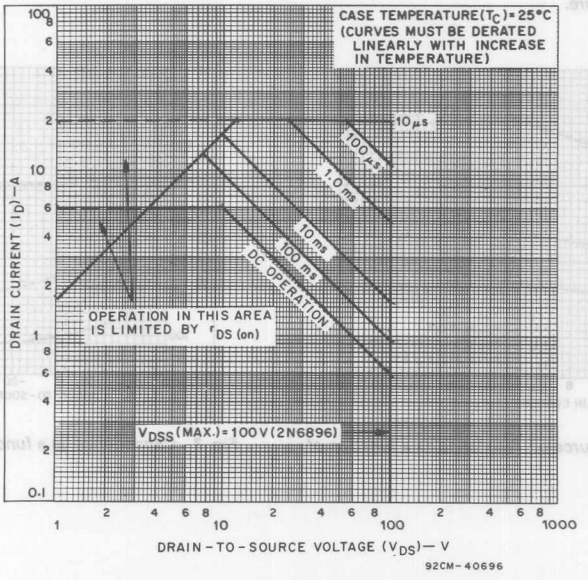


Fig. 1 - Maximum safe operating areas.

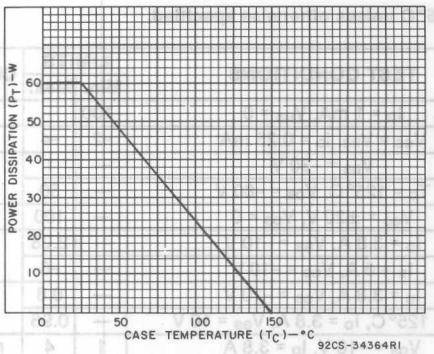


Fig. 2 - Power dissipation vs. temperature derating curve.

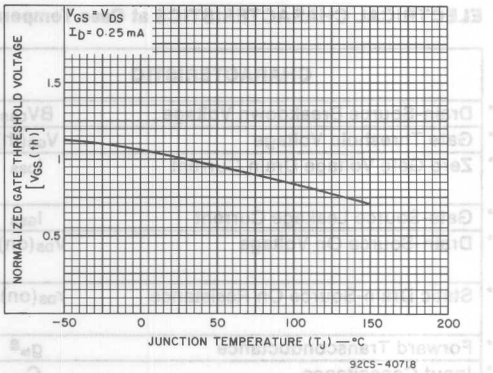


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

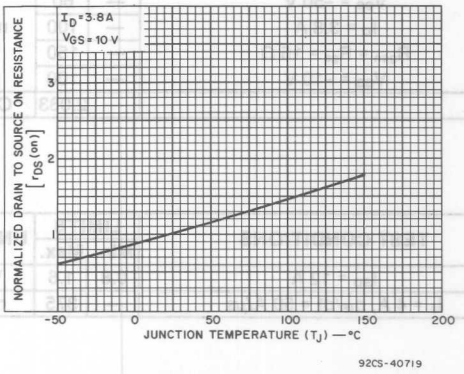


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

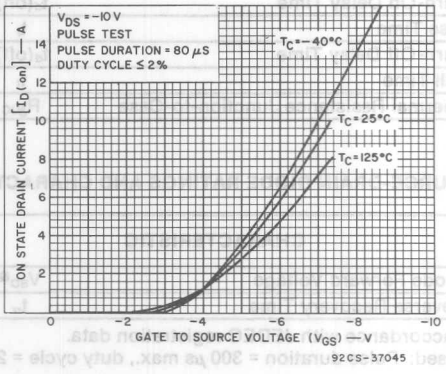


Fig. 5 - Typical transfer characteristics.

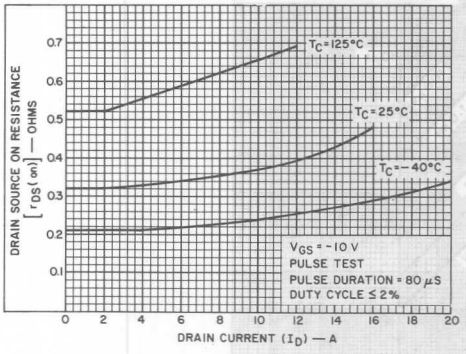


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

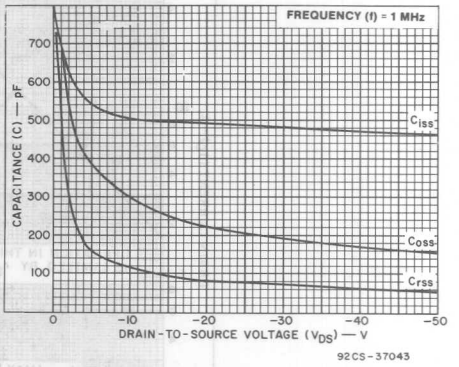


Fig. 7 - Capacitance as a function of drain-to-source voltage.

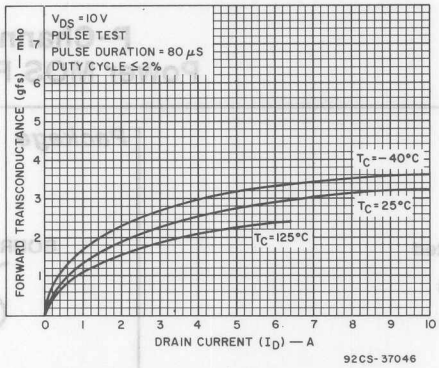


Fig. 8 - Typical forward transconductance as a function of drain current.

HARRIS

2N6897

P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

August 1991

Features

- -12A, -100V
- $r_{DS(on)} = 0.3\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

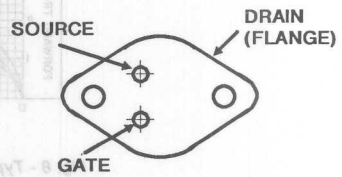
Description

The 2N6897 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This device can be operated directly from an integrated circuit.

The 2N6897 is supplied in the JEDEC TO-204AA metal package.

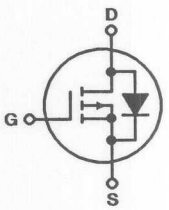
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6897	UNITS
Drain-Source Voltage	V_{DSS}	-100*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	-100*	V
Continuous Drain Current			
RMS Continuous	I_D	-12*	A
Pulsed Drain Current	I_{DM}	-30*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	100*	W
Above T_C = +25°C, Derate Linearly		0.8*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (At distances ≥ ⅛" (3.17mm) from seating plane for 10s max)	T_L	260*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1875

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 7.6 A, V_{GS} = -10 V	—	2.28	V
			I_D = 12 A, V_{GS} = -10 V	—	-4.8	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 7.6 A, V_{GS} = -10 V	—	0.3	Ω
			T_C = 125°C, I_D = 7.6 A, V_{GS} = 10 V	—	0.465	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 7.6 A	2	8	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	400	1500	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	200	700	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	60	240	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	60	ns
*	Rise Time	t_r	I_D = 7.6 A	—	175	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	275	
*	Fall Time	t_f	V_{GS} = -10 V	—	175	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	1.25	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 12 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 100 A/μs	—	500	ns

*In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

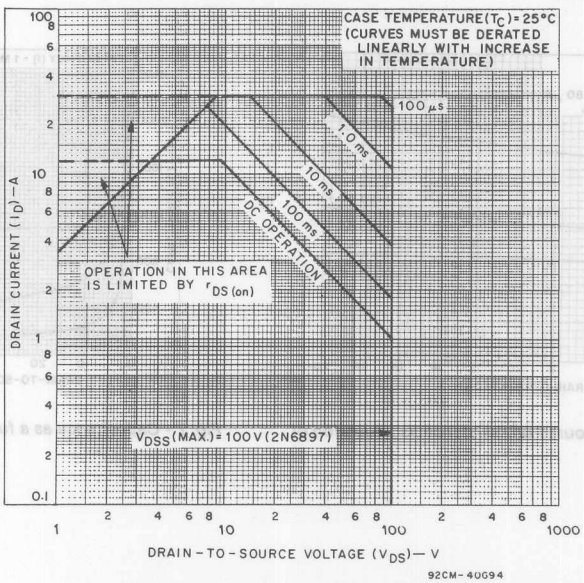


Fig. 1 - Maximum safe operating areas.

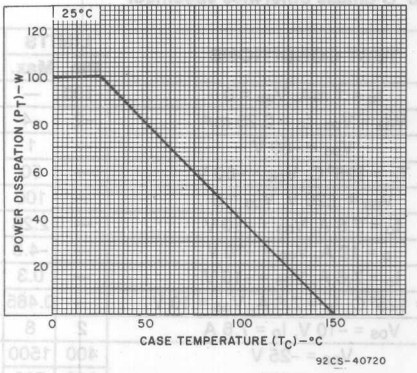


Fig. 2 - Power dissipation vs. temperature derating curve.

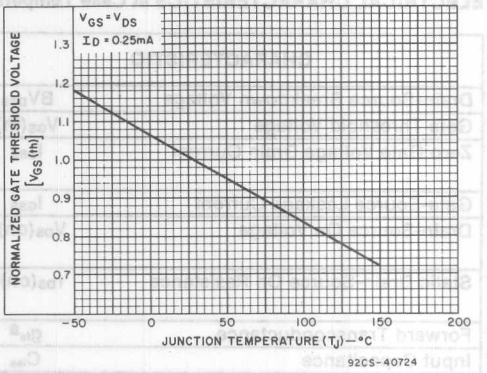


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

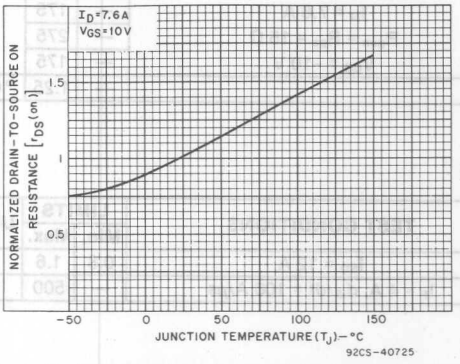


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

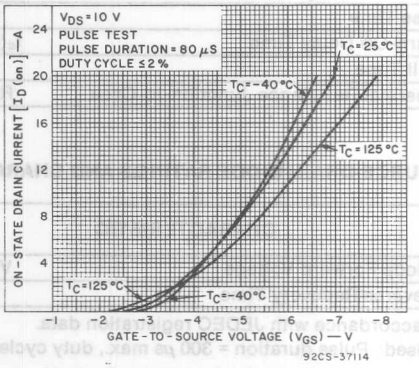


Fig. 5 - Typical transfer characteristics.

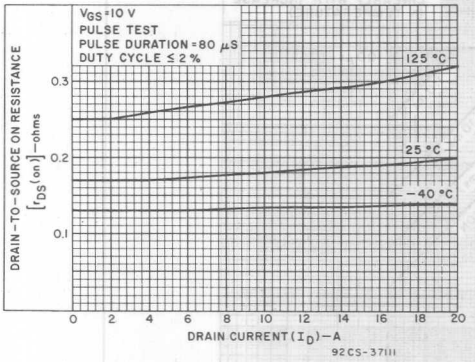


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

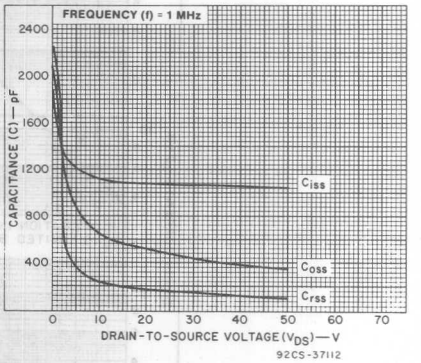


Fig. 7 - Capacitance as a function of drain-to-source voltage.

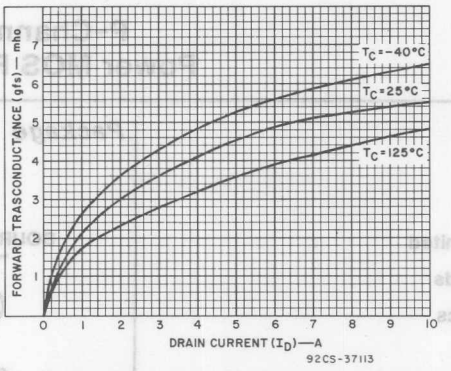


Fig. 8 - Typical forward transconductance as a function of drain current.

HARRIS

2N6898

P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

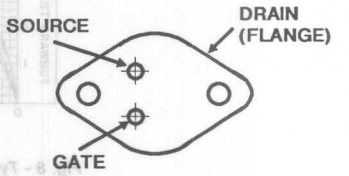
August 1991

Features

- -25A, -100V
- $r_{DS(on)}$ = 0.20Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-204AE
BOTTOM VIEW



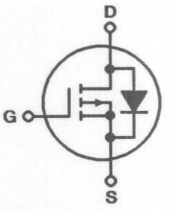
Description

The 2N6898 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This device can be operated directly from an integrated circuit.

The 2N6898 is supplied in the JEDEC TO-204AE steel package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	2N6898	UNITS
Drain-Source Voltage ..... V_{DSS}	-100*	V
Drain-Gate Voltage (R_{GS} = 1MΩ) ..... V_{DGR}	-100*	V
Continuous Drain Current		
RMS Continuous ..... I_D	-25*	A
Pulsed Drain Current ..... I_{DM}	-60*	A
Gate-Source Voltage ..... V_{GS}	±20*	V
Maximum Power Dissipation		
T_C = +25°C ..... P_D	150*	W
Above T_C = +25°C, Derate Linearly	1.2*	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering ..... T_L	260*	°C
(At distances ≥ ⅛" (3.17mm) from seating plane for 10s max)		

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1876

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 15.8 A, V_{GS} = -10 V	—	3.16	V
			I_D = 25 A, V_{GS} = -10 V	—	-6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 15.8 A, V_{GS} = -10 V	—	0.2	Ω
			T_C = 125°C, I_D = 15.8 A, V_{GS} = 10 V	—	0.24	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 15.8 A	4	16	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	—	3000	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1500	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	—	500	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	50	ns
*	Rise Time	t_r	I_D = 12.5 A	—	250	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 50 Ω	—	400	
*	Fall Time	t_f	V_{GS} = -10 V	—	250	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	0.83	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 25 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 100 A/μs	—	750	ns

*In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

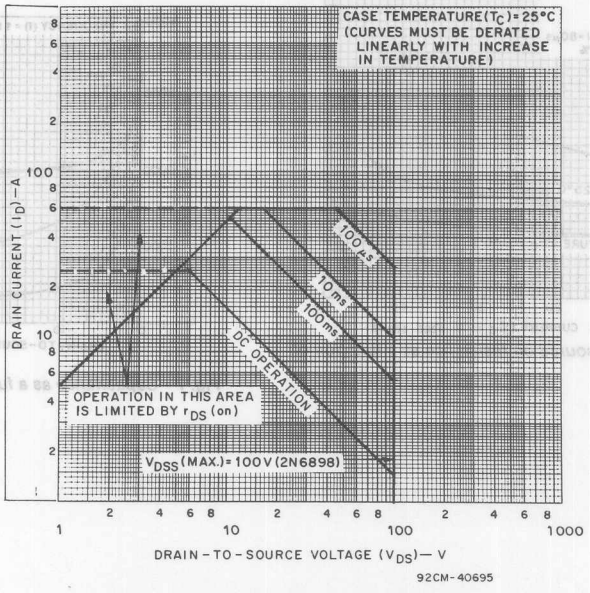


Fig. 1 - Maximum safe operating areas.

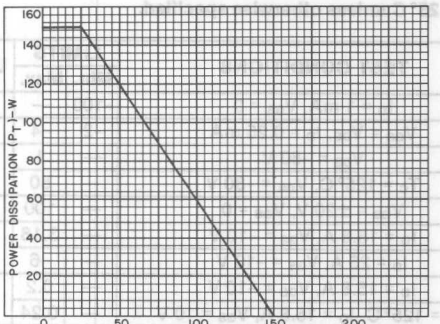


Fig. 2 - Power dissipation vs. temperature derating curve.

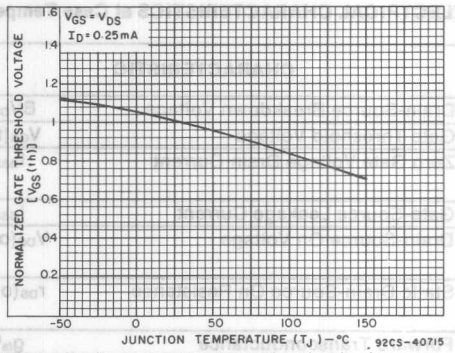


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

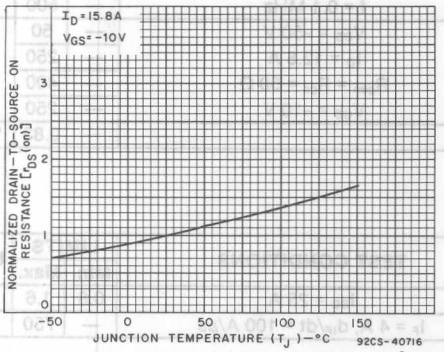


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

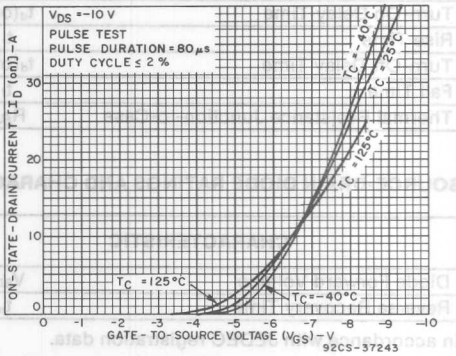


Fig. 5 - Typical transfer characteristics.

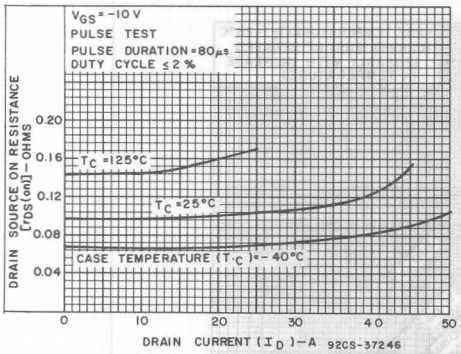


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

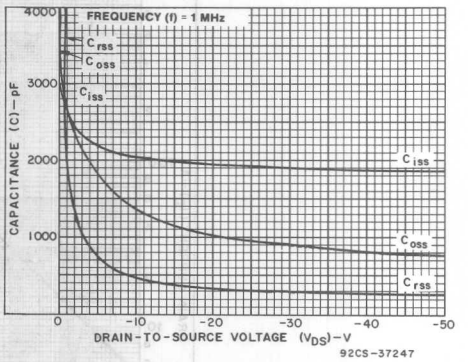


Fig. 7 - Capacitance as a function of drain-to-source voltage.

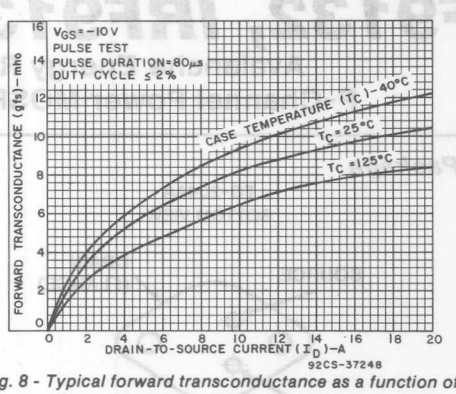


Fig. 8 - Typical forward transconductance as a function of drain current.

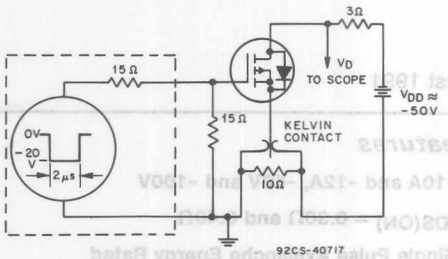


Fig. 9 - Switching time test circuit.

HARRIS

IRF9130, IRF9131 IRF9132, IRF9133

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -10A and -12A, -60V and -100V
- $r_{DS(ON)}$ = 0.30Ω and 0.40Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

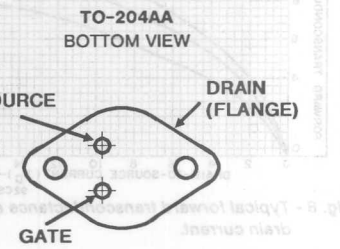
Description

The IRF9130, IRF9131, IRF9132 and IRF9133 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

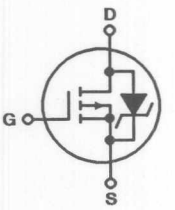
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9130	IRF9131	IRF9132	IRF9133	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-12	-12	-10	-10	A
T_C = 100°C ..... I_D	-7.5	-7.5	-6.5	-6.5	A
Pulsed Drain Current (3) ..... I_{DM}	-48	-48	-40	-40	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	75	75	75	75	W
Linear Derating Factor ..... (See Figure 14)	0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	500	500	500	500	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 5.2mH, R_G = 25Ω, Peak I_L = 12A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2220

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9130, IRF9132	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9131, IRF9133			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9130, IRF9131	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-12	-	-	A
IRF9132, IRF9133			-10	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9130, IRF9131	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -6.5A	-	0.25	0.30	Ω
IRF9132, IRF9133			-	0.30	0.40	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -6.5A	2	3.7	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	500	-	pF
Output Capacitance	C_{OSS}		-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -6.5A, Z_O = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	60	ns
Rise Time	t_r		-	70	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	140	ns
Fall Time	t_f		-	70	140	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -15A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	25	45	nC
Gate-Source Charge	Q_{gs}		-	13	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-12	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-48	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -12A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 12A, dI_F/dt = 100A/μs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -12A, dI_F/dt = 100A/μs	-	1.8	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 5.2mH, R_G = 25Ω, Peak I_L = 12A (See Figures 15 and 16)

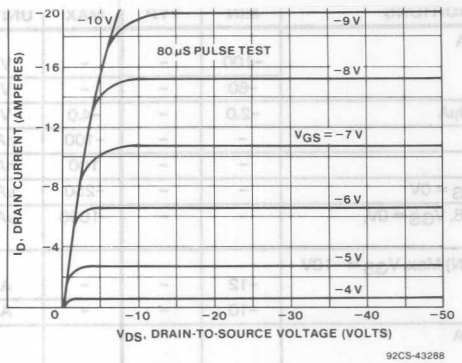


Fig. 1 - Typical Output Characteristics

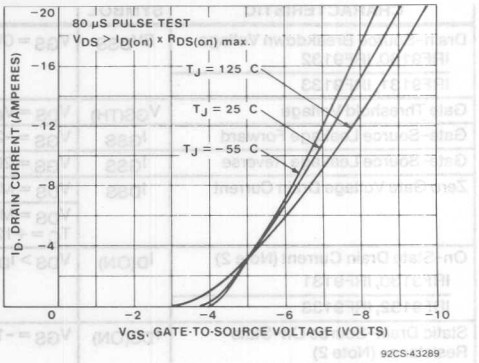


Fig. 2 - Typical Transfer Characteristics

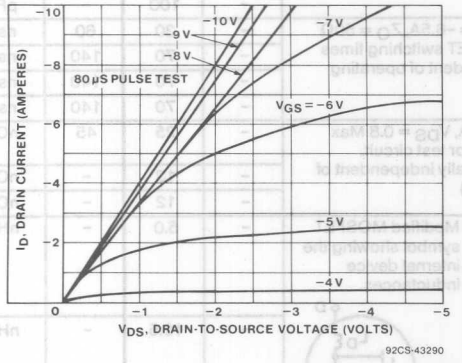


Fig. 3 - Typical Saturation Characteristics

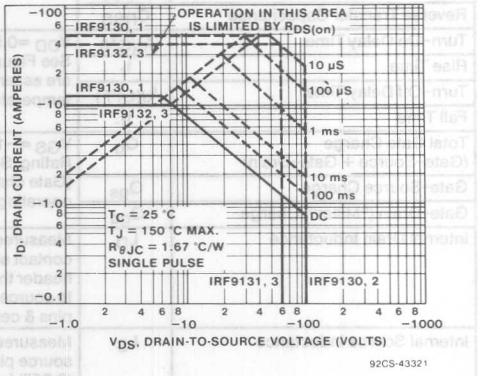


Fig. 4 - Maximum Safe Operating Area

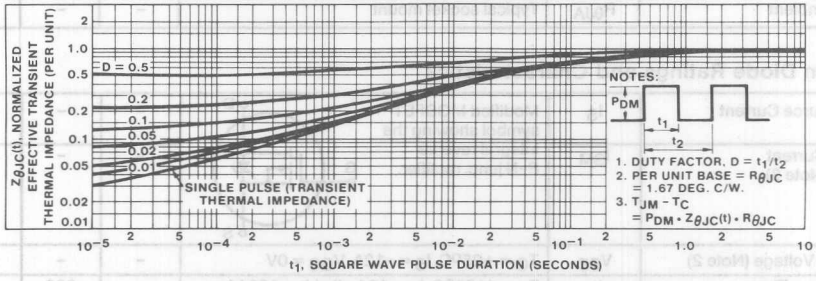


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

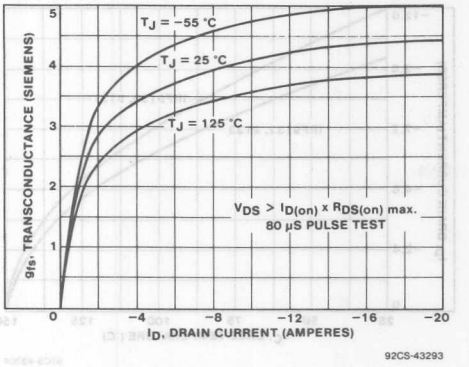


Fig. 6 - Typical Transconductance Vs. Drain Current

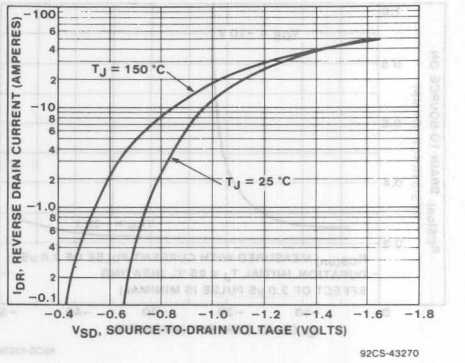


Fig. 7 - Typical Source-Drain Diode Forward Voltage

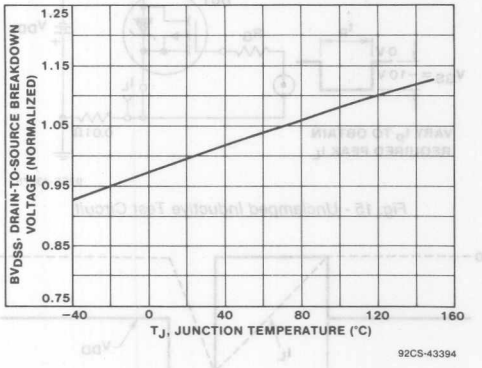


Fig. 8 - Breakdown Voltage Vs. Temperature

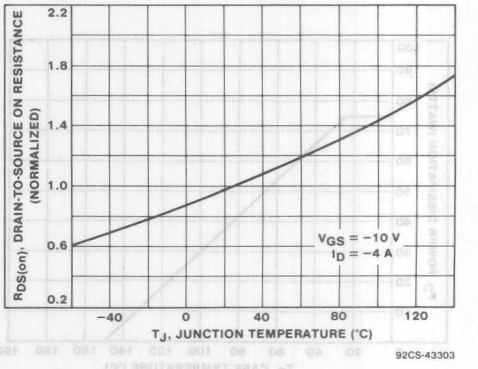


Fig. 9 - Normalized On-Resistance Vs. Temperature

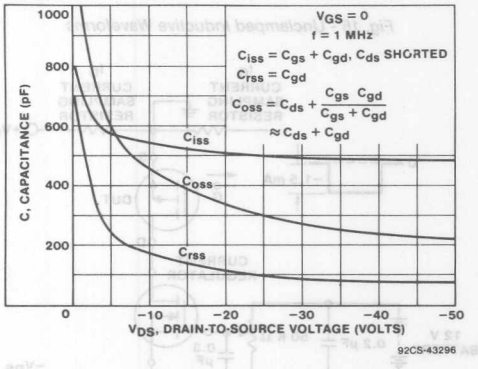


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

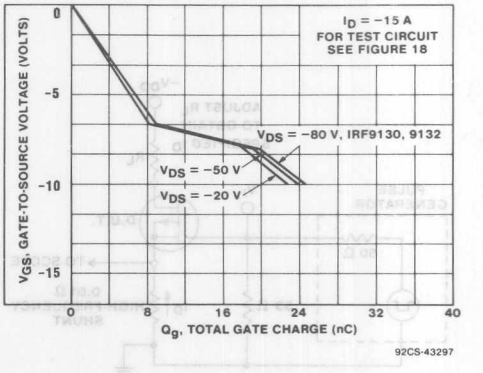


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

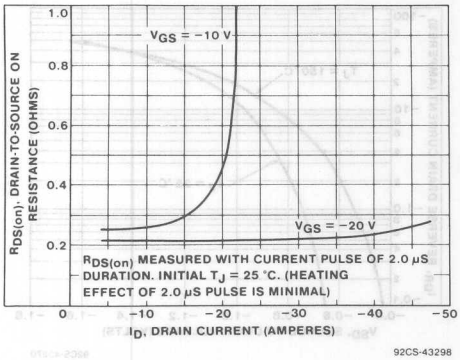


Fig. 12 - Typical On-Resistance Vs. Drain Current

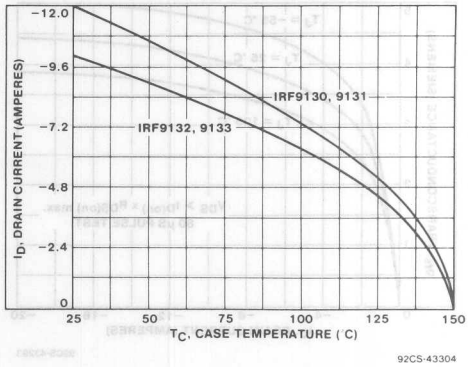


Fig. 13 - Maximum Drain Current Vs. Case Temperature

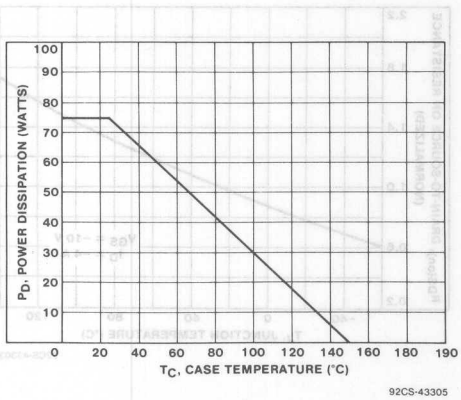


Fig. 14 - Power Vs. Temperature Derating Curve

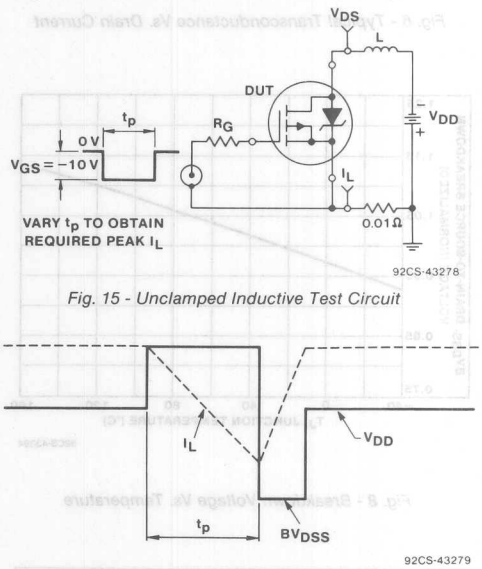


Fig. 15 - Unclamped Inductive Test Circuit

Fig. 16 - Unclamped Inductive Waveforms

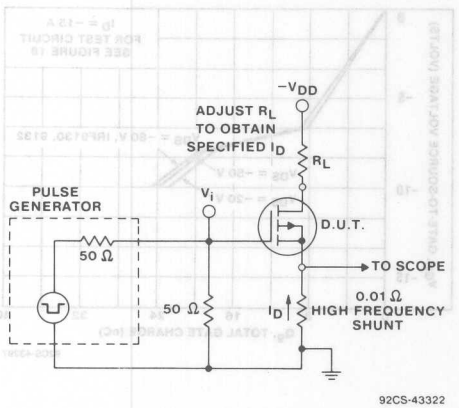


Fig. 17 - Switching Time Test Circuit

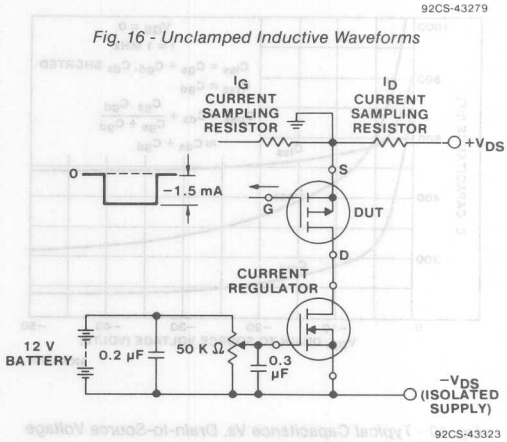


Fig. 18 - Gate Charge Test Circuit

HARRIS

IRF9140, IRF9141 IRF9142, IRF9143

Avalanche Energy Rated P-Channel Power MOSFETs

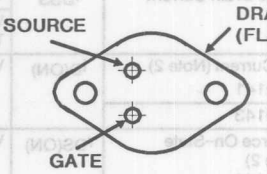
August 1991

Features

- -19A and -15A, -60V and -100V
- $r_{DS(ON)}$ = 0.20Ω and 0.30Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AA
BOTTOM VIEW



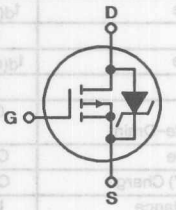
Description

The IRF9140, IRF9141, IRF9142 and IRF9143 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9140	IRF9141	IRF9142	IRF9143	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-19	-19	-15	-15	A
T_C = 100°C ..... I_D	-12	-12	-10	-10	A
Pulsed Drain Current (3) ..... I_{DM}	-76	-76	-60	-60	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	125	125	125	125	W
Linear Derating Factor ..... (See Figure 14)	1	1	1	1	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	960	960	960	960	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

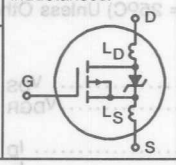
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 4mH, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

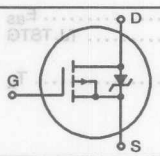
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File Number 2278

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9140, IRF9142	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	–	–	V
IRF9141, IRF9143			-60	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	–	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	-1000	μA
On-State Drain Current (Note 2) IRF9140, IRF9141	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-19	–	–	A
IRF9142, IRF9143			-15	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF9140, IRF9141	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	–	0.15	0.20	Ω
IRF9142, IRF9143			–	0.22	0.30	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -10A	5	7	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	–	1100	–	pF
Output Capacitance	C_{OSS}		–	550	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	250	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -19A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	–	16	20	ns
Rise Time	t_r		–	65	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	47	70	ns
Fall Time	t_f		–	28	90	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -19A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	70	90	nC
Gate-Source Charge	Q_{gs}		–	14	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	56	–	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances.	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad. 	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	-19	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	-76	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -19A, V_{GS} = 0V	–	–	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 19A, dI_F/dt = 100A/μs	–	170	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -19A, dI_F/dt = 100A/μs	–	0.8	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 4mH, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

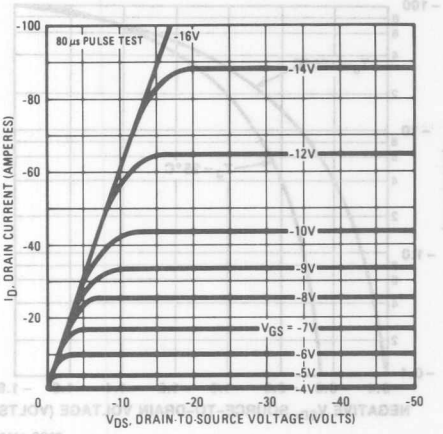


Fig. 1 - Typical output characteristics.

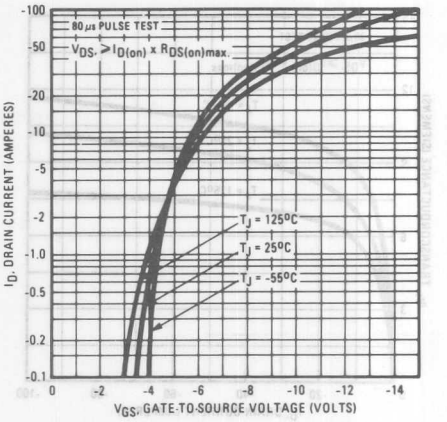


Fig. 2 - Typical transfer characteristics.

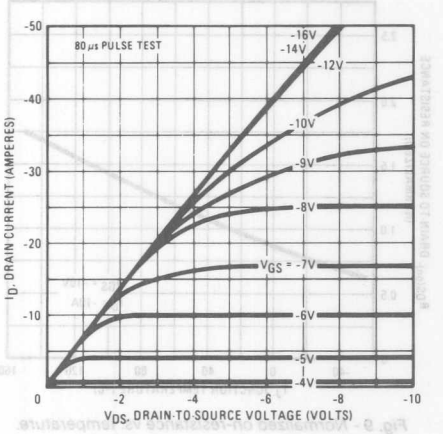


Fig. 3 - Typical saturation characteristics.

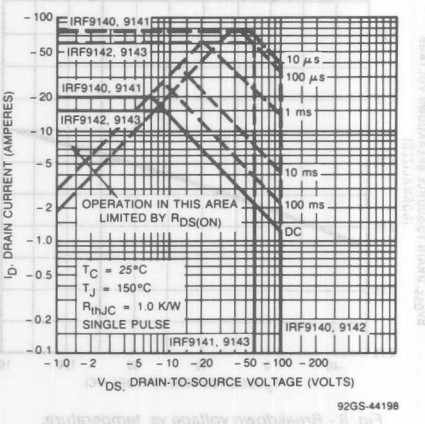


Fig. 4 - Maximum safe operating area.

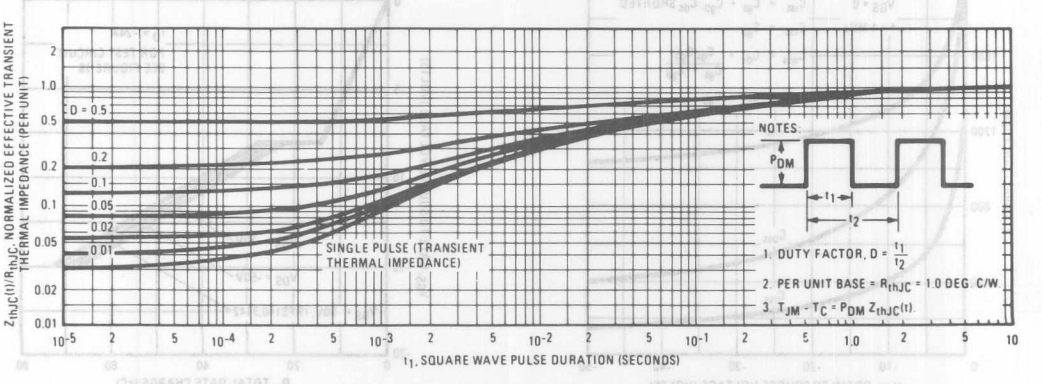


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

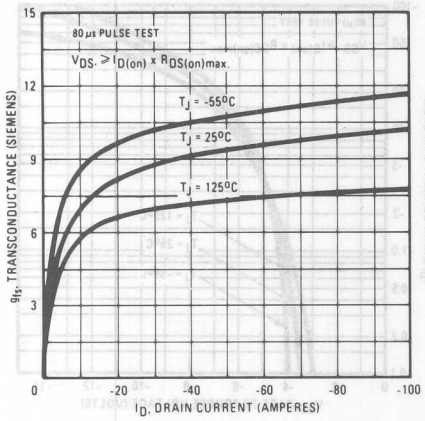


Fig. 6 - Typical transconductance vs. drain current.

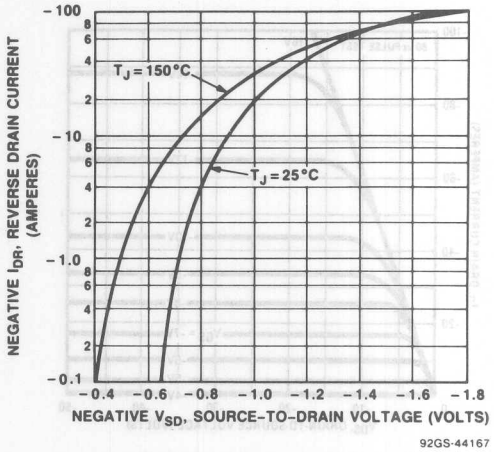


Fig. 7 - Typical source-drain diode forward voltage.

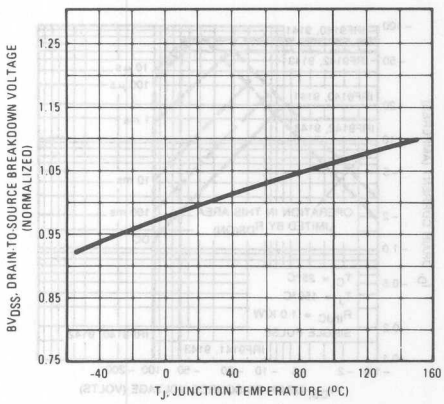


Fig. 8 - Breakdown voltage vs. temperature.

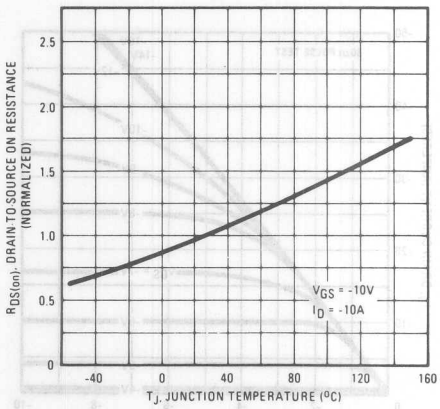


Fig. 9 - Normalized on-resistance vs. temperature.

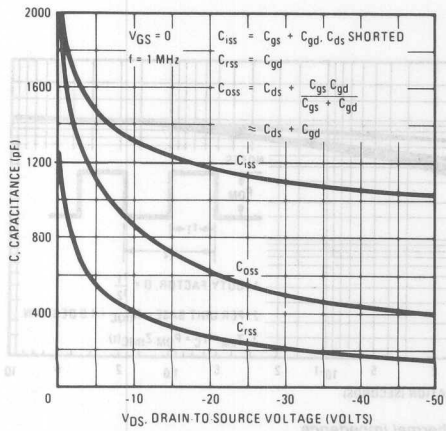


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

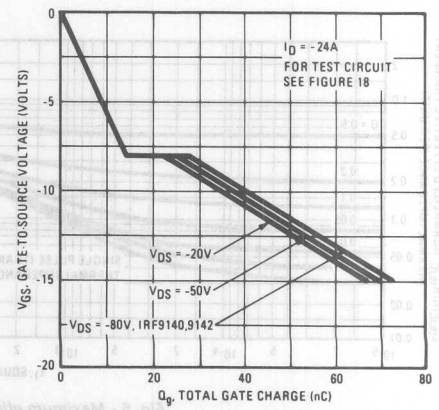


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

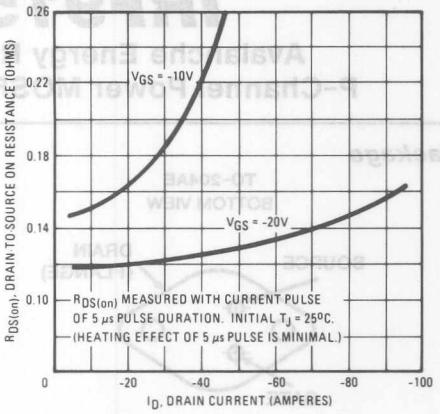


Fig. 12 - Typical on-resistance vs. drain current.

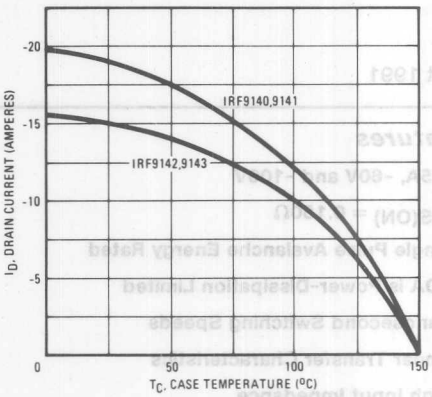


Fig. 13 - Maximum drain current vs. case temperature.

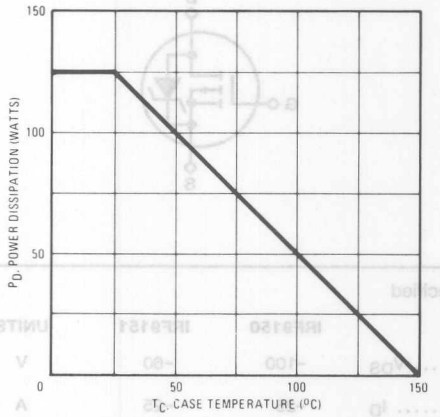


Fig. 14 - Power vs. temperature derating curve.

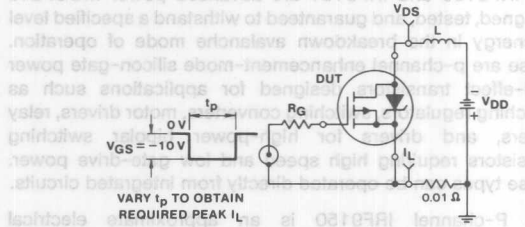


Fig. 15 - Unclamped inductive test circuit.

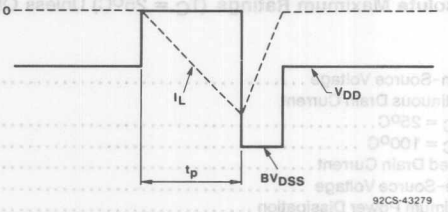


Fig. 16 - Unclamped inductive waveforms.

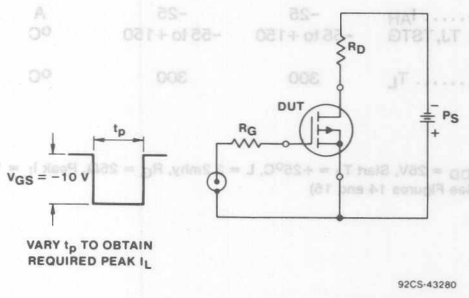


Fig. 17 - Switching time test circuit.

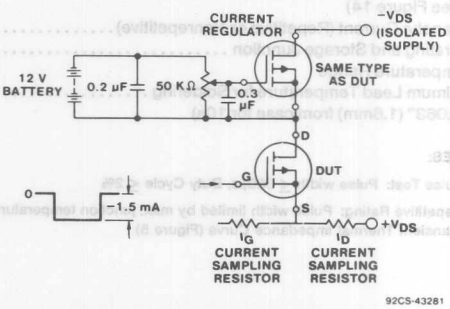


Fig. 18 - Gate charge test circuit.

Avalanche Energy Rated P-Channel Power MOSFETs

Features

- -25A, -60V and -100V
- $r_{DS(ON)}$ = 0.150Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

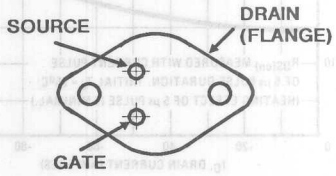
The IRF9150 and IRF9151 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The P-channel IRF9150 is an approximate electrical complement to the N-channel IRF9150.

The IRF types are supplied in the JEDEC TO-204AE metal package.

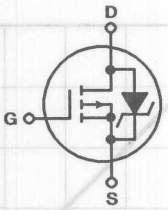
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRF9150	IRF9151	UNITS
Drain-Source Voltage	V_{DS}	-100	-60	V
Continuous Drain Current				
T_C = 25°C	I_D	-25	-25	A
T_C = 100°C	I_D	-18	-18	A
Pulsed Drain Current	I_{DM}	-100	-100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation (See Figure 18)	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (3) (See Figure 14)	E_{as}	1300	1300	mJ
Avalanche Current (Repetitive or Nonrepetitive)	I_{AR}	-25	-25	A
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 25V, Start T_J = +25°C, L = 3.2mhy, R_G = 25Ω, Peak I_L = 19A (See Figures 14 and 15)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2280

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9150	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9151			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 1)	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, V_{GS} = 10V	-25	-	-	A
Static Drain-Source On-State Resistance (Note 1)	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	-	0.09	0.15	Ω
Forward Transconductance (Note 1)	g_{ts}	V_{DS} = -10V, I_D = -12.5A	4	10	-	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	2400	-	pF
Output Capacitance	C_{OSS}		-	850	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	400	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = -50V, I_D = -25A, R_G = 6.8Ω, R_D = 2Ω. See Figures 16 and 17. (MOSFET switching times are essentially independent of operating temperature.)	-	16	24	ns
Rise Time	t_r		-	110	160	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	65	100	ns
Fall Time	t_f		-	46	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -25A, V_{DS} = 0.8 Max Rating. See Figures 11 & 19 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	82	120	nC
Gate-Source Charge	Q_{gs}		-	14	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	42	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-25	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-100	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = 25A, V_{GS} = 0V	-	0.9	1.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	-	150	300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	0.3	0.7	1.5	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 25V, Start T_J = +25°C, L = 3.2mhy, R_G = 25Ω, Peak I_L = 25A (See Figures 14 and 15)

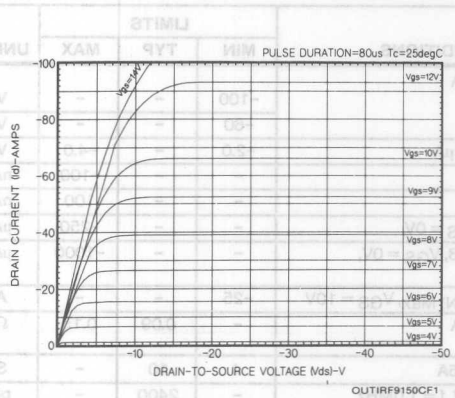


Fig. 1 - Typical output characteristics.

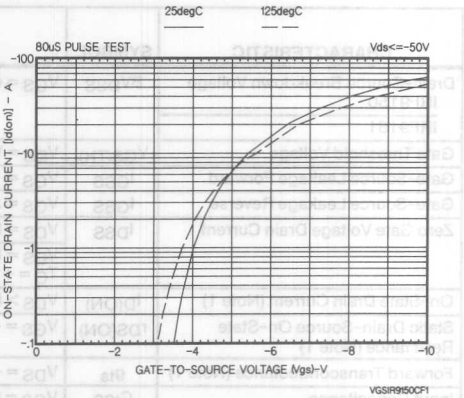


Fig. 2 - Typical transfer characteristics.

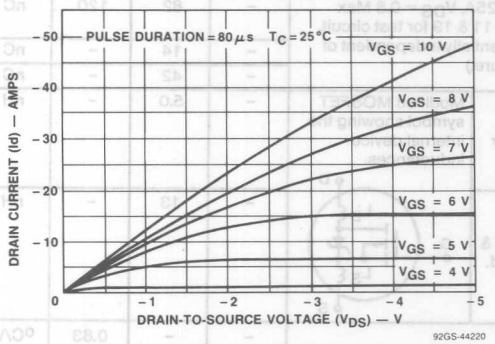


Fig. 3- Typical saturation characteristics.

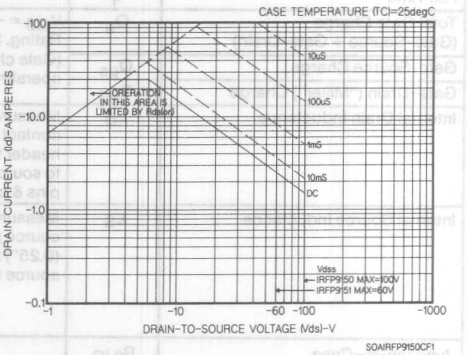


Fig. 4 - Maximum safe operating area.

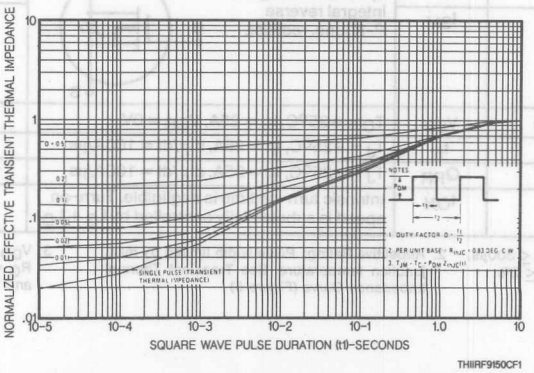


Fig. 5 - Maximum effective transient thermal impedance.

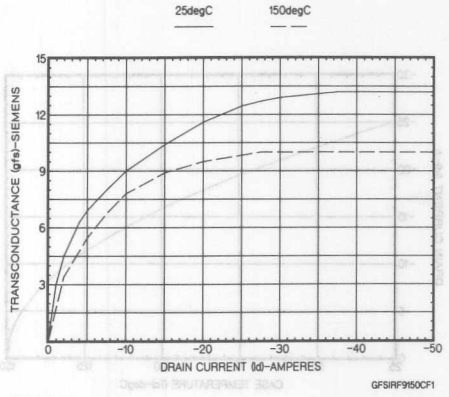


Fig. 6 - Typical transconductance vs. drain current.

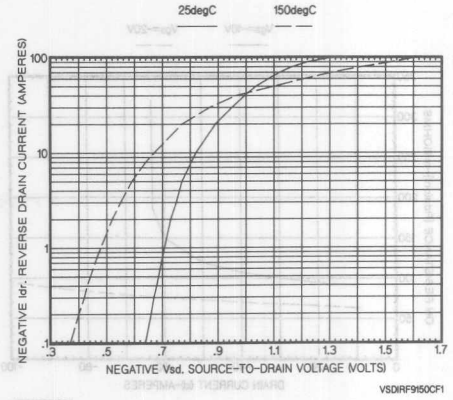


Fig. 7 - Typical source-drain diode forward voltage.

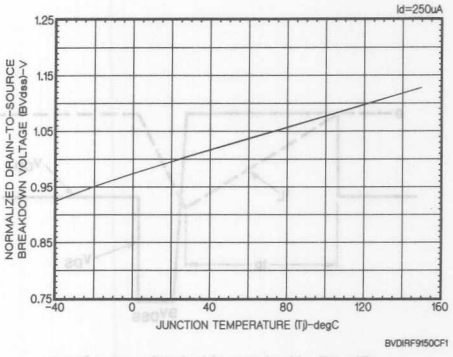


Fig. 8 - Normalized breakdown voltage vs. temperature.

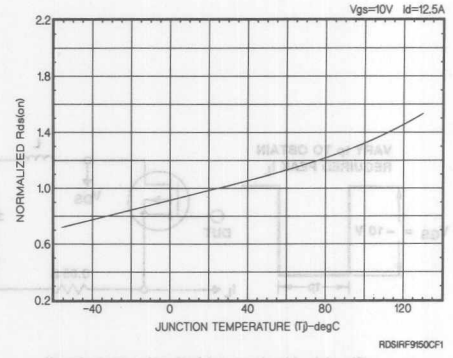


Fig. 9 - Normalized on-resistance vs. temperature.

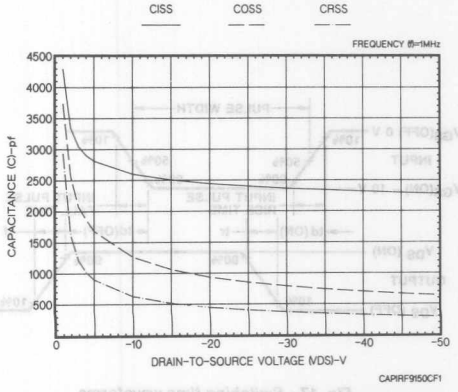


Fig. 10 - Typical capacitance vs. drain-to source voltage.

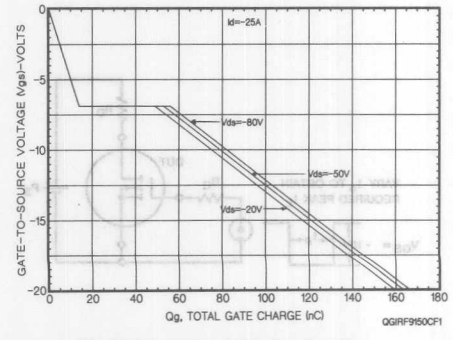


Fig. 11 - Typical gate charge vs. gate-to source voltage.

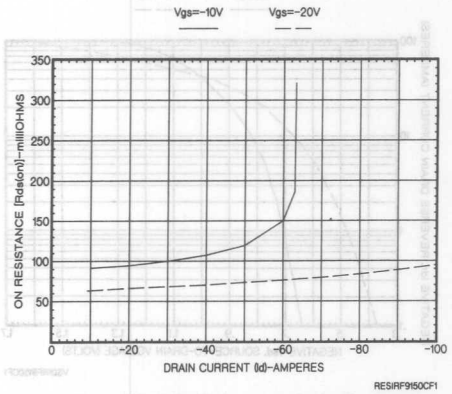


Fig. 12 - Typical on-resistance vs. drain current.

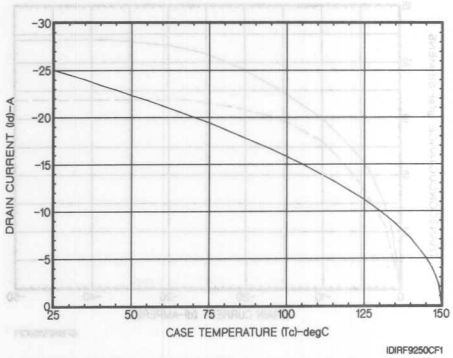


Fig. 13 - Maximum drain current vs. case temperature.

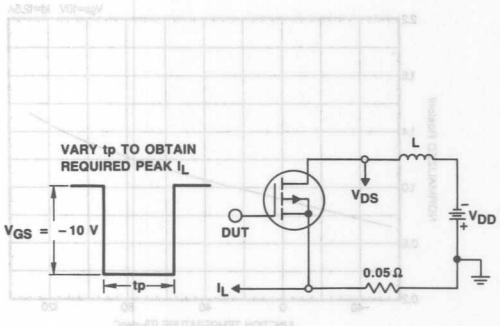


Fig. 14 - Unclamped inductive test circuit.

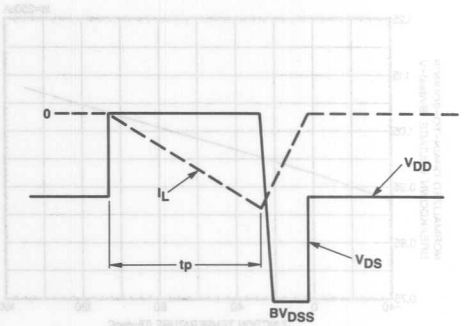


Fig. 15 - Unclamped inductive waveforms.

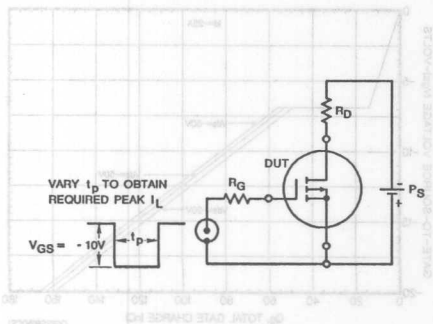


Fig. 16 - Switching time test circuit.

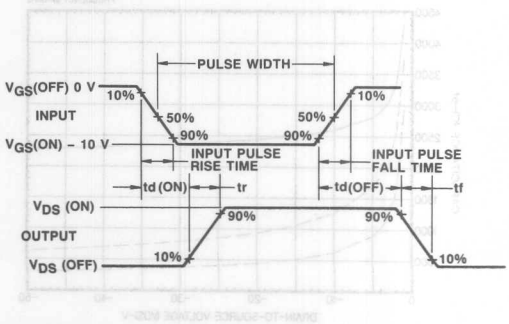


Fig. 17 - Switching time waveforms.

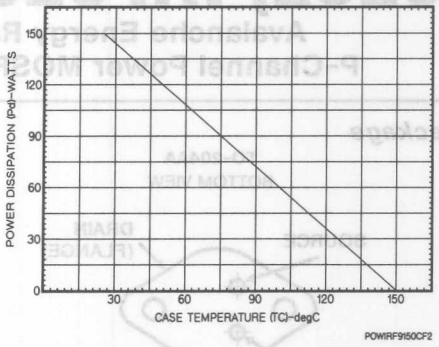


Fig. 18 - Power vs. temperature derating curve.

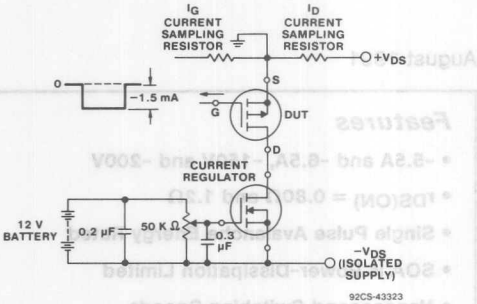


Fig. 19 - Gate charge test circuit.

HARRIS

IRF9230, IRF9231 IRF9232, IRF9233

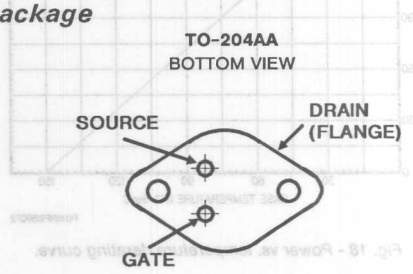
Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -5.5A and -6.5A, -150V and -200V
- $r_{DS(ON)}$ = 0.80Ω and 1.2Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package



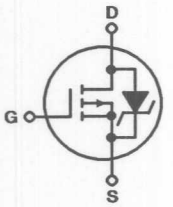
Description

The IRF9230, IRF9231, IRF9232 and IRF9233 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9230	IRF9231	IRF9232	IRF9233	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-6.5	-6.5	-5.5	-5.5	A
T_C = 100°C ..... I_D	-4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current (3) ..... I_{DM}	-26	-26	-22	-22	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	75	75	75	75	W
Linear Derating Factor ..... (See Figure 14)	0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	500	500	500	500	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 17.75mH, R_G = 25Ω, Peak I_L = 6.5A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2226

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9230, IRF9232	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRF9231, IRF9233			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9230, IRF9231	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-6.5	-	-	A
IRF9232, IRF9233			-5.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9230, IRF9231	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -3.5A	-	0.5	0.8	Ω
IRF9232, IRF9233			-	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -3.5A	2.2	3.5	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	550	-	pF
Output Capacitance	C_{OSS}		-	170	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -6.5A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	40	80	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -6.5A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	31	45	nC
Gate-Source Charge	Q_{gs}		-	18	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	13	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-6.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-26	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -6.5A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -6.5A, dI_F/dt = 100A/μs	-	400	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -6.5A, dI_F/dt = 100A/μs	-	2.6	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 17.75mH, R_G = 25Ω, Peak I_L = 6.5A (See Figures 15 and 16)

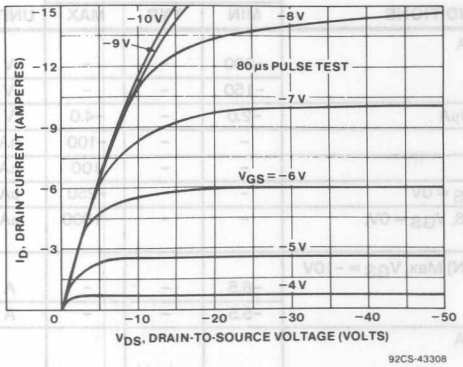


Fig. 1 - Typical output characteristics.

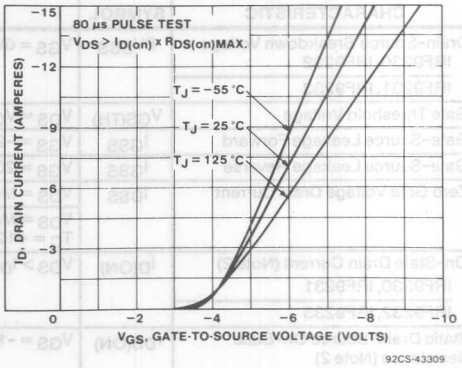


Fig. 2 - Typical transfer characteristics.

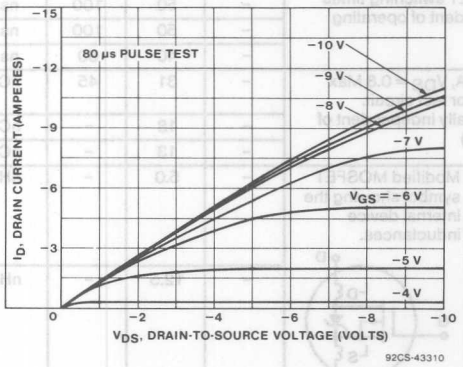


Fig. 3 - Typical saturation characteristics.

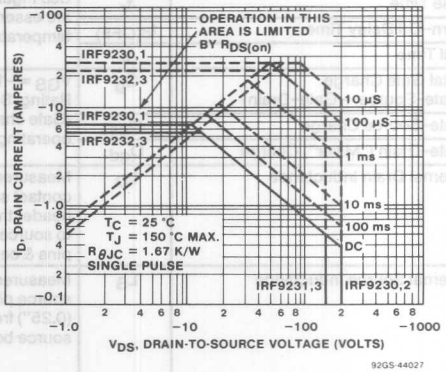


Fig. 4 - Maximum safe operating area.

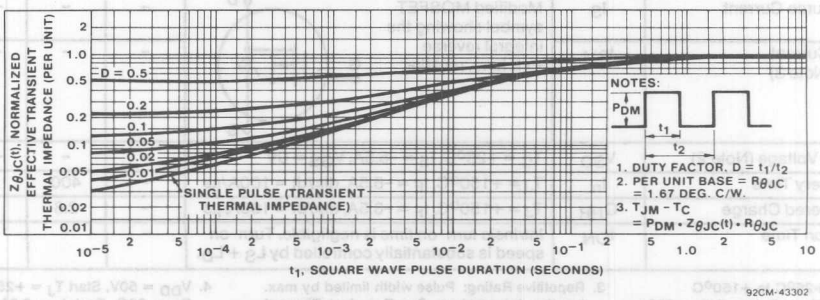


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

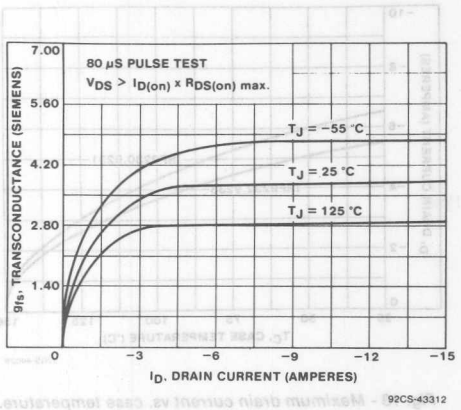


Fig. 6 - Typical transconductance vs. drain current.

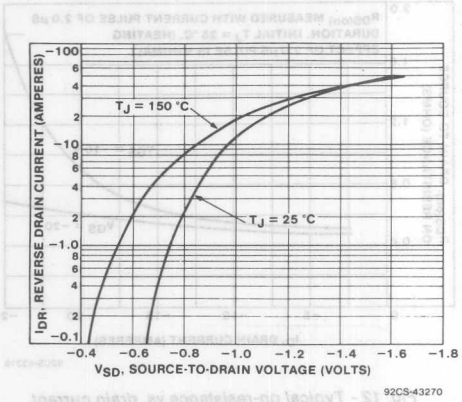


Fig. 7 - Typical source-drain diode forward voltage.

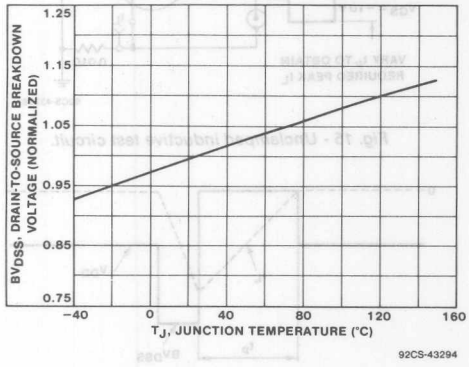


Fig. 8 - Breakdown voltage vs. temperature.

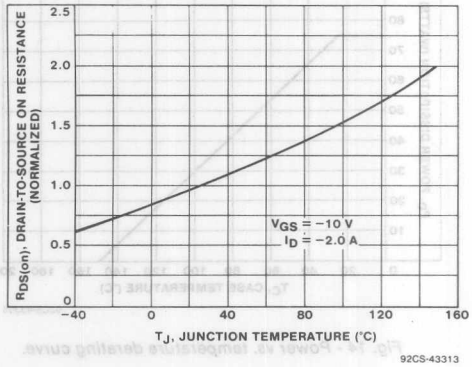


Fig. 9 - Normalized on-resistance vs. temperature.

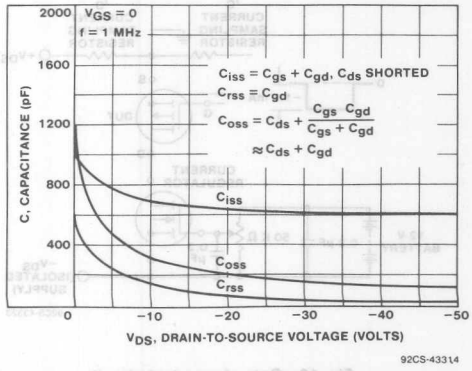


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

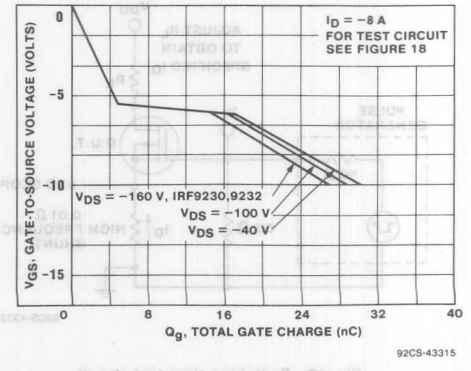


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

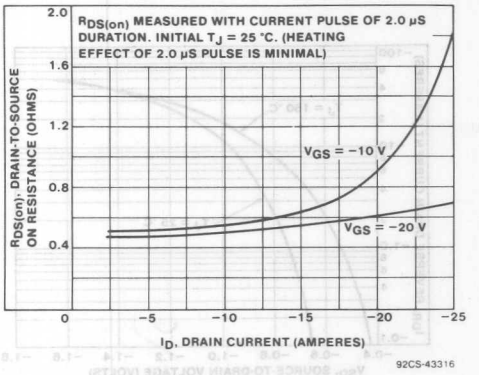


Fig. 12 - Typical on-resistance vs. drain current.

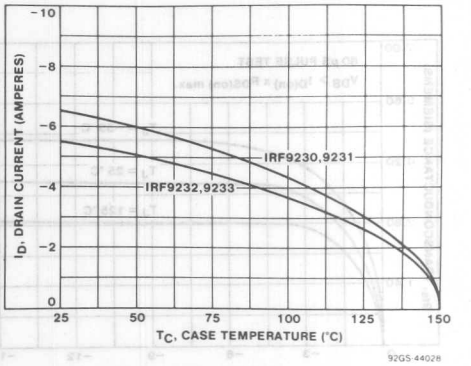


Fig. 13 - Maximum drain current vs. case temperature.

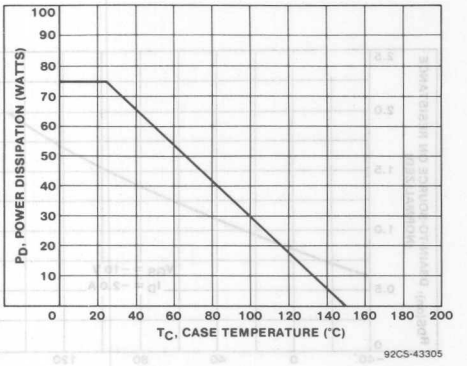


Fig. 14 - Power vs. temperature derating curve.

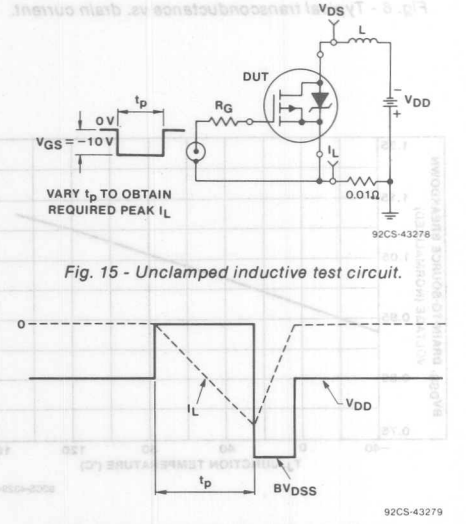


Fig. 15 - Unclamped inductive test circuit.

Fig. 16 - Unclamped inductive waveforms.

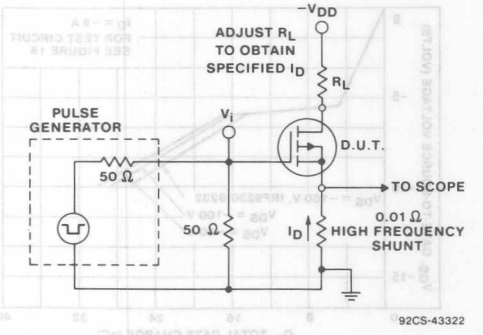


Fig. 17 - Switching time test circuit.

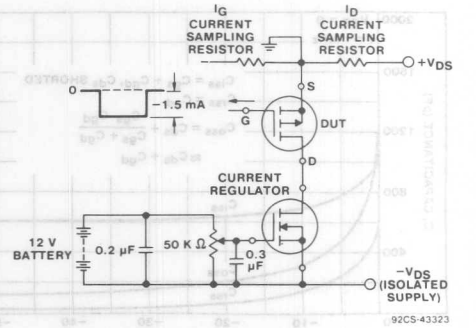


Fig. 18 - Gate charge test circuit.

HARRIS IRF9240, IRF9241 IRF9242, IRF9243

Avalanche Energy Rated P-Channel Power MOSFETs

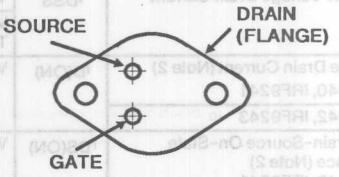
August 1991

Features

- -9A and -11A, -150V and -200V
- $r_{DS(ON)}$ = 0.50Ω and 0.7Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-204AA
BOTTOM VIEW



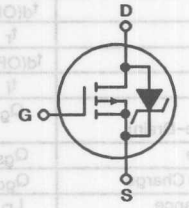
Description

The IRF9240, IRF9241, IRF9242 and IRF9243 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9240	IRF9241	IRF9242	IRF9243	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-11	-11	-9	-9	A
T_C = 100°C ..... I_D	-7	-7	-6	-6	A
Pulsed Drain Current (3) ..... I_{DM}	-44	-44	-36	-36	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	125	125	125	125	W
Linear Derating Factor ..... (See Figure 14)	1	1	1	1	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	790	790	790	790	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

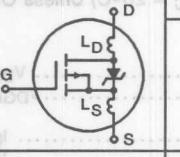
NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 9.8mH, R_G = 25Ω, Peak I_L = 11A (See Figures 15 and 16)

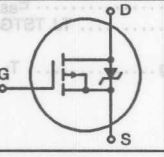
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
Copyright © Harris Corporation 1991

File Number 2279

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9240, IRF9242	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRF9241, IRF9243			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9240, IRF9241	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-11	-	-	A
IRF9242, IRF9243			-9	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9240, IRF9241	$r_{DS(ON)}$	V_{GS} = 10V, I_D = -6A	-	0.35	0.5	Ω
IRF9242, IRF9243			-	0.55	0.7	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -6A	4	6	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	1100	-	pF
Output Capacitance	C_{OSS}		-	375	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	150	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =100 BV_{DSS}, I_D = -11A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	18	22	ns
Rise Time	t_r		-	45	68	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	75	90	ns
Fall Time	t_f		-	29	44	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -11A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	70	90	nC
Gate-Source Charge	Q_{gs}		-	55	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	15	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-11	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-44	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -11A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -11A, dI_F/dt = 100A/μs	-	270	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -11A, dI_F/dt = 100A/μs	-	2	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 9.8mH, R_G = 25Ω, Peak I_L = 11A (See Figures 15 and 16)

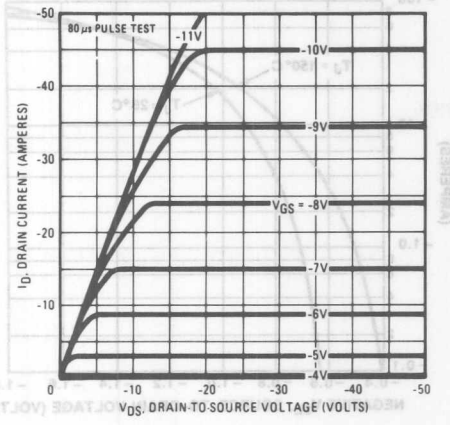


Fig. 1 - Typical output characteristics.

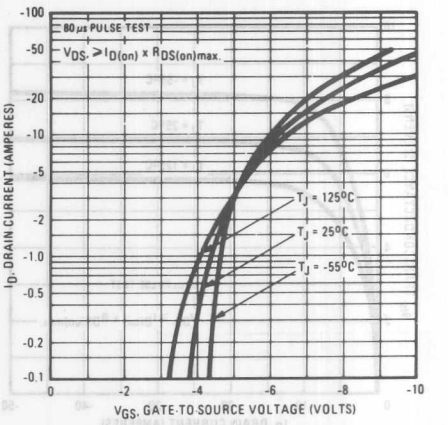


Fig. 2 - Typical transfer characteristics.

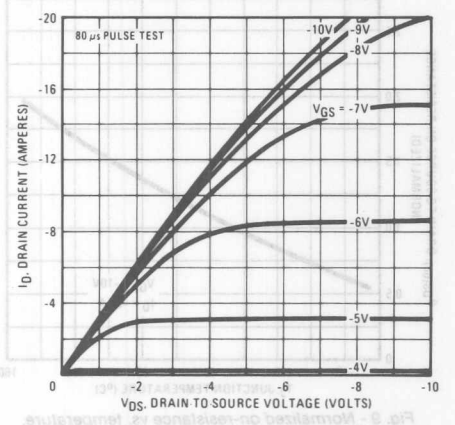


Fig. 3 - Typical saturation characteristics.

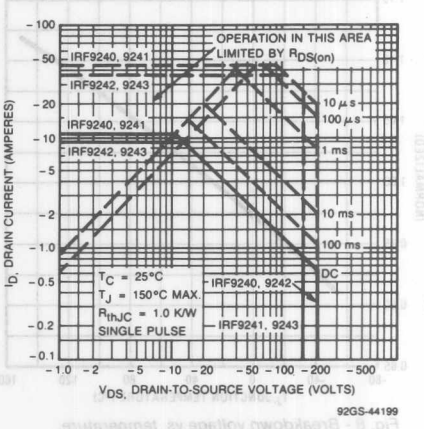


Fig. 4 - Maximum safe operating area.

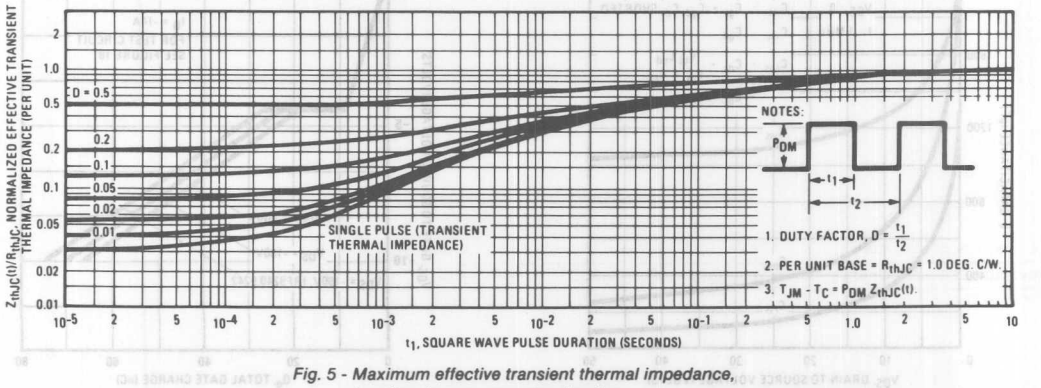


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

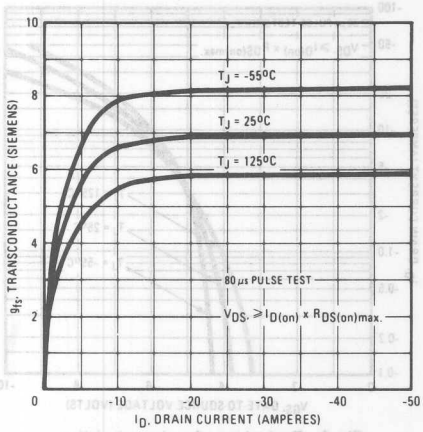


Fig. 6 - Typical transconductance vs. drain current.

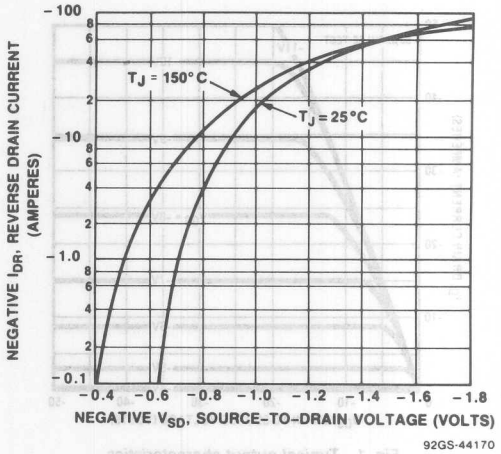


Fig. 7 - Typical source-drain diode forward voltage.

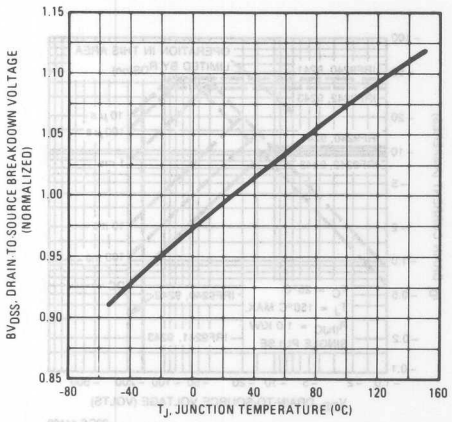


Fig. 8 - Breakdown voltage vs. temperature.

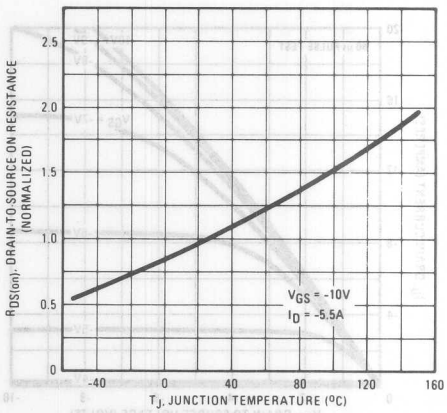


Fig. 9 - Normalized on-resistance vs. temperature.

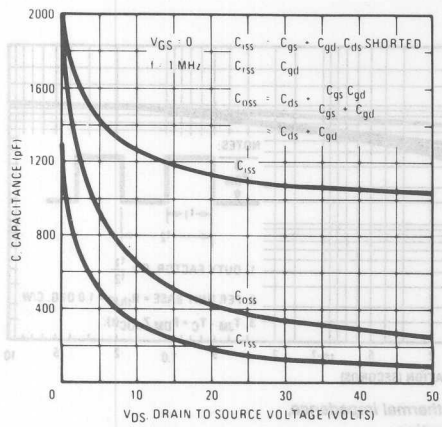


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

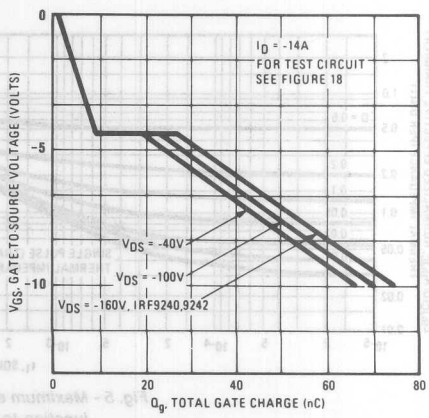


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

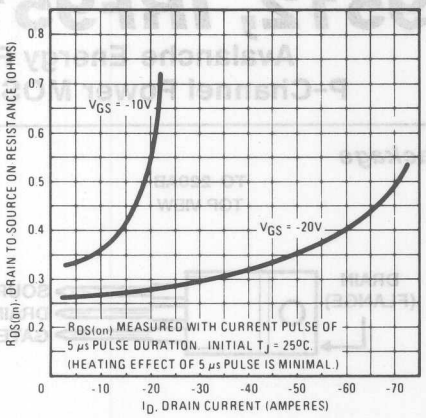


Fig. 12 - Typical on-resistance vs. drain current.

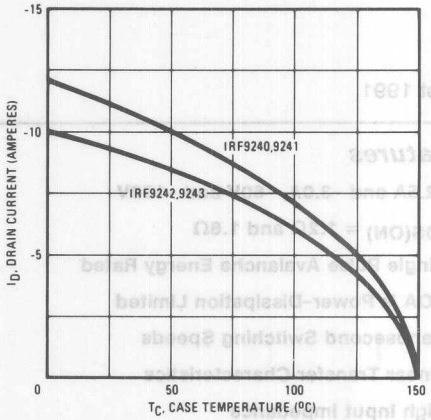


Fig. 13 - Maximum drain current vs. case temperature.

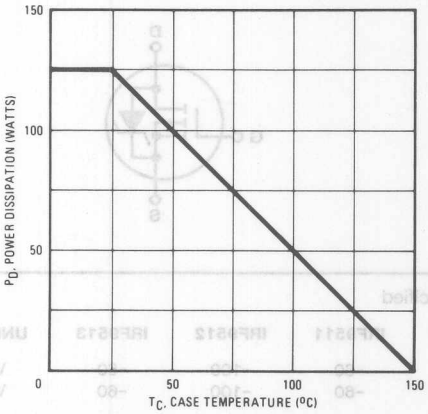


Fig. 14 - Power vs. temperature derating curve.

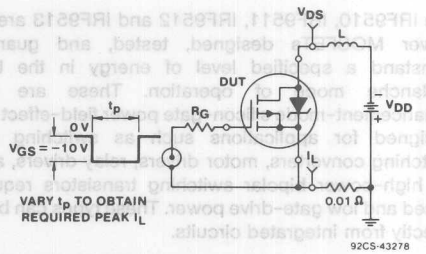


Fig. 15 - Unclamped inductive test circuit.

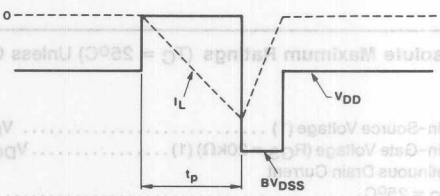


Fig. 16 - Unclamped inductive waveforms.

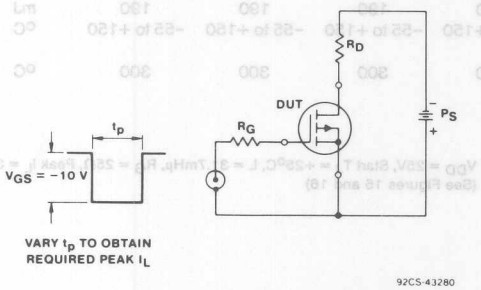


Fig. 17 - Switching time test circuit.

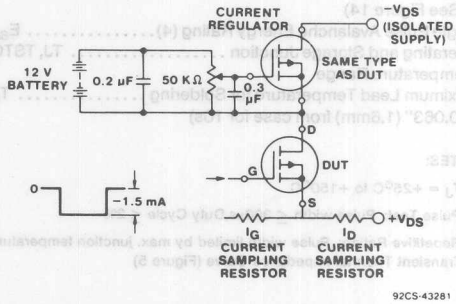


Fig. 18 - Gate charge test circuit.

HARRIS

IRF9510, IRF9511 IRF9512, IRF9513

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -2.5A and -3.0A, -60V and -100V
- $r_{DS(ON)}$ = 1.2Ω and 1.6Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

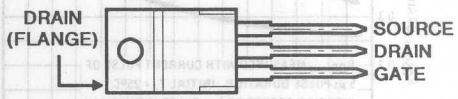
Description

The IRF9510, IRF9511, IRF9512 and IRF9513 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9510	IRF9511	IRF9512	IRF9513	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-3.0	-3.0	-2.5	-2.5	A
T_C = 100°C ..... I_D	-2.0	-2.0	-1.5	-1.5	A
Pulsed Drain Current (3) ..... I_{DM}	-12	-12	-10	-10	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	20	20	20	20	W
Linear Derating Factor ..... (See Figure 14)	0.16	0.16	0.16	0.16	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	190	190	190	190	mJ
Operating and Storage Junction ..... TJ, TSTG Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 31.7mHμ, R_G = 25Ω, Peak I_L = 3.0A (See Figures 15 and 16)

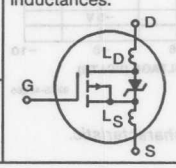
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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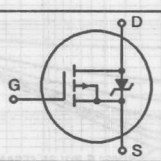
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9510, IRF9512	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9511, IRF9513			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9510, IRF9511	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-3.0	-	-	A
IRF9512, IRF9513			-2.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9510, IRF9511	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -1.5A	-	1.0	1.2	Ω
IRF9512, IRF9513			-	1.2	1.6	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, I_D = -1.5A	0.8	1.1	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	180	-	pF
Output Capacitance	C_{OSS}		-	85	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =-50 BV_{DSS}, I_D = -3.0A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	15	30	ns
Rise Time	t_r		-	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	20	40	ns
Fall Time	t_f		-	20	40	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -3A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	8.5	11	nC
Gate-Source Charge	Q_{gs}		-	3.8	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	4.7	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	6.4	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-3.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-12	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -3.0A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -3.0A, dI_F/dt = 100A/μs	-	120	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -3.0A, dI_F/dt = 100A/μs	-	6.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 31.7mH, R_G = 25Ω, Peak I_L = 3.0A (See Figures 15 and 16)

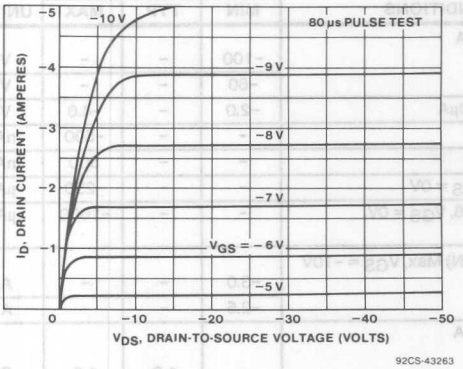


Fig. 1 - Typical Output Characteristics

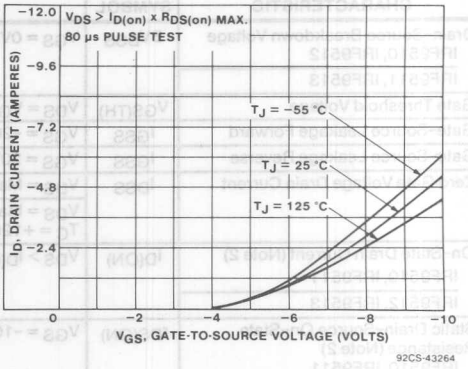


Fig. 2 - Typical Transfer Characteristics

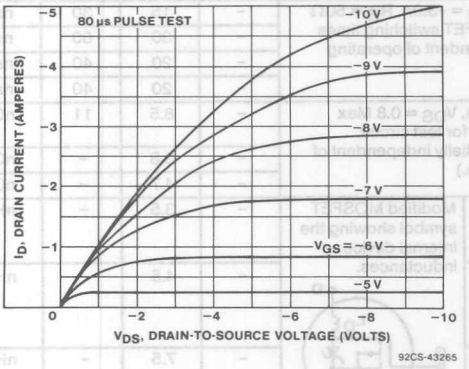


Fig. 3 - Typical saturation characteristic.

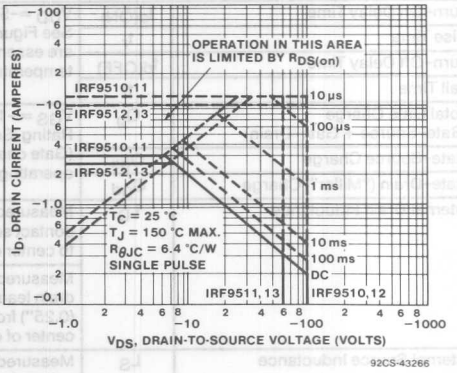


Fig. 4 - Maximum safe operating area.

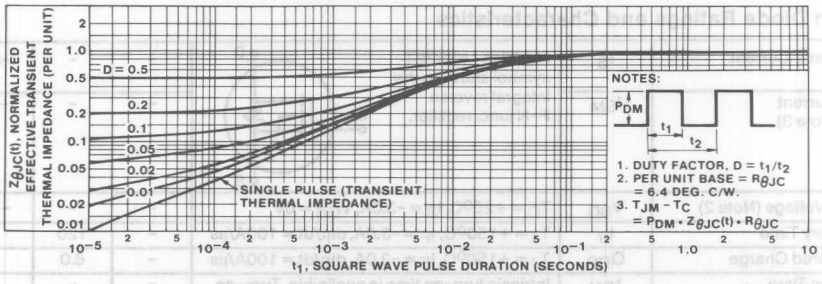


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

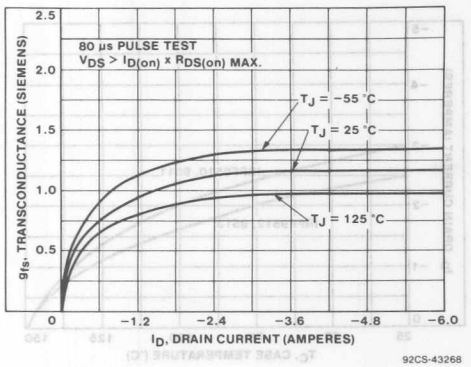


Fig. 6 - Typical transconductance vs. drain current.

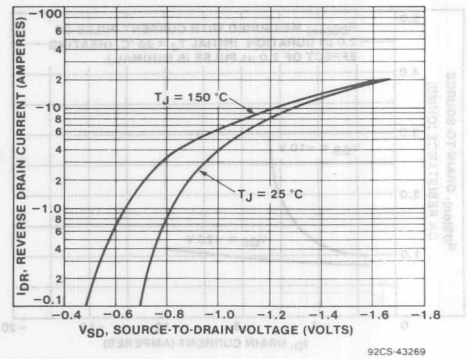


Fig. 7 - Typical source-drain diode forward voltage.

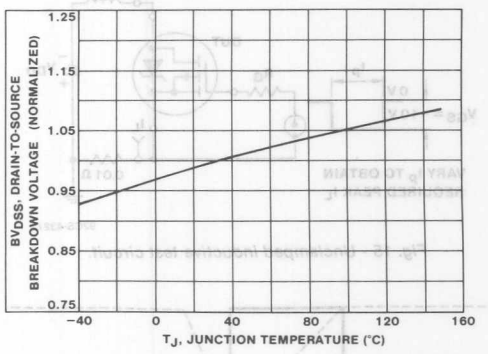


Fig. 8 - Breakdown voltage vs. temperature.

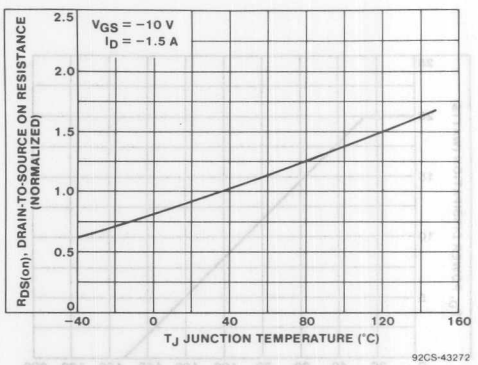


Fig. 9 - Normalized on-resistance vs. temperature.

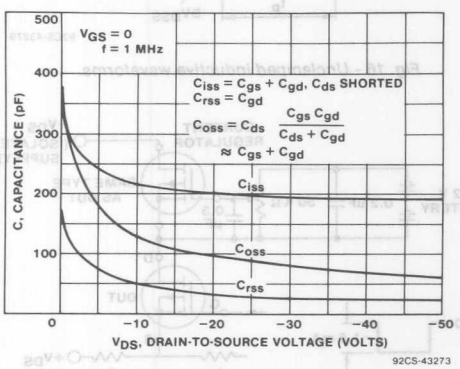


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

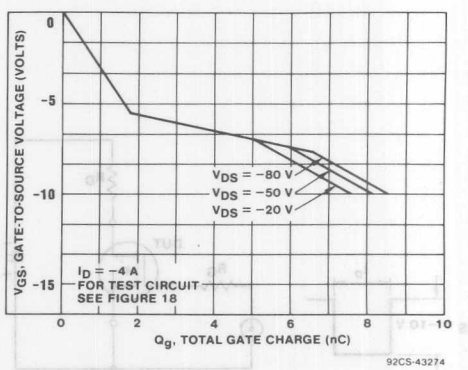


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

5 P-CHANNEL POWER MOSFETs

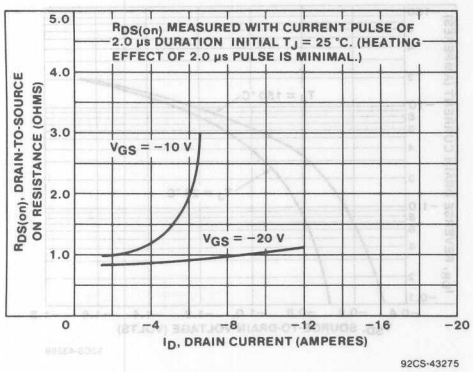


Fig. 12 - Typical on-resistance vs. drain current.

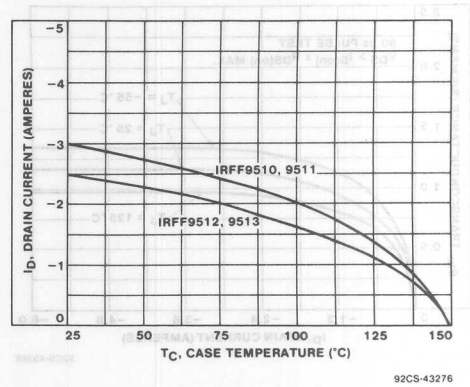


Fig. 13 - Maximum drain current vs. case temperature.

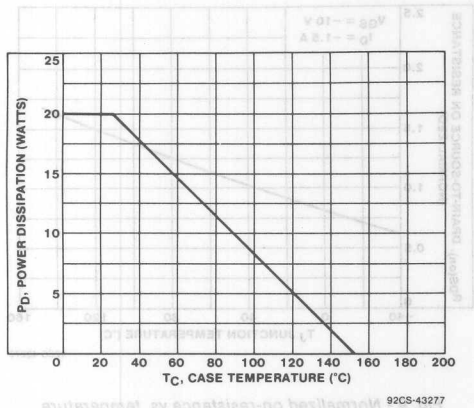


Fig. 14 - Power vs. temperature derating curve.

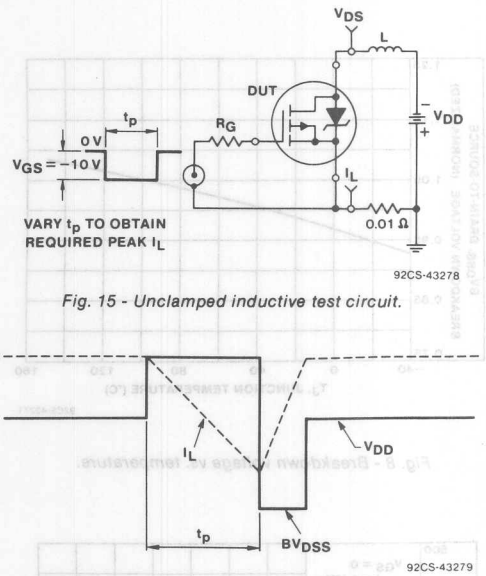


Fig. 15 - Unclamped inductive test circuit.

Fig. 16 - Unclamped inductive waveforms.

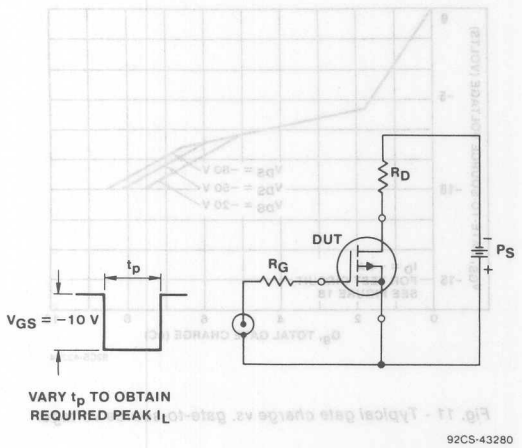


Fig. 17 - Switching time test circuit.

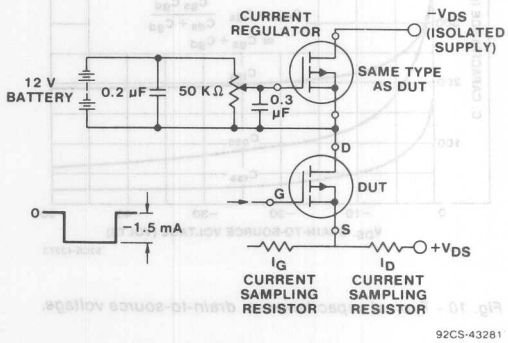


Fig. 18 - Gate charge test circuit.

HARRIS IRF9520, IRF9521 IRF9522, IRF9523

Avalanche Energy Rated P-Channel Power MOSFETs

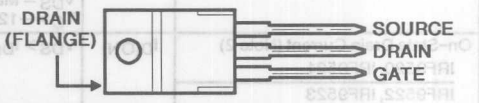
August 1991

Features

- -5A and -6A, -60V and -100V
- $r_{DS(ON)}$ = 0.6Ω and 0.8Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-220AB
TOP VIEW



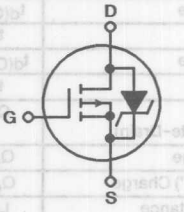
Description

The IRF9520, IRF9521, IRF9522 and IRF9523 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9520	IRF9521	IRF9522	IRF9523	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-6	-6	-5	-5	A
T_C = 100°C ..... I_D	-4	-4	-3.5	-3.5	A
Pulsed Drain Current (3) ..... I_{DM}	-24	-24	-20	-20	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	40	40	40	40	W
Linear Derating Factor ..... (See Figure 14)	0.32	0.32	0.32	0.32	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	370	370	370	370	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 15.4mHμ, R_G = 25Ω, Peak I_L = 6.0A (See Figures 15 and 16)

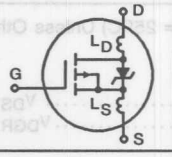
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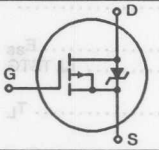
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9520, IRF9522	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9521, IRF9523			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9520, IRF9521	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-6	-	-	A
IRF9522, IRF9523			-5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9520, IRF9521	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -3.5A	-	0.5	0.6	Ω
IRF9522, IRF9523			-	0.6	0.8	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -3.5A	0.9	2	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	300	-	pF
Output Capacitance	C_{OSS}		-	200	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -6.0A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	25	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	50	100	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -6A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	22	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	3.12	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-6.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-24	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -6.0A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -6.0A, dI_F/dt = 100A/μs	-	230	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -6.0A, dI_F/dt = 100A/μs	-	1.3	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 15.4mH, R_G = 25Ω, Peak I_L = 6.0A (See Figures 15 and 16)

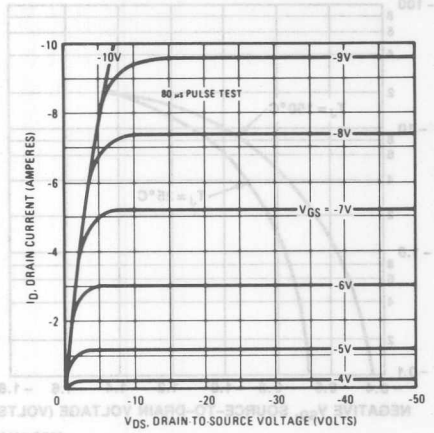


Fig. 1 - Typical output characteristics.

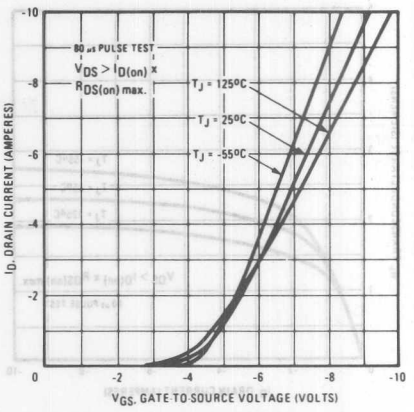


Fig. 2 - Typical transfer characteristics.

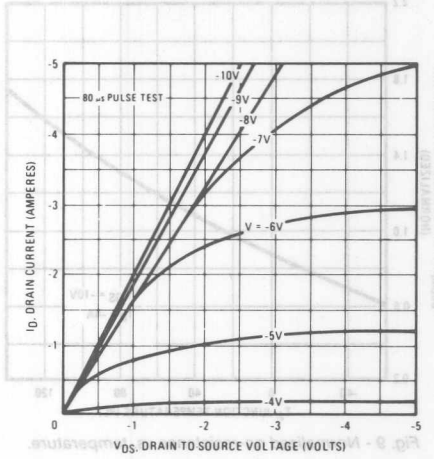


Fig. 3 - Typical saturation characteristics.

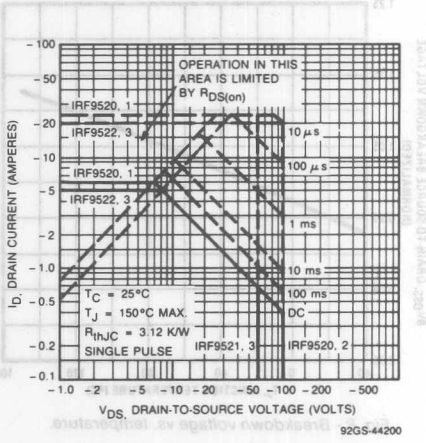


Fig. 4 - Maximum safe operating area.

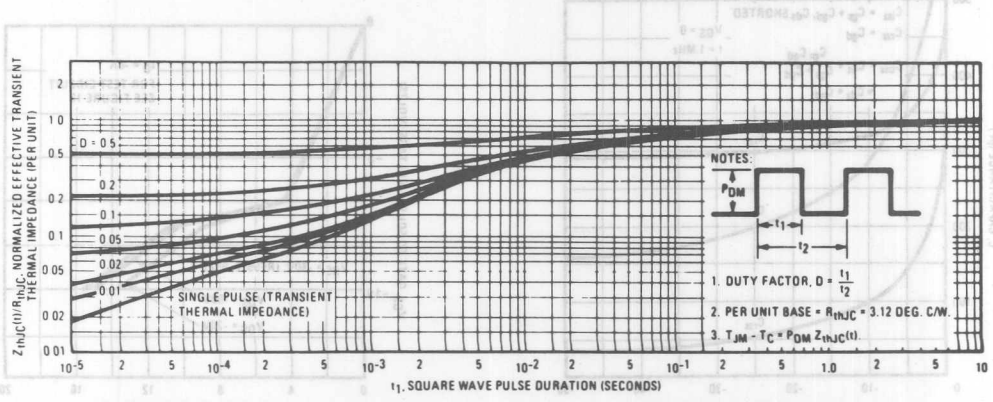


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

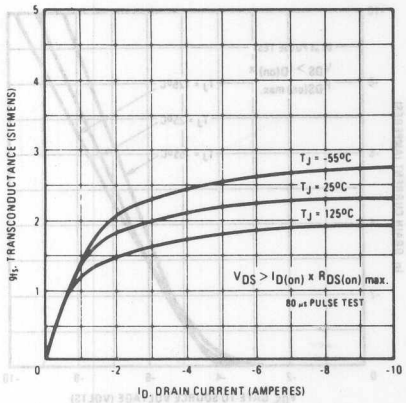


Fig. 6 - Typical transconductance vs. drain current.

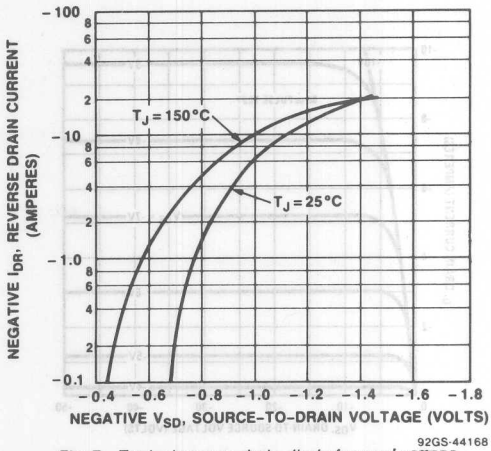


Fig. 7 - Typical source-drain diode forward voltage.

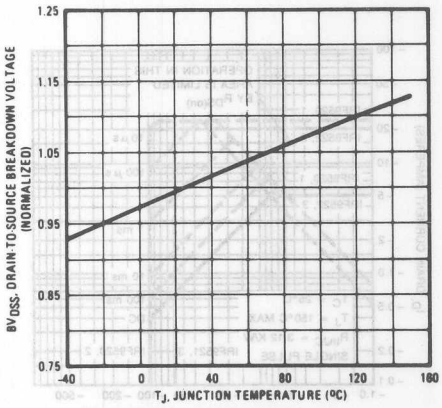


Fig. 8 - Breakdown voltage vs. temperature.

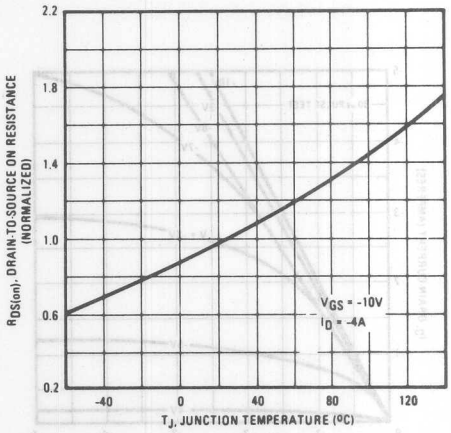


Fig. 9 - Normalized on-resistance vs. temperature.

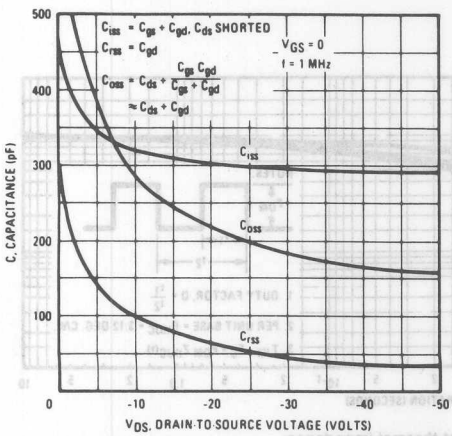


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

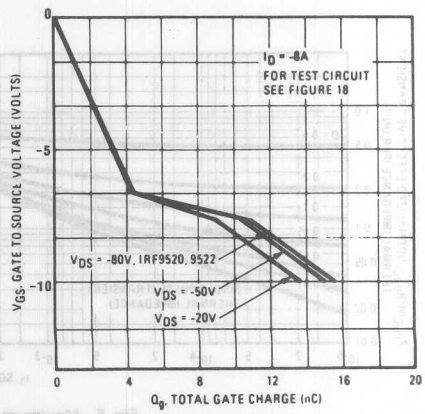


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

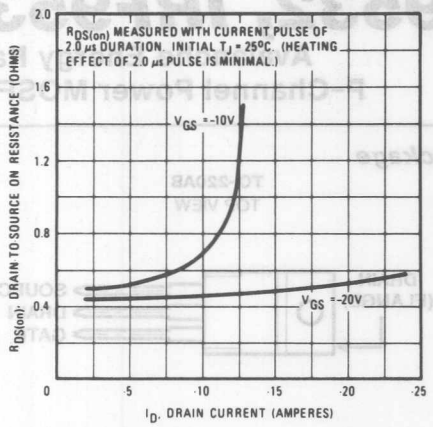


Fig. 12 - Typical on-resistance vs. drain current.

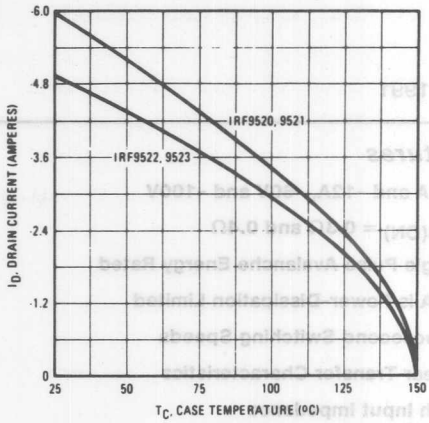


Fig. 13 - Maximum drain current vs. case temperature.

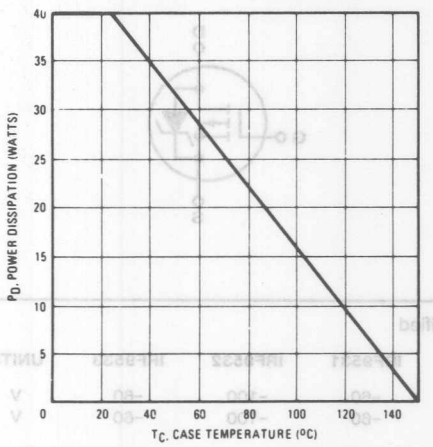


Fig. 14 - Power vs. temperature derating curve.

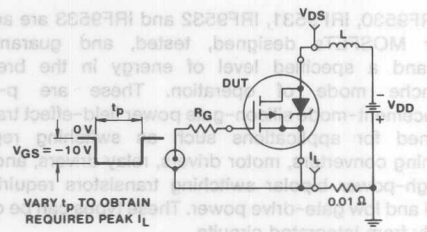


Fig. 15 - Unclamped inductive test circuit.

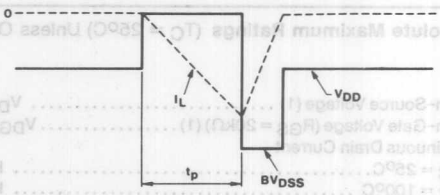


Fig. 16 - Unclamped inductive waveforms.

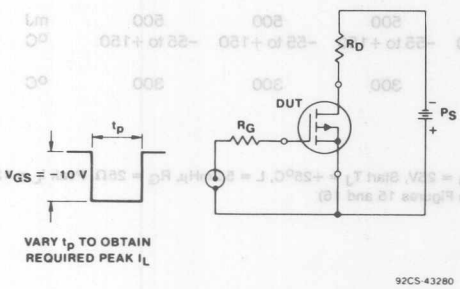


Fig. 17 - Switching time test circuit.

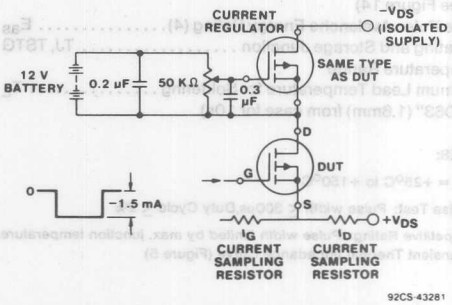


Fig. 18 - Gate charge test circuit.

HARRIS IRF9530, IRF9531 IRF9532, IRF9533

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -10A and -12A, -60V and -100V
- $r_{DS(ON)}$ = 0.3Ω and 0.4Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

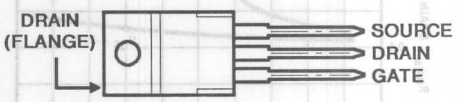
Description

The IRF9530, IRF9531, IRF9532 and IRF9533 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9530	IRF9531	IRF9532	IRF9533	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-12	-12	-10	-10	A
T_C = 100°C ..... I_D	-7.5	-7.5	-6.5	-6.5	A
Pulsed Drain Current (3) ..... I_{DM}	-48	-48	-40	-40	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	75	75	75	75	W
Linear Derating Factor ..... (See Figure 14)	0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	500	500	500	500	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 5.2mHμ, R_G = 25Ω, Peak I_L = 12A (See Figures 15 and 16)

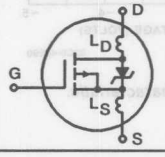
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2221

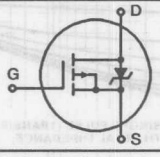
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9530, IRF9532	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9531, IRF9533			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9530, IRF9531	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-12	-	-	A
IRF9532, IRF9533			-10	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9530, IRF9531	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -6.5A	-	0.25	0.3	Ω
IRF9532, IRF9533			-	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 6.5A	2.0	3.8	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	500	-	pF
Output Capacitance	C_{OSS}		-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -12A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	60	ns
Rise Time	t_r		-	70	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	140	ns
Fall Time	t_f		-	70	140	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -12A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	25	45	nC
Gate-Source Charge	Q_{gs}		-	13	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-12	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-48	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -12A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -12A, dI_F/dt = 100A/μs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -12A, dI_F/dt = 100A/μs	-	1.8	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 5.2mH, R_G = 25Ω, Peak I_L = 12A (See Figures 15 and 16)

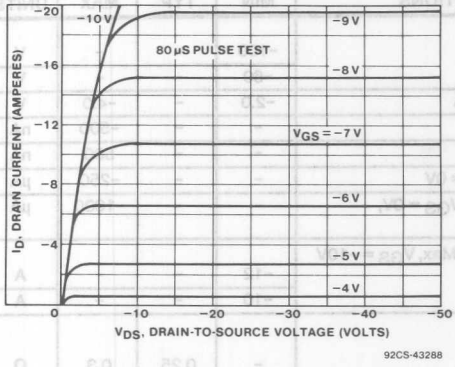


Fig. 1 - Typical Output Characteristics

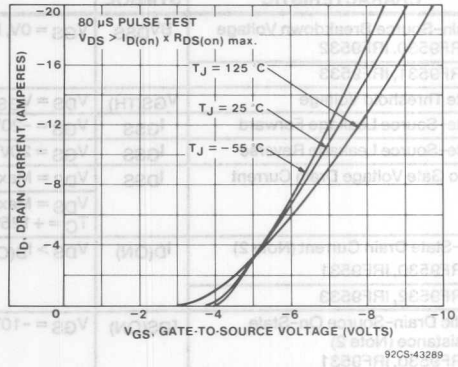


Fig. 2 - Typical Transfer Characteristics

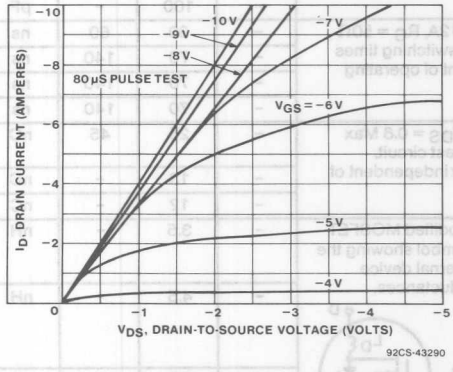


Fig. 3 - Typical saturation characteristic.

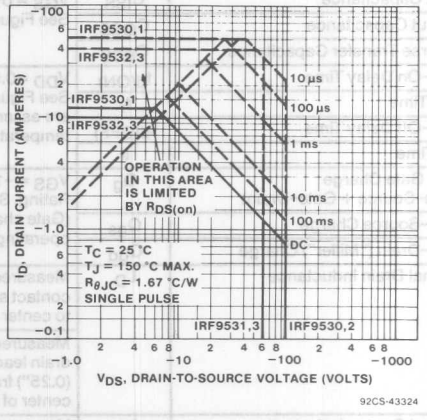


Fig. 4 - Maximum safe operating area.

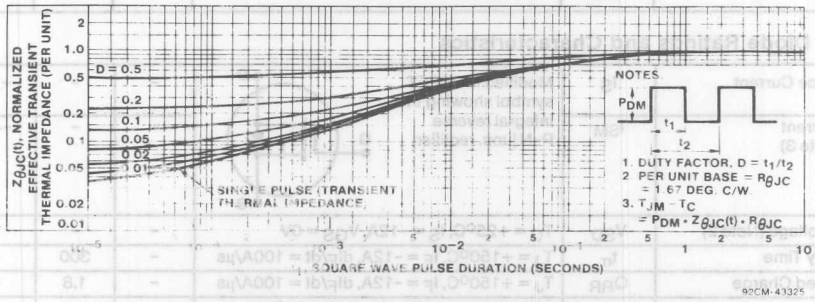


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

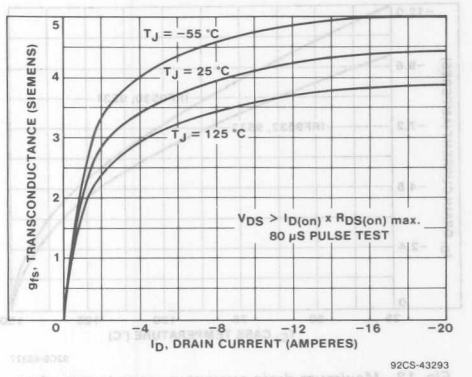


Fig. 6 - Typical transconductance vs. drain current.

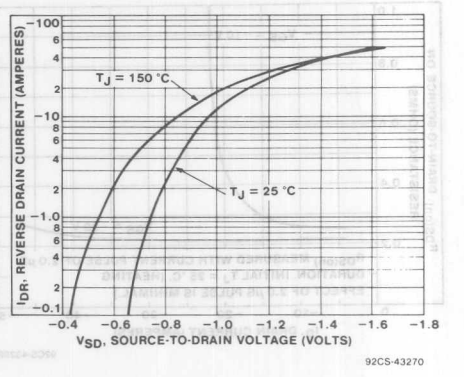


Fig. 7 - Typical source-drain diode forward voltage.

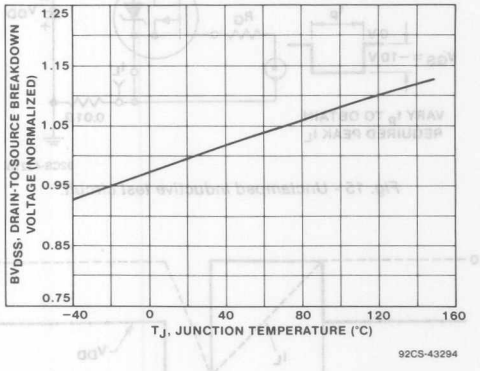


Fig. 8 - Breakdown voltage vs. temperature.

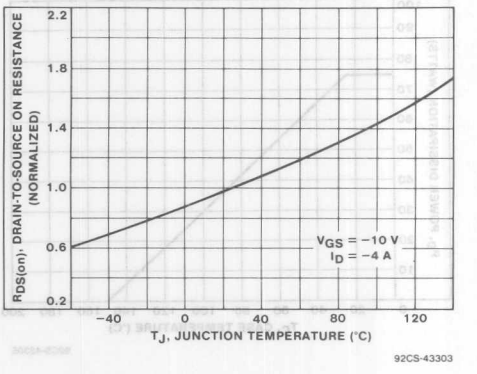


Fig. 9 - Normalized on-resistance vs. temperature.

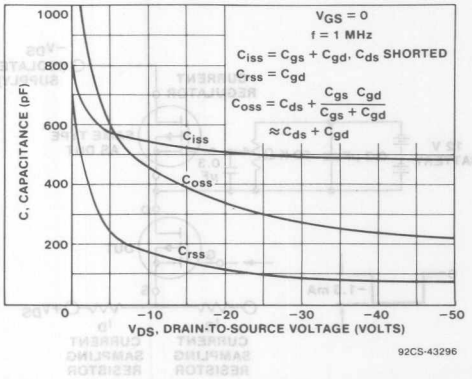


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

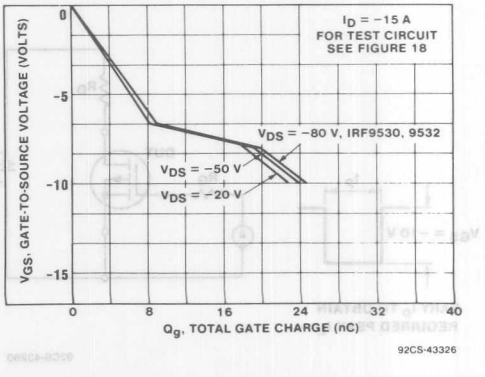


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

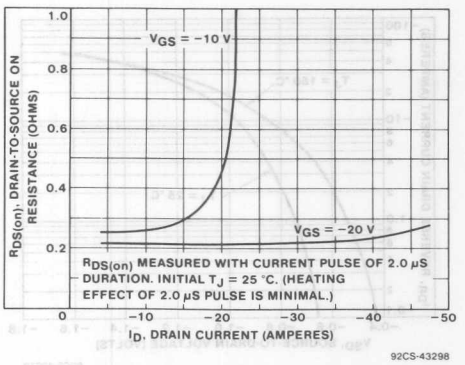


Fig. 12 - Typical on-resistance vs. drain current.

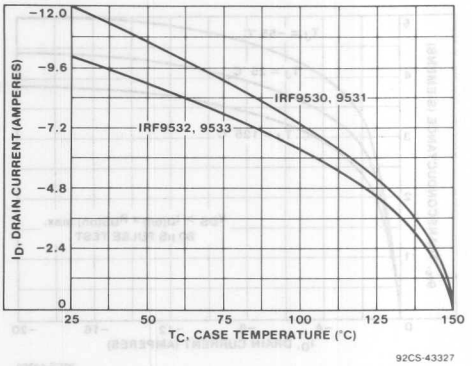


Fig. 13 - Maximum drain current vs. case temperature.

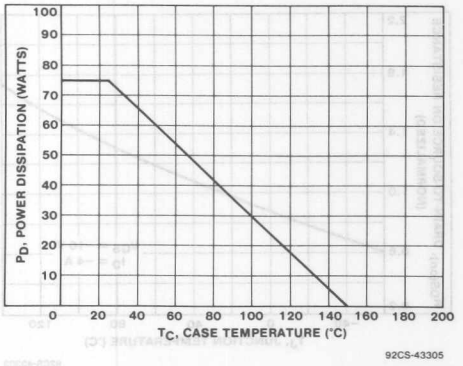


Fig. 14 - Power vs. temperature derating curve.

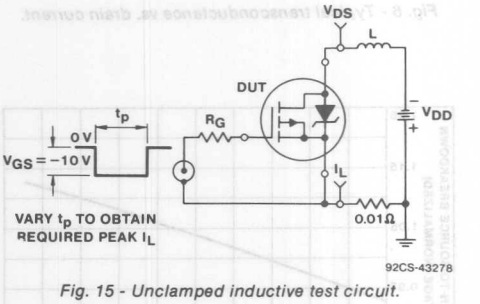


Fig. 15 - Unclamped inductive test circuit.

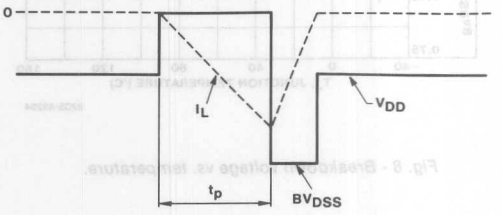


Fig. 16 - Unclamped inductive waveforms.

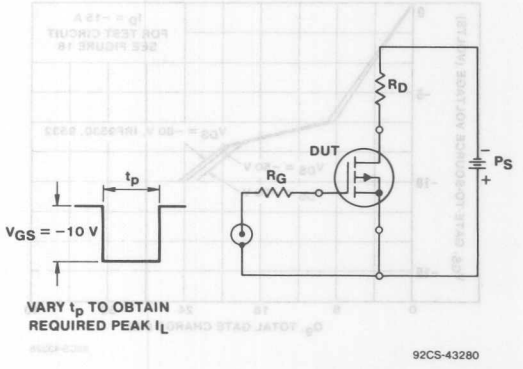


Fig. 17 - Switching time test circuit.

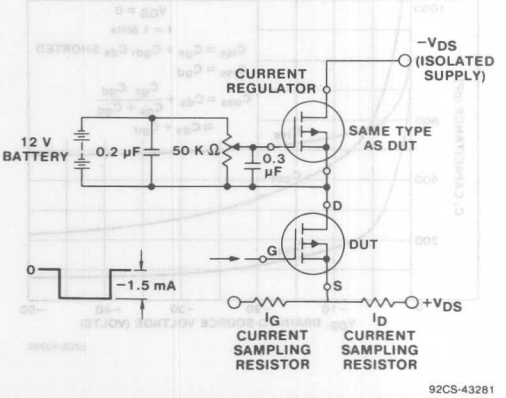


Fig. 18 - Gate charge test circuit.

IRF9540, IRF9541 IRF9542, IRF9543

Avalanche Energy Rated P-Channel Power MOSFETs

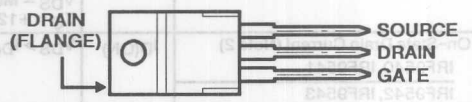
August 1991

Features

- -15A and -19A, -60V and -100V
- $r_{DS(ON)}$ = 0.20Ω and 0.30Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-220AB
TOP VIEW



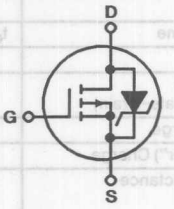
Description

The IRF9540, IRF9541, IRF9542 and IRF9543 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRF9540	IRF9541	IRF9542	IRF9543	UNITS
Drain-Source Voltage (1)	V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current						
T_C = 25°C	I_D	-19	-19	-15	-15	A
T_C = 100°C	I_D	-12	-12	-10	-10	A
Pulsed Drain Current (3)	I_{DM}	-76	-76	-60	-60	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation (See Figure 14)	P_D	125	125	125	125	W
Linear Derating Factor (See Figure 14)		1	1	1	1	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	960	960	960	960	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 4mH, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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Drain-Source Breakdown Voltage IRF9540, IRF9542	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9541, IRF9543			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9540, IRF9541	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-19	-	-	A
IRF9542, IRF9543			-15	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9540, IRF9541	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	-	0.15	0.20	Ω
IRF9542, IRF9543			-	0.22	0.30	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -6A	5	7	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	1100	-	pF
Output Capacitance	C_{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	250	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -19A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	16	20	ns
Rise Time	t_r		-	65	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	47	70	ns
Fall Time	t_f		-	28	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -19A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	70	90	nC
Gate-Source Charge	Q_{gs}		-	14	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	56	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-19	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-76	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -19A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 19A, dI_F/dt = 100A/μs	-	170	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 19A, dI_F/dt = 100A/μs	-	0.8	0	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 4mH, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

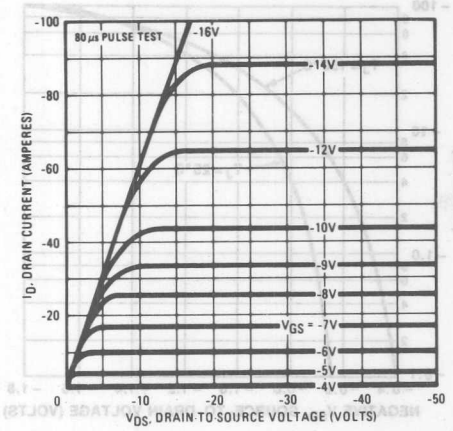


Fig. 1 - Typical output characteristics.

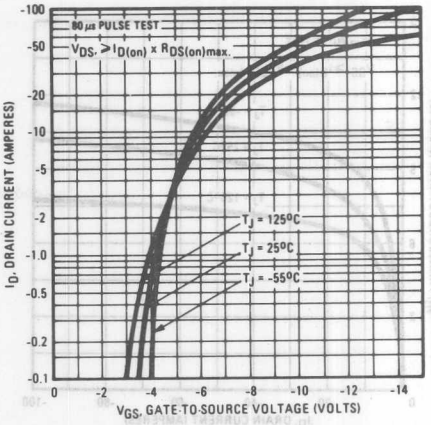


Fig. 2 - Typical transfer characteristics.

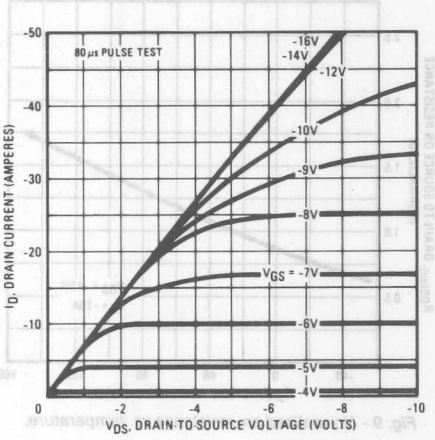


Fig. 3 - Typical saturation characteristics.

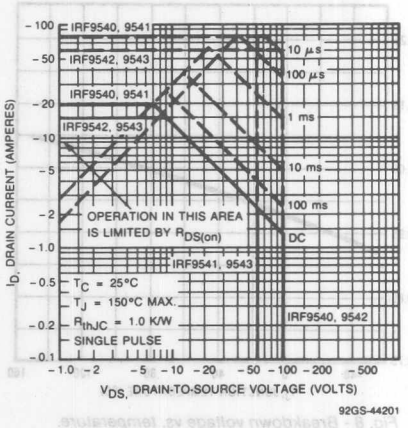


Fig. 4 - Maximum safe operating area.

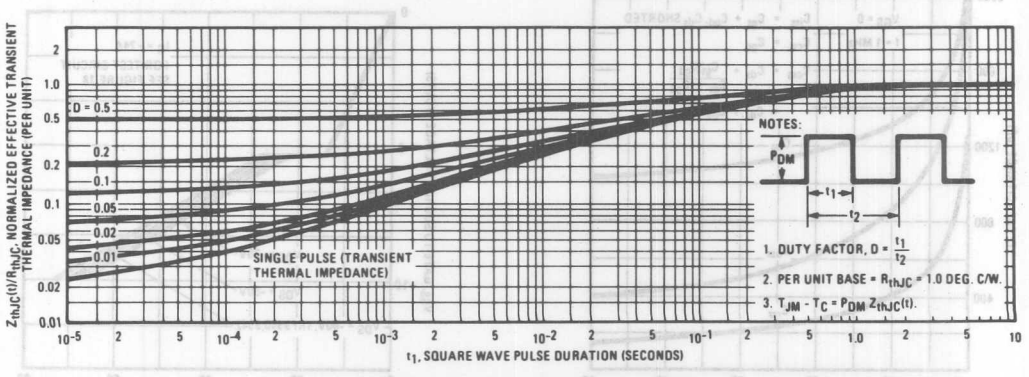


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

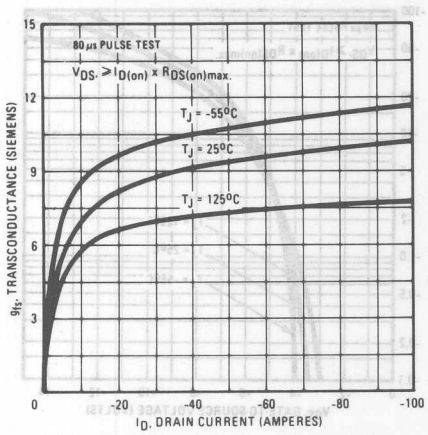


Fig. 6 - Typical transconductance vs. drain current.

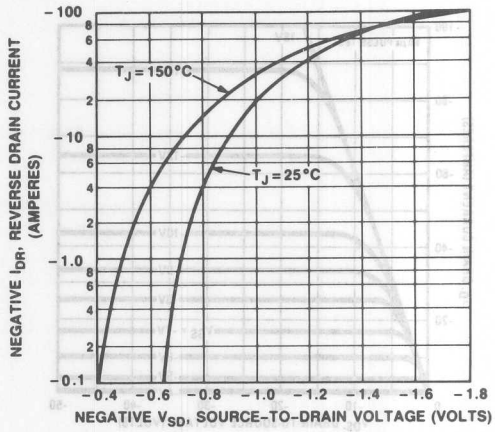


Fig. 7 - Typical source-drain diode forward voltage.

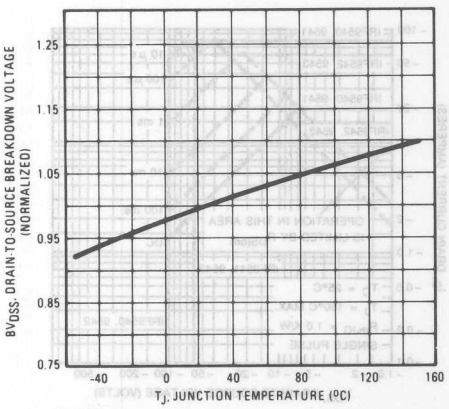


Fig. 8 - Breakdown voltage vs. temperature.

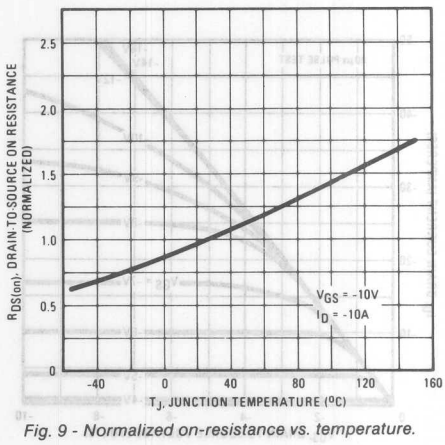


Fig. 9 - Normalized on-resistance vs. temperature.

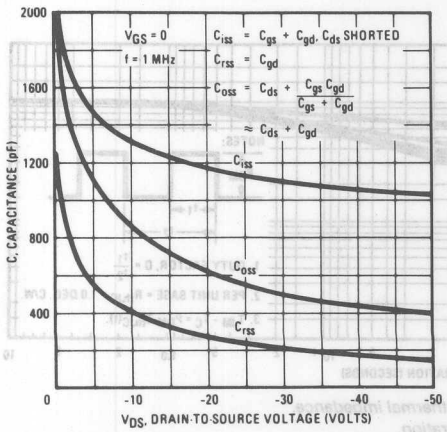


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

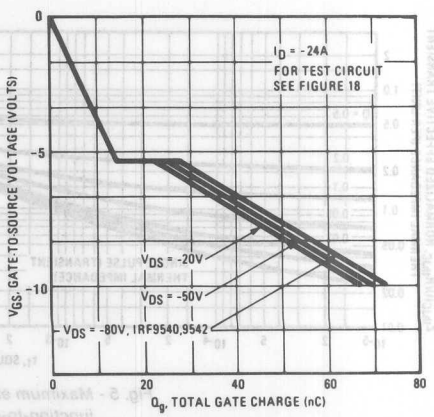


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

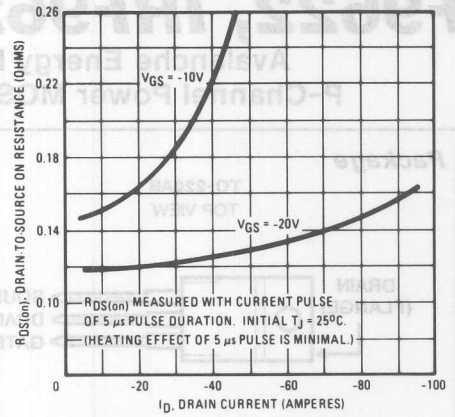


Fig. 12 - Typical on-resistance vs. drain current.

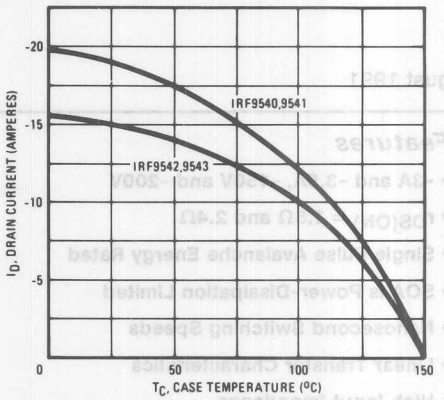


Fig. 13 - Maximum drain current vs. case temperature.

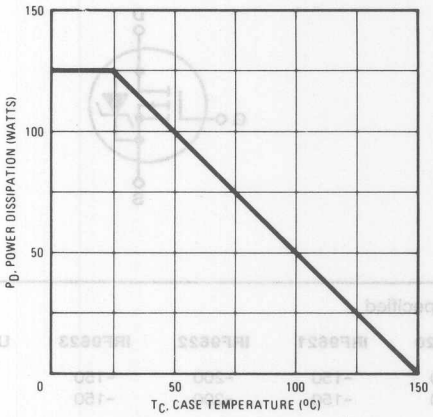


Fig. 14 - Power vs. temperature derating curve.

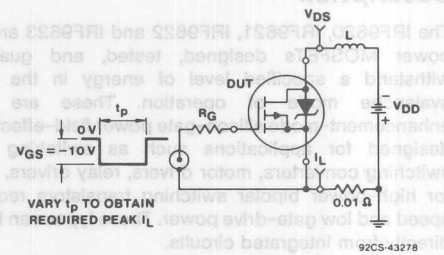


Fig. 15 - Unclamped inductive test circuit.

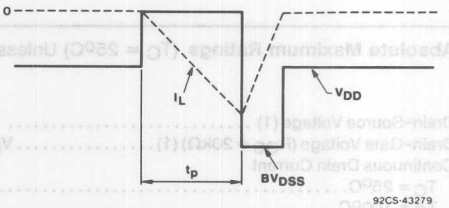


Fig. 16 - Unclamped inductive waveforms.

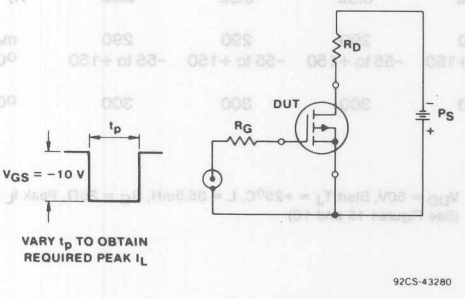


Fig. 17 - Switching time test circuit.

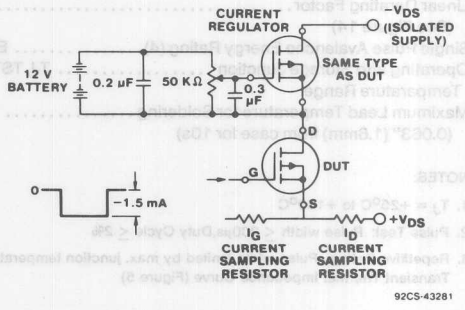


Fig. 18 - Gate charge test circuit.

HARRIS

IRF9620, IRF9621 IRF9622, IRF9623

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -3A and -3.5A, -150V and -200V
- $r_{DS(ON)}$ = 1.5Ω and 2.4Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

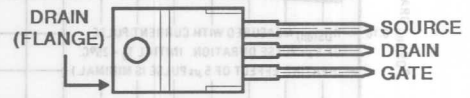
Description

The IRF9620, IRF9621, IRF9622 and IRF9623 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

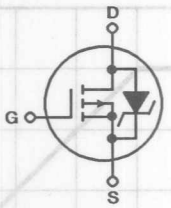
Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9620	IRF9621	IRF9622	IRF9623	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-3.5	-3.5	-3	-3	A
T_C = 100°C ..... I_D	-2	-2	-1.5	-1.5	A
Pulsed Drain Current (3) ..... I_{DM}	-14	-14	-12	-12	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	40	40	40	40	W
Linear Derating Factor ..... (See Figure 14)	0.32	0.32	0.32	0.32	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	290	290	290	290	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 35.5mH, R_G = 25Ω, Peak I_L = 3.5A (See Figures 15 and 16)

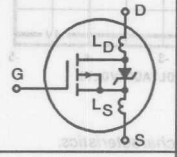
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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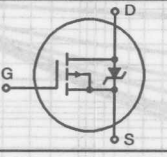
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9620, IRF9622	BV_{DSS}	V_{GS} = 0V, I_D = -250µA	-200	-	-	V
IRF9621, IRF9623			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250µA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	µA
On-State Drain Current (Note 2) IRF9620, IRF9621	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-3.5	-	-	A
IRF9622, IRF9623			-3	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9620, IRF9621	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -1.5A	-	1.0	1.5	Ω
IRF9622, IRF9623			-	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.5A	1	1.8	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	350	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -3.5A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	120	ns
Fall Time	t_f		-	50	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -3.5A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	22	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	3.12	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-3.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-14	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -3.5A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -3.5A, dI_F/dt = 100A/µs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -3.5A, dI_F/dt = 100A/µs	-	1.9	-	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 35.5mH, R_G = 25Ω, Peak I_L = 3.5A (See Figures 15 and 16)

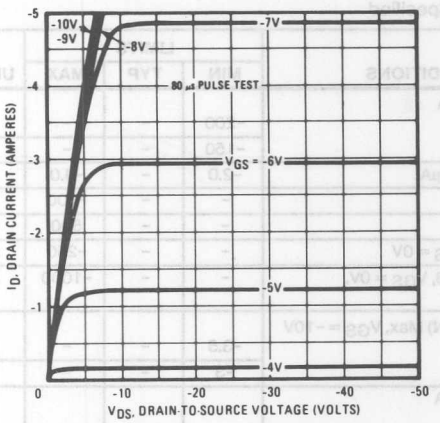


Fig. 1 - Typical output characteristics.

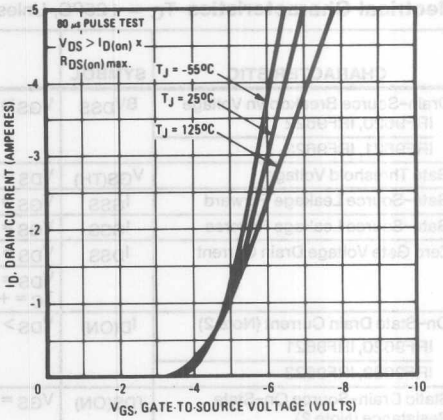


Fig. 2 - Typical transfer characteristics.

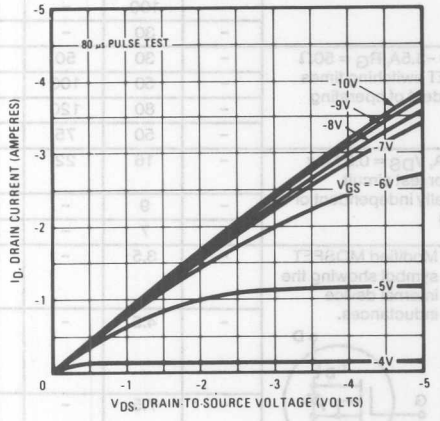


Fig. 3 - Typical saturation characteristics.

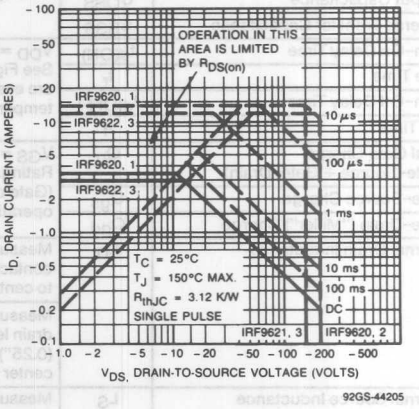


Fig. 4 - Maximum safe operating area.

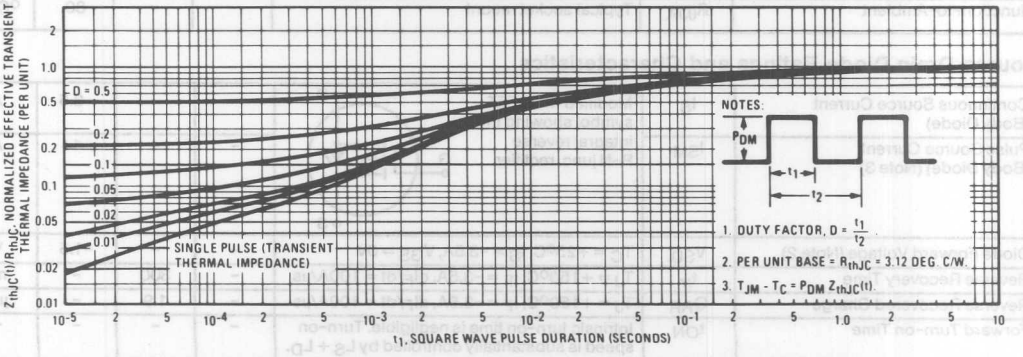


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

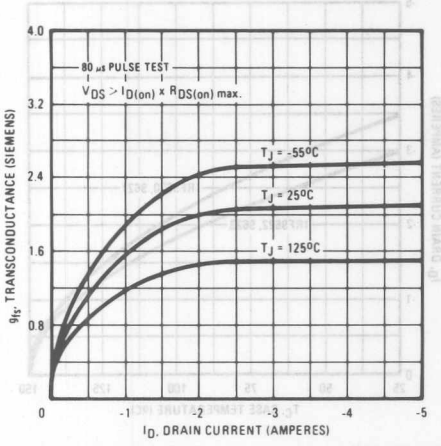


Fig. 6 - Typical transconductance vs. drain current.

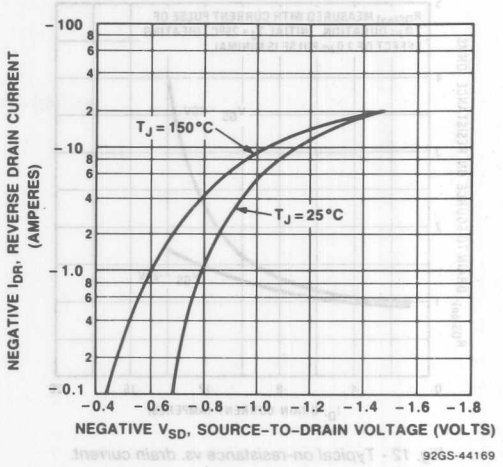


Fig. 7 - Typical source-drain diode forward voltage.

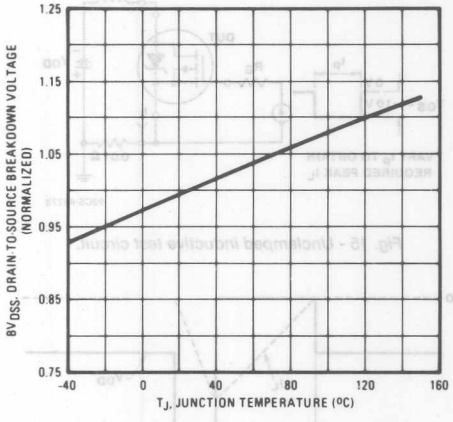


Fig. 8 - Breakdown voltage vs. temperature.

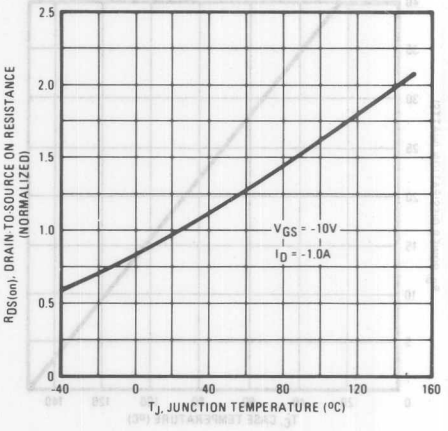


Fig. 9 - Normalized on-resistance vs. temperature.

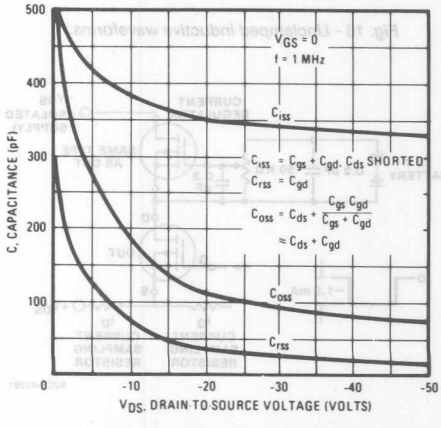


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

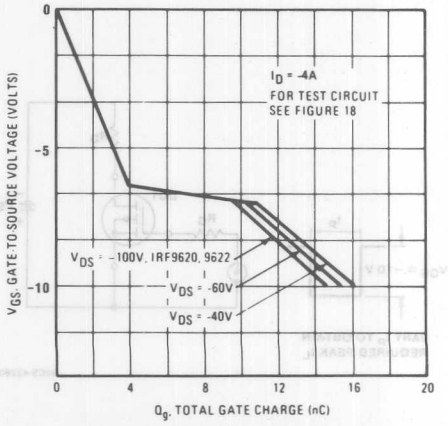


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

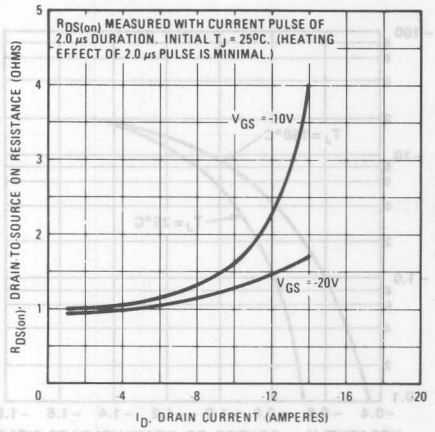


Fig. 12 - Typical on-resistance vs. drain current.

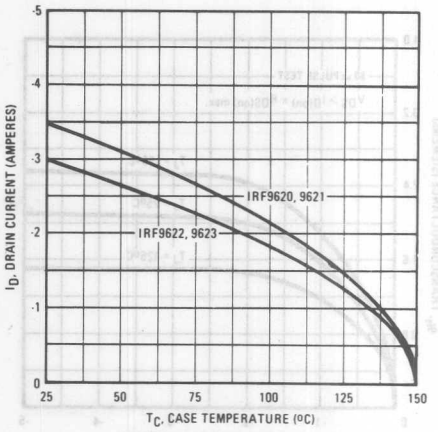


Fig. 13 - Maximum drain current vs. case temperature.

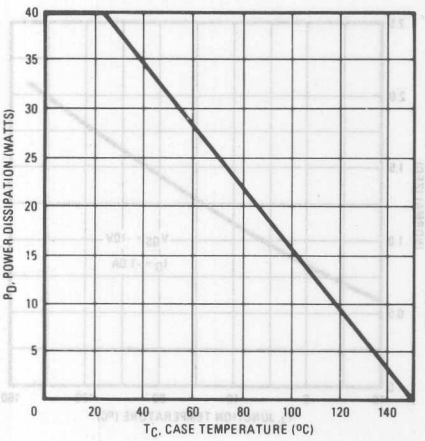


Fig. 14 - Power vs. temperature derating curve.

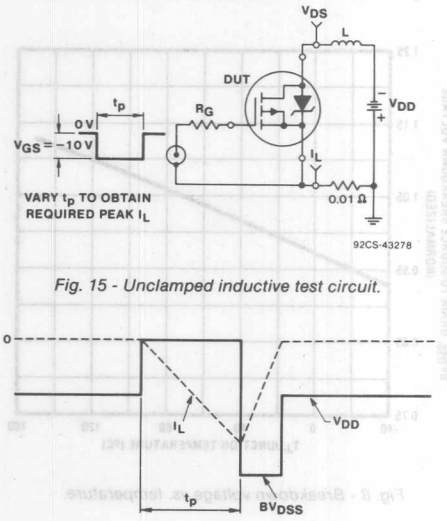


Fig. 15 - Unclamped inductive test circuit.

Fig. 16 - Unclamped inductive waveforms.

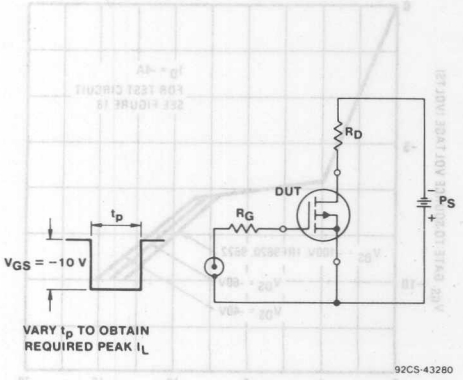


Fig. 17 - Switching time test circuit.

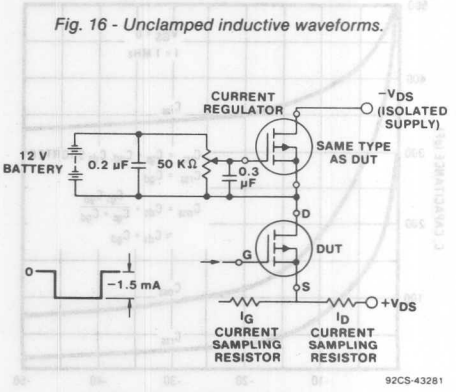


Fig. 18 - Gate charge test circuit.

IRF9630, IRF9631
IRF9632, IRF9633

Avalanche Energy Rated P-Channel Power MOSFETs

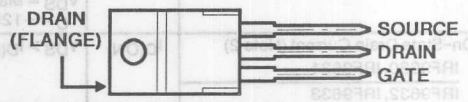
August 1991

Features

- -5.5A and -6.5A, -150V and -200V
- $r_{DS(ON)}$ = 0.8Ω and 1.2Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-220AB
TOP VIEW



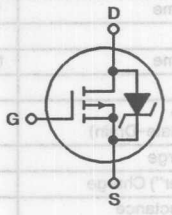
Description

The IRF9630, IRF9631, IRF9632 and IRF9633 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



5 P-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9630	IRF9631	IRF9632	IRF9633	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-6.5	-6.5	-5.5	-5.5	A
T_C = 100°C ..... I_D	-4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current (3) ..... I_{DM}	-26	-26	-22	-22	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	75	75	75	75	W
Linear Derating Factor ..... (See Figure 14)	0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	500	500	500	500	mJ
Operating and Storage Junction ..... TJ, TSTG Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 17.55mH, R_G = 25Ω, Peak I_L = 6.5A (See Figures 15 and 16)

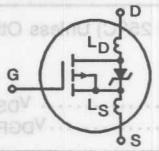
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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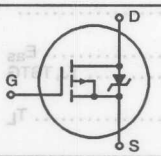
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9630, IRF9632	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRF9631, IRF9633			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9630, IRF9631	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-6.5	-	-	A
IRF9632, IRF9633			-5.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9630, IRF9631	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -3.5A	-	0.5	0.8	Ω
IRF9632, IRF9633			-	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 3.5A	2.2	3.5	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	550	-	pF
Output Capacitance	C_{OSS}		-	170	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -6.5A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	40	80	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -6.5A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	31	45	nC
Gate-Source Charge	Q_{gs}		-	18	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	13	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-6.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-26	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -6.5A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -6.5A, dI_F/dt = 100A/μs	-	400	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -6.5A, dI_F/dt = 100A/μs	-	2.6	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 17.75mH, R_G = 25Ω, Peak I_L = 6.5A (See Figures 15 and 16)

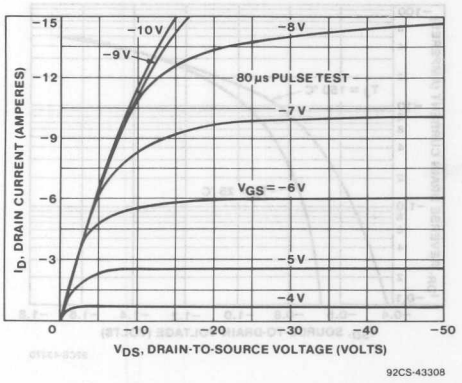


Fig. 1 - Typical output characteristics.

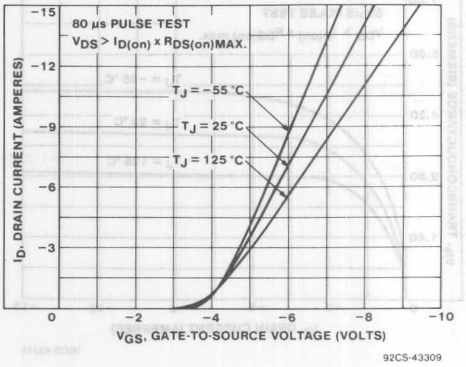


Fig. 2 - Typical transfer characteristics.

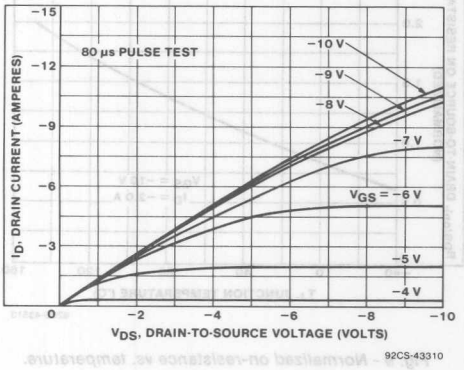


Fig. 3 - Typical saturation characteristics.

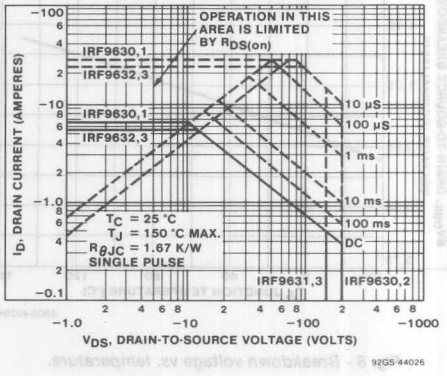


Fig. 4 - Maximum safe operating area.

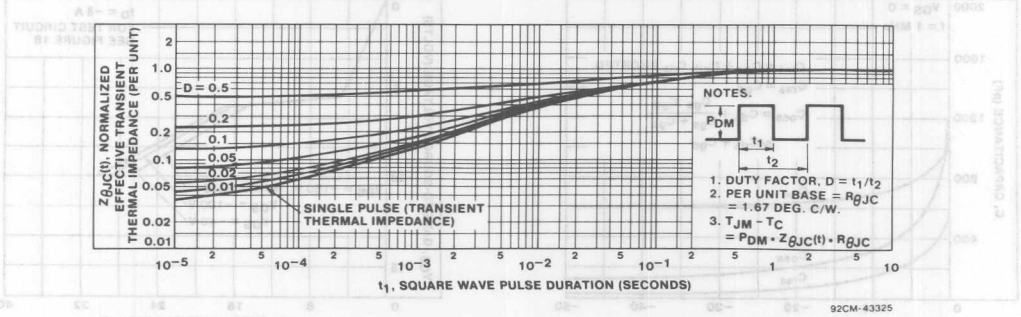


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

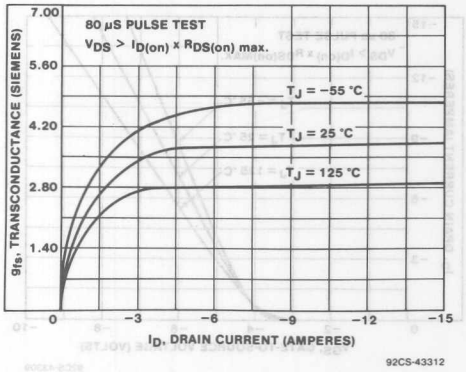


Fig. 6 - Typical transconductance vs. drain current.

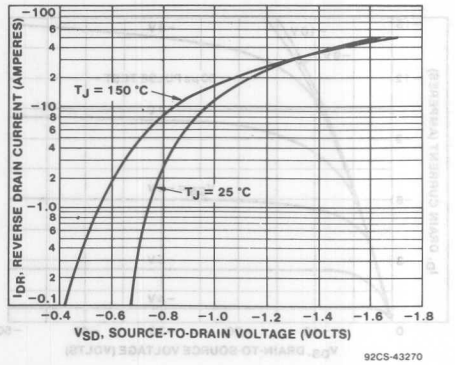


Fig. 7 - Typical source-drain diode forward voltage.

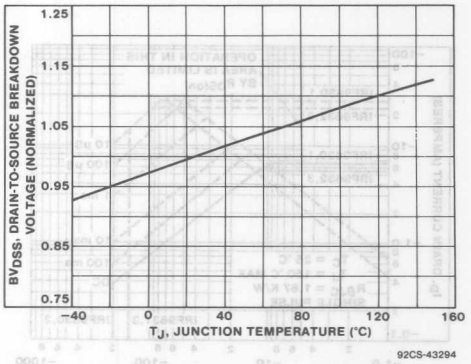


Fig. 8 - Breakdown voltage vs. temperature.

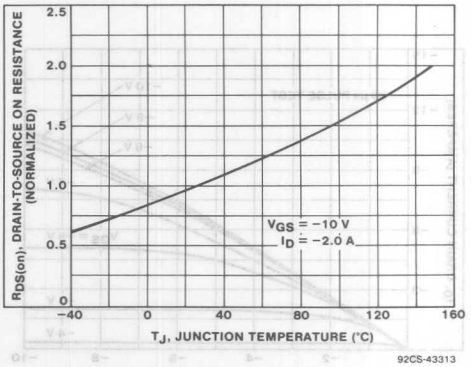


Fig. 9 - Normalized on-resistance vs. temperature.

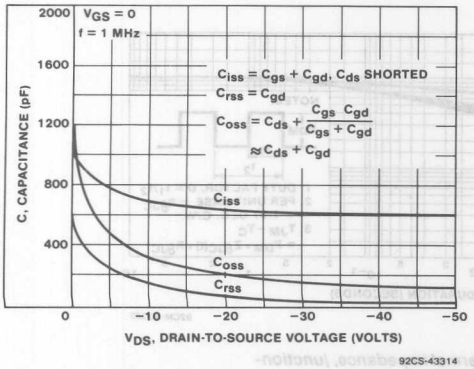


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

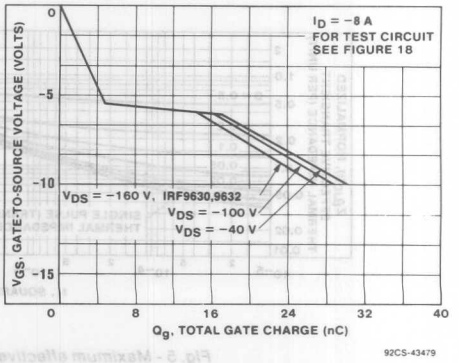


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

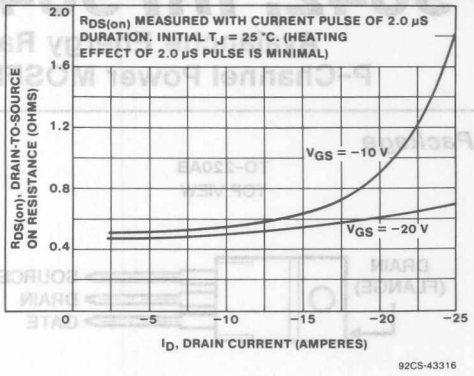


Fig. 12 - Typical on-resistance vs. drain current.

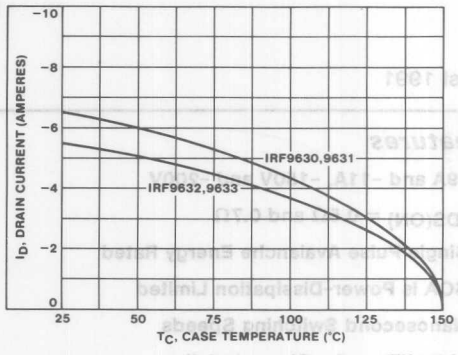


Fig. 13 - Maximum drain current vs. case temperature.

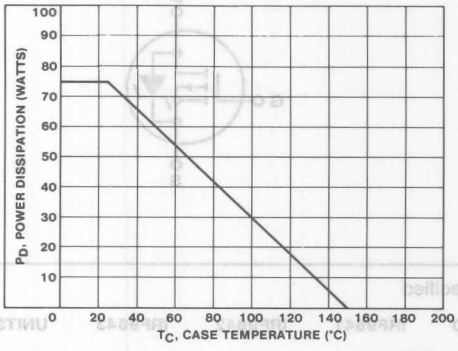


Fig. 14 - Power vs. temperature derating curve.

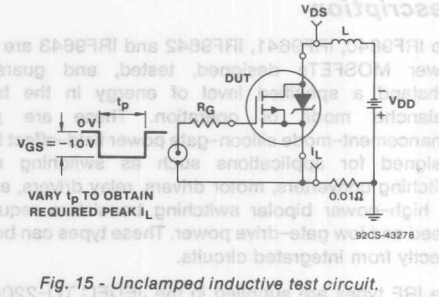


Fig. 15 - Unclamped inductive test circuit.

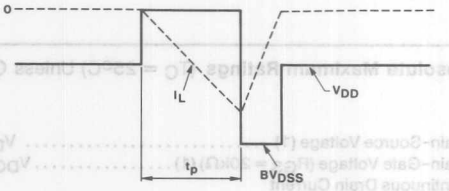


Fig. 16 - Unclamped inductive waveforms.

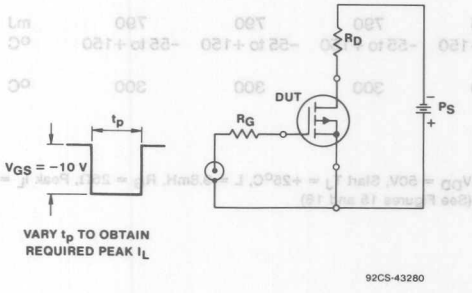


Fig. 17 - Switching time test circuit.

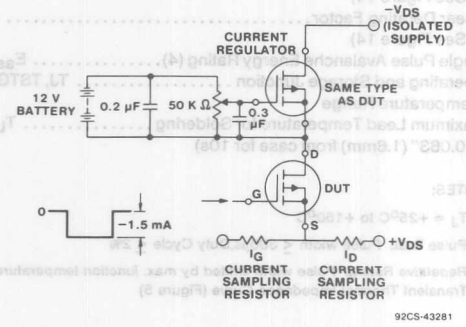


Fig. 18 - Gate charge test circuit.

HARRIS

IRF9640, IRF9641 IRF9642, IRF9643

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -9A and -11A, -150V and -200V
- $r_{DS(ON)}$ = 0.5Ω and 0.7Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

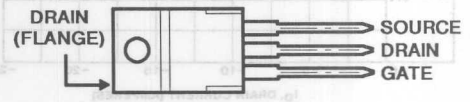
Description

The IRF9640, IRF9641, IRF9642 and IRF9643 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRF9640	IRF9641	IRF9642	IRF9643	UNITS
Drain-Source Voltage (1)	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current						
T_C = 25°C	I_D	-11	-11	-9	-9	A
T_C = 100°C	I_D	-7	-7	-6	-6	A
Pulsed Drain Current (3)	I_{DM}	-44	-44	-36	-36	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation (See Figure 14)	P_D	125	125	125	125	W
Linear Derating Factor (See Figure 14)		1	1	1	1	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	790	790	790	790	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 9.8mH, R_G = 25Ω, Peak I_L = 11A (See Figures 15 and 16)

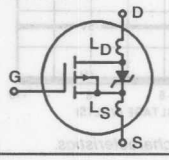
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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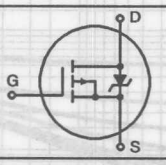
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9640, IRF9642	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRF9641, IRF9643			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9640, IRF9641	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-11	-	-	A
IRF9642, IRF9643			-9	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9640, IRF9641	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -6A	-	0.35	0.5	Ω
IRF9642, IRF9643			-	0.55	0.7	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -6A	4	6	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	1100	-	pF
Output Capacitance	C_{OSS}		-	375	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	150	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -11A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	18	22	ns
Rise Time	t_r		-	45	68	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	75	90	ns
Fall Time	t_f		-	29	44	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -11A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	70	90	nC
Gate-Source Charge	Q_{gs}		-	55	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	15	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-11	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-44	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -11A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -11A, dI_F/dt = 100A/μs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -11A, dI_F/dt = 100A/μs	-	1.9	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 9.8mH, R_G = 25Ω, Peak I_L = 11A (See Figures 15 and 16)

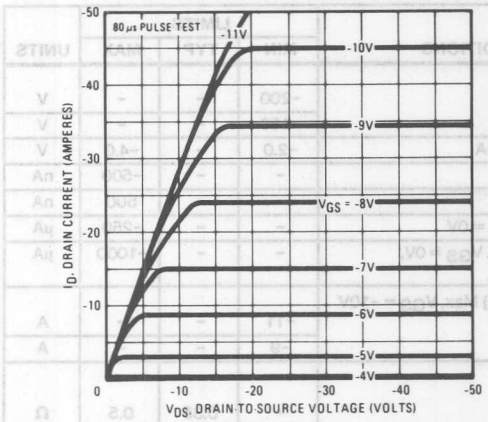


Fig. 1 - Typical output characteristics.

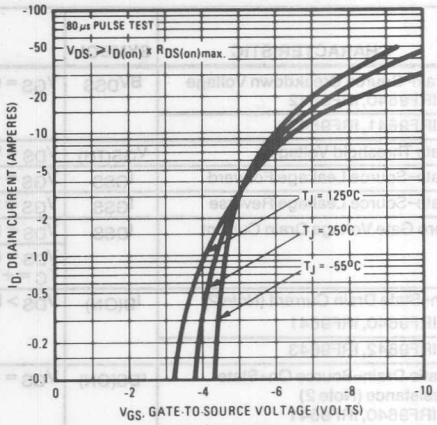


Fig. 2 - Typical transfer characteristics.

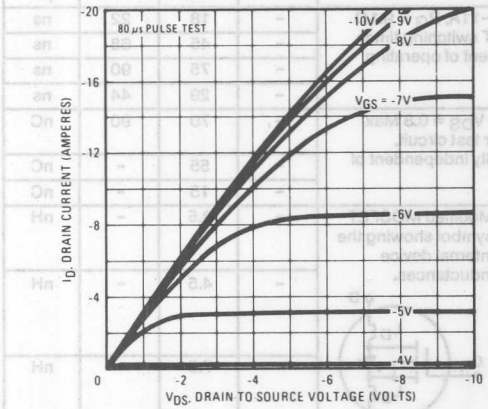


Fig. 3 - Typical saturation characteristics.

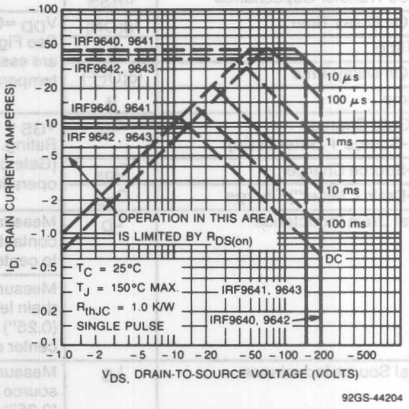


Fig. 4 - Maximum safe operating area.

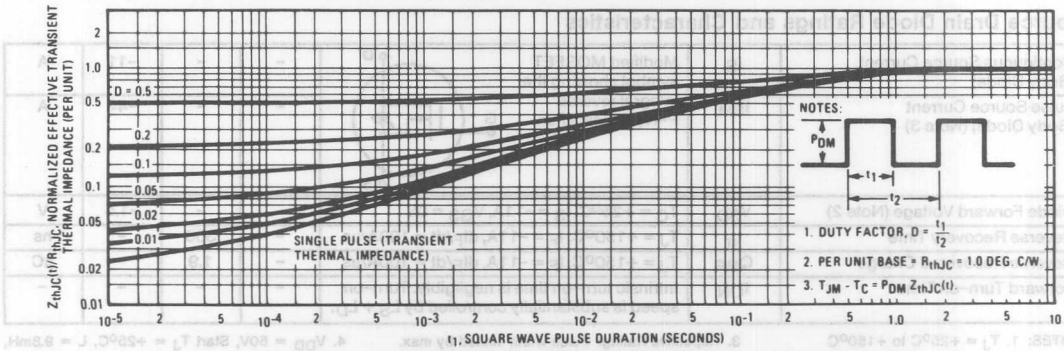


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

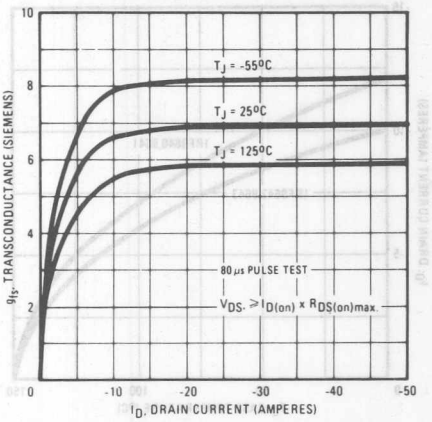


Fig. 6 - Typical transconductance vs. drain current.

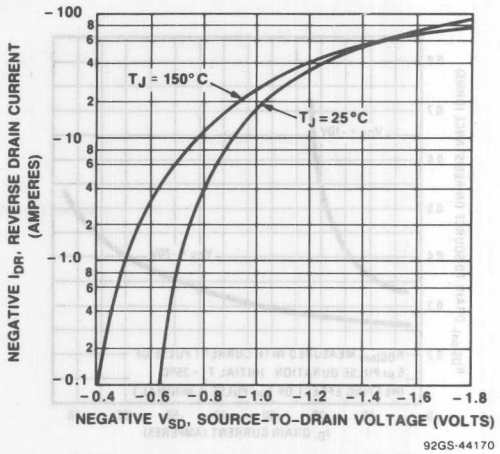


Fig. 7 - Typical source-drain diode forward voltage.

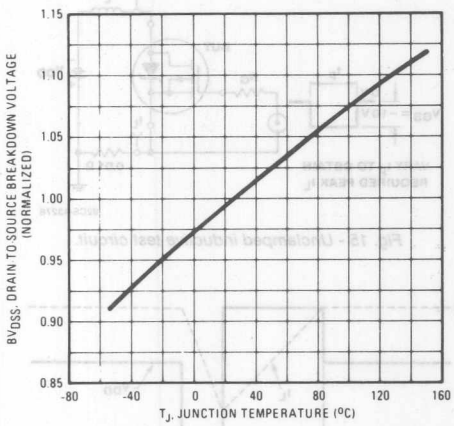


Fig. 8 - Breakdown voltage vs. temperature.

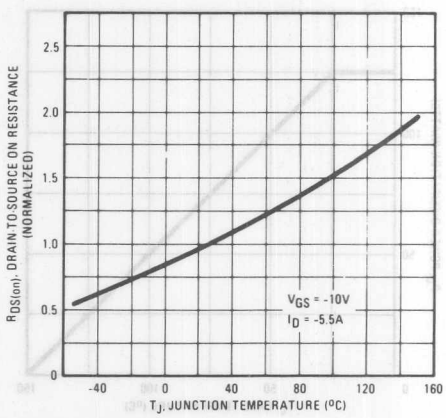


Fig. 9 - Normalized on-resistance vs. temperature.

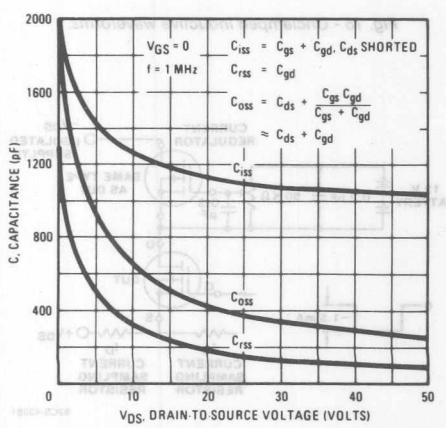


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

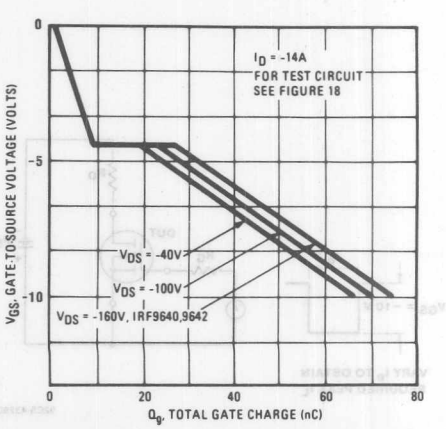


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

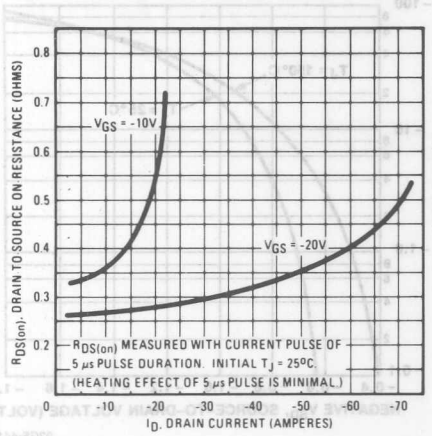


Fig. 12 - Typical on-resistance vs. drain current.

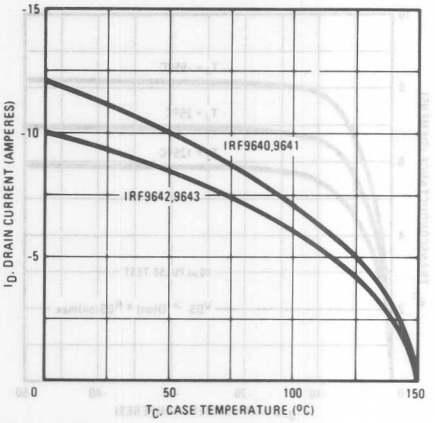


Fig. 13 - Maximum drain current vs. case temperature.

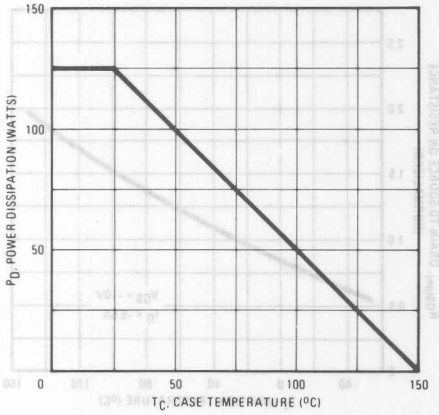


Fig. 14 - Power vs. temperature derating curve.

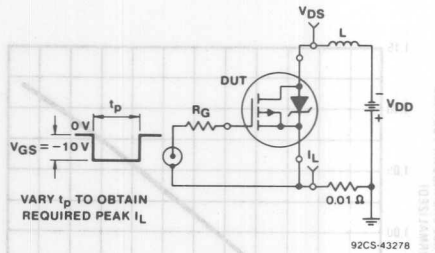


Fig. 15 - Unclamped inductive test circuit.

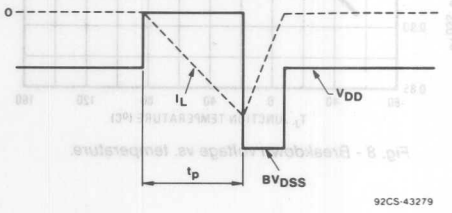


Fig. 16 - Unclamped inductive waveforms.

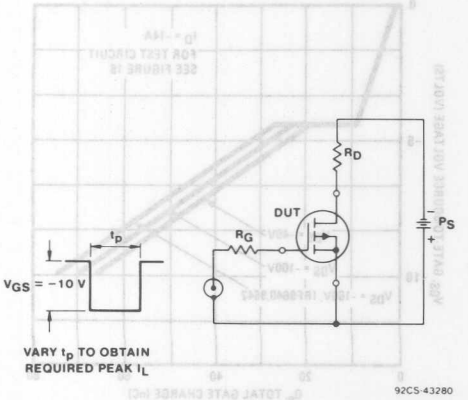


Fig. 17 - Switching time test circuit.

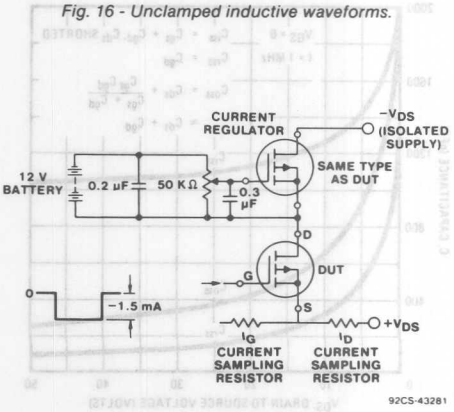


Fig. 18 - Gate charge test circuit.

HARRIS

IRFD9110
IRFD9113

Avalanche Energy Rated P-Channel Power MOSFETs

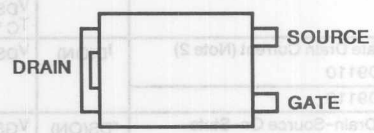
August 1991

Features

- -0.6A and -0.7V, -60V and -100V
- $r_{DS(ON)}$ = 1.2Ω and 1.6Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

4-PIN DUAL-IN-LINE
TOP VIEW



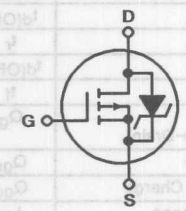
Description

The IRFD9110 and IRFD9113 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-Pin dual-in-line plastic package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



5

P-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFD9110	IRFD9113	UNITS
Drain-Source Voltage (1)	V_{DS}	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-100	-60	V
Continuous Drain Current T_C = 25°C	I_D	-0.7	-0.6	A
Pulsed Drain Current	I_{DM}	-3.0	-2.5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation (See Figure 13)	P_D	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	W/°C
Single Pulse Avalanche Energy Rating (3)	E_{as}	190	190	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

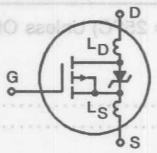
1. T_J = 25°C to 150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. V_{DD} = 25V, Start T_J = +25°C, L = 582mh, R_G = 25Ω, Peak I_L = 0.7A (See Figures 14 and 15)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

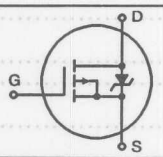
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File Number 2215

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD9110	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRFD9113			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFD9110	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-0.7	-	-	A
IRFD9113			-0.6	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD9110	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -0.3A	-	1.0	1.2	Ω
IRFD9113			-	1.2	1.6	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≤ 50V, I_D = -0.6A	0.59	0.88	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 9	-	180	-	pF
Output Capacitance	C_{OSS}		-	85	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5, I_D = 0.7A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature.)	-	15	30	ns
Rise Time	t_r		-	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	20	40	ns
Fall Time	t_f		-	20	40	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -0.7A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	11	15	nC
Gate-Source Charge	Q_{gs}		-	5.7	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	5.3	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from header to source bonding pad. 	-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-0.7	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-3.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -0.7A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -0.7A, dI_F/dt = 100A/μs	-	120	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -0.7A, dI_F/dt = 100A/μs	-	6.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. V_{DD} = 25V, Start T_J = +25°C, L = 582mH, R_G = 25Ω, Peak I_L = 0.7A (See Figures 14 and 15)

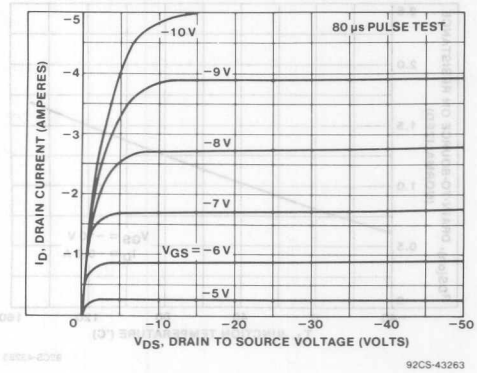


Fig. 1 - Typical Output Characteristics

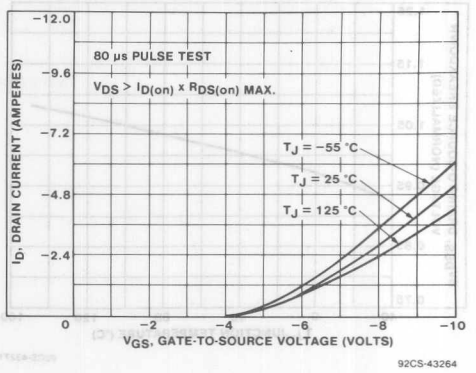


Fig. 2 - Typical Transfer Characteristics

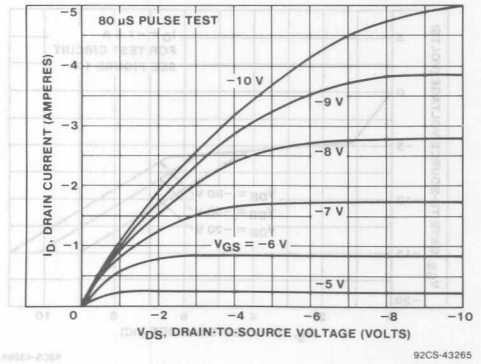


Fig. 3 - Typical Saturation Characteristics

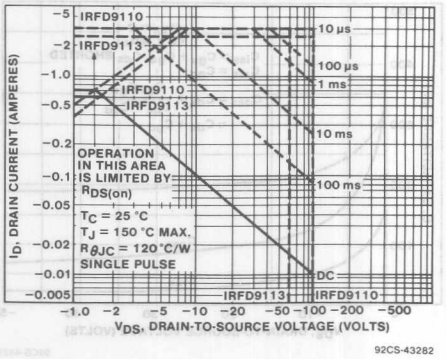


Fig. 4 - Maximum Safe Operating Area

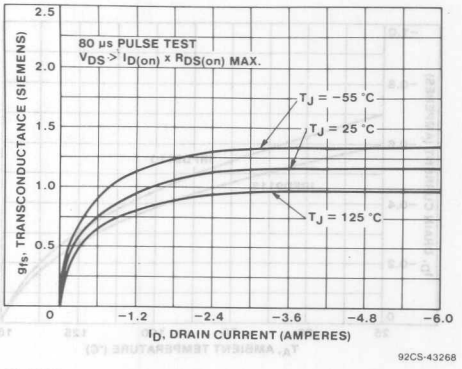


Fig. 5 - Typical Transconductance Vs. Drain Current

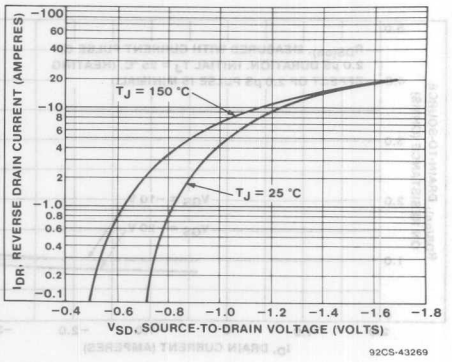


Fig. 6 - Typical Source-Drain Diode Forward Voltage

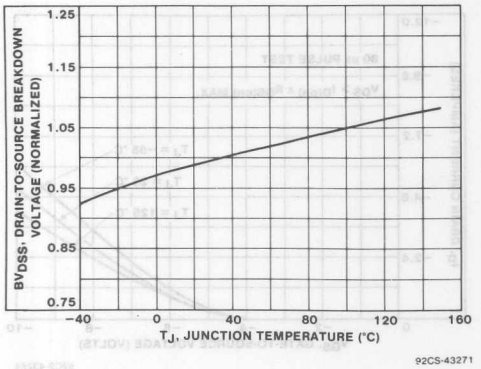


Fig. 7 - Breakdown Voltage Vs. Temperature

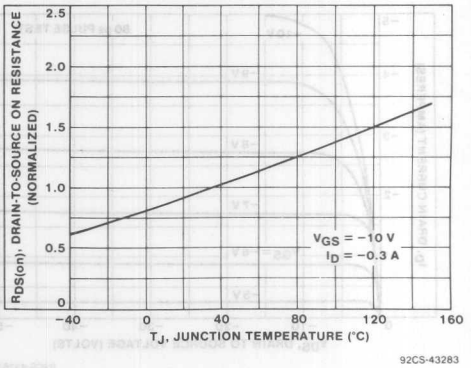


Fig. 8 - Normalized On-Resistance Vs. Temperature

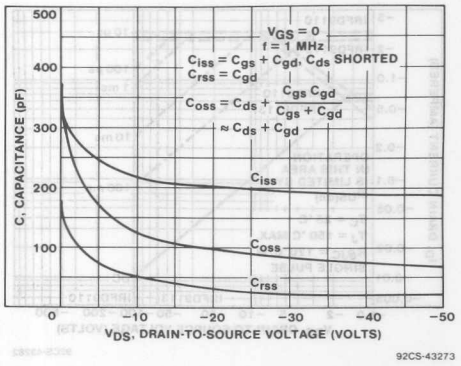


Fig. 9 - Typical Capacitance Vs. Drain-to-Source Voltage

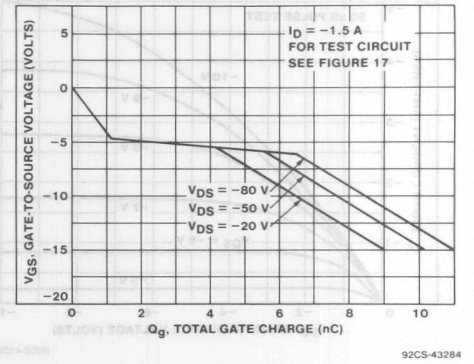


Fig. 10 - Typical Gate Charge Vs. Gate-to-Source Voltage

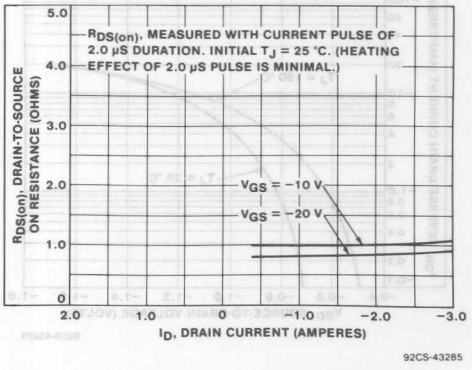


Fig. 11 - Typical On-Resistance Vs. Drain Current

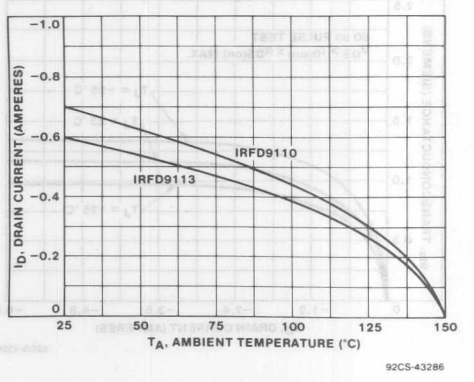


Fig. 12 - Maximum Drain Current Vs. Case Temperature

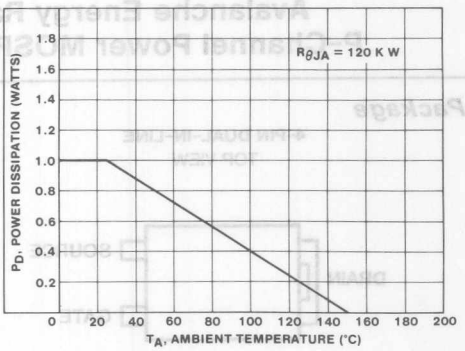


Fig. 13 - Power Vs. Temperature Derating Curve

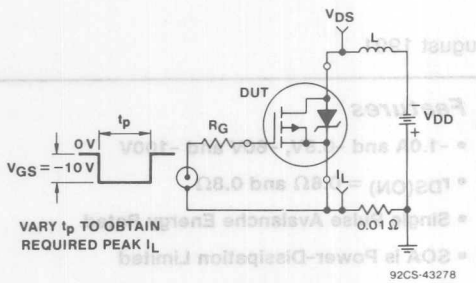


Fig. 14 - Unclamped Inductive Test Circuit

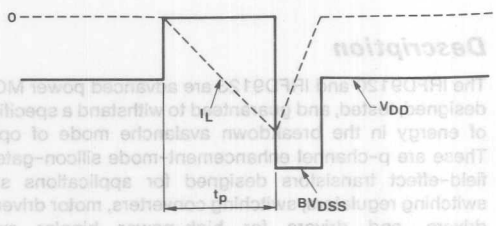


Fig. 15 - Unclamped Inductive Waveforms

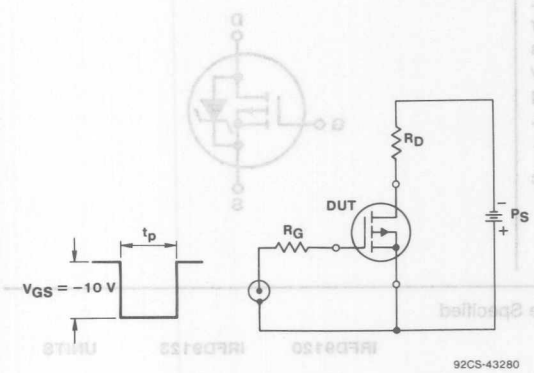


Fig. 16 - Switching Time Test Circuit

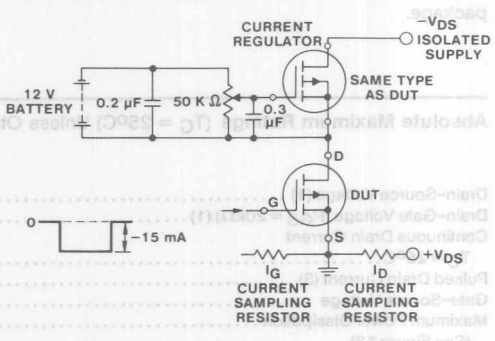


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFD9120
IRFD9123

Avalanche Energy Rated P-Channel Power MOSFETs

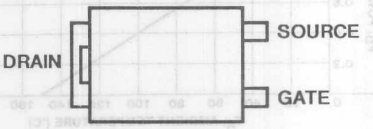
August 1991

Features

- -1.0A and -0.8V, -60V and -100V
- $r_{DS(ON)}$ = 0.6Ω and 0.8Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

4-PIN DUAL-IN-LINE
TOP VIEW



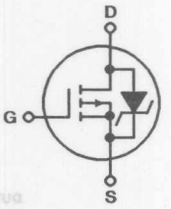
Description

The IRFD9120 and IRFD9123 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-Pin dual-in-line plastic package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFD9120	IRFD9123	UNITS
Drain-Source Voltage (1)	V_{DS}	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-100	-60	V
Continuous Drain Current T_C = 25°C	I_D	-1.0	-0.8	A
Pulsed Drain Current (3)	I_{DM}	-8.0	-6.4	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation (See Figure 13)	P_D	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	370	370	mJ
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

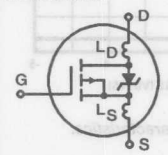
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 555mH, R_G = 25Ω, Peak I_L = 1.0A (See Figures 14 and 15)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

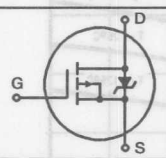
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File Number 2285

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD9120	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRFD9123			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFD9120	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-1.0	-	-	A
IRFD9123			-0.08	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD9120	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -0.8A	-	0.5	0.6	Ω
IRFD9123			-	0.6	0.8	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≤ 50V, I_D = -0.8A	0.8	1.2	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 9	-	300	-	pF
Output Capacitance	C_{OSS}		-	200	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5, I_D = 1.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature.)	-	25	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	50	100	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -1.0A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	20	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from header to source bonding pad. 	-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-1.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-8.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -1.0A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -4.0A, dI_F/dt = 100A/μs	-	150	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -4.0A, dI_F/dt = 100A/μs	-	0.9	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 555mH, R_G = 25Ω, Peak I_L = 1.0A (See Figures 14 and 15)

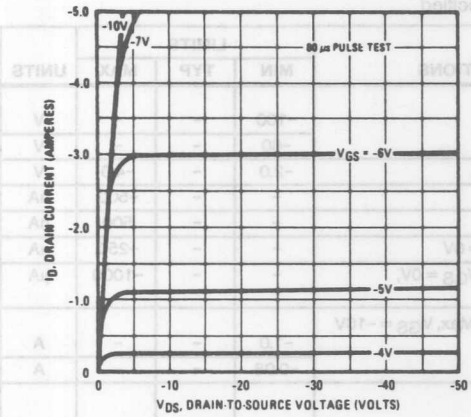


Fig. 1 - Typical output characteristics.

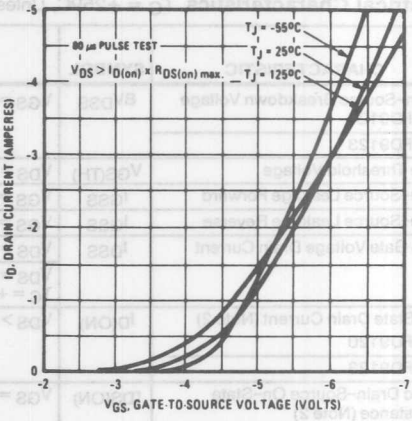


Fig. 2 - Typical transfer characteristics.

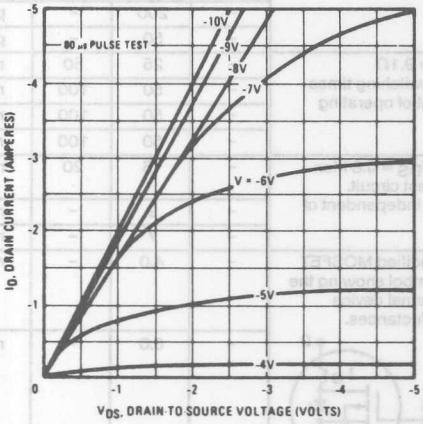


Fig. 3 - Typical saturation characteristics.

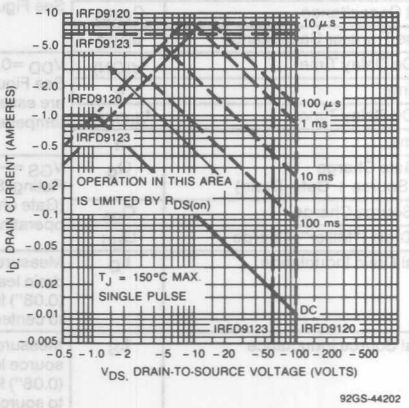


Fig. 4 - Maximum safe operating area.

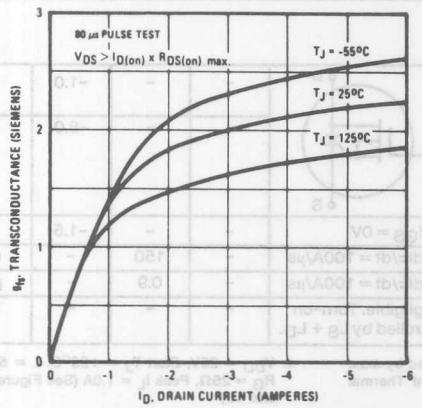


Fig. 5 - Typical transconductance vs. drain current.

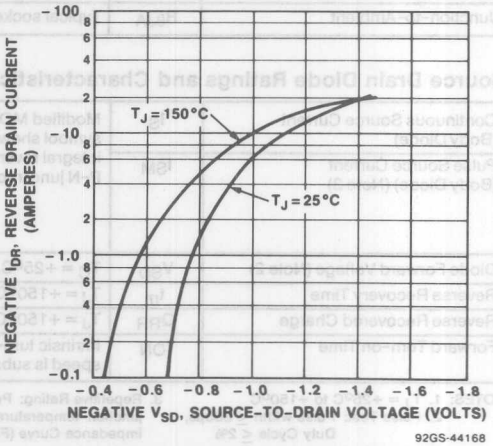


Fig. 6 - Typical source-drain diode forward voltage.

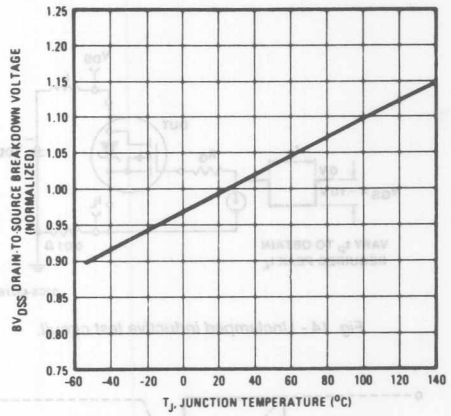


Fig. 7 - Breakdown voltage vs. temperature.

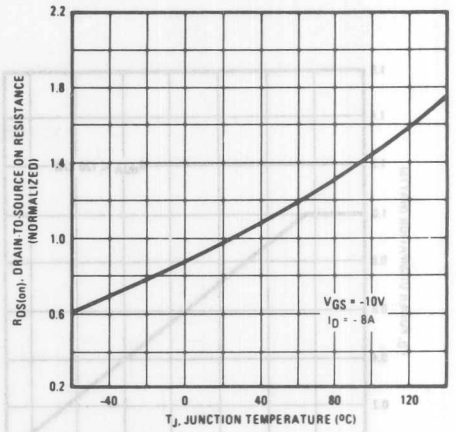


Fig. 8 - Normalized on-resistance vs. temperature.

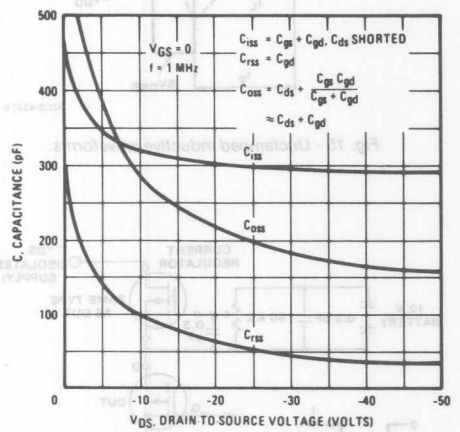


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

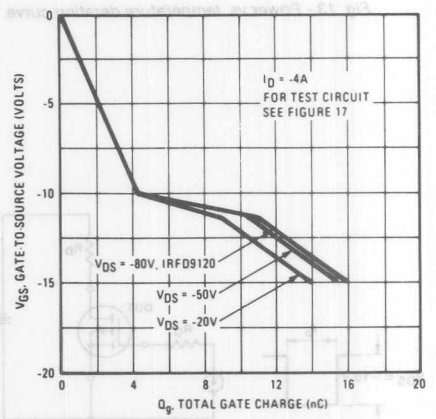


Fig. 10 - Typical gate charge vs. gate-to-source voltage.

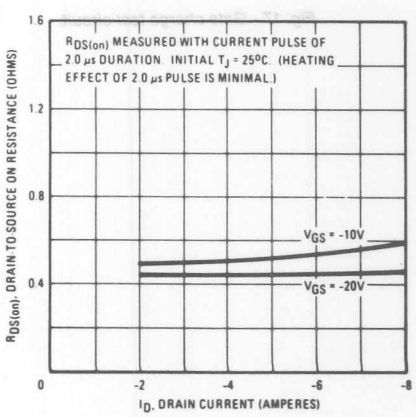


Fig. 11 - Typical on-resistance vs. drain current.

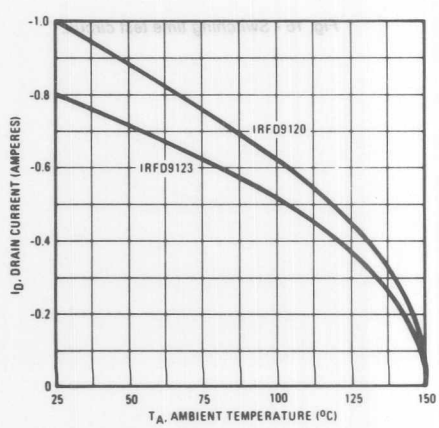


Fig. 12 - Maximum drain current vs. case temperature.

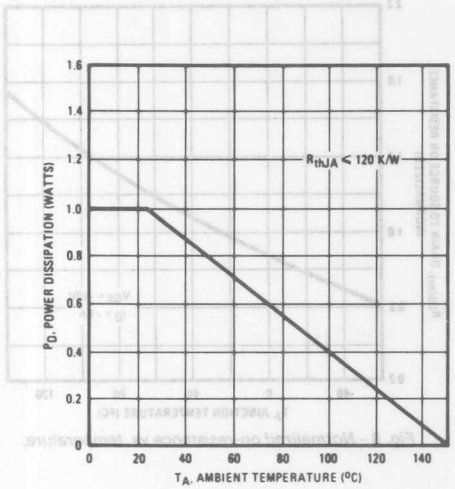


Fig. 13 - Power vs. temperature derating curve.

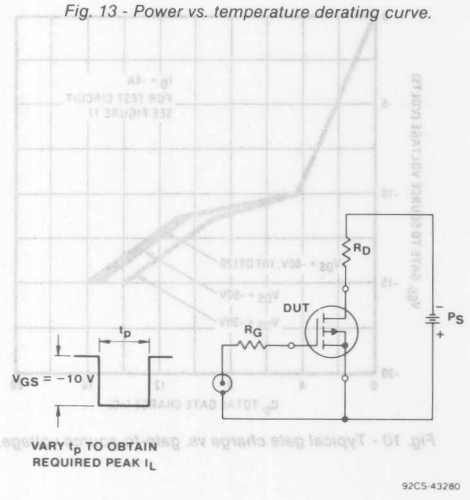
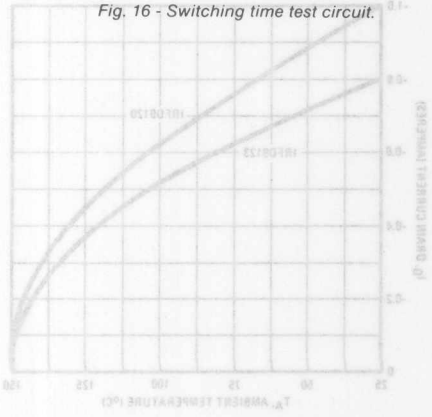


Fig. 16 - Switching time test circuit.



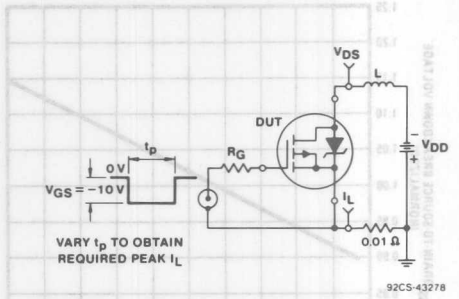


Fig. 14 - Unclamped inductive test circuit.

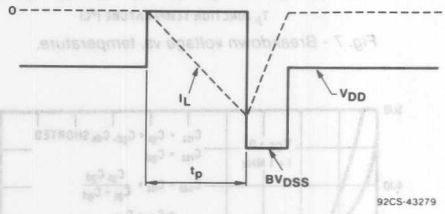


Fig. 15 - Unclamped inductive waveforms.

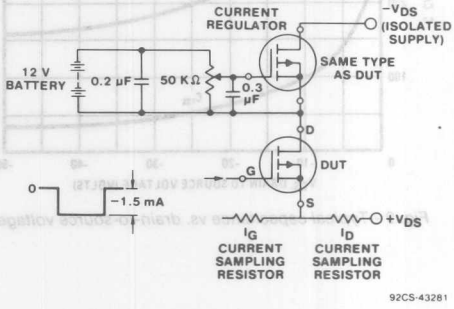
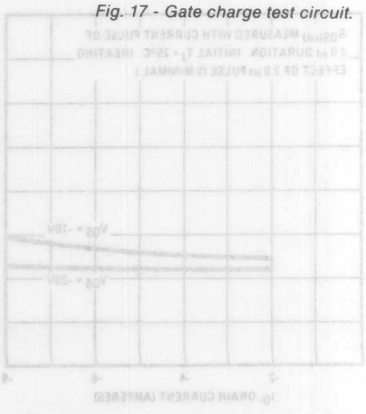


Fig. 17 - Gate charge test circuit.



HARRIS

IRFD9220
IRFD9223

Avalanche Energy Rated P-Channel Power MOSFETs

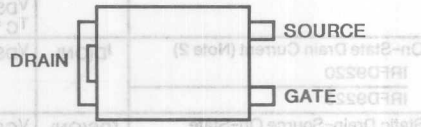
August 1991

Features

- -0.45A and -0.6V, -150V and -200V
- $r_{DS(ON)}$ = 1.5Ω and 2.4Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

4-PIN DUAL-IN-LINE
TOP VIEW



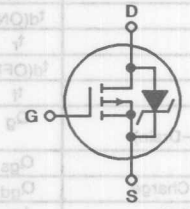
Description

The IRFD9220 and IRFD9223 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-Pin dual-in-line plastic package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFD9220	IRFD9223	UNITS
Drain-Source Voltage (1)	V_{DS}	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-200	-150	V
Continuous Drain Current T_C = 25°C	I_D	-0.6	-0.45	A
Pulsed Drain Current (3)	I_{DM}	-4.8	-3.6	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation (See Figure 13)	P_D	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	290	290	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

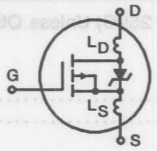
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 1210mH, R_G = 25Ω, Peak I_L = 0.6A (See Figures 14 and 15)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

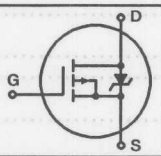
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File Number **2286**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD9220	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRFD9223			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFD9220	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-0.6	-	-	A
IRFD9223			-0.45	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD9220	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -0.3A	-	1.0	1.5	Ω
IRFD9223			-	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≤ 50V, I_D = -0.3A	0.6	1.0	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 9	-	350	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5, I_D = 0.6A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature.)	-	15	40	ns
Rise Time	t_r		-	25	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	120	ns
Fall Time	t_f		-	50	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -0.6A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	22	nC
Gate-Source Charge	Q_{gs}		-	10	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	4	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from header to source bonding pad. 	-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-0.6	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-4.8	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -0.6A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -0.6A, dI_F/dt = 100A/μs	-	150	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -0.6A, dI_F/dt = 100A/μs	-	0.5	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 1210mH, R_G = 25Ω, Peak I_L = 0.6A (See Figures 14 and 15)

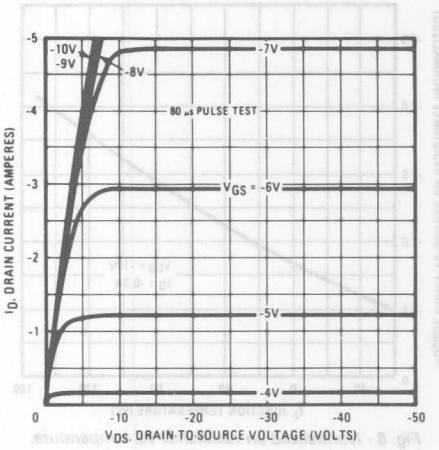


Fig. 1 - Typical output characteristics.

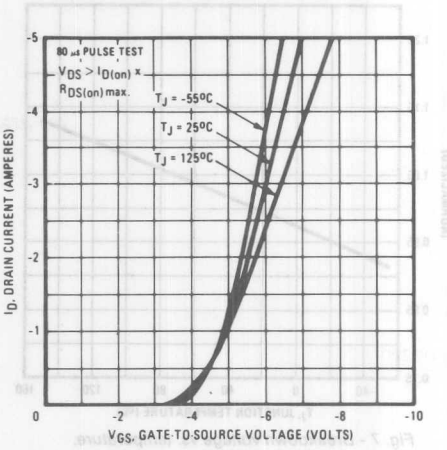


Fig. 2 - Typical transfer characteristics.

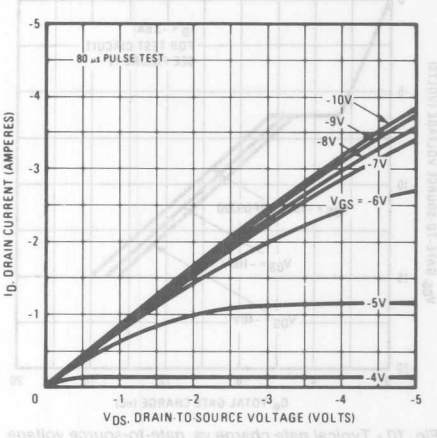


Fig. 3 - Typical saturation characteristics.

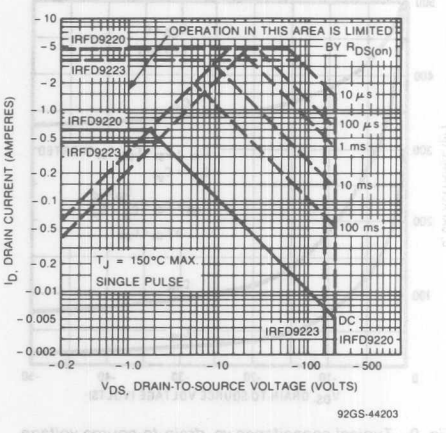


Fig. 4 - Maximum safe operating area.

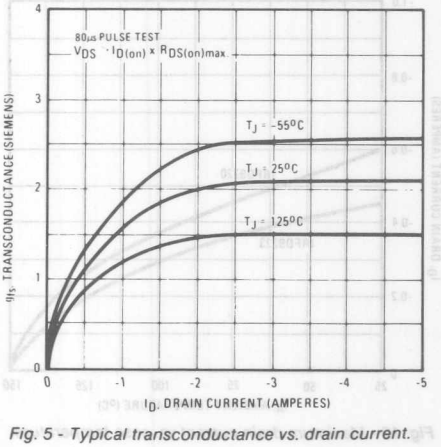


Fig. 5 - Typical transconductance vs. drain current.

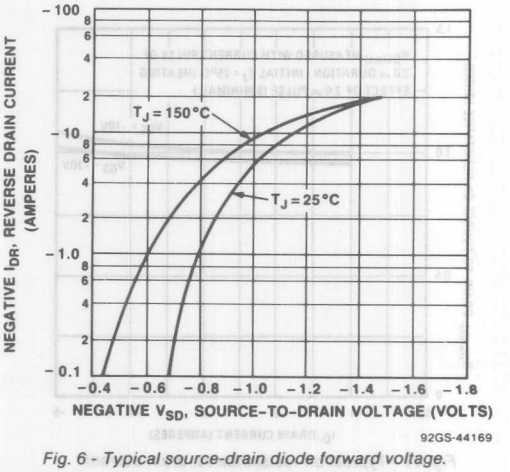


Fig. 6 - Typical source-drain diode forward voltage.

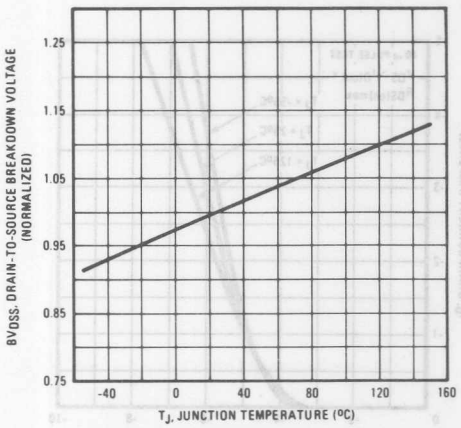


Fig. 7 - Breakdown voltage vs. temperature.

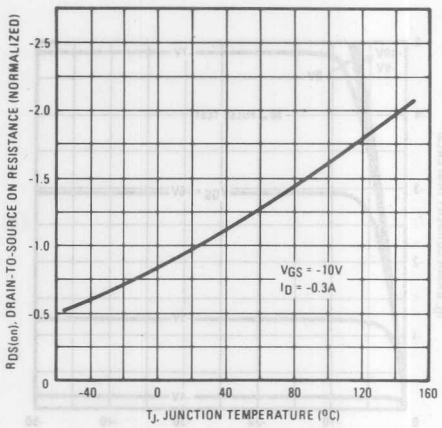


Fig. 8 - Normalized on-resistance vs. temperature.

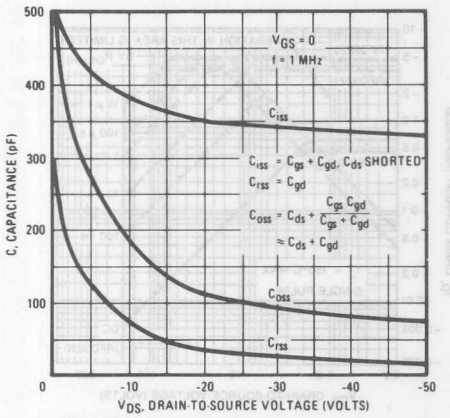


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

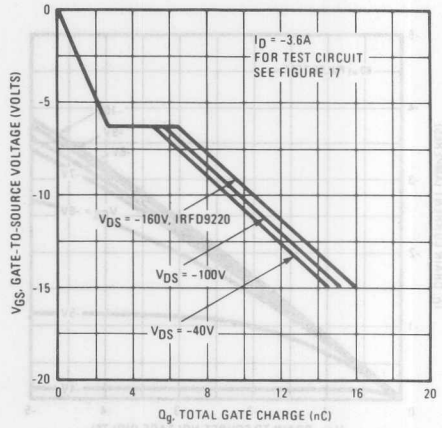


Fig. 10 - Typical gate charge vs. gate-to-source voltage.

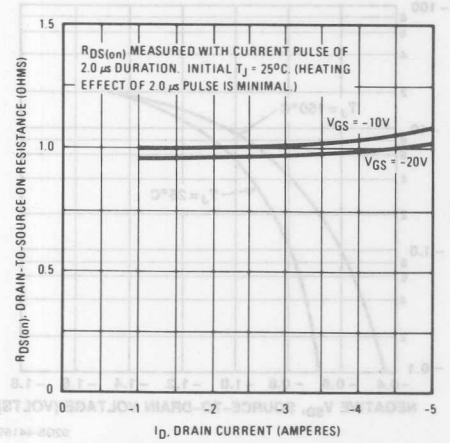


Fig. 11 - Typical on-resistance vs. drain current.

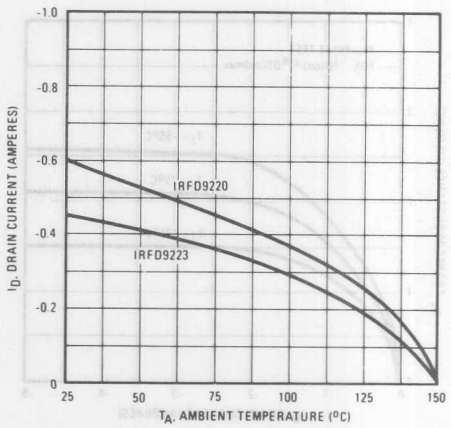


Fig. 12 - Maximum drain current vs. case temperature.

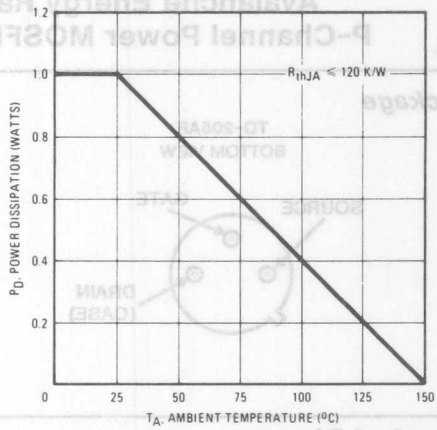


Fig. 13 - Power vs. temperature derating curve.

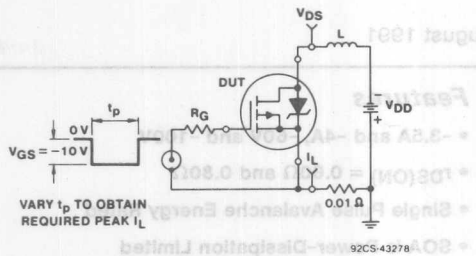


Fig. 14 - Unclamped inductive test circuit.

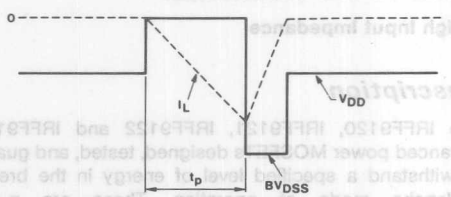


Fig. 15 - Unclamped inductive waveforms.

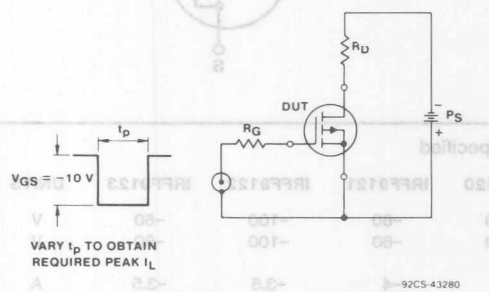


Fig. 16 - Switching time test circuit.

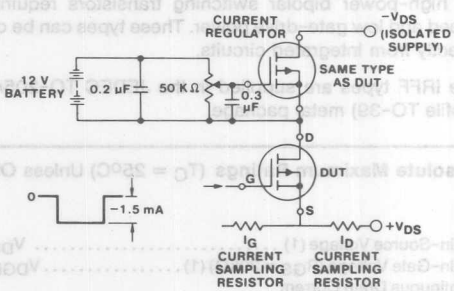


Fig. 17 - Gate charge test circuit.

HARRIS

IRFF9120, IRFF9121 IRFF9122, IRFF9123

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

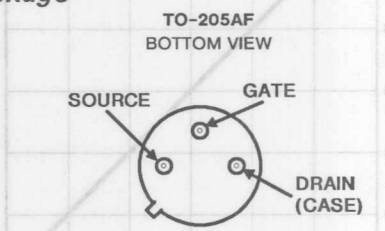
- -3.5A and -4A, -60V and -100V
- $r_{DS(ON)}$ = 0.60Ω and 0.80Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFF9120, IRFF9121, IRFF9122 and IRFF9123 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

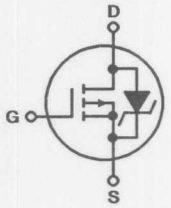
The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Package



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFF9120	IRFF9121	IRFF9122	IRFF9123	UNITS
Drain-Source Voltage (1)	V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current T_C = 25°C	I_D	-4	-4	-3.5	-3.5	A
Pulsed Drain Current (3)	I_{DM}	-16	-16	-14	-14	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation (See Figure 14)	P_D	20	20	20	20	W
Linear Derating Factor (See Figure 14)		0.16	0.16	0.16	0.16	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	370	370	370	370	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

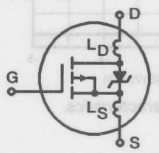
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 34.7mH, R_G = 25Ω, Peak I_L = 4.0A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

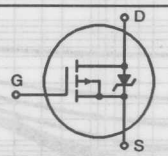
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File Number 2287

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF9120, IRFF9122	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRFF9121, IRFF9123			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFF9120, IRFF9121	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-4	-	-	A
IRFF9122, IRFF9123			-3.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF9120, IRFF9121	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -2A	-	0.5	0.6	Ω
IRFF9122, IRFF9123			-	0.6	0.8	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq I_{D(ON)} \times r_{DS(ON)}$ Max, I_D = -2A	1.25	2	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	300	-	pF
Output Capacitance	C_{OSS}		-	200	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -4A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	25	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	50	100	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -4A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	22	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5mm (0.2") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5mm (0.2") from header to source bonding pad. 	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	6.25	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-4	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-16	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -4A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 4A, dI_F/dt = 100A/μs	-	230	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -4A, dI_F/dt = 100A/μs	-	1.3	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 34.7mH, R_G = 25Ω, Peak I_L = 4A (See Figures 15 and 16)

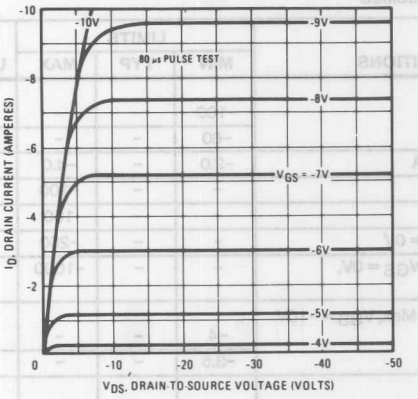


Fig. 1 - Typical output characteristics.

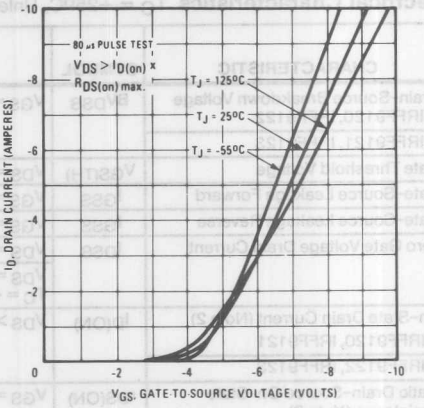


Fig. 2 - Typical transfer characteristics.

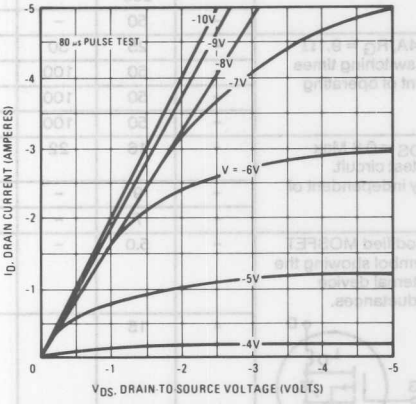


Fig. 3 - Typical saturation characteristics.

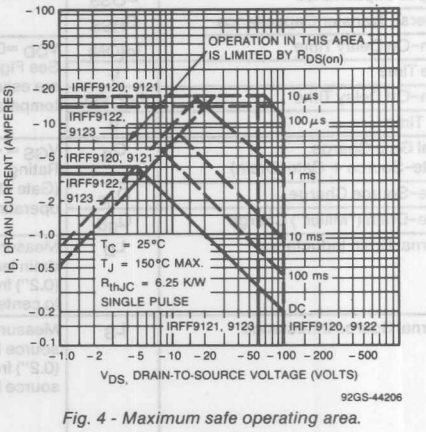


Fig. 4 - Maximum safe operating area.

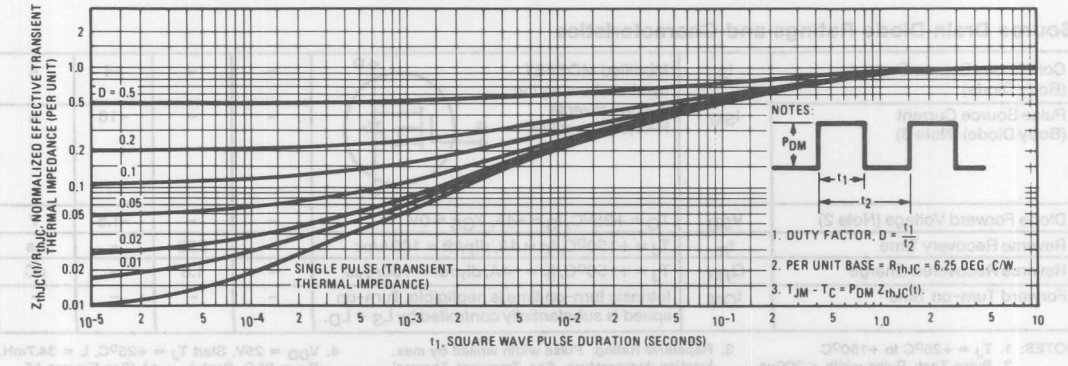


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

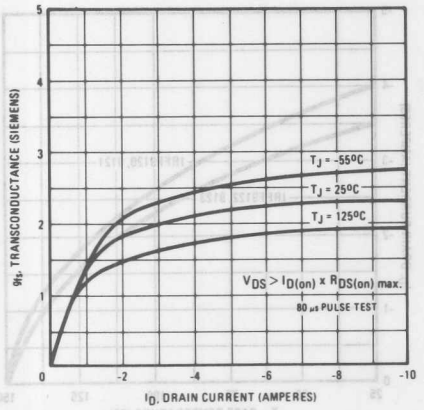


Fig. 6 - Typical transconductance vs. drain current.

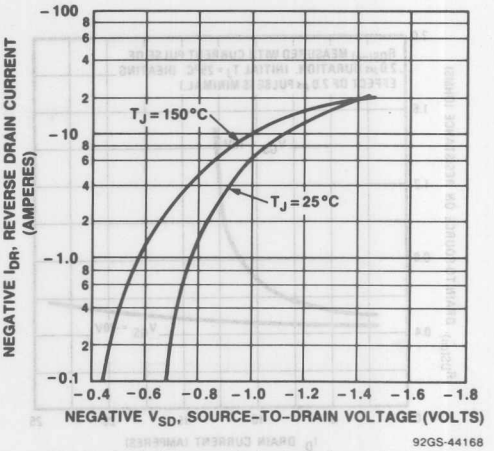


Fig. 7 - Typical source-drain diode forward voltage.

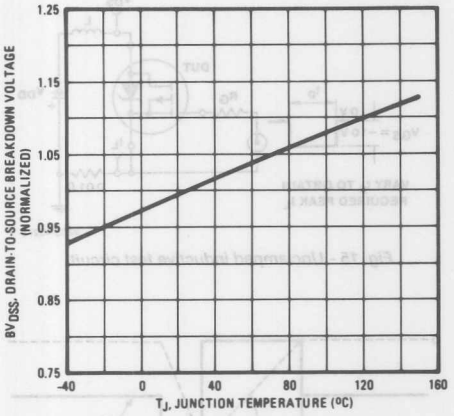


Fig. 8 - Breakdown voltage vs. temperature.

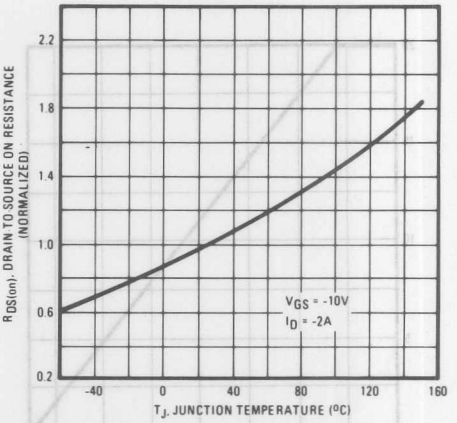


Fig. 9 - Normalized on-resistance vs. temperature.

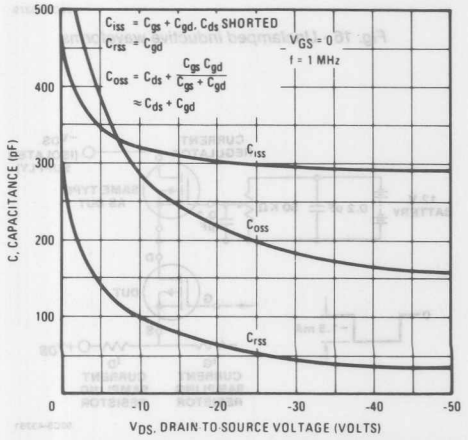


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

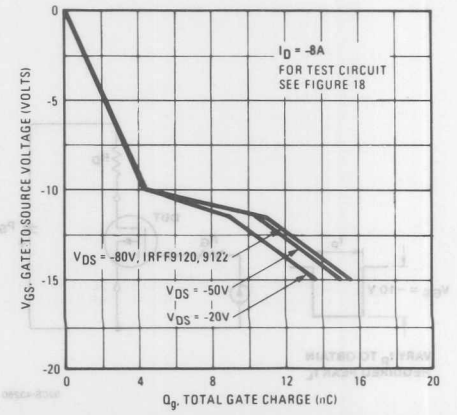


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

5 P-CHANNEL POWER MOSFETs

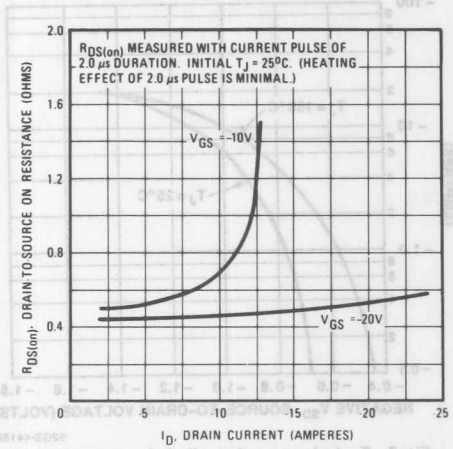


Fig. 12 - Typical on-resistance vs. drain current.

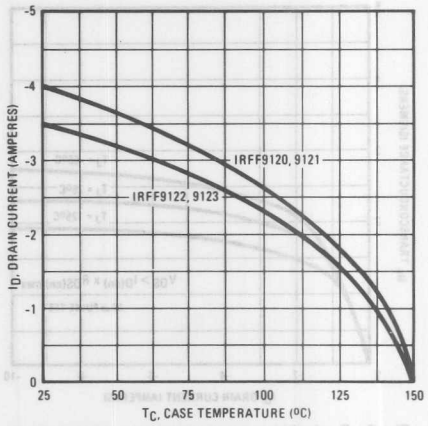


Fig. 13 - Maximum drain current vs. case temperature.

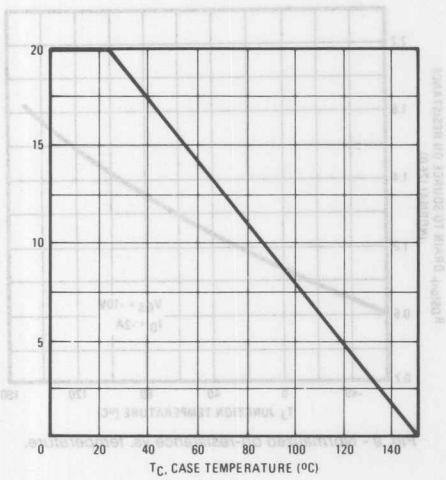


Fig. 14 - Power vs. temperature derating curve.

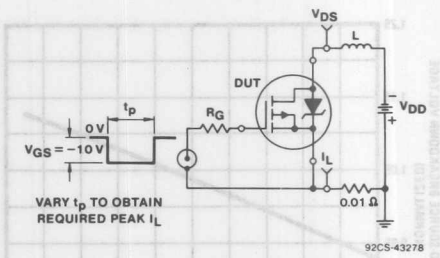


Fig. 15 - Unclamped inductive test circuit.

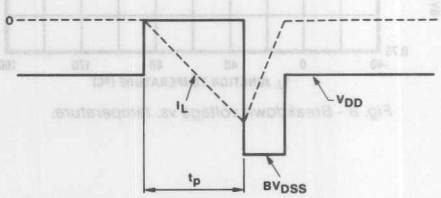


Fig. 16 - Unclamped inductive waveforms.

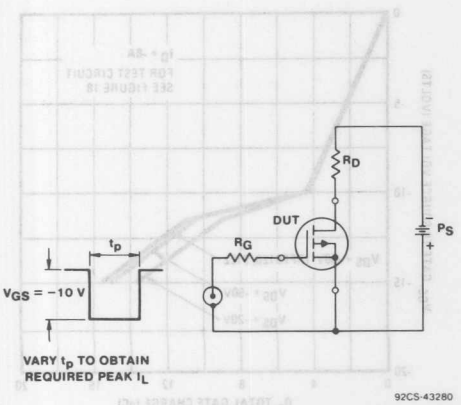


Fig. 17 - Switching time test circuit.

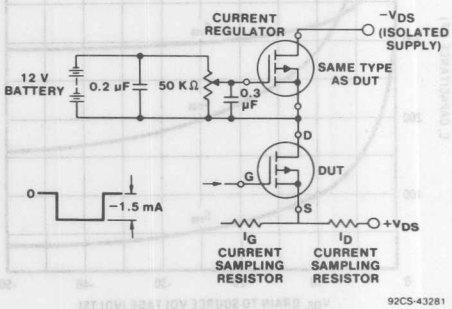


Fig. 18 - Gate charge test circuit.

HARRIS IRFF9130, IRFF9131 IRFF9132, IRFF9133

Avalanche Energy Rated P-Channel Power MOSFETs

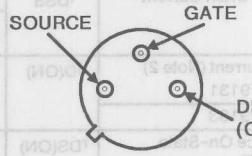
August 1991

Features

- -5.5A and -6.5A, -60V and -100V
- $r_{DS(ON)}$ = 0.30Ω and 0.40Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-205AF
BOTTOM VIEW



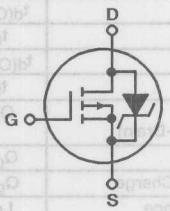
Description

The IRFF9130, IRFF9131, IRFF9132 and IRFF9133 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRFF9130	IRFF9131	IRFF9132	IRFF9133	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current T_C = 25°C ..... I_D	-6.5	-6.5	-5.5	-5.5	A
Pulsed Drain Current (3) ..... I_{DM}	-26	-26	-22	-22	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	25	25	25	25	W
Linear Derating Factor ..... (See Figure 14)	0.2	0.2	0.2	0.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	500	500	500	500	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

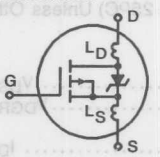
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 17.75mH, R_G = 25Ω, Peak I_L = 6.5A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

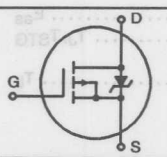
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File Number 2216

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF9130, IRFF9132	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRFF9131, IRFF9133			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFF9130, IRFF9131	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-6.5	-	-	A
IRFF9132, IRFF9133			-5.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF9130, IRFF9131	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -3A	-	0.25	0.3	Ω
IRFF9132, IRFF9133			-	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{ts}	$V_{DS} \geq I_{D(ON)} \times r_{DS(ON)}$ Max, I_D = -3A	2.5	3.5	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	500	-	pF
Output Capacitance	C_{OSS}		-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -6.5A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	60	ns
Rise Time	t_r		-	70	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	140	ns
Fall Time	t_f		-	70	140	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -6.5A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	25	45	nC
Gate-Source Charge	Q_{gs}		-	13	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5mm (0.2") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5mm (0.2") from header to source bonding pad. 	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-6.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-26	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -6.5A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -6.5A, dI_F/dt = 100A/μs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -6.5A, dI_F/dt = 100A/μs	-	1.8	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 17.75mH, R_G = 25Ω, Peak I_L = 6.5A (See Figures 15 and 16)

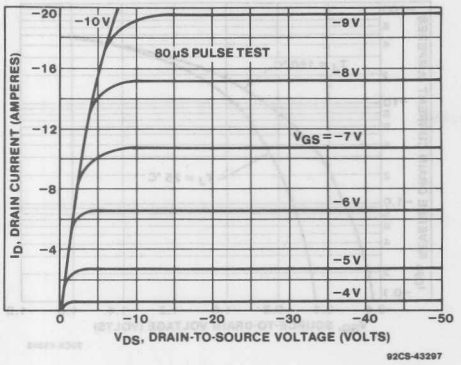


Fig. 1 - Typical Output Characteristics

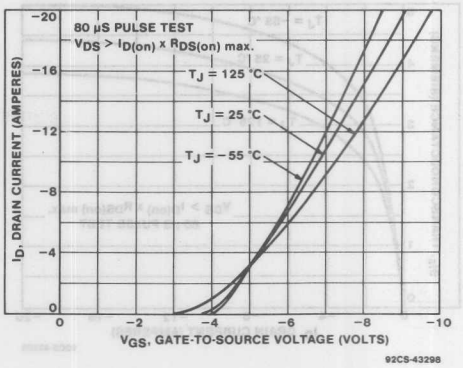


Fig. 2 - Typical Transfer Characteristics

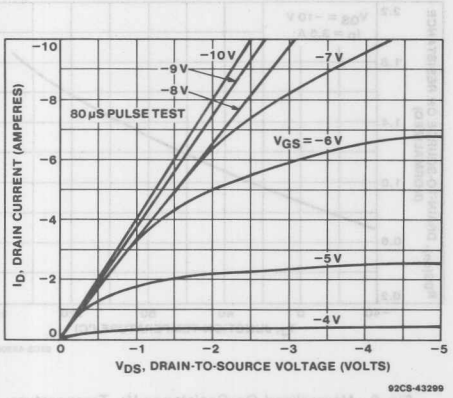


Fig. 3 - Typical Saturation Characteristics

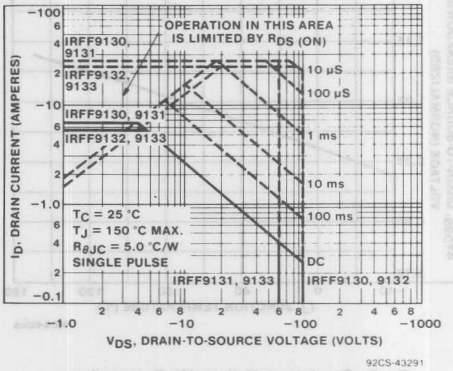


Fig. 4 - Maximum Safe Operating Area

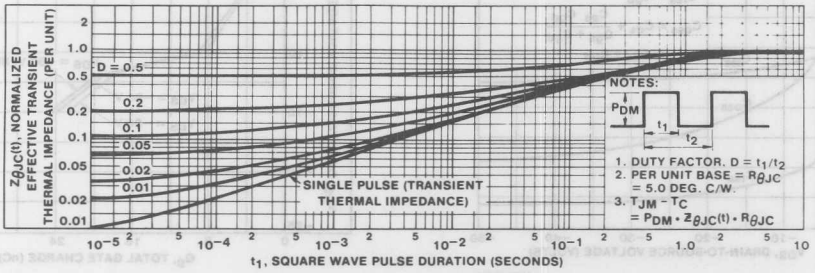


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

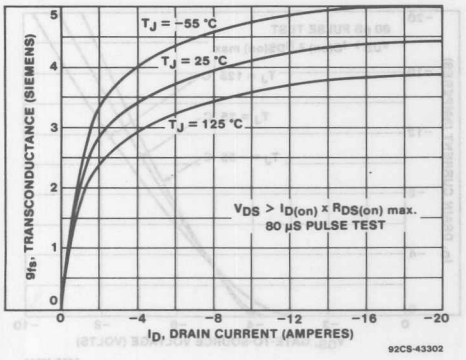


Fig. 6 - Typical Transconductance Vs. Drain Current

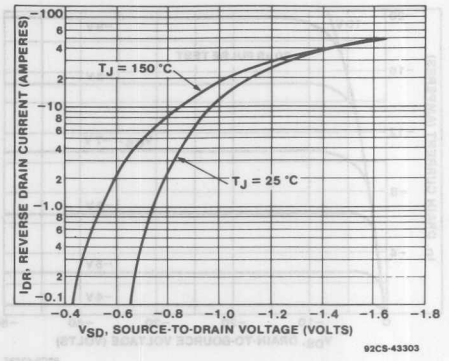


Fig. 7 - Typical Source-Drain Diode Forward Voltage

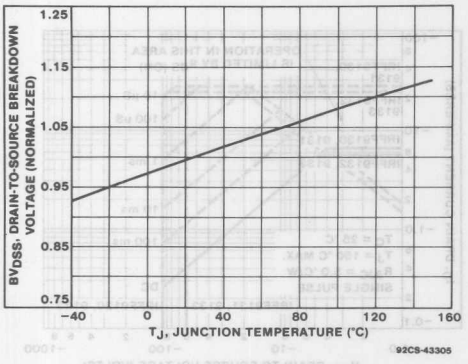


Fig. 8 - Breakdown Voltage Vs. Temperature

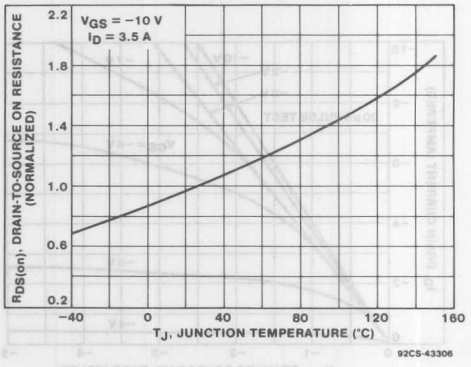


Fig. 9 - Normalized On-Resistance Vs. Temperature

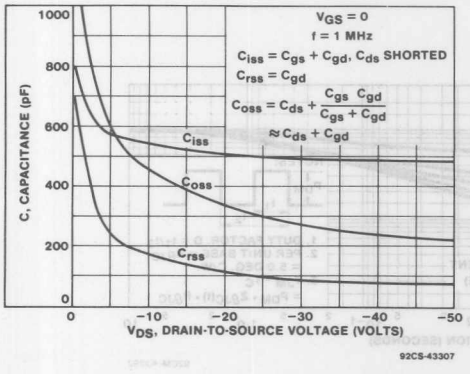


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

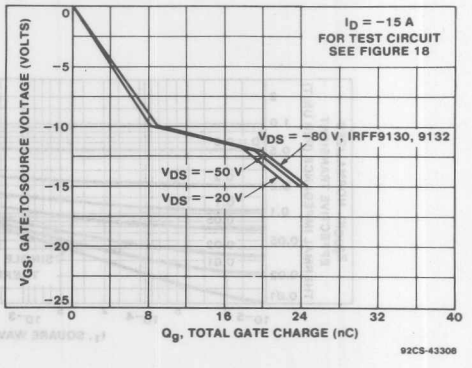


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

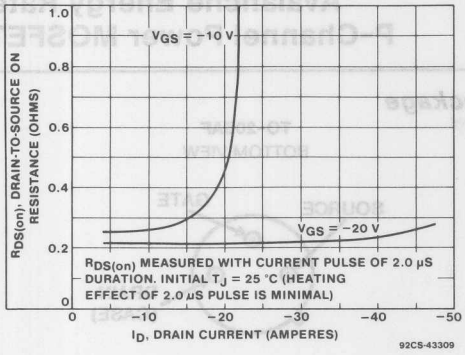


Fig. 12 - Typical On-Resistance Vs. Drain Current

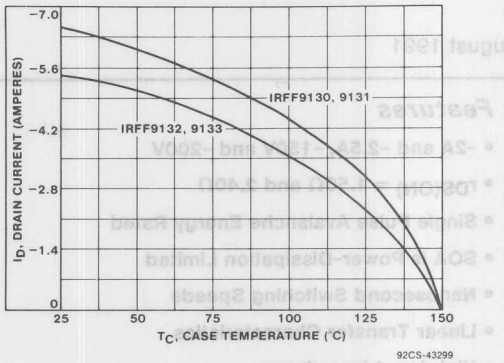


Fig. 13 - Maximum Drain Current Vs. Case Temperature

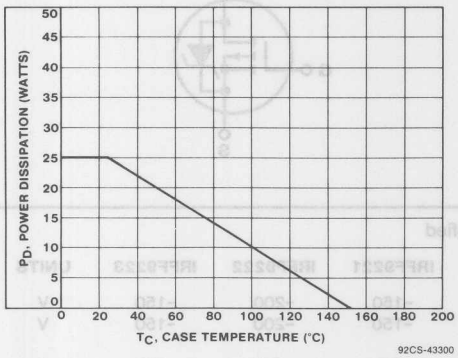


Fig. 14 - Power Vs. Temperature Derating Curve

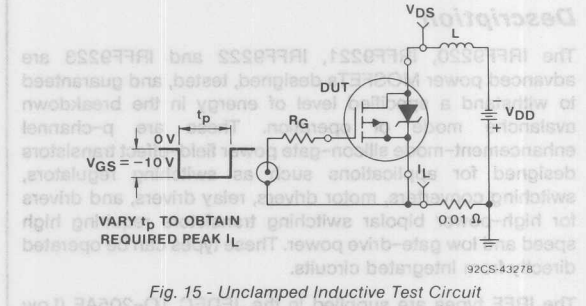


Fig. 15 - Unclamped Inductive Test Circuit

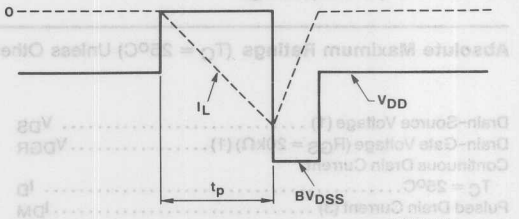


Fig. 16 - Unclamped Inductive Waveforms

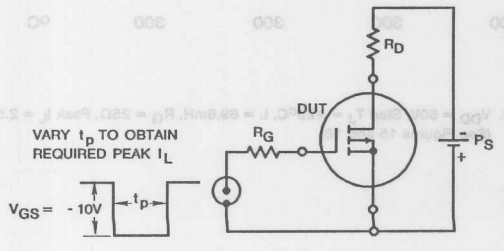


Fig. 17 - Switching Time Test Circuit

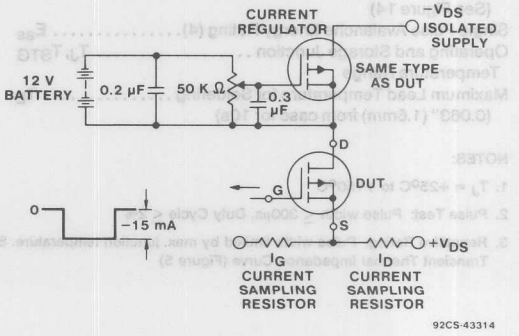


Fig. 18 - Gate Charge Test Circuit

HARRIS IRFF9220, IRFF9221 IRFF9222, IRFF9223

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -2A and -2.5A, -150V and -200V
- $r_{DS(ON)}$ = 1.50Ω and 2.40Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

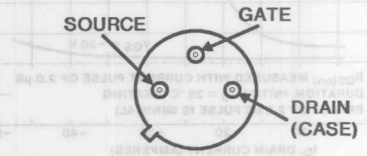
Description

The IRFF9220, IRFF9221, IRFF9222 and IRFF9223 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRFF9220	IRFF9221	IRFF9222	IRFF9223	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current T_C = 25°C ..... I_D	-2.5	-2.5	-2.0	-2.0	A
Pulsed Drain Current (3) ..... I_{DM}	-10	-10	-8	-8	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	20	20	20	20	W
Linear Derating Factor ..... (See Figure 14)	0.16	0.16	0.16	0.16	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	290	290	290	290	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

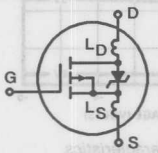
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 69.6mH, R_G = 25Ω, Peak I_L = 2.5A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

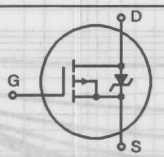
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File Number 2288

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF9220, IRFF9222	BV_{DSS}	V_{GS} = 0V, I_D = -250µA	-200	-	-	V
IRFF9221, IRFF9223			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250µA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	µA
On-State Drain Current (Note 2) IRFF9220, IRFF9221	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-2.5	-	-	A
IRFF9222, IRFF9223			-2.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF9220, IRFF9221	$r_{DS(ON)}$	V_{GS} = -10V, I_D = 1.5A	-	1.0	1.5	Ω
IRFF9222, IRFF9223			-	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.5A	1	1.8	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	350	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -2.5A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	15	40	ns
Rise Time	t_r		-	25	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	120	ns
Fall Time	t_f		-	50	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -2.5V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	22	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5mm (0.2") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5mm (0.2") from header to source bonding pad. 	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	6.25	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-2.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-10	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -2.5A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -2.5A, dI_F/dt = 100A/µs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -2.5A, dI_F/dt = 100A/µs	-	1.9	-	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 69.6mH, R_G = 25Ω, Peak I_L = 2.5A (See Figures 15 and 16)

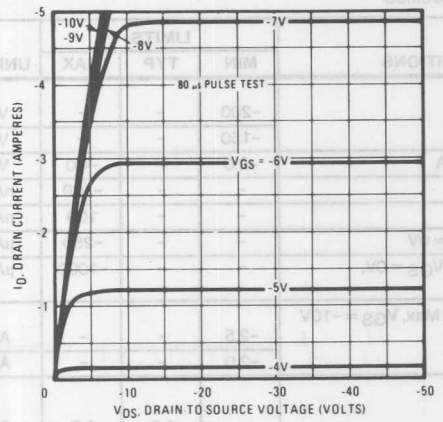


Fig. 1 - Typical output characteristics.

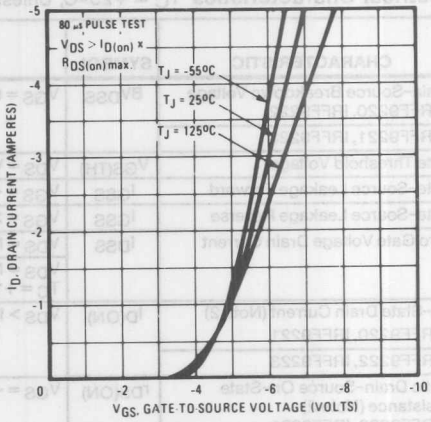


Fig. 2 - Typical transfer characteristics.

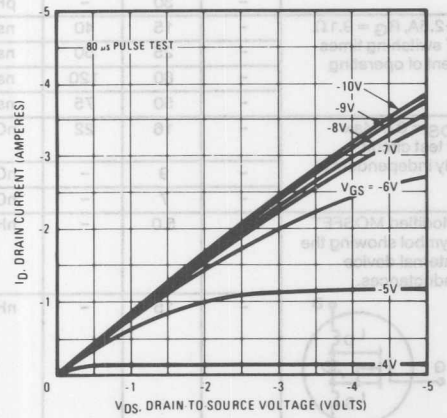


Fig. 3 - Typical saturation characteristics.

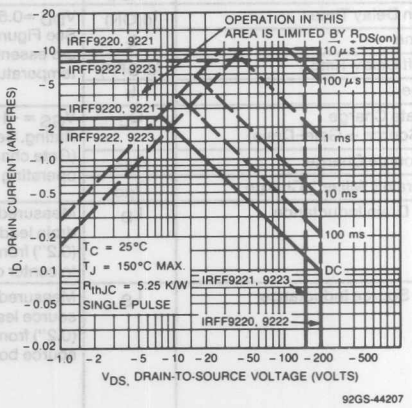


Fig. 4 - Maximum safe operating area.

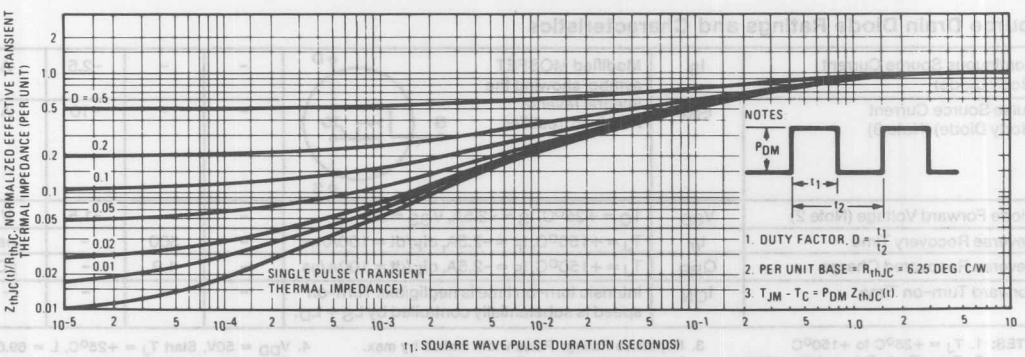


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

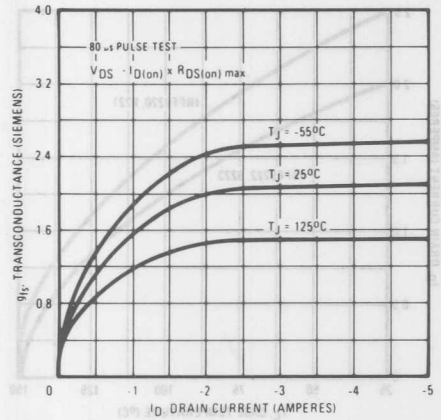


Fig. 6 - Typical transconductance vs. drain current.

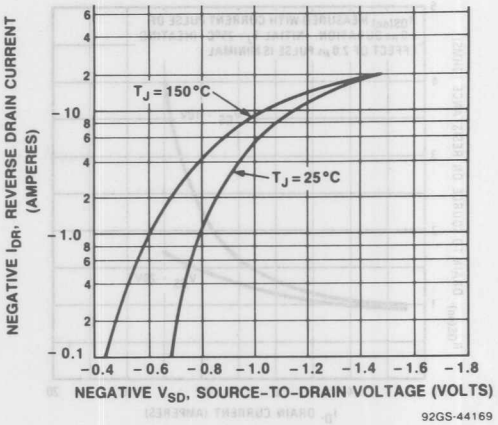


Fig. 7 - Typical source-drain diode forward voltage.

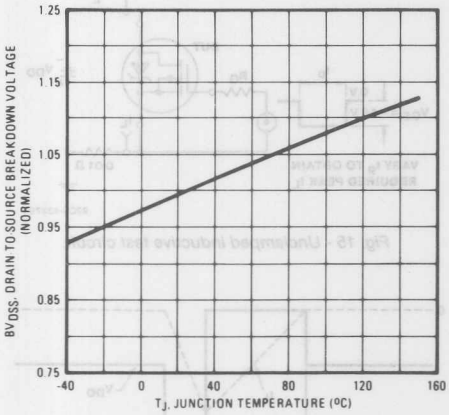


Fig. 8 - Breakdown voltage vs. temperature.

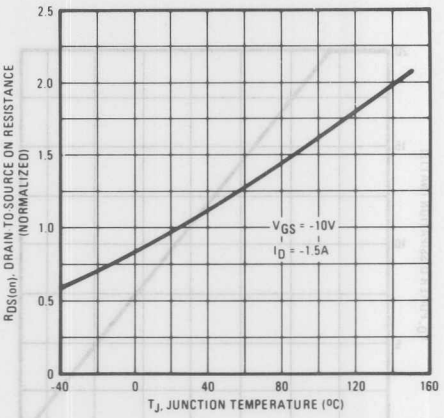


Fig. 9 - Normalized on-resistance vs. temperature.

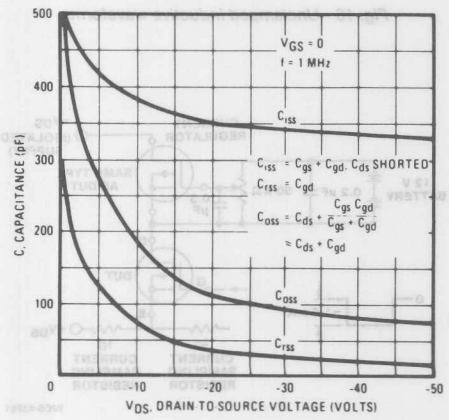


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

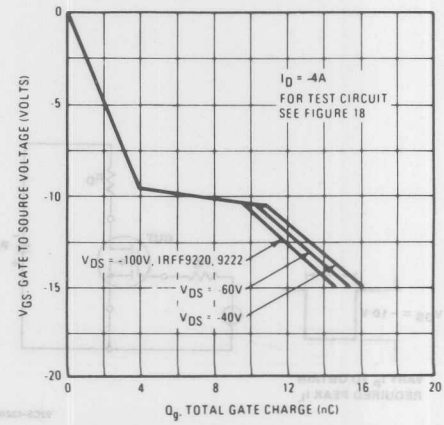


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

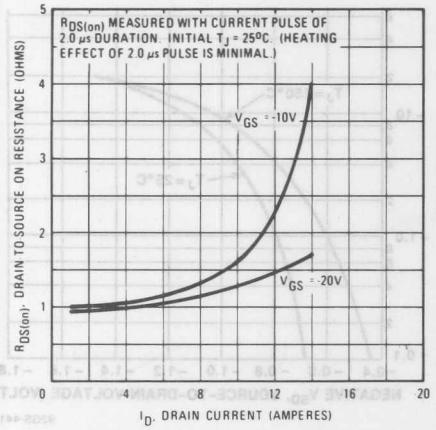


Fig. 12 - Typical on-resistance vs. drain current.

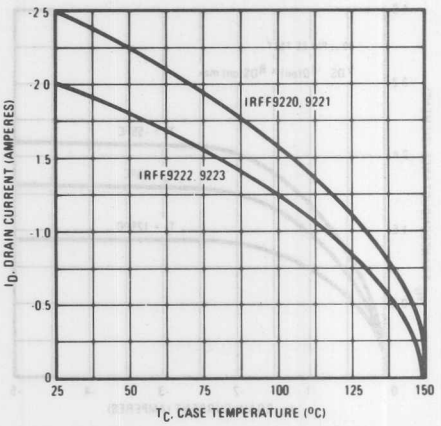


Fig. 13 - Maximum drain current vs. case temperature.

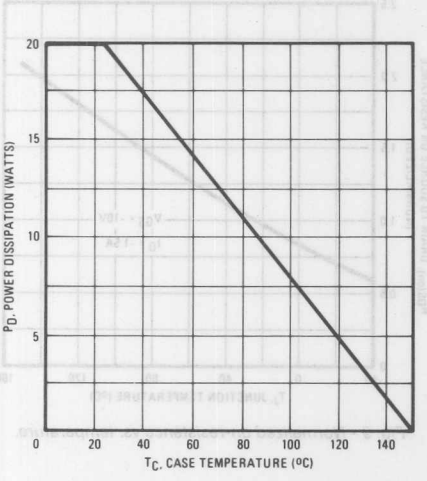


Fig. 14 - Power vs. temperature derating curve.

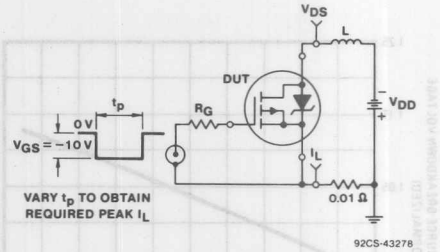


Fig. 15 - Unclamped inductive test circuit.

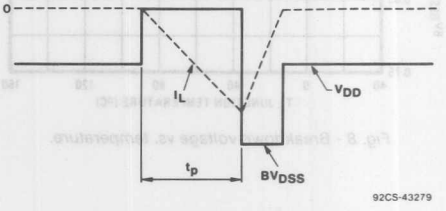


Fig. 16 - Unclamped inductive waveforms.

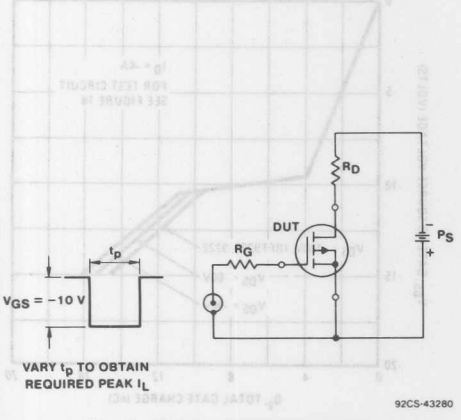


Fig. 17 - Switching time test circuit.

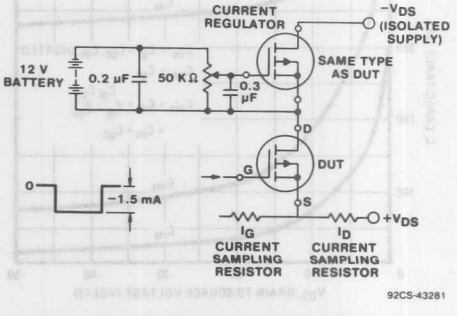


Fig. 18 - Gate charge test circuit.

HARRIS IRFF9230, IRFF9231 IRFF9232, IRFF9233

Avalanche Energy Rated P-Channel Power MOSFETs

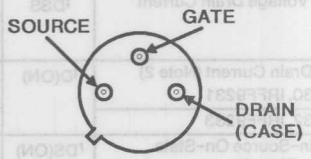
August 1991

Features

- -3.5A and -4.0A, -150V and -200V
- $r_{DS(ON)}$ = 0.8Ω and 1.20Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-205AF
BOTTOM VIEW



Description

The IRFF9230, IRFF9231, IRFF9232 and IRFF9233 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



5 P-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFF9230	IRFF9231	IRFF9232	IRFF9233	UNITS
Drain-Source Voltage (1)	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current T_C = 25°C	I_D	-4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current (3)	I_{DM}	-16	-16	-14	-14	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation (See Figure 14)	P_D	25	25	25	25	W
Linear Derating Factor (See Figure 14)		0.2	0.2	0.2	0.2	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	500	500	500	500	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

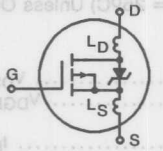
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 46.9mH, R_G = 25Ω, Peak I_L = 4.0A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

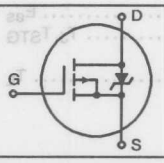
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File Number 2225

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF9230, IRFF9232	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRFF9231, IRFF9233			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFF9230, IRFF9231	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-4.0	-	-	A
IRFF9232, IRFF9233			-3.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF9230, IRFF9231	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -2.0A	-	0.5	0.8	Ω
IRFF9232, IRFF9233			-	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{ts}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -2.0A	2.2	3.5	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	550	-	pF
Output Capacitance	C_{OSS}		-	170	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -4.0A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	40	80	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -4.0V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	31	45	nC
Gate-Source Charge	Q_{gs}		-	18	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	13	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5mm (0.2") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5mm (0.2") from header to source bonding pad. 	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-4.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-16	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -4.0A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -4.0A, dI_F/dt = 100A/μs	-	400	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -4.0A, dI_F/dt = 100A/μs	-	2.6	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 46.9mH, R_G = 25Ω, Peak I_L = 4.0A (See Figures 15 and 16)

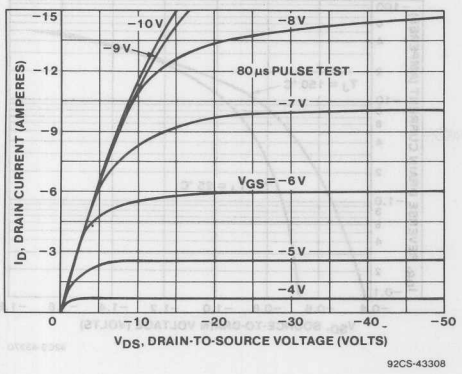


Fig. 1 - Typical output characteristics.

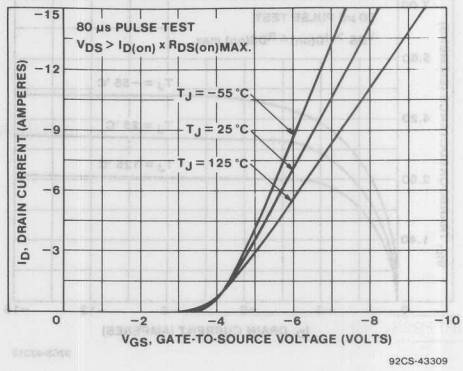


Fig. 2 - Typical transfer characteristics.

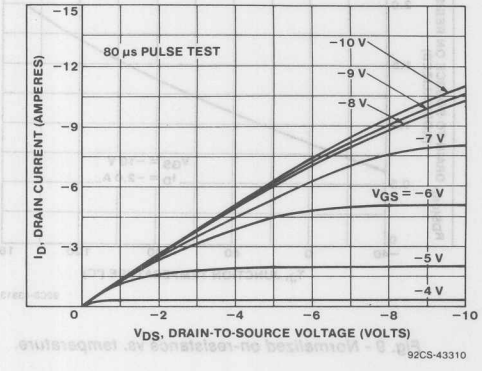


Fig. 3 - Typical saturation characteristics.

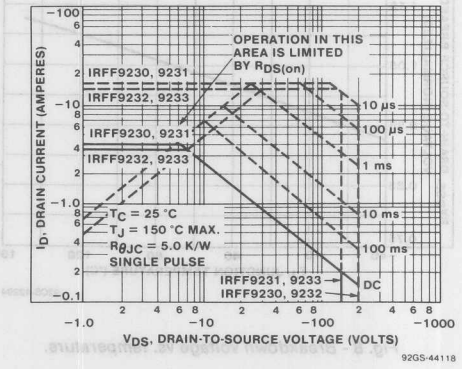


Fig. 4 - Maximum safe operating area.

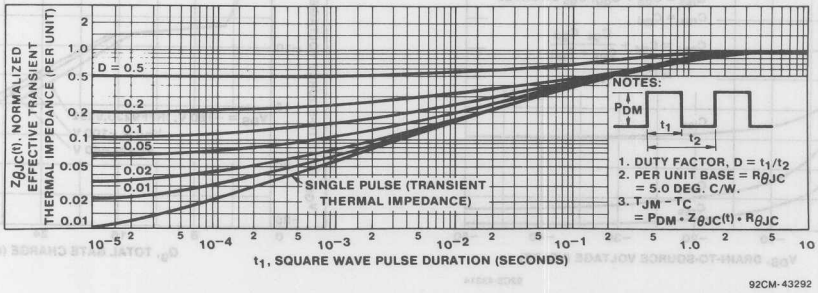


Fig. 5 - Maximum effective transient thermal impedance, junction-

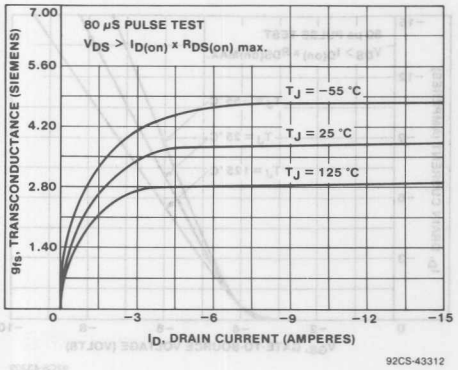


Fig. 6 - Typical transconductance vs. drain current.

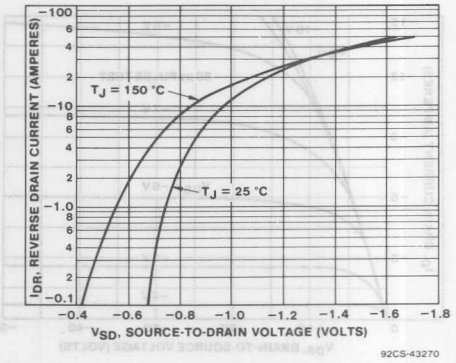


Fig. 7 - Typical source-drain diode forward voltage.

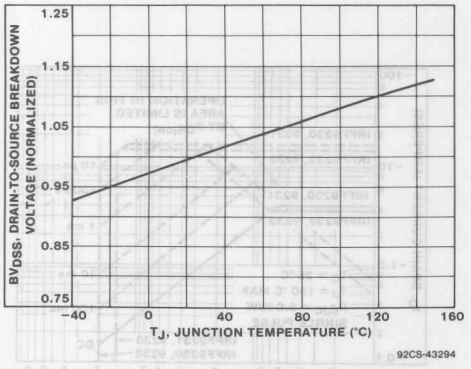


Fig. 8 - Breakdown voltage vs. temperature.

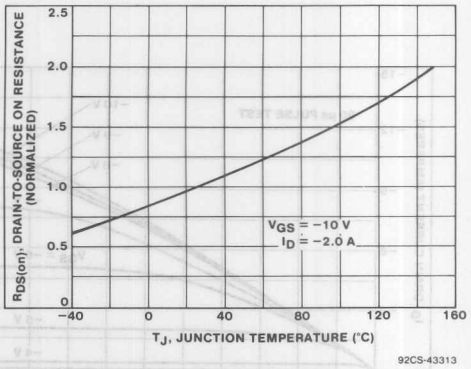


Fig. 9 - Normalized on-resistance vs. temperature.

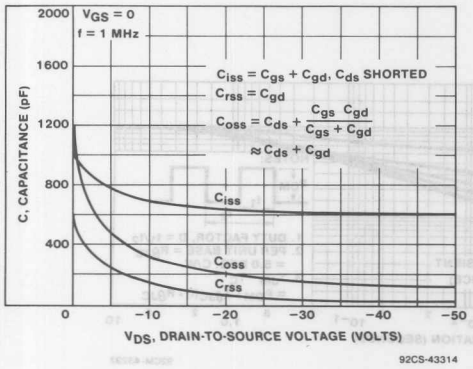


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

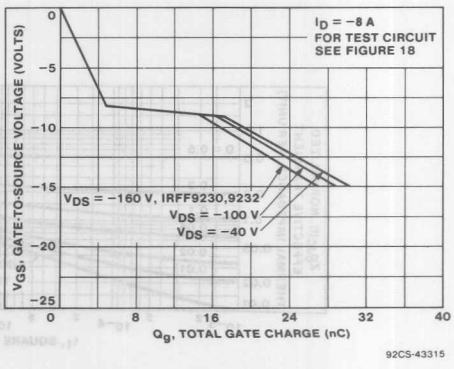


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

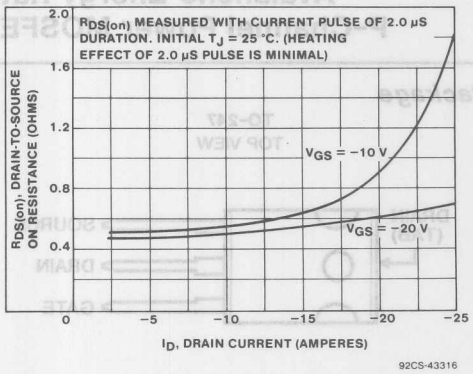


Fig. 12 - Typical on-resistance vs. drain current.

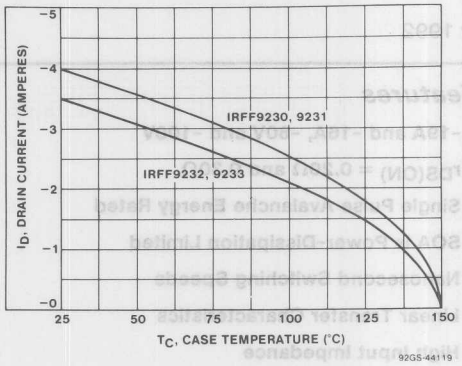


Fig. 13 - Maximum drain current vs. case temperature.

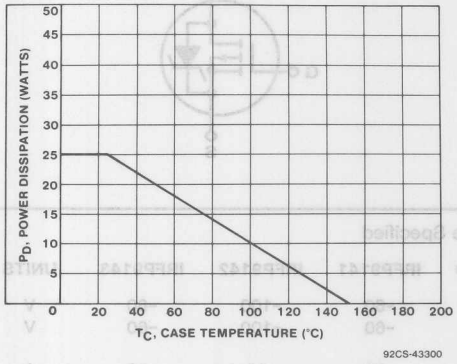


Fig. 14 - Power vs. temperature derating curve.

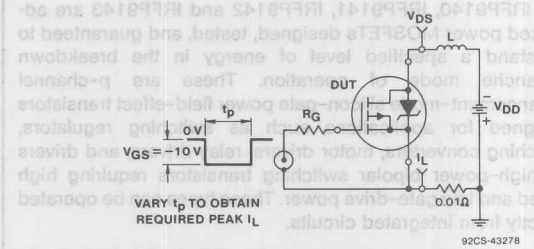


Fig. 15 - Unclamped inductive test circuit.

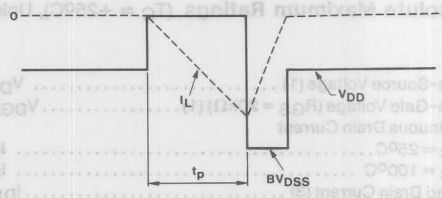


Fig. 16 - Unclamped inductive waveforms.

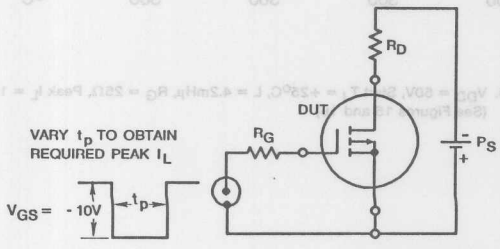


Fig. 17 - Switching time test circuit.

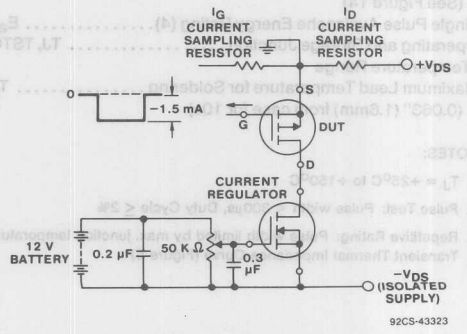


Fig. 18 - Gate charge test circuit.

HARRIS

IRFP9140/P9141
IRFP9142/P9143

Avalanche Energy Rated P-Channel Power MOSFETs

May 1992

Features

- -19A and -16A, -60V and -100V
- $r_{DS(ON)}$ = 0.20Ω and 0.30Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

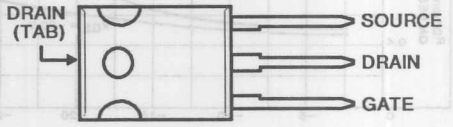
Description

The IRFP9140, IRFP9141, IRFP9142 and IRFP9143 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

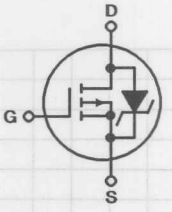
Package

TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP9140	IRFP9141	IRFP9142	IRFP9143	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-60	-100	-60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-60	-100	-60	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-19	-19	-16	-16	A
T_C = 100°C ..... I_D	-12	-12	-10	-10	A
Pulsed Drain Current (3) ..... I_{DM}	-76	-76	-64	-64	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	150	150	150	150	W
Linear Derating Factor ..... (See Figure 14)	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	960	960	960	960	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

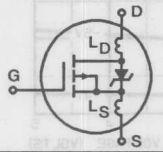
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.2mHμ, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

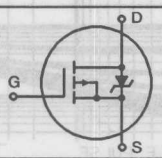
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File Number 2292.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP9140, IRFP9142	BV_{DSS}	V_{GS} = 0V, I_D = -250µA	-100	-	-	V
IRFP9141, IRFP9143			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = -250µA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRFP9140, IRFP9141	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = -10V	-19	-	-	A
IRFP9142, IRFP9143			-16	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP9140, IRFP9141	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	-	0.14	0.20	Ω
IRFP9142, IRFP9143			-	0.20	0.30	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \leq$ -50V, I_D = -10A	5.3	7.9	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	1200	-	pF
Output Capacitance	C_{OSS}		-	570	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	160	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = -50V, I_D = -19A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	16	20	ns
Rise Time	t_r		-	65	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	47	70	ns
Fall Time	t_f		-	28	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -19A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	37	55	nC
Gate-Source Charge	Q_{gs}		-	8.7	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	22	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad. 	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-19	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-76	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = -19A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = -18A, dI_F/dt = 100A/µs	-	210	-	ns
Reverse Recovered Charge	Q_{RR}		-	2.0	-	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.2mHµ, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

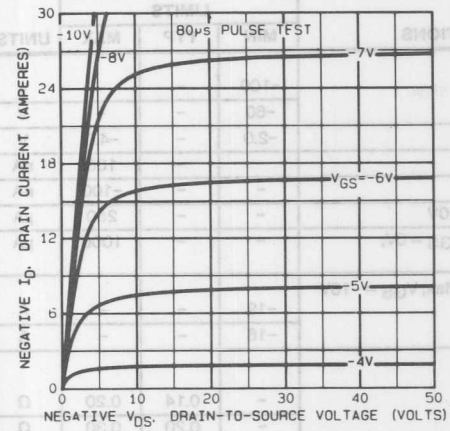


Fig. 1 – Typical output characteristics.

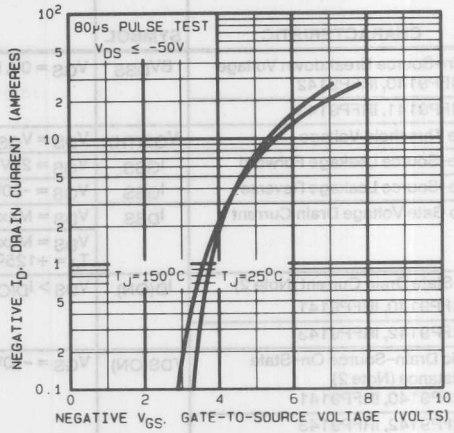


Fig. 2 – Typical transfer characteristics.

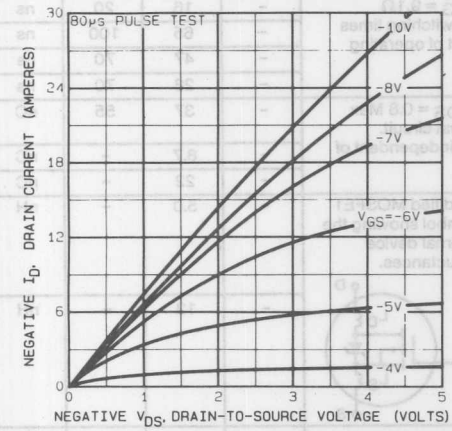


Fig. 3 – Typical saturation characteristics.

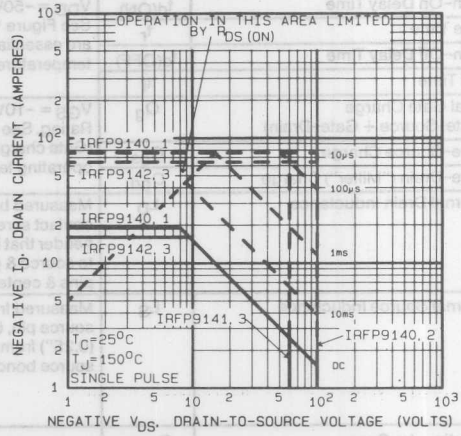


Fig. 4 – Maximum safe operating area.

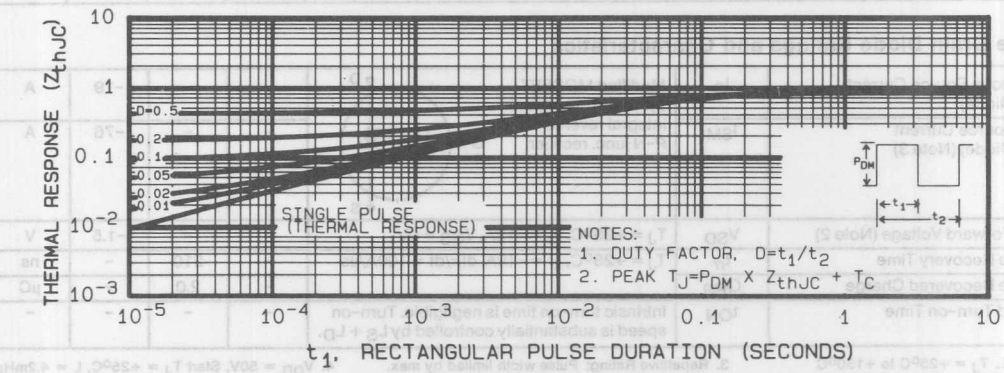


Fig. 5 – Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

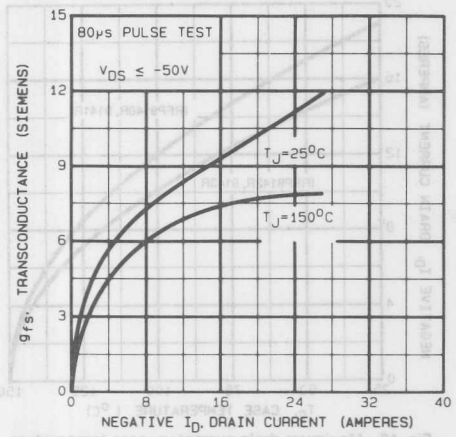


Fig. 6 - Typical transconductance vs. drain current.

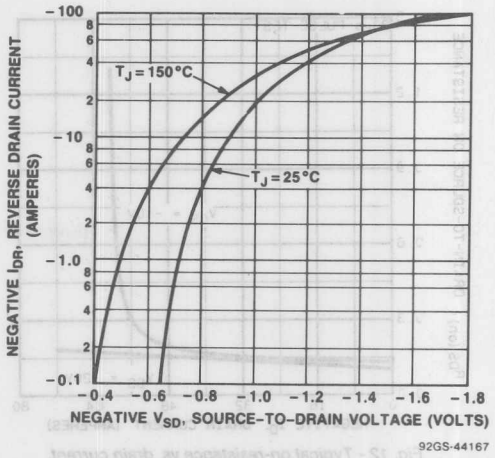


Fig. 7 - Typical source-drain diode forward voltage.

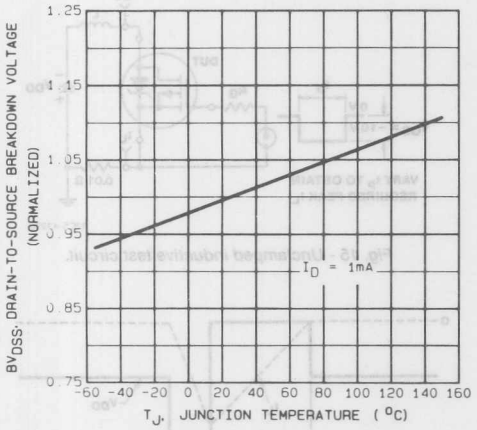


Fig. 8 - Breakdown voltage vs. temperature.

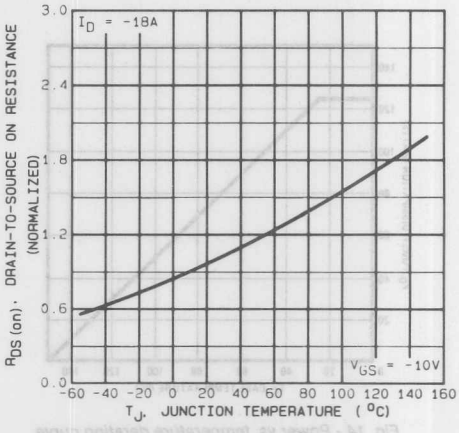


Fig. 9 - Normalized on-resistance vs. temperature.

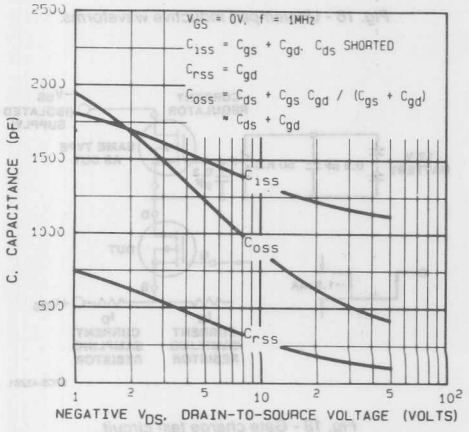


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

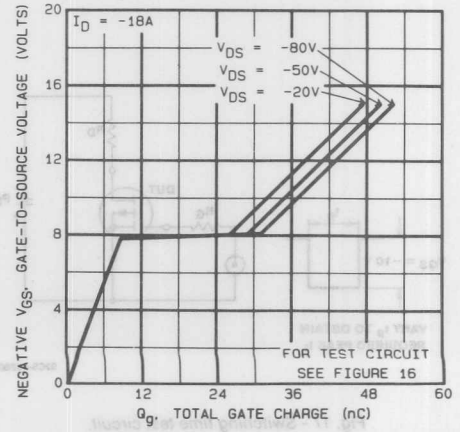


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

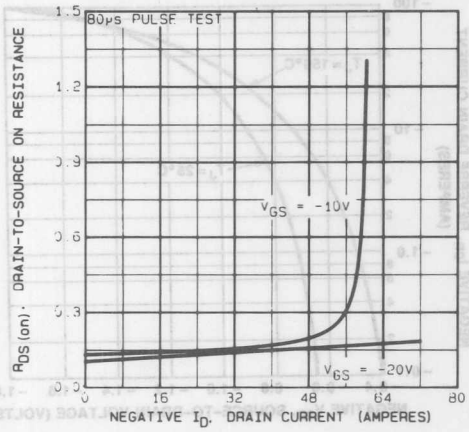


Fig. 12 - Typical on-resistance vs. drain current.

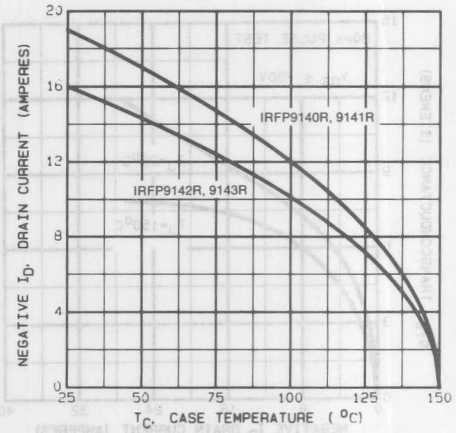


Fig. 13 - Maximum drain current vs. case temperature.

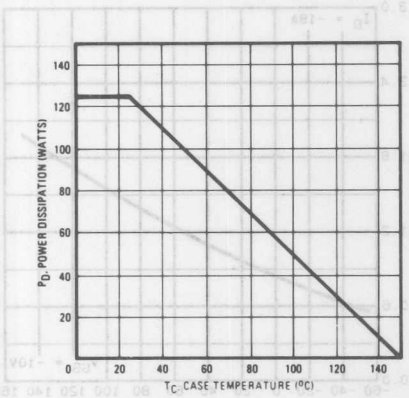


Fig. 14 - Power vs. temperature derating curve.

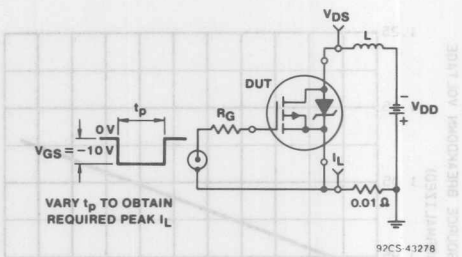


Fig. 15 - Unclamped inductive test circuit.

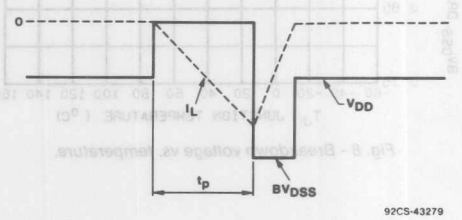


Fig. 16 - Unclamped inductive waveforms.

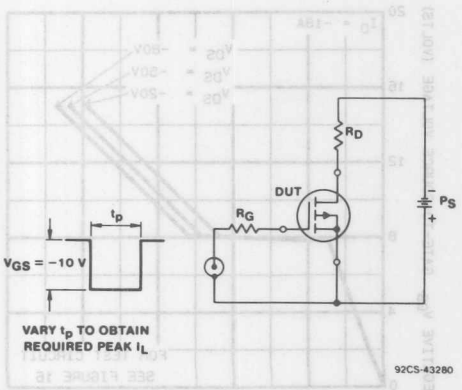


Fig. 17 - Switching time test circuit.

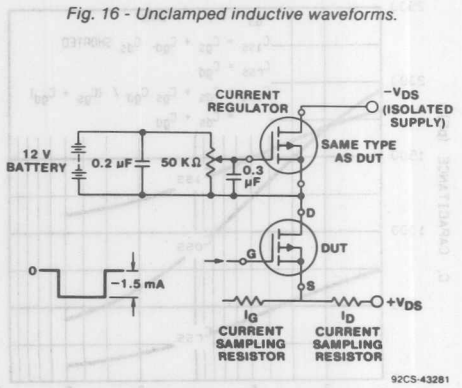


Fig. 18 - Gate charge test circuit.

HARRIS

IRFP9150
IRFP9151

Avalanche Energy Rated P-Channel Power MOSFETs

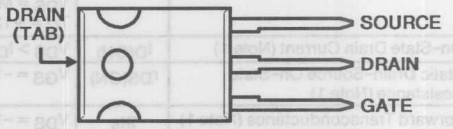
August 1991

Features

- -25A, -60V and -100V
- $r_{DS(ON)} = 0.150\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-247
TOP VIEW



Description

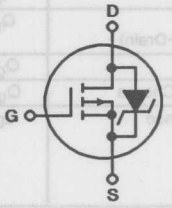
The IRFP9150 and IRFP9151 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The P-channel IRFP9150 is an approximate electrical complement to the N-channel IRF9150.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



5
P-CHANNEL POWER MOSFETs

Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

		IRFP9150	IRFP9151	UNITS
Drain-Source Voltage	V_{DS}	-100	-60	V
Continuous Drain Current				
$T_C = 25^oC$	I_D	-25	-25	A
$T_C = 100^oC$	I_D	-18	-18	A
Pulsed Drain Current	I_{DM}	-100	-100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation (See Figure 18)	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/^{o}C
Single Pulse Avalanche Energy Rating (3) (See Figure 14)	E_{as}	1300	1300	mJ
Avalanche Current (Repetitive or Nonrepetitive)	I_{AR}	-25	-25	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^{o}C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	^{o}C

NOTES:

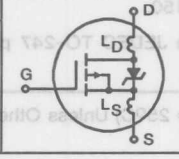
1. Pulse Test: Pulse width $\leq$ 300μs, Duty Cycle $\leq$ 2%
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 25V, Start T_J = +25°C, L = 3.2mhy, $R_G = 25\Omega$, Peak I_L = 25A (See Figures 14 and 15)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

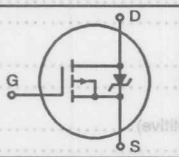
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File Number 2293

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP9150	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRFP9151			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 1)	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	-25	-	-	A
Static Drain-Source On-State Resistance (Note 1)	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	-	0.09	0.15	Ω
Forward Transconductance (Note 1)	g_{fs}	V_{DS} = -10V, I_D = -12.5A	4	10	-	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	2400	-	pF
Output Capacitance	C_{OSS}		-	850	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	400	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = -50V, I_D = -25A, R_G = 6.8Ω, R_D = 2Ω. See Figures 16 and 17. (MOSFET switching times are essentially independent of operating temperature.)	-	16	24	ns
Rise Time	t_r		-	110	160	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	65	100	ns
Fall Time	t_f		-	46	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -25A, V_{DS} = 0.8 Max Rating. See Figures 11 & 19 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	82	120	nC
Gate-Source Charge	Q_{gs}		-	14	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	42	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-25	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-100	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 25A, V_{GS} = 0V	-	-0.9	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	-	150	300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	0.3	0.7	1.5	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)

3. V_{DD} = 25V, Start T_J = +25°C, L = 3.2mhy, R_G = 25Ω, Peak I_L = 25A (See Figures 14 and 15)

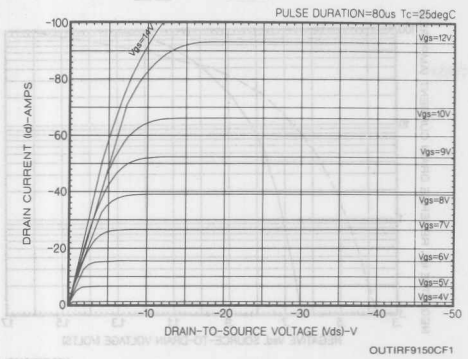


Fig. 1 - Typical output characteristics.

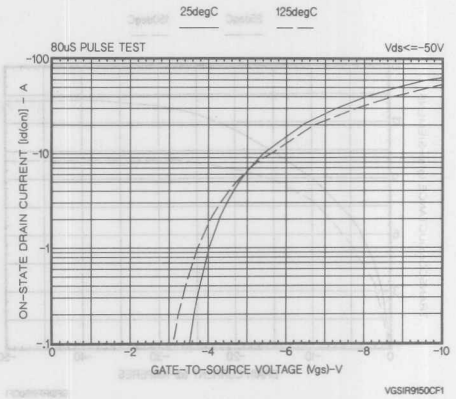


Fig. 2 - Typical transfer characteristics.

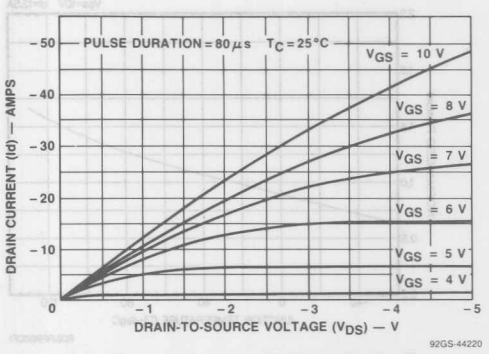


Fig. 3- Typical saturation characteristics.

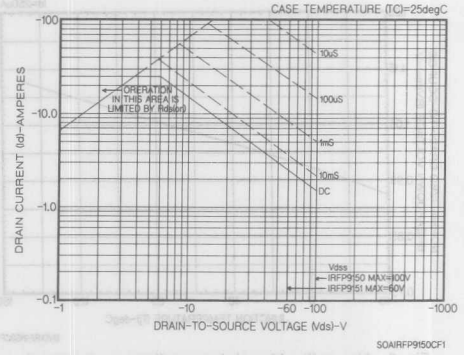


Fig. 4 - Maximum safe operating area.

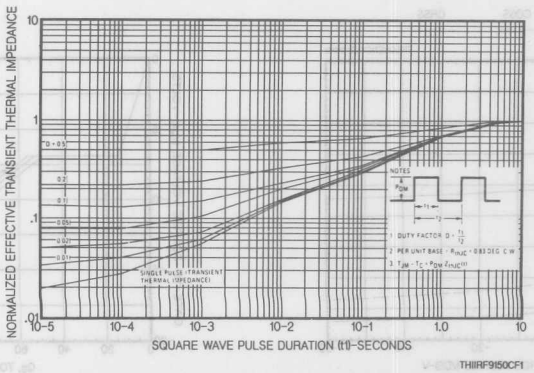


Fig. 5 - Maximum effective transient thermal impedance.

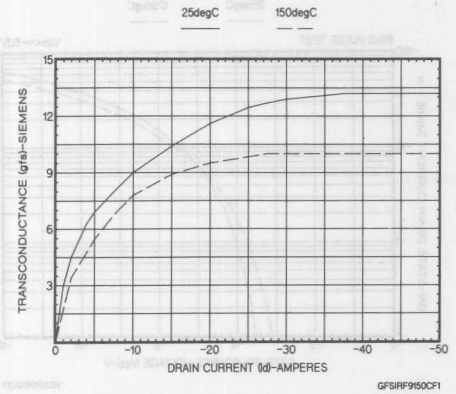


Fig. 6 - Typical transconductance vs. drain current.

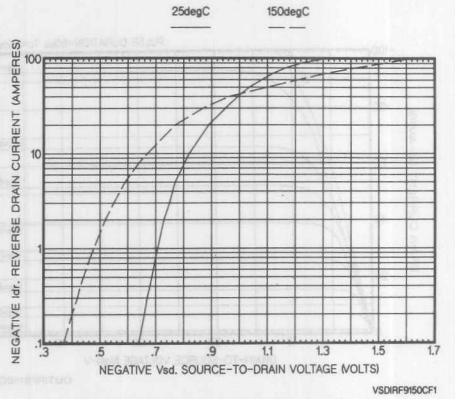


Fig. 7 - Typical source-drain diode forward voltage.

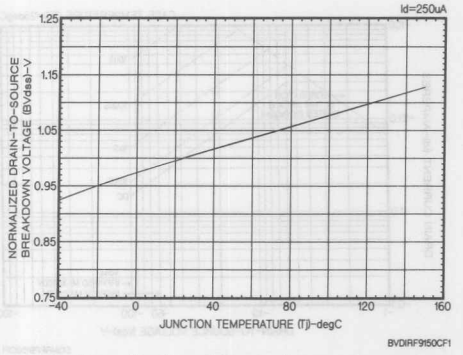


Fig. 8 - Normalized breakdown voltage vs. temperature.

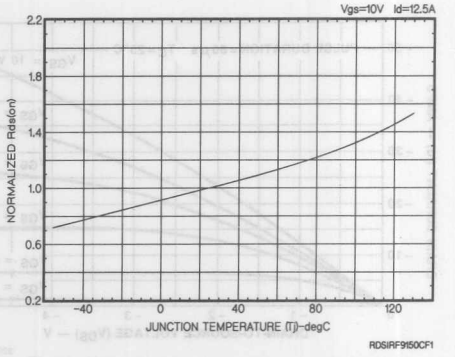


Fig. 9 - Normalized on-resistance vs. temperature.

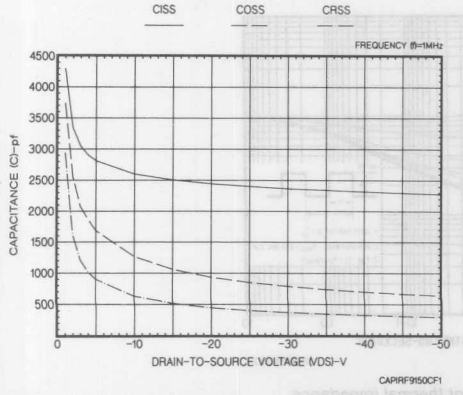


Fig. 10 - Typical capacitance vs. drain-to source voltage.

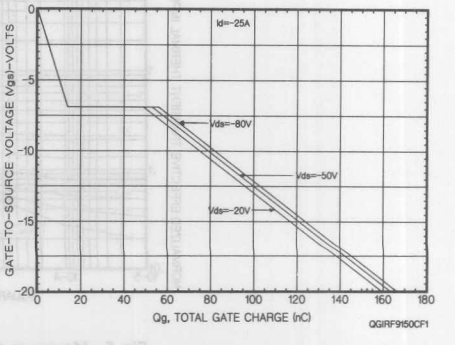


Fig. 11 - Typical gate charge vs. gate-to source voltage.

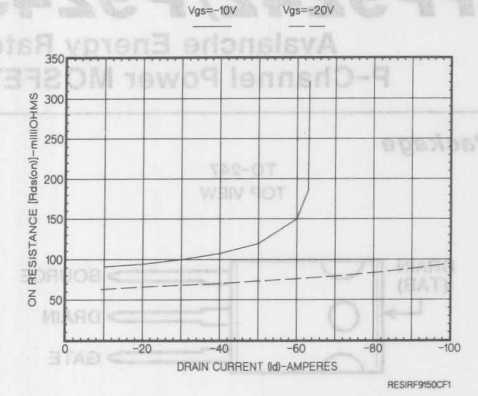


Fig. 12 - Typical on-resistance vs. drain current.

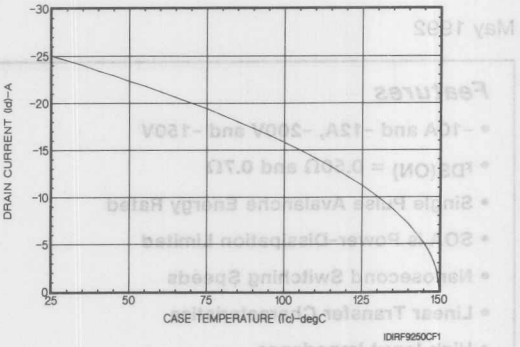


Fig. 13 - Maximum drain current vs. case temperature.

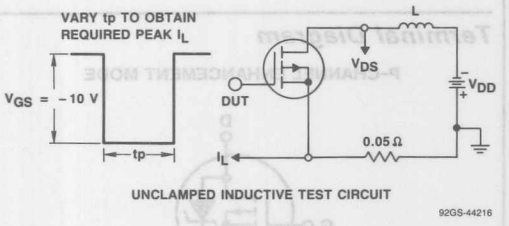


Fig. 14 - Unclamped inductive test circuit.

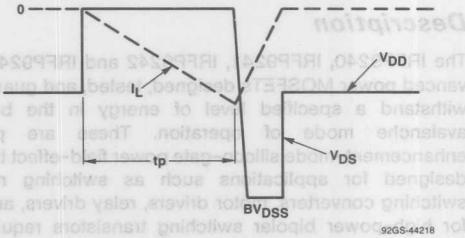


Fig. 15 - Unclamped inductive waveforms.

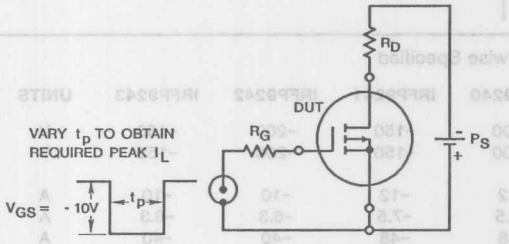


Fig. 16 - Switching time test circuit.

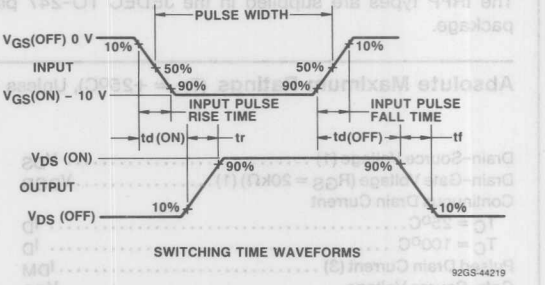


Fig. 17 - Switching time waveforms.

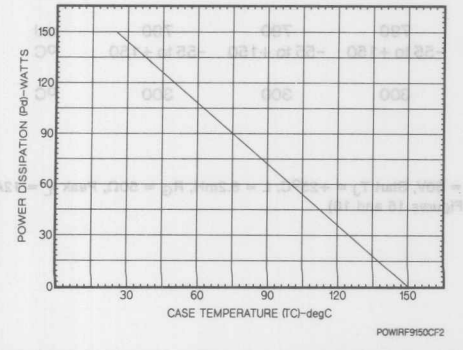


Fig. 18 - Power vs. temperature derating curve.

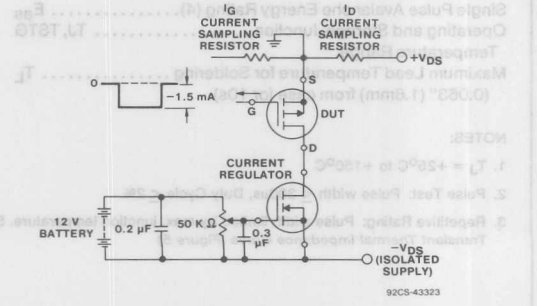


Fig. 19 - Gate charge test circuit.

HARRIS

IRFP9240/P9241
IRFP9242/P9243

Avalanche Energy Rated P-Channel Power MOSFETs

May 1992

Features

- -10A and -12A, -200V and -150V
- $r_{DS(ON)}$ = 0.50Ω and 0.7Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

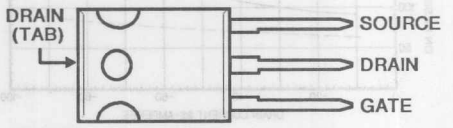
Description

The IRFP9240, IRFP9241, IRFP9242 and IRFP9243 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

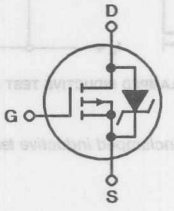
Package

TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP9240	IRFP9241	IRFP9242	IRFP9243	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-12	-12	-10	-10	A
T_C = 100°C ..... I_D	-7.5	-7.5	-6.3	-6.3	A
Pulsed Drain Current (3) ..... I_{DM}	-48	-48	-40	-40	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	150	150	150	150	W
Linear Derating Factor ..... (See Figure 14)	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	790	790	790	790	mJ
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

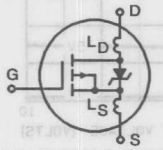
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 8.2mH, R_G = 50Ω, Peak I_L = 12A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

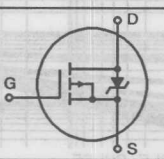
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File Number 2294.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP9240, IRFP9242	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRFP9241, IRFP9243			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFP9240, IRFP9241	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = -10V	-12	-	-	A
IRFP9242, IRFP9243			-10	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP9240, IRFP9241	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -6.3A	-	0.38	0.50	Ω
IRFP9242, IRFP9243			-	0.50	0.70	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \leq$ -50V, I_D = -6.3A	3.8	5.7	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	1400	-	pF
Output Capacitance	C_{OSS}		-	350	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	140	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = -100V, I_D = -12A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	18	22	ns
Rise Time	t_r		-	45	68	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	75	90	ns
Fall Time	t_f		-	29	44	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -12A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	38	57	nC
Gate-Source Charge	Q_{gs}		-	8.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	21	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-12	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-48	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = -12A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = -11A, dI_F/dt = 100A/μs	-	210	-	ns
Reverse Recovered Charge	Q_{RR}		-	2.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 8.2mHμ, R_G = 50Ω, Peak I_L = 12A (See Figures 15 and 16)

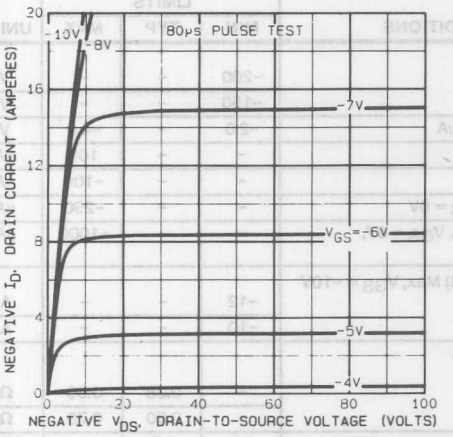


Fig. 1 - Typical output characteristics.

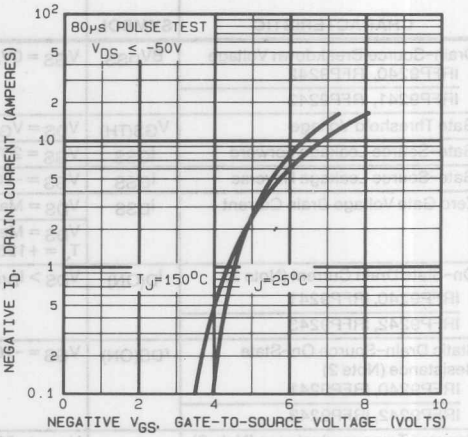


Fig. 2 - Typical transfer characteristics.

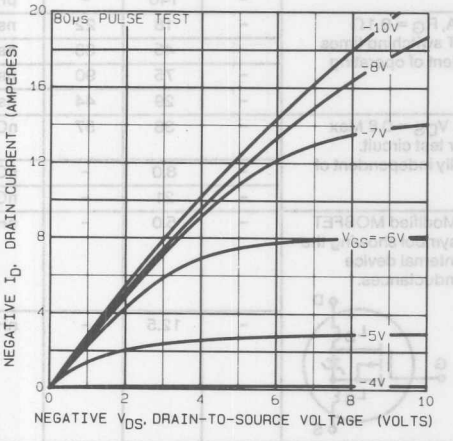


Fig. 3 - Typical saturation characteristics.

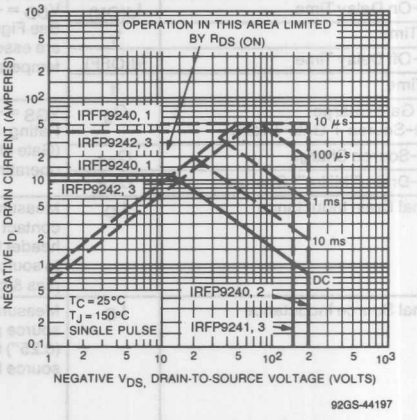


Fig. 4 - Maximum safe operating area.

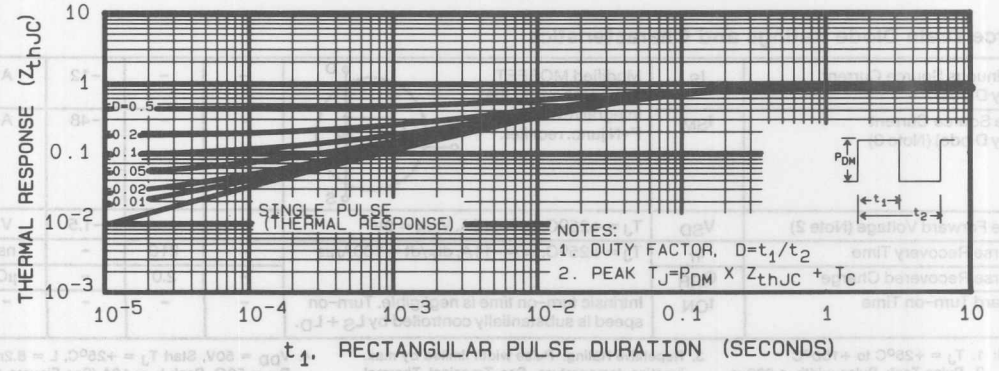


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

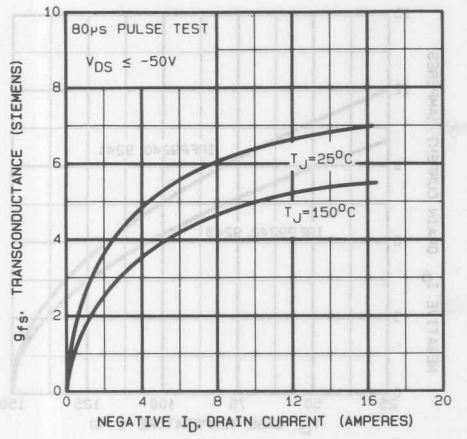


Fig. 6 - Typical transconductance vs. drain current.

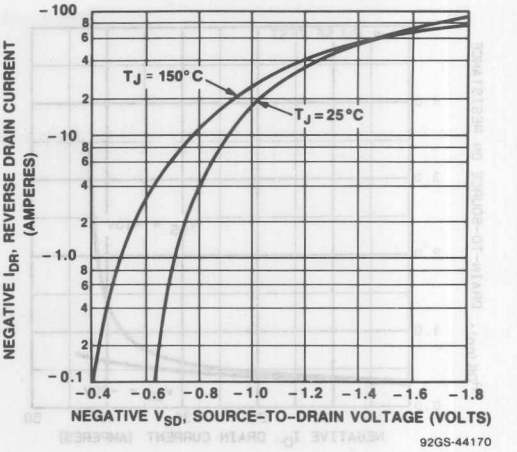


Fig. 7 - Typical source-drain diode forward voltage.

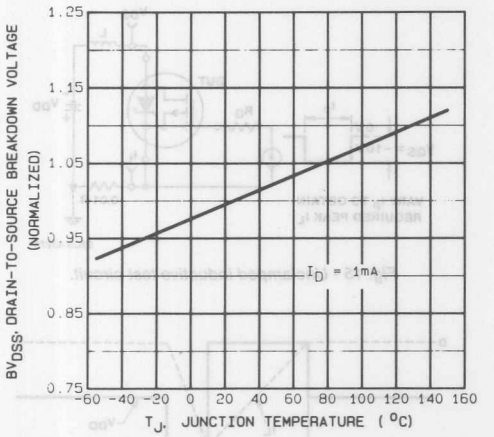


Fig. 8 - Breakdown voltage vs. temperature.

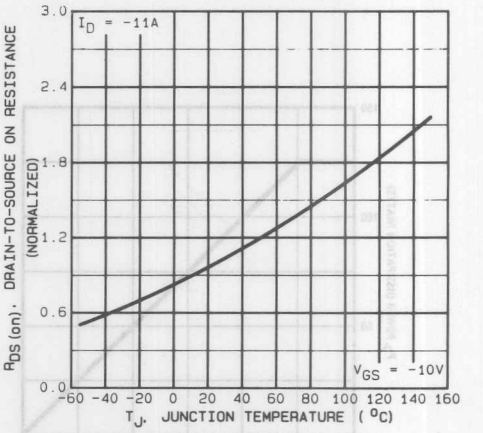


Fig. 9 - Normalized on-resistance vs. temperature.

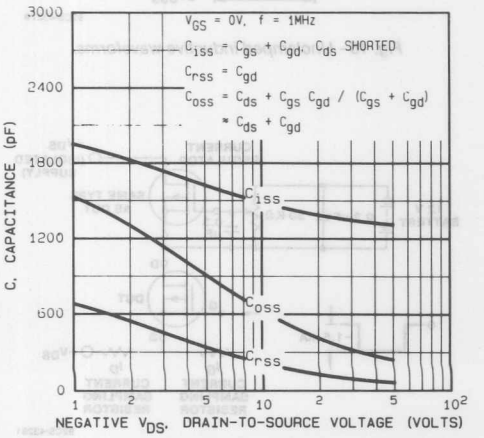


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

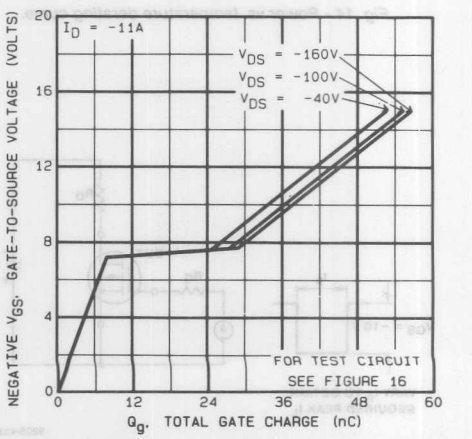


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

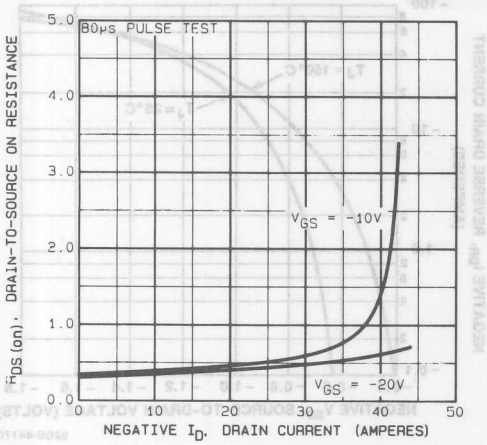


Fig. 12 - Typical on-resistance vs. drain current.

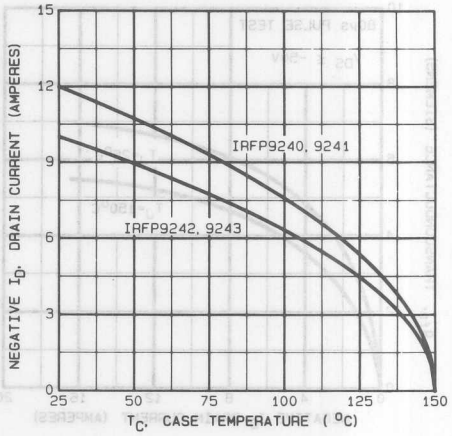


Fig. 13 - Maximum drain current vs. case temperature.

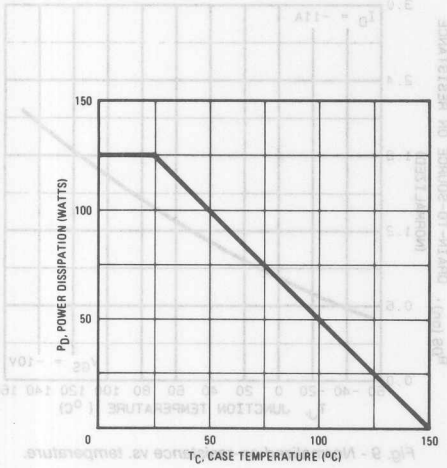


Fig. 14 - Power vs. temperature derating curve.

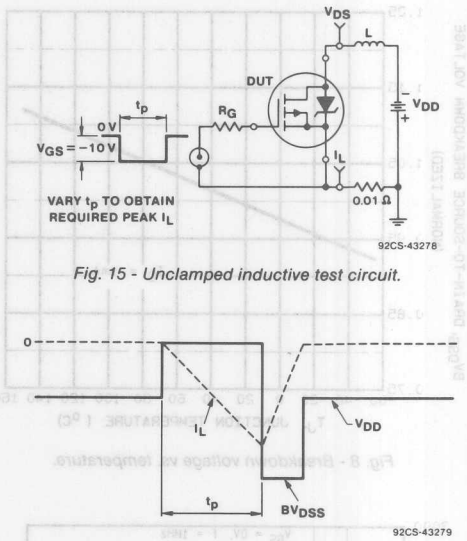


Fig. 15 - Unclamped inductive test circuit.

Fig. 16 - Unclamped inductive waveforms.

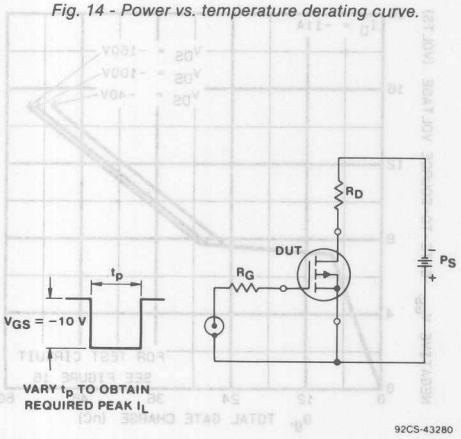


Fig. 17 - Switching time test circuit.

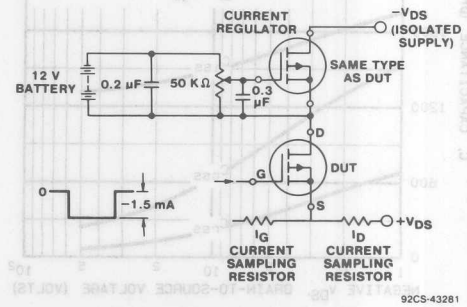


Fig. 18 - Gate charge test circuit.

HARRIS

RFL1P08
RFL1P10

P-Channel Enhancement-Mode Power Field-Effect Transistors

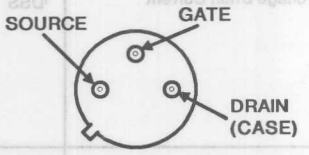
August 1991

Features

- 1A, -80V and -100V
- $r_{DS(ON)} = 3.65\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-205AF
BOTTOM VIEW



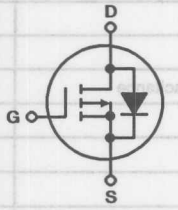
Description

The RFL1P08 and RFL1P10 are P-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL series types are supplied in the JEDEC TO-205AF metal package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

		RFL1P08	RFL1P10	UNITS
Drain-Source Voltage	V_{DS}	-80	-100	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$)	V_{DGR}	-80	-100	V
Continuous Drain Current				
RMS Continuous	I_D	1	1	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	8.33	8.33	W
Above $T_C = +25^oC$, Derate Linearly		0.0667	0.0667	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1535.1**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL1P08 MIN	LIMITS RFL1P08 MAX	LIMITS RFL1P10 MIN	LIMITS RFL1P10 MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	-80	-	-100	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -65V	-	-1	-	-	μA
		V_{DS} = -80V	-	-	-	-1	μA
		T_C = +125°C, V_{DS} = -65V	-	-50	-	-	μA
		V_{DS} = -80V	-	-	-	-50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	-	±100	-	±100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = -10V	-	-3.65	-	-3.65	V
		I_D = 2A, V_{GS} = -10V	-	-9.3	-	-9.3	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = -10V	-	3.65	-	3.65	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = -10V	200	-	200	-	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1MHz	-	150	-	150	pF
Output Capacitance	C_{OSS}		-	80	-	80	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	30	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = -50V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = -10V	7 (typ)	25	7 (typ)	25	ns
Rise Time	t_r		15 (typ)	45	15 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		14 (typ)	45	14 (typ)	45	ns
Fall Time	t_f		11 (typ)	25	11 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	15	-	15	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL1P08 MIN	LIMITS RFL1P08 MAX	LIMITS RFL1P10 MIN	LIMITS RFL1P10 MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	-	-1.4	-	-1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	-	135 (typ)	-	135 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

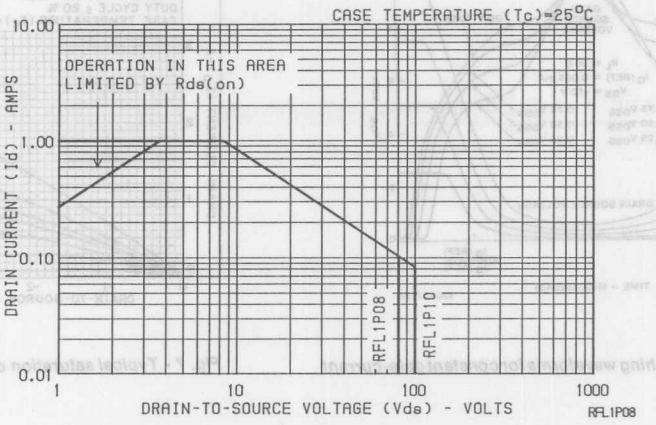


Fig. 1 - Maximum operating areas for all types.

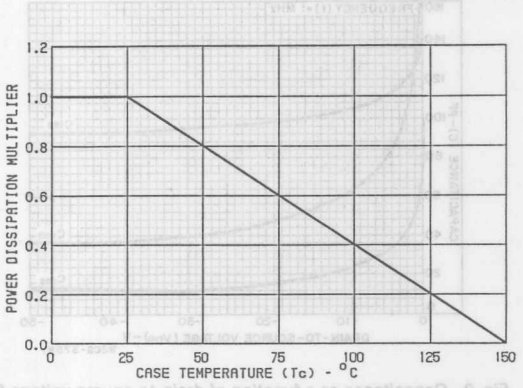


Fig. 2 – Normalized power dissipation vs temperature derating curve.

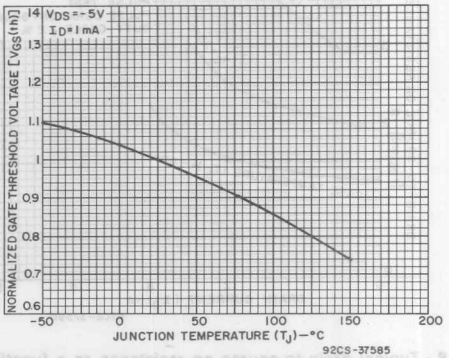


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

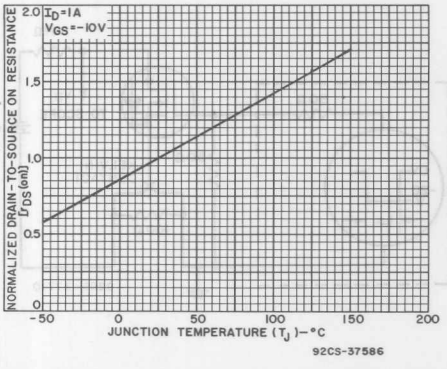


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

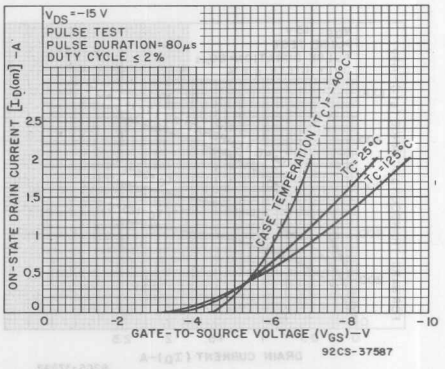


Fig. 5 - Typical transfer characteristics for all types.

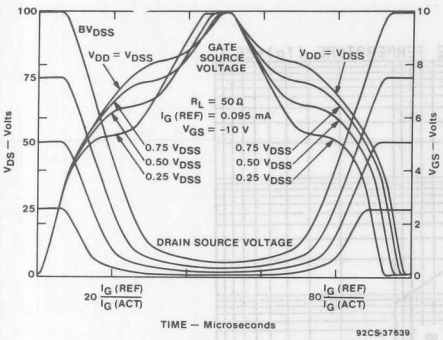


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

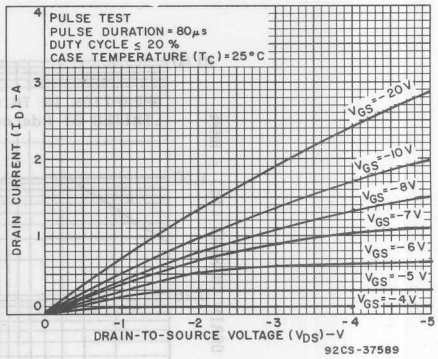


Fig. 7 - Typical saturation characteristics for all types.

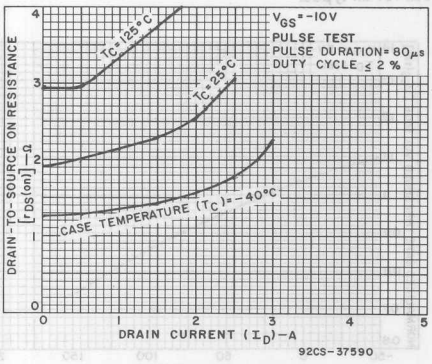


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

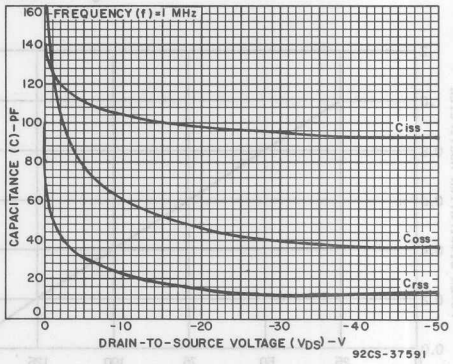


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

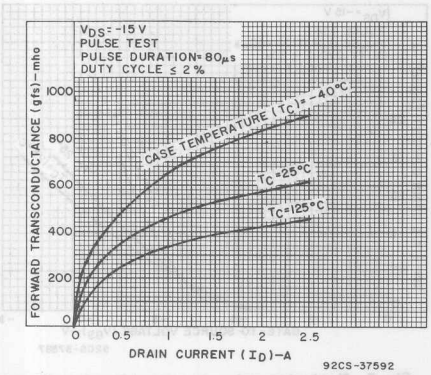


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

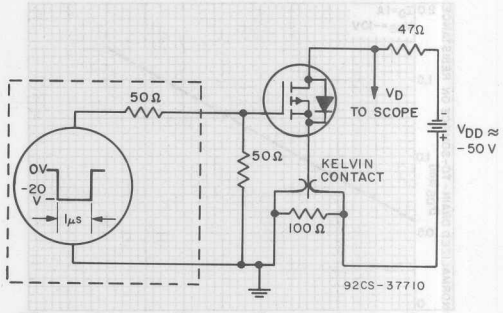


Fig. 11 - Switching time test circuit.

RFP2P08
RFP2P10

P-Channel Enhancement-Mode Power Field-Effect Transistors

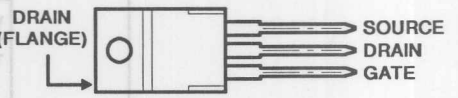
August 1991

Features

- -2A, -80V and -100V
- $r_{DS(ON)} = 3.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-220AB
TOP VIEW



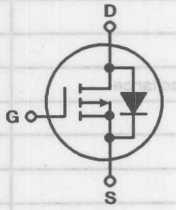
Description

The RFP2P08 and RFP2P10 are P-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		RFP2P08	RFP2P10	UNITS
Drain-Source Voltage	V_{DS}	-80	-100	V
Drain-Gate Voltage (R_{GS} = 1mΩ)	V_{DGR}	-80	-100	V
Continuous Drain Current				
RMS Continuous	I_D	2	2	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	25	25	W
Above T_C = +25°C, Derate Linearly		0.2	0.2	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2870

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP2P08 MIN	RFP2P08 MAX	RFP2P10 MIN	RFP2P10 MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	-80	-	-100	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -65V	-	-1	-	-	μA
		V_{DS} = -80V	-	-	-	-1	μA
		T_C = +125°C, V_{DS} = -65V	-	-50	-	-	μA
		V_{DS} = -80V	-	-	-	-50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	-	±100	-	±100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = -10V	-	-3.5	-	-3.5	V
		I_D = 2A, V_{GS} = -10V	-	-9.0	-	-9.0	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = -10V	-	3.5	-	3.5	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = -10V	200	-	200	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1MHz	-	150	-	150	pF
Output Capacitance	C_{OSS}		-	80	-	80	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	30	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = -50V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = -10V	7 (typ)	25	7 (typ)	25	ns
Rise Time	t_r		15 (typ)	45	15 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		14 (typ)	45	14 (typ)	45	ns
Fall Time	t_f		11 (typ)	25	11 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	5	-	5	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP2P08 MIN	RFP2P08 MAX	RFP2P10 MIN	RFP2P10 MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	-	-1.4	-	-1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	-	135 (typ)	-	135 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

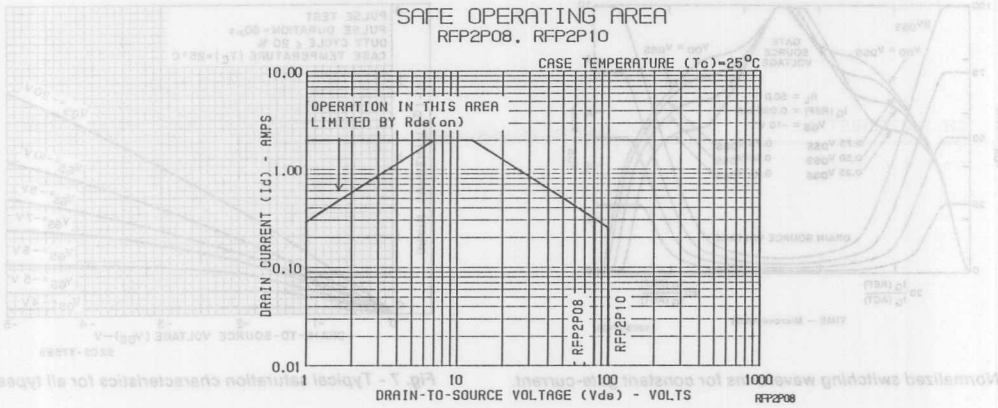


Fig. 1 - Maximum operating areas for all types.

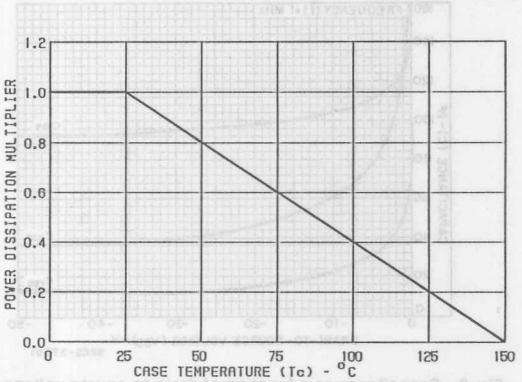


Fig. 2 – Normalized power dissipation vs temperature derating curve.

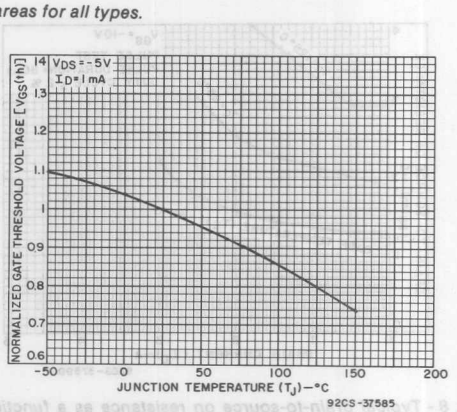


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

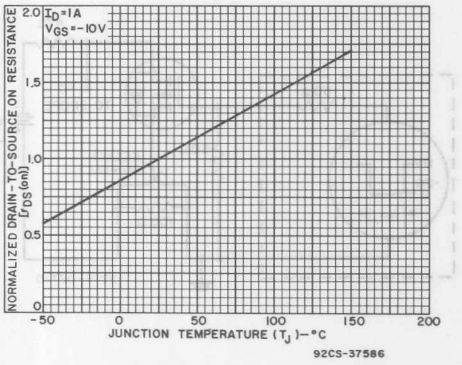


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

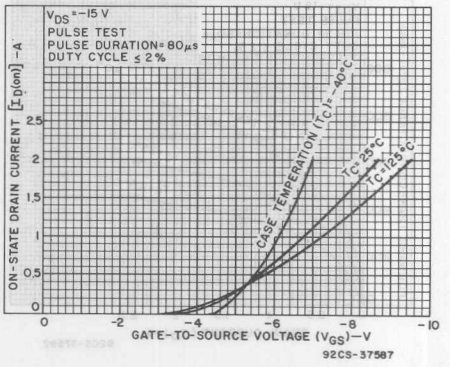


Fig. 5 - Typical transfer characteristics for all types.

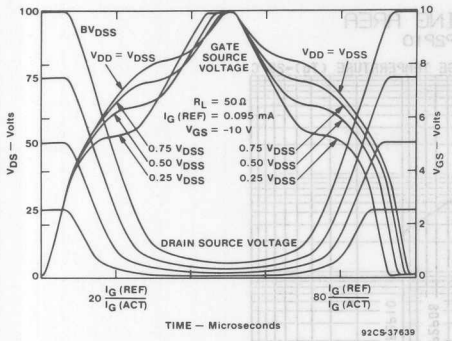


Fig. 6 - Normalized switching waveforms for constant gate-current.

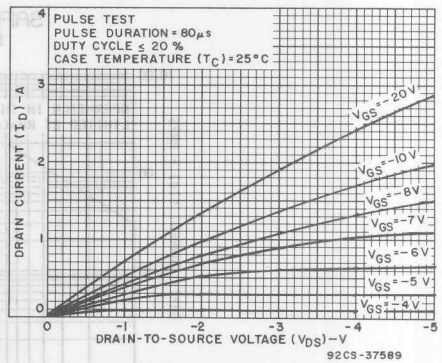


Fig. 7 - Typical saturation characteristics for all types.

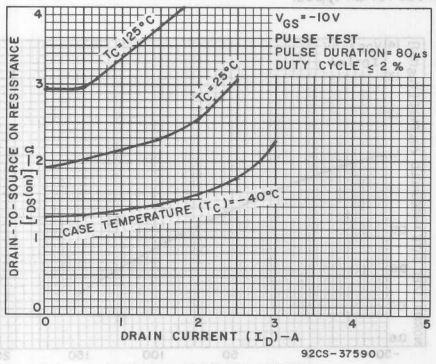


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

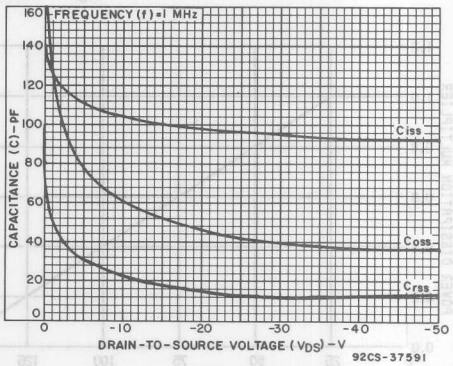


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

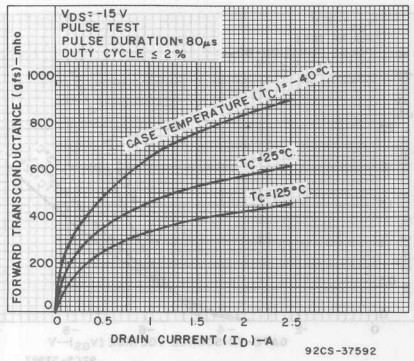


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

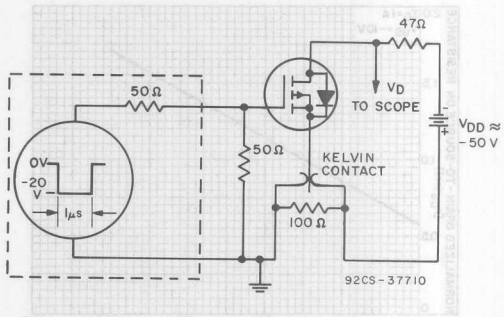


Fig. 11 - Switching time test circuit.

HARRIS

RFM5P12/5P15
RFP5P12/5P15

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -5A, -120V and -150V
- $r_{DS(on)} = 1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

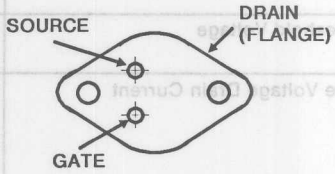
Description

The RFM5P12 and RFM5P15 and the RFP5P12 and RFP5P15 are p-channel enhancement-mode silicon gate power field-effect transistors designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

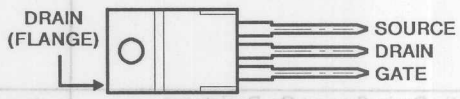
The RFM series types are supplied in the JEDEC TO-204AA metal package and the RFP series types in the JEDEC TO-220AB plastic package. All these types are supplied without an internal gate zener diode.

Packages

TO-204AA
BOTTOM VIEW

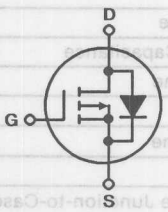


TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

	RFM5P12	RFM5P15	RFP5P12	RFP5P15	UNITS
Drain-Source Voltage ..... V_{DS}	-120	-150	-120	-150	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	-120	-150	-120	-150	V
Continuous Drain Current					
RMS Continuous ..... I_D	5	5	5	5	A
Pulsed Drain Current ..... I_{DM}	15	15	15	15	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1463**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM5P12 RFP5P12		RFM5P15 RFP5P15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-120	—	-150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1 mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100 V	—	1	—	—	μA
		V_{DS} = -120 V	—	—	—	1	
		T_C = 125°C, V_{DS} = -100 V	—	50	—	—	
		T_C = 125°C, V_{DS} = -120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 2.5 A, V_{GS} = -10 V	—	-2.5	—	-2.5	V
		I_D = 5A, V_{GS} = -10 V	—	-8	—	-8	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 2.5 A, V_{GS} = -10 V	—	1	—	1	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 2.5 A	0.75	—	0.75	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	700	—	700	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	100	—	100	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 1/2 BV_{DSS}	20(typ.)	60	20(typ.)	60	ns
Rise Time	t_r	I_D = 2.5 A	36(typ.)	100	36(typ.)	100	
Turn-Off Delay Time	$t_{d(off)}$	R_{gen} = R_{gs} = 50Ω	63(typ.)	150	63(typ.)	150	
Fall Time	t_f	V_{GS} = 10 V	40(typ.)	100	40(typ.)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM5P12, RFM5P15	—	1.67	—	1.67	°C/W
		RFP5P12, RFP5P15	—	2.083	—	2.083	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM5P12 RFP5P12		RFM5P15 RFP5P15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 2.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100A/μs	300(typ.)		300(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

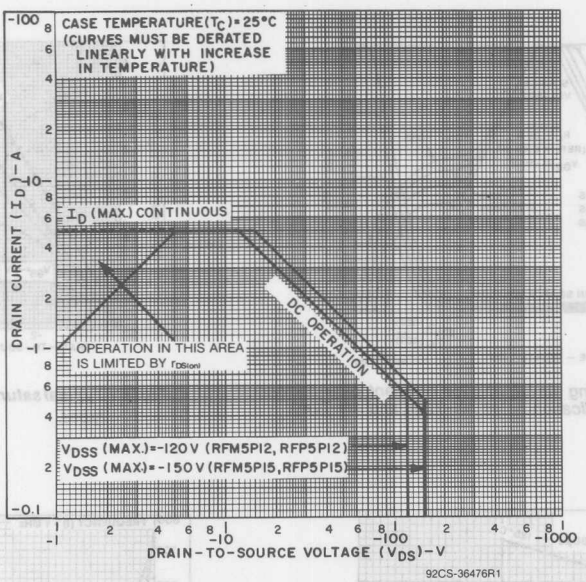


Fig. 1 - Maximum safe operating areas for all types.

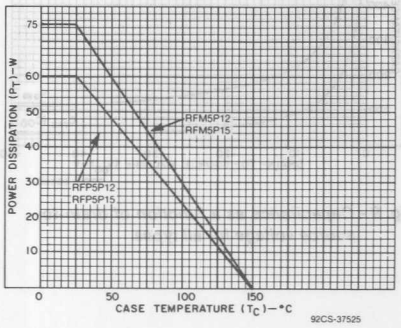


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

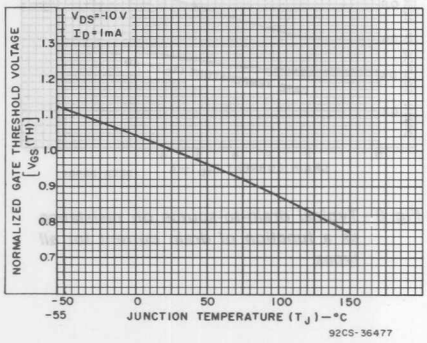


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

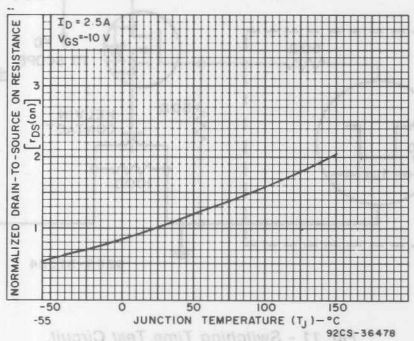


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

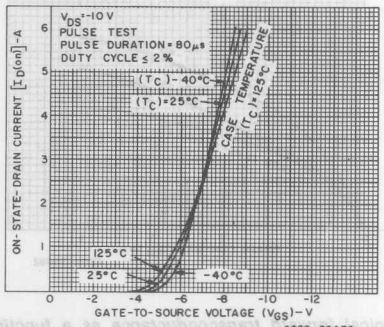


Fig. 5 - Typical transfer characteristics for all types.

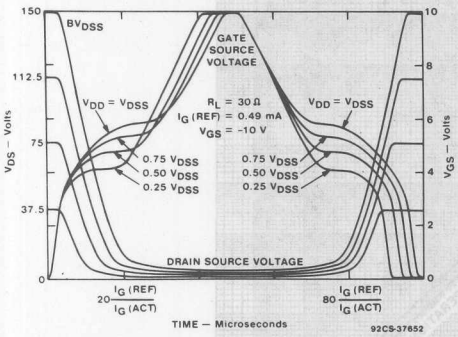


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

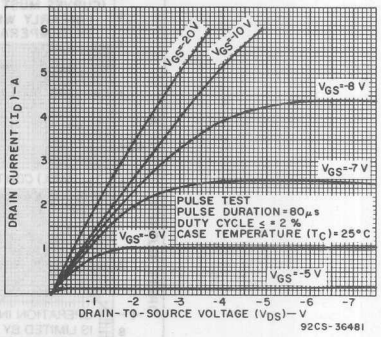


Fig. 7 - Typical saturation characteristics for all types.

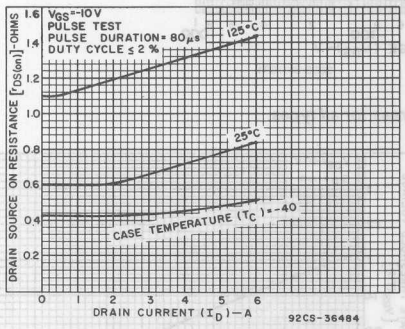


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

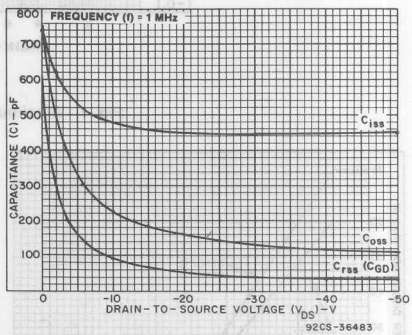


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

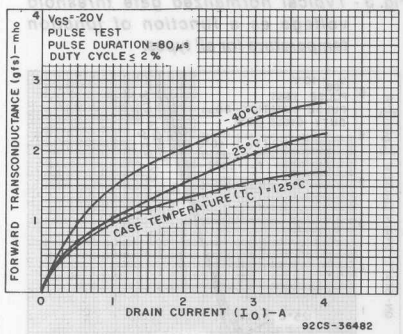


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

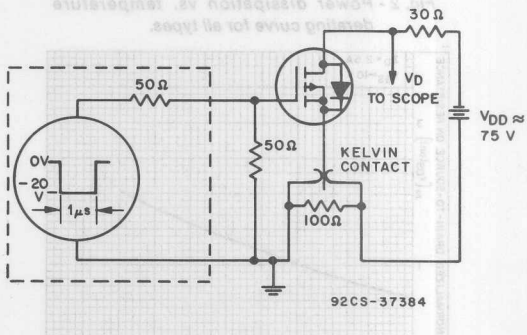


Fig. 11 - Switching Time Test Circuit.

RFM6P08/6P10
RFP6P08/6P10

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -6A, -80V and -100V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

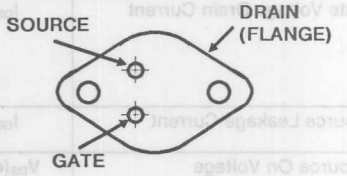
Description

The RFM6P08 and RFM6P10 and the RFP6P08 and RFP6P10 are p-channel enhancement-mode silicon gate power field-effect transistors designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

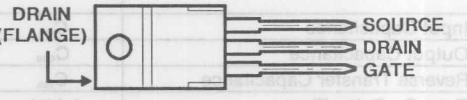
The RFM series types are supplied in the JEDEC TO-204AA metal package and the RFP series types in the JEDEC TO-220AB plastic package. All these types are supplied without an internal gate zener diode.

Packages

TO-204AA
BOTTOM VIEW

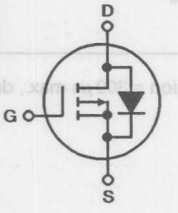


TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	RFM6P08	RFM6P10	RFP6P08	RFP6P10	UNITS
Drain-Source Voltage ..... V_{DS}	80	100	80	100	V
Drain-Gate Voltage (R_{GS} = 1mΩ) ..... V_{DGR}	80	100	80	100	V
Continuous Drain Current					
RMS Continuous ..... I_D	6	6	6	6	A
Pulsed Drain Current ..... I_{DM}	20	20	20	20	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	60	60	W
Above T_C = +25°C, Derate Linearly	0.6	0.6	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1490**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6P08 RFP6P08		RFM6P10 RFP6P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V V_{DS}=-80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=-65 V V_{DS}=-80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=3 A V_{GS}=-10 V	—	-1.8	—	-1.8	V
		I_D=6 A V_{GS}=-10 V	—	-6	—	-6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=3 A V_{GS}=-10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=3 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	800	—	800	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	350	—	350	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	150	—	150	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	11(typ)	60	11(typ)	60	ns
Rise Time	t_r	I_D=3 A	48(typ)	100	48(typ)	100	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	102(typ)	150	102(typ)	150	ns
Fall Time	t_f	V_{GS}=10 V	70(typ)	100	70(typ)	100	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM6P08, RFM6P10	—	1.67	—	1.67	°C/W
		RFP6P08, RFP6P10	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6P08 RFP6P08		RFM6P10 RFP6P10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=3 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=50 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

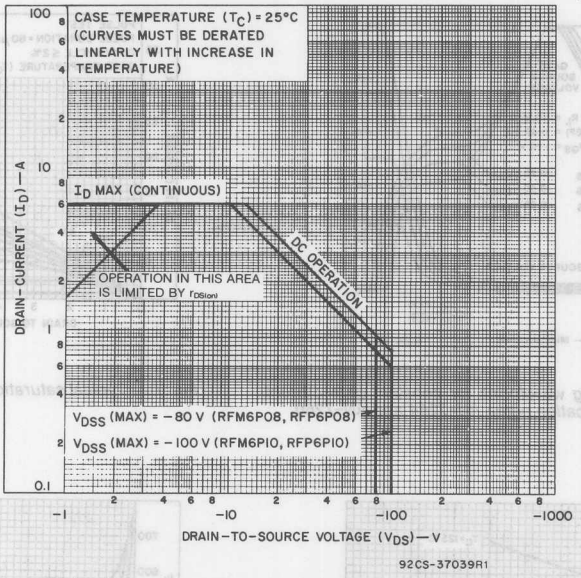


Fig. 1 — Maximum safe operating areas for all types.

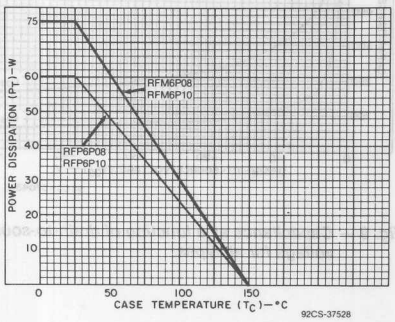


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

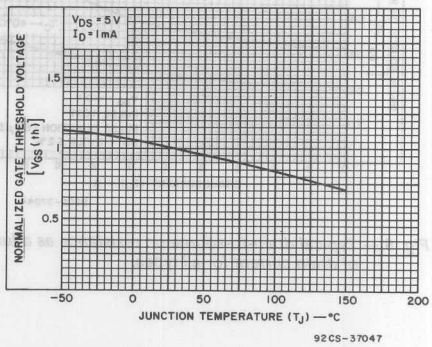


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

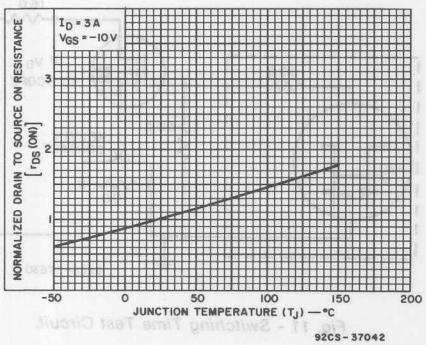


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

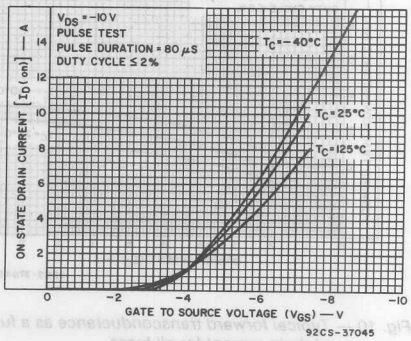


Fig. 5 — Typical transfer characteristics for all types.

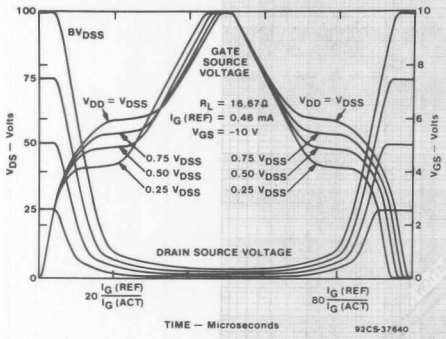


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

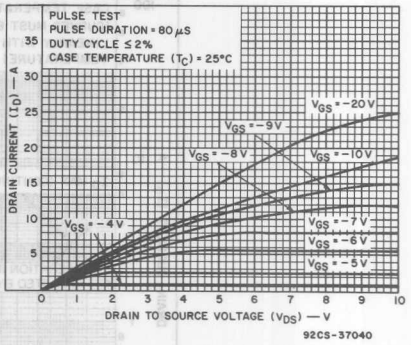


Fig. 7 — Typical saturation characteristics for all types.

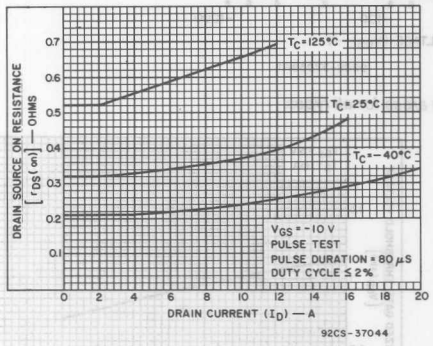


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

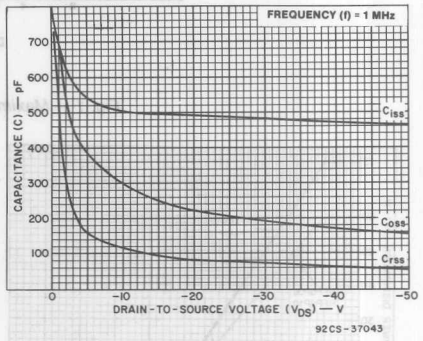


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

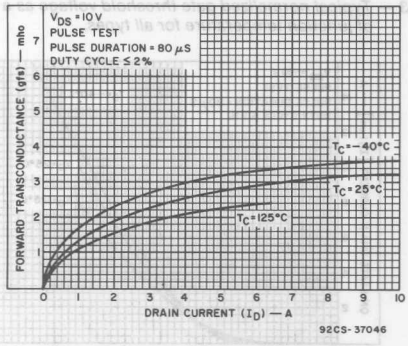


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

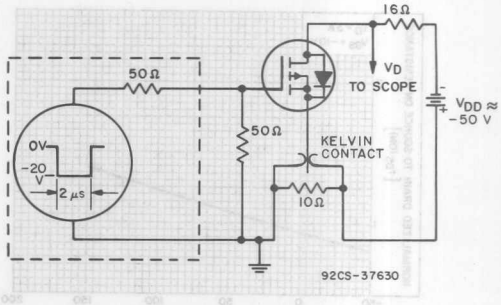


Fig. 11 - Switching Time Test Circuit.

HARRIS RFD8P05/05SM RFP8P05

P-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

August 1991

Features

- -8A, -50V
- $r_{DS(on)}$ = 0.300 Ω
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

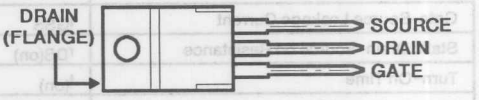
Description

The RFD8P05, RFD8P05SM and RFP8P05 p-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

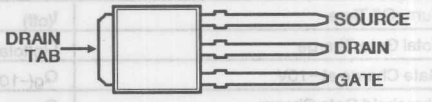
The RFD8P05 is supplied in the JEDEC TO-251AA plastic package and the RFD8P05SM in the TO-252AA plastic package. The RFP8P05 is supplied in the JEDEC TO-220AB plastic package.

Packages

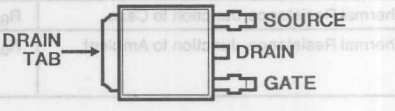
TO-220AB
TOP VIEW



TO-251AA
TOP VIEW

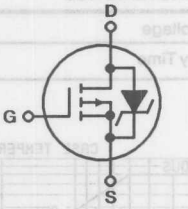


TO-252AA
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS}	-50V
Drain-Gate Voltage, (R_{GS} = 1MΩ), V_{DGR}	-50V
Gate-Source Voltage, V_{GS}	±20V
Drain Current:	
RMS Continuous, I_D	-8A
Pulsed, I_{DM}	-20A
Avalanche Current, I_{AS}	See Figure 2
Power Dissipation, P_D:	
T_C = +25°C	40W
Derate Above T_C = +25°C	0.27W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55°C to +175°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

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File Number 2384

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V	-50	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25 mA	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V	-	1	µA
		T_C = 150°C		50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V, V_{DS} = 0V	-	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 8A, V_{GS} = -10V	-	0.300	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -25V, I_D = 4A Ig1 = Ig2 = 0.2A V_{GS} (clamp): -10V, +0.6V R_L = 6.25Ω (See Figure 12)	-	60	ns
Turn-On Delay Time	$t_{d(on)}$		-	16 (typ)	ns
Rise Time	t_r		-	30 (typ)	ns
Turn-Off Delay Time	$t_{d(off)}$		-	42 (typ)	ns
Fall Time	t_f			20 (typ)	ns
Turn-Off Time	$t_{(off)}$		-	100	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V, V_{DD} = -40V	-	80	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V, I_D = 8A	-	40	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V, R_L = 5Ω	-	2	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 8A, V_{DS} = -15V	-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -25V, I_D = 4A, R_L = 6.25Ω L = 0.2µH, Ig1 = Ig2 = 0.2A V_{GS} (clamp): -10V, +0.6V	-	8	µJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$		-	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	TO-220AB	-	80	°C/W
		TO-251AA, TO-252AA	-	100	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 8A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 8A, d_{ISD}/dt = 100A/µs	-	125	ns

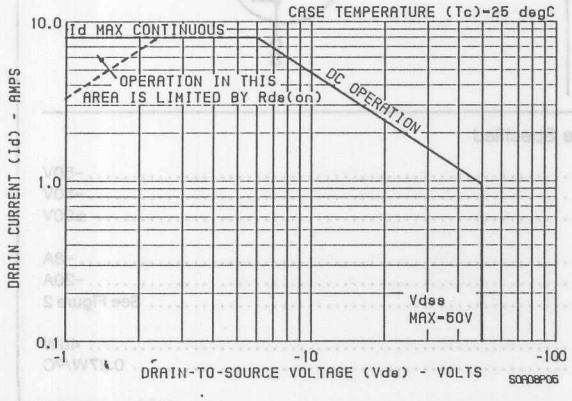


Figure 1 – Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

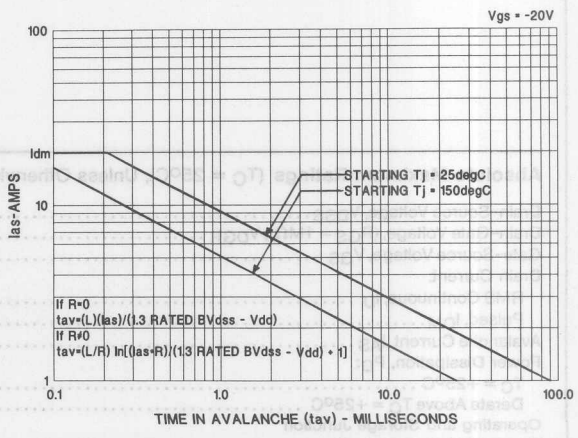


Figure 2 – Unclamped inductive-switching safe-operating-area curve. (Single pulse UIS SOA). See Figure 13 for test circuit.

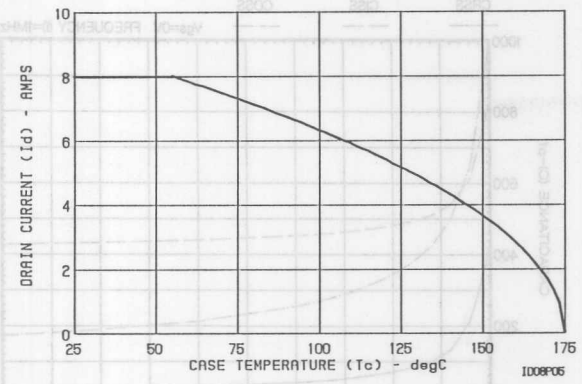


Figure 3 – Maximum continuous drain current vs. temperature.

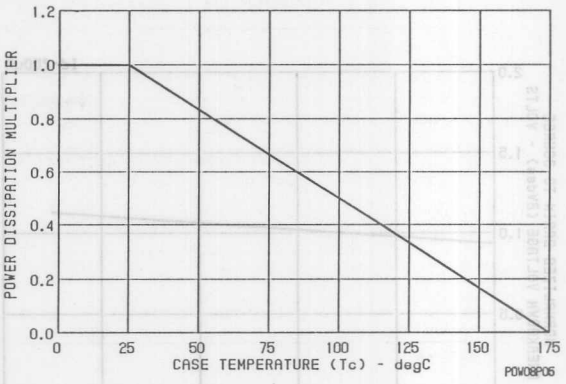


Figure 4 – Normalized power dissipation vs temperature derating curve.

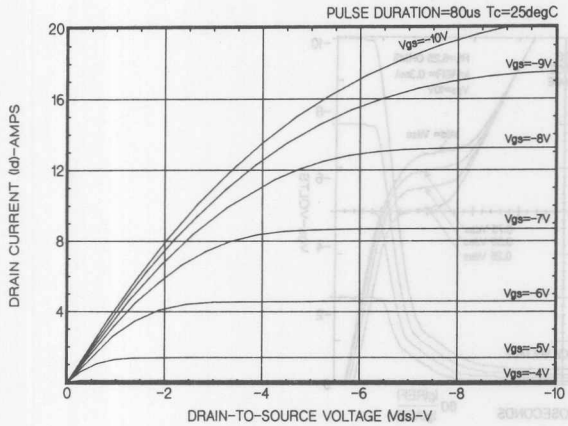


Figure 5 – Typical saturation characteristics.

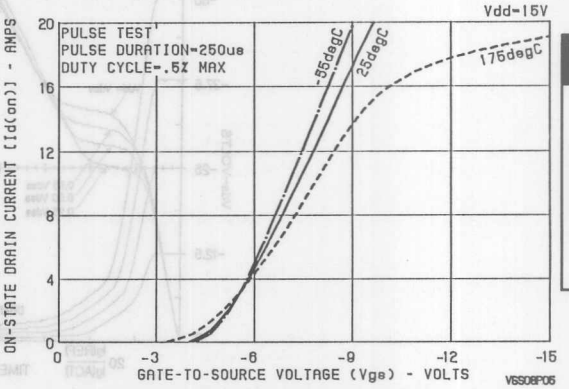


Figure 6 – Typical transfer characteristics.

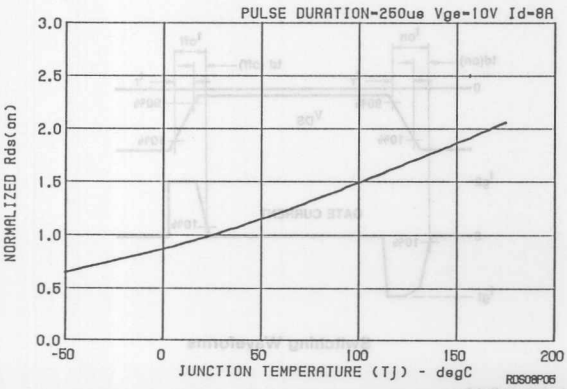


Figure 7 – Normalized rDS(on) vs junction temperature

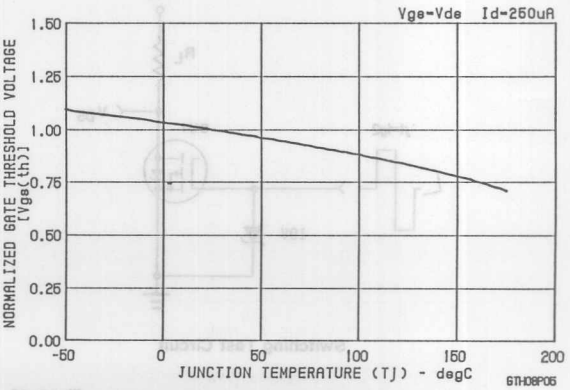


Figure 8 – Normalized gate threshold voltage.

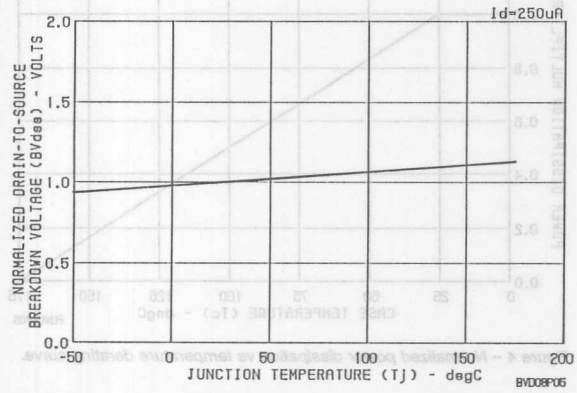


Figure 9 – Normalized drain source breakdown voltage vs temperature.

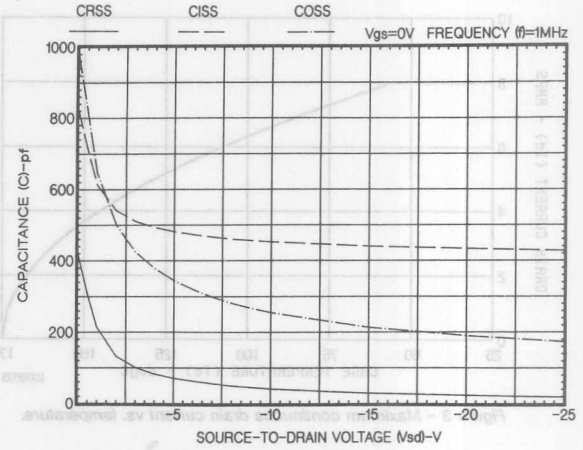


Figure 10 – Typical capacitance vs voltage.

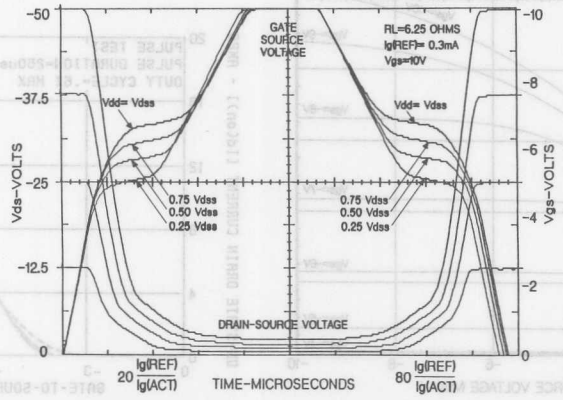
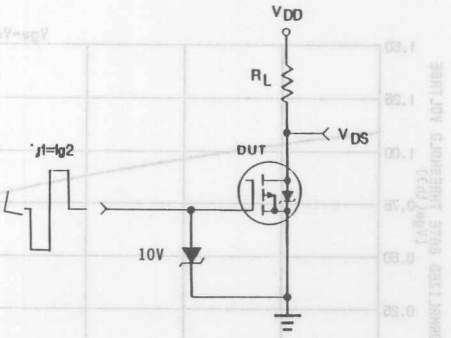
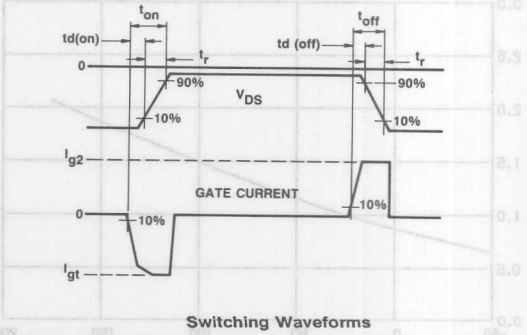


Fig. 11 – Normalized switching waveforms for constant gate-current.
Refer to Harris application notes AN-7254 and AN-7260.

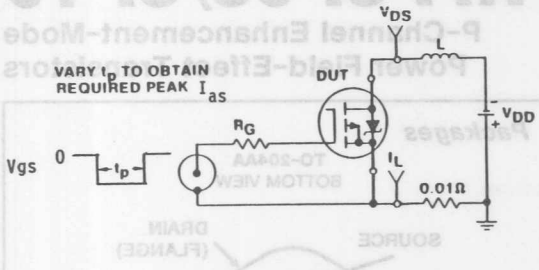


Switching Test Circuit

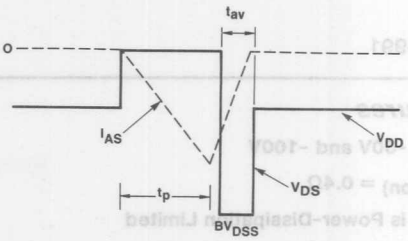


Switching Waveforms

Figure 12 – Resistive switching.



UIS Test Circuit



UIS Waveforms

Figure 13 – Unclamped-inductive-switching test.

HARRIS

RFM8P08/8P10
RFP8P08/8P10

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -8A, -80V and -100V
- $r_{DS(on)} = 0.4\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

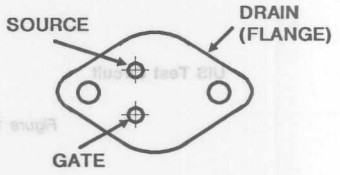
Description

The RFM8P08 and RFM8P10 and the RFP8P08 and RFP8P10 are p-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

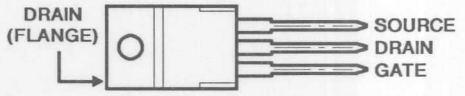
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

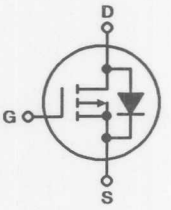


TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

	RFM8P08	RFM8P10	RFP8P08	RFP8P10	UNITS
Drain-Source Voltage ..... V_{DS}	-80	-100	-80	-100	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	-80	-100	-80	-100	V
Continuous Drain Current					
RMS Continuous ..... I_D	8	8	8	8	A
Pulsed Drain Current ..... I_{DM}	20	20	20	20	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	100	100	75	75	W
Above $T_C = +25^oC$, Derate Linearly	0.8	0.8	0.6	0.6	W/^{o}C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1496

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8P08 RFP8P08		RFM8P10 RFP8P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V V_{DS}=-80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=-65 V V_{DS}=-80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=4 A V_{GS}=-10 V	—	-1.6	—	-1.6	V
		I_D=8 A V_{GS}=-10 V	—	-4.0	—	-4.0	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=4 A V_{GS}=-10 V	—	.4	—	.4	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=-10 V I_D=4 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	1500	—	1500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	700	—	700	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	300	—	300	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	18(typ)	60	18(typ)	60	ns
Rise Time	t_r	I_D=4 A	70(typ)	150	70(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	166(typ)	275	166(typ)	275	ns
Fall Time	t_f	V_{GS}=-10 V	94(typ)	175	94(typ)	175	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM8P08, RFM8P10	—	1.25	—	1.25	°C/W
		RFP8P08, RFP8P10	—	1.67	—	1.67	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8P08 RFP8P08		RFM8P10 RFP8P10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 4A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	200(typ.)		200(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

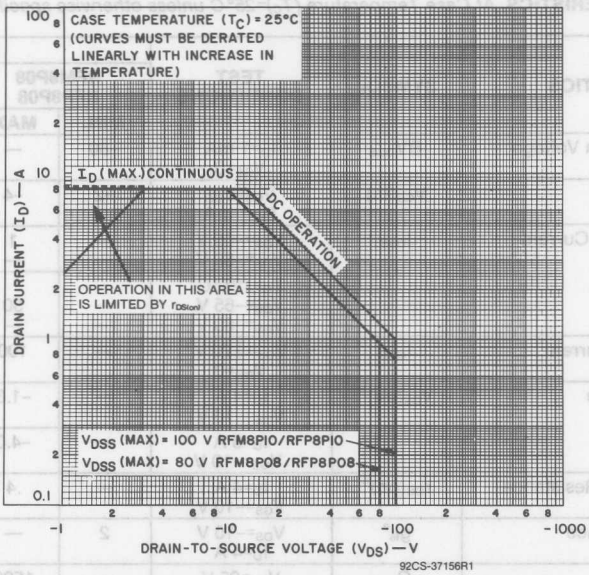


Fig. 1 — Maximum operating areas for all types.

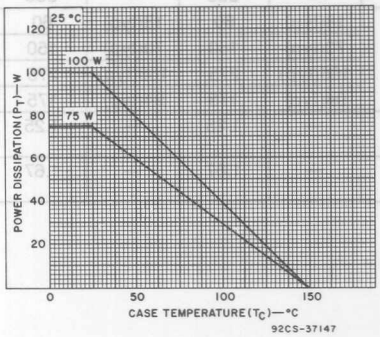


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

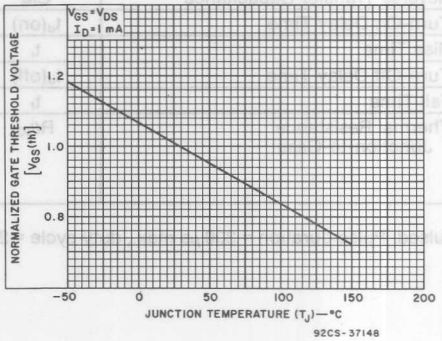


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

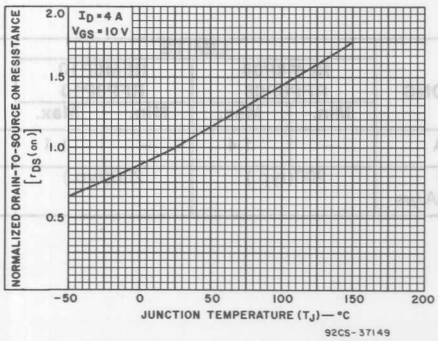


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

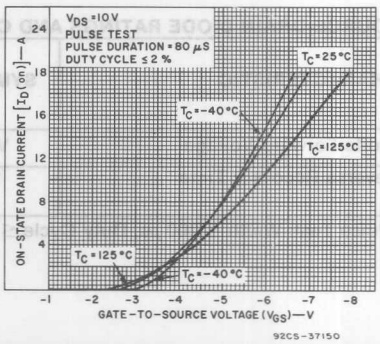


Fig. 5 — Typical transfer characteristics for all types.

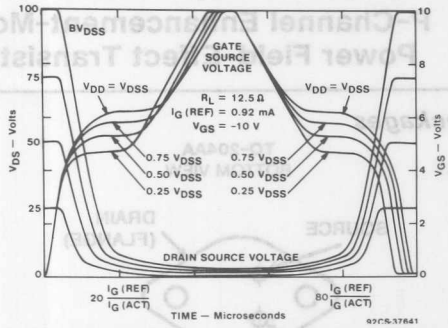


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

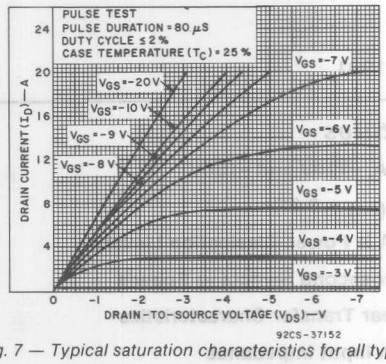


Fig. 7 — Typical saturation characteristics for all types.

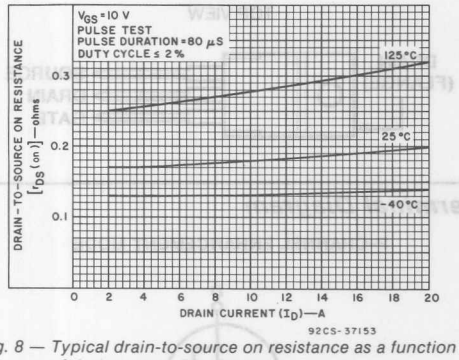


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

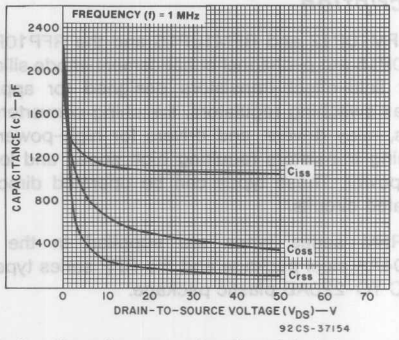


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

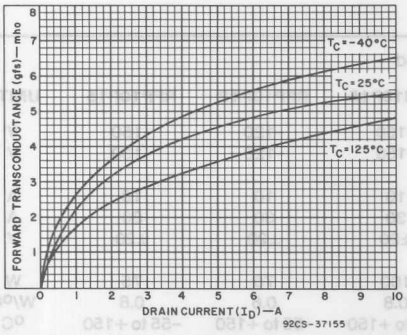


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

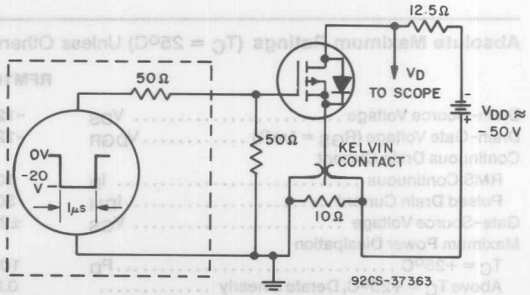


Fig. 11 — Switching Time Test Circuit.

5

P-CHANNEL POWER MOSFETs

HARRIS

RFM10P12/10P15
RFP10P12/10P15

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -10A, -120V and -150V
- $r_{DS(on)} = 0.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

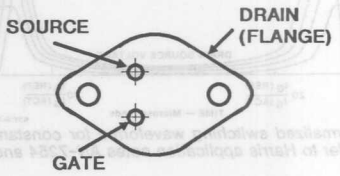
Description

The RFM10P12 and RFM10P15 and the RFP10P12 and RFP10P15 are p-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

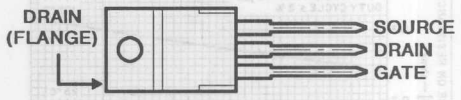
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

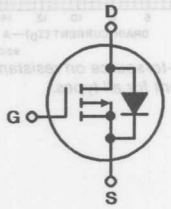


TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

	RFM10P12	RFM10P15	RFP10P12	RFP10P15	UNITS
Drain-Source Voltage ..... V_{DS}	-120	-150	-120	-150	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	-120	-150	-120	-150	V
Continuous Drain Current					
RMS Continuous ..... I_D	10	10	10	10	A
Pulsed Drain Current ..... I_{DM}	30	30	30	30	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	100	100	75	75	W
Above $T_C = +25^oC$, Derate Linearly	0.8	0.8	0.6	0.6	$W/^oC$
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1595**

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10P12 RFP10P12		RFM10P15 RFP10P15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	-120	—	-150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100 V	—	1	—	—	μA
		V_{DS} = -120 V	—	—	—	1	
		T_C = 125° C V_{DS} = -100 V	—	50	—	—	
		V_{DS} = -120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 5 A V_{GS} = -10 V	—	-2.5	—	-2.5	V
		I_D = 10 A V_{GS} = -10 V	—	-6.0	—	-6.0	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 5 A V_{GS} = -10 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V I_D = 5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS} = -25 V	—	1700	—	1700	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	600	—	600	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	350	—	350	
Turn-On Delay Time	$t_{d(on)}$	V_{DS} = -75 V	24(typ)	50	24(typ)	50	ns
Rise Time	t_r	I_D = 5 A	74(typ)	150	74(typ)	150	
Turn-Off Delay Time	$t_{d(off)}$	R_{gen} = R_{gs} = 50 Ω	138(typ)	225	138(typ)	225	
Fall Time	t_f	V_{GS} = -10 V	61(typ)	100	61(typ)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10P12, RFM10P15	—	1.25	—	1.25	°C/W
		RFP10P12, RFP10P15	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10P12 RFP10P12		RFM10P15 RFP10P15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, dI_F/d_t = 100 A/μs	210 (typ.)		210 (typ.)		ns

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

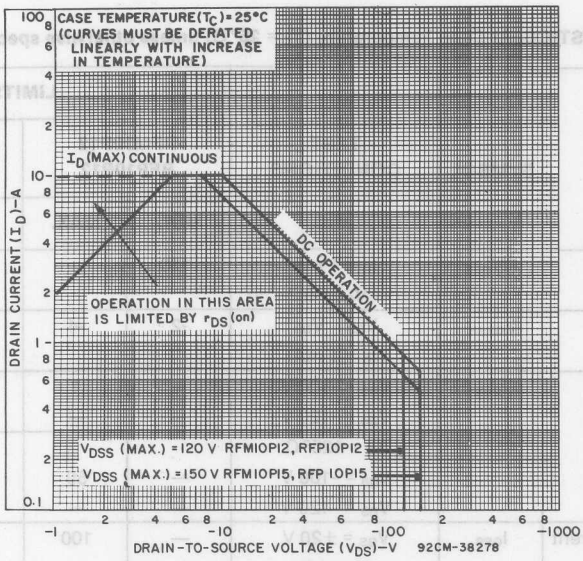


Fig. 1 - Maximum safe operating areas for all types.

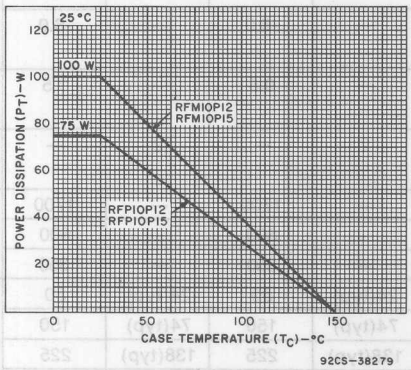


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

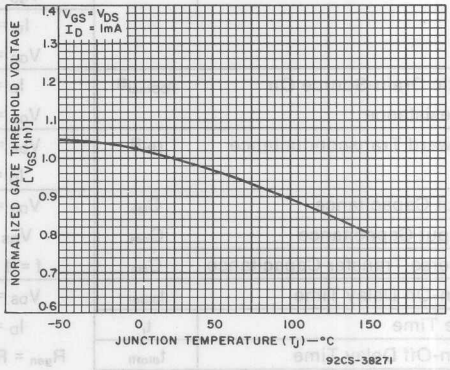


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

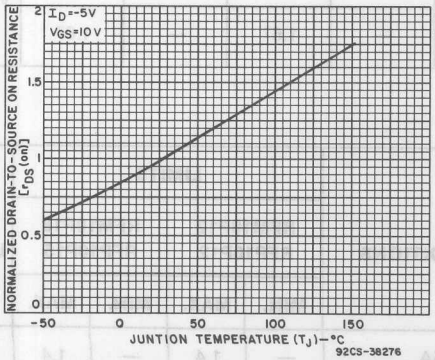


Fig. 4 - Normalized drain-to-source on resistance as as function of junction temperature for all types.

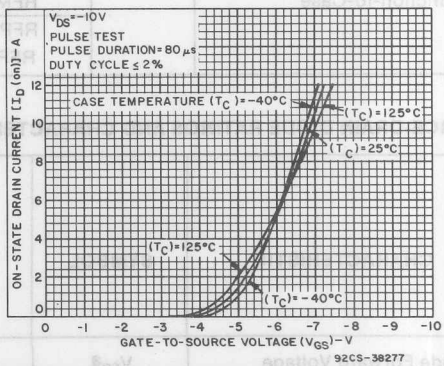


Fig. 5 - Typical transfer characteristics for all types.

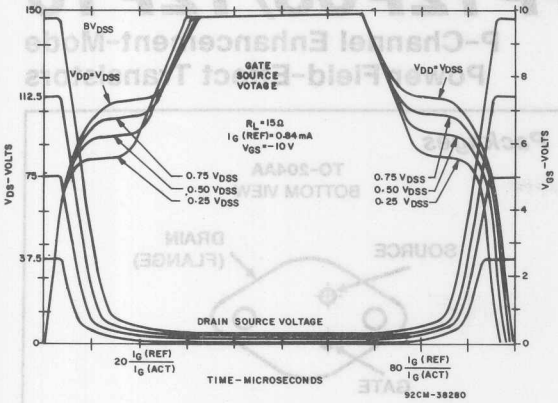


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

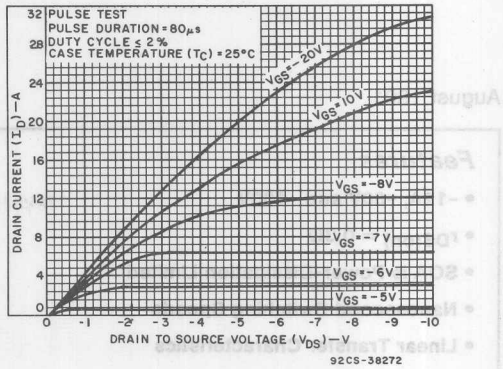


Fig. 7 - Typical saturation characteristics for all types.

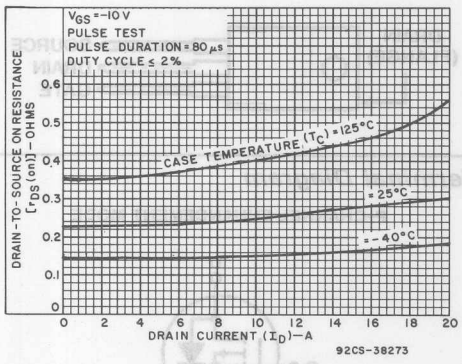


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

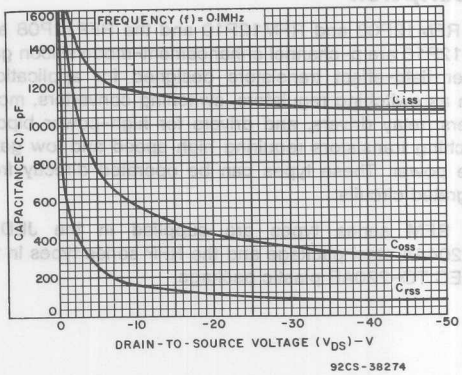


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

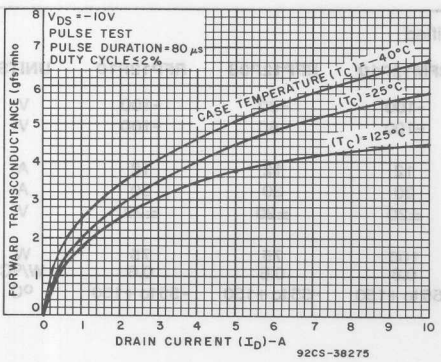


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

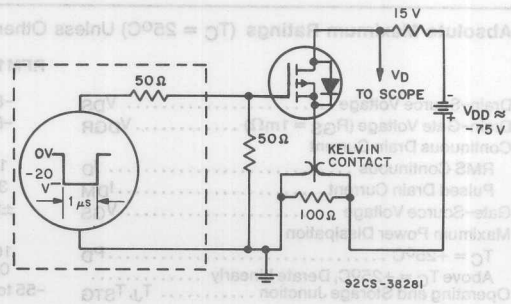


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFM12P08/12P10
RFP12P08/12P10

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -12A, -80V and -100V
- $r_{DS(on)} = 0.3\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

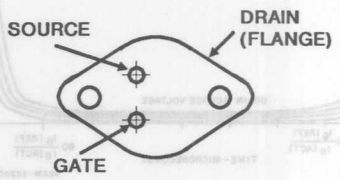
Description

The RFM12P08 and RFM12P10 and the RFP12P08 and RFP12P10 are p-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

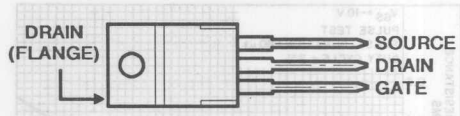
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

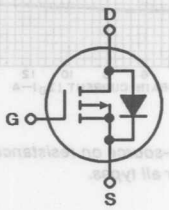


TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	RFM12P08	RFM12P10	RFP12P08	RFP12P10	UNITS
Drain-Source Voltage ..... V_{DS}	-80	-100	-80	-100	V
Drain-Gate Voltage (R_{GS} = 1mΩ) ..... V_{DGR}	-80	-100	-80	-100	V
Continuous Drain Current					
RMS Continuous ..... I_D	12	12	12	12	A
Pulsed Drain Current ..... I_{DM}	30	30	30	30	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	100	100	75	75	W
Above T_C = +25°C, Derate Linearly	0.8	0.8	0.6	0.6	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1495

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12P08 RFP12P08		RFM12P10 RFP12P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V V_{DS}=-80 V	— —	1 —	— —	— 1	μA
		T_C=125°C V_{DS}=-65 V V_{DS}=-80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm$20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=-10 V	—	-1.8	—	-1.8	V
		I_D=12 A V_{GS}=-10 V	—	-4.8	—	-4.8	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=-10 V	—	.3	—	.3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=-10 V I_D=6 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=-25 V	—	1500	—	1500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	700	—	700	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	300	—	300	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	18(typ)	60	18(typ)	60	ns
Rise Time	t_r	I_D=6 A	90(typ)	175	90(typ)	175	ns
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=R_{gs}$=50 Ω	144(typ)	275	144(typ)	275	ns
Fall Time	t_f	V_{GS}=-10 V	94(typ)	175	94(typ)	175	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM12P08, RFM12P10	—	1.25	—	1.25	°C/W
		RFP12P08, RFP12P10	—	1.67	—	1.67	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12P08 RFP12P08		RFM12P10 RFP12P10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

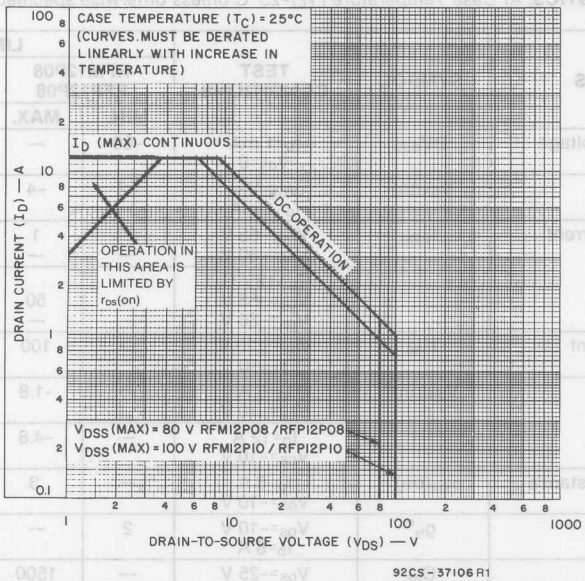


Fig. 1 — Maximum safe operating areas for all types.

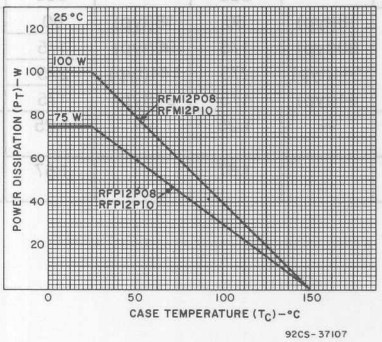


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

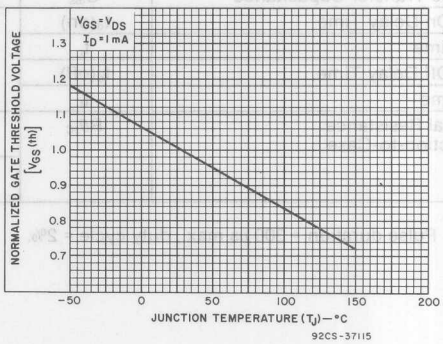


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

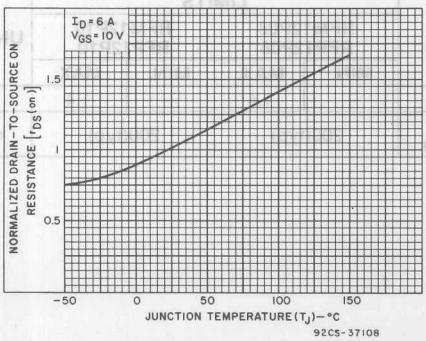


Fig. 4 — Normalized drain-to-source on resistance as a function of junction temperature for all types.

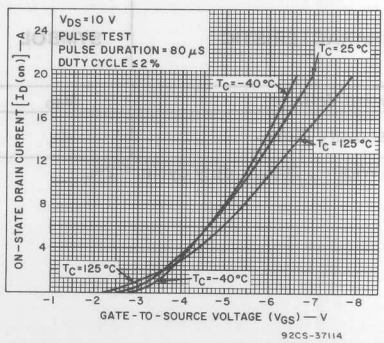


Fig. 5 — Typical transfer characteristics for all types.

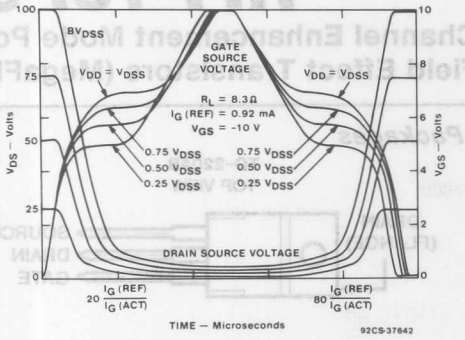


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

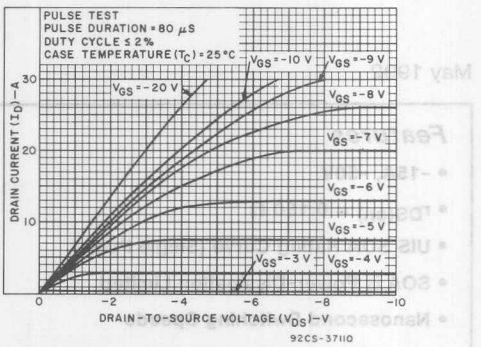


Fig. 7 — Typical saturation characteristics for all types.

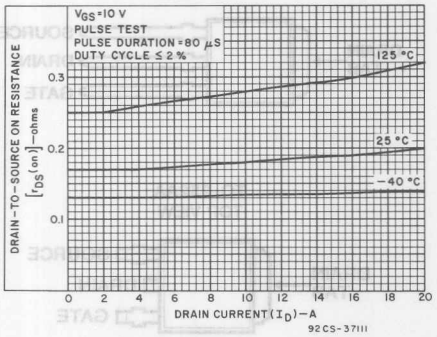


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

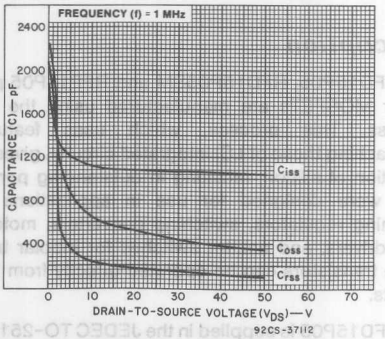


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

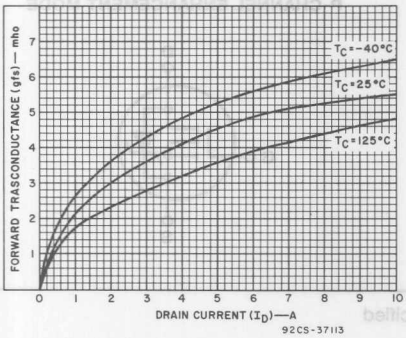


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

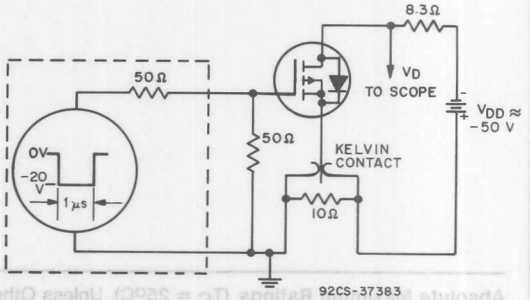


Fig. 11 — Switching Time Test Circuit

HARRIS

RFD15P05/05SM
RFP15P05

P-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

May 1992

Features

- -15A, -50V
- $r_{DS(on)}$ = 0.150 Ω
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

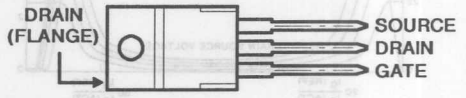
Description

The RFD15P05, RFD15P05SM and RFP15P05 p-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

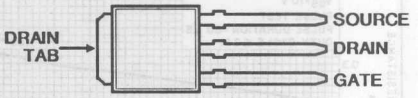
The RFD15P05 is supplied in the JEDEC TO-251AA plastic package and the RFD15P05SM in the TO-252AA plastic package. The RFP15P05 is supplied in the JEDEC TO-220AB plastic package.

Packages

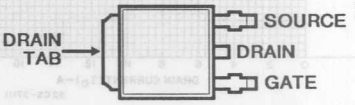
TO-220AB
TOP VIEW



TO-251AA
TOP VIEW



TO-252AA
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS}	-50V
Drain-Gate Voltage, (R_{GS} = 1MΩ), V_{DGR}	-50V
Gate-Source Voltage, V_{GS}	±20V
Drain Current:	
RMS Continuous, I_D	-15A
Pulsed, I_{DM}	-40A
Avalanche Current, I_{AS}	See Figure 2
Power Dissipation, P_D:	
T_C = +25°C	80W
Derate Above T_C = +25°C	0.533W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55°C to +175°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

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File Number 2387.1

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V		-50	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25 mA		-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V		-	1	µA
		T_C = 150°C			50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V, V_{DS} = 0V		-	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 15A, V_{GS} = -10V		-	0.150	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -25V, I_D = 7.5A Ig1 = Ig2 = 0.4A V_{GS} (clamp): -10V, +0.6V R_L = 3.3Ω (See Figure 12)		-	60	ns
Turn-On Delay Time	$t_{d(on)}$			-	16 (typ)	ns
Rise Time	t_r			-	30 (typ)	ns
Turn-Off Delay Time	$t_{d(off)}$			-	50 (typ)	ns
Fall Time	t_f				20 (typ)	ns
Turn-Off Time	$t_{(off)}$			-	100	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V	V_{DD} = -40V	-	150	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V	I_D = 15A	-	75	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V	R_L = 2.67Ω	-	3.5	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 15A, V_{DS} = -15V		-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -25V, I_D = 7.5A, R_L = 3.33Ω L = 0.2µH, Ig1 = Ig2 = 0.4A V_{GS} (clamp): -10V, +0.6V		-	17	µJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$	TO-220AB, TO-251AA, TO-252AA		-	1.875	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	TO-251AA, TO-252AA		-	100	°C/W
		TO-220AB		-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 15A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 15A, d_{ISD}/dt = 100A/µs	-	125	ns

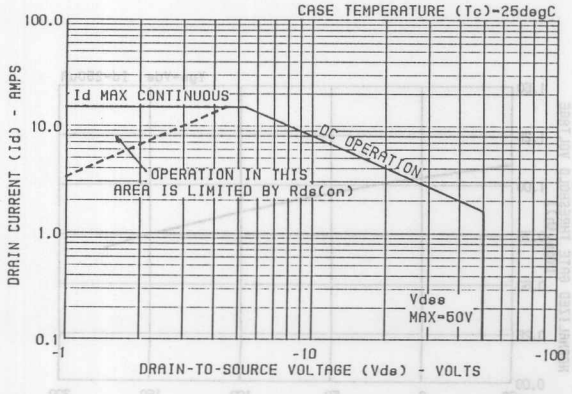


Figure 1 – Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

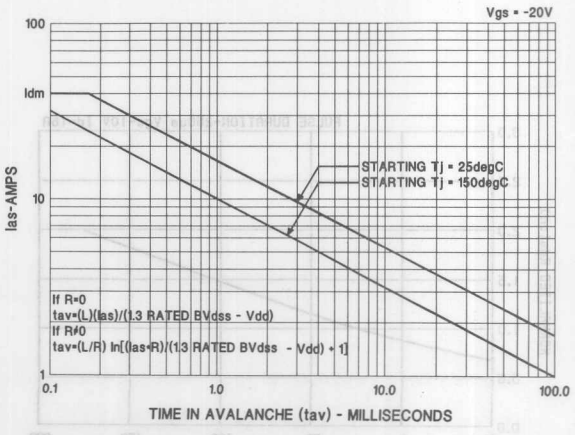


Figure 2 – Unclamped inductive-switching safe-operating-area curve. (Single pulse UIS SOA). See Figure 13 for test circuit.

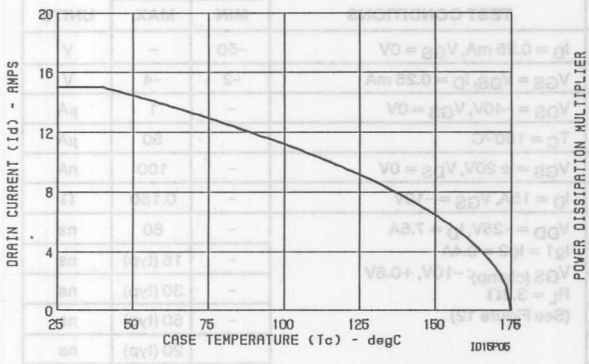


Figure 3 – Maximum continuous drain current vs. temperature.

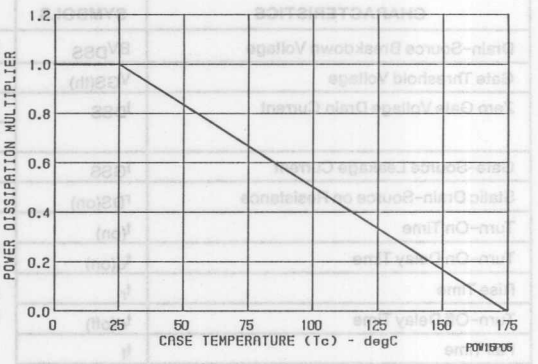


Figure 4 – Normalized power dissipation vs temperature derating curve.

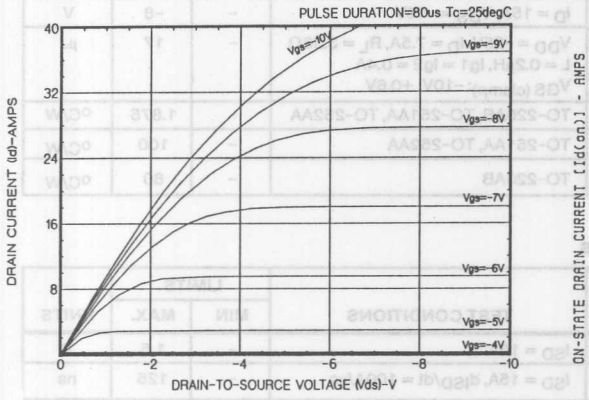


Figure 5 – Typical saturation characteristics.

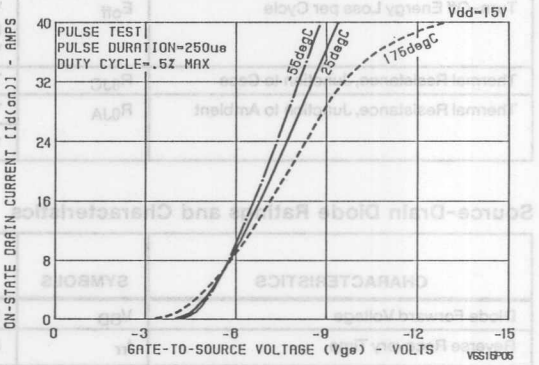


Figure 6 – Typical transfer characteristics.

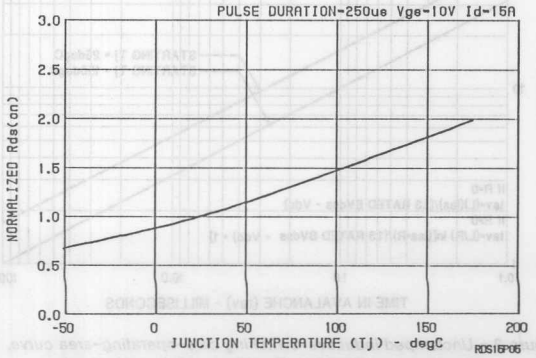


Figure 7 – Normalized rDS(on) vs junction temperature.

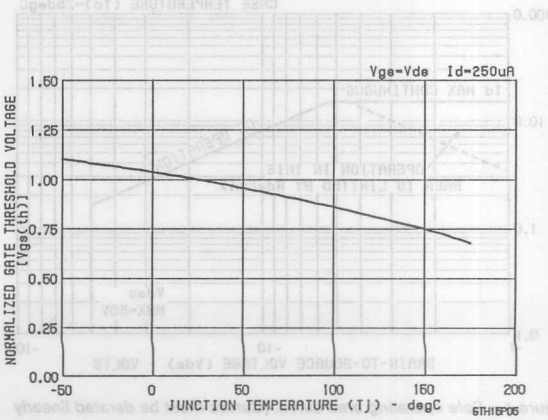


Figure 8 – Normalized gate threshold voltage.

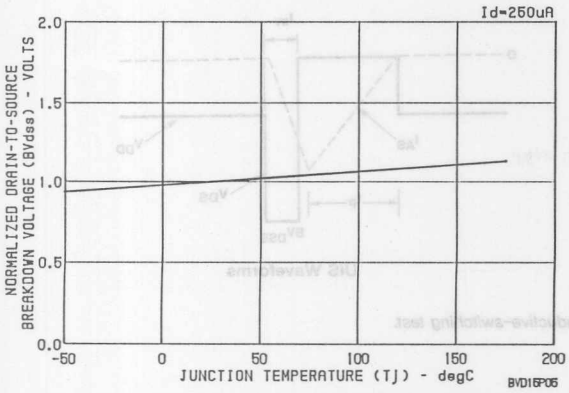


Figure 9 - Normalized drain source breakdown voltage vs temperature.

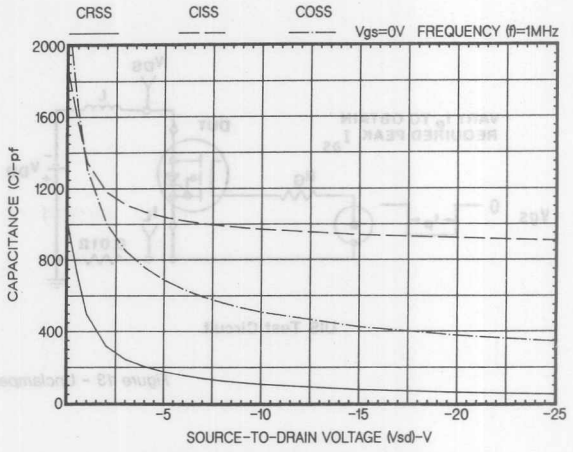


Figure 10 - Typical capacitance vs voltage.

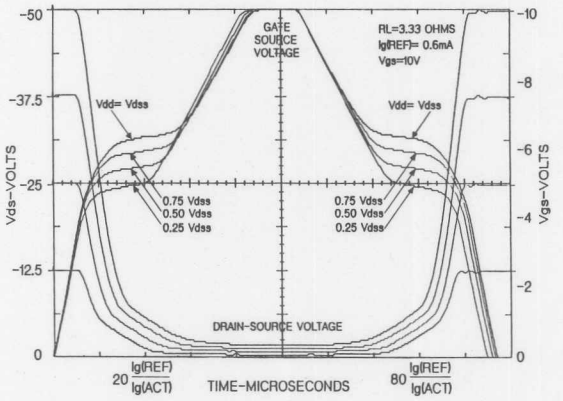


Fig. 11 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

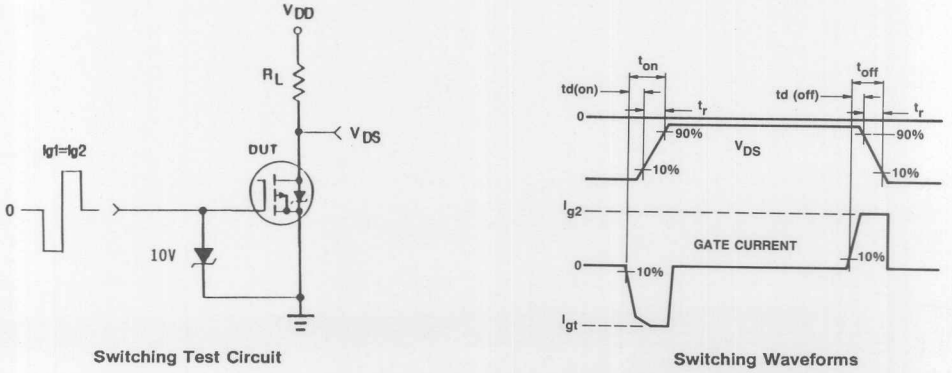
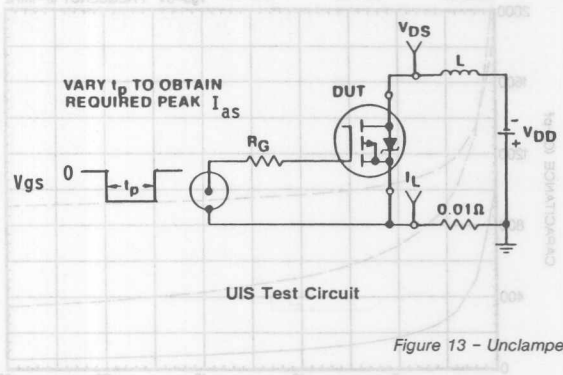
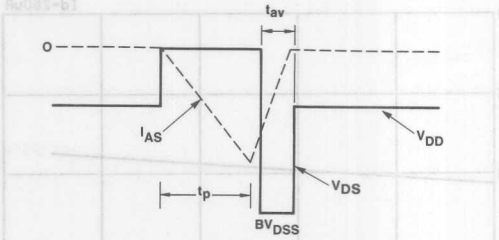


Figure 12 - Resistive switching.



UIS Test Circuit



UIS Waveforms

Figure 13 – Unclamped-inductive-switching test.

RFH25P08/25P10
RFK25P08/25P10

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -25A, -100V and -80V
- $r_{DS(on)} = 0.15\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

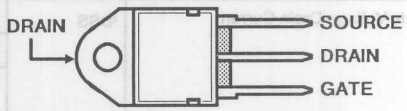
Description

The RFH25P08 and RFH25P10 and the RFK25P08 and RFK25P10 are p-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

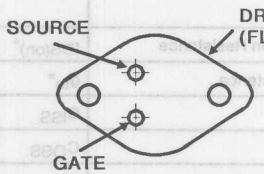
The RFH series types are supplied in the JEDEC TO-218AC plastic package and the RFK series types in the JEDEC TO-204AE steel package.

Packages

TO-218AC
TOP VIEW

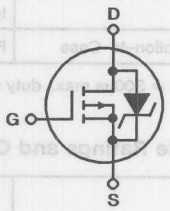


TO-204AE
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

	RFH25P08	RFH25P10	RFK25P08	RFK25P10	UNITS
Drain-Source Voltage ..... V_{DS}	-80	-100	-80	-100	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	-80	-100	-80	-100	V
Continuous Drain Current					
RMS Continuous ..... I_D	-25	-25	-25	-25	A
Pulsed Drain Current ..... I_{DM}	-60	-60	-60	-60	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	150	150	150	150	W
Above $T_C = +25^oC$, Derate Linearly	1.2	1.2	1.2	1.2	$W/^oC$
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1632**

Electrical Characteristics (T_C = 25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFH25P08 RFK25P08 MIN.	MAX.	LIMITS RFH25P10 RFK25P10 MIN.	MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1.0mA, V_{GS} = 0	-80	-	-100	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -65V	-	-1	-	-	µA
		V_{DS} = -80V	-	-	-	-1	µA
		T_C = 125°C, V_{DS} = -65V	-	-50	-	-	µA
		T_C = 125°C, V_{DS} = -80V	-	-	-	-50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	-	100	-	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 12.5A, V_{GS} = -10V	-	-1.88	-	-1.88	V
		I_D = 25A, V_{GS} = -10V	-	-4.5	-	-4.5	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 12.5A, V_{GS} = -10V	-	0.15	-	0.15	Ω
Forward Transconductance	g_{ts}*	I_D = 12.5A, V_{DS} = -10V	4	-	4	-	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1MHz	-	3000	-	3000	pF
Output Capacitance	C_{OSS}		-	1500	-	1500	pF
Reverse Transfer Capacitance	C_{RSS}		-	600	-	600	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 12.5A, V_{DS} = -50V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = -10V	35 (typ)	50	35 (typ)	50	ns
Rise Time	t_r		165 (typ)	250	165 (typ)	250	ns
Turn-Off Delay Time	$t_{d(off)}$		270 (typ)	400	270 (typ)	400	ns
Fall Time	t_f		165 (typ)	250	165 (typ)	250	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFK25P08, RFK25P10	-	0.83	-	0.83	°C/W

* Pulsed: Pulse duration = 300µs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFH25P08 RFK25P08 MIN	MAX	LIMITS RFH25P10 RFK25P10 MIN	MAX	UNITS
Diode Forward Voltage	V_{SD}**	I_{SD} = -12.5A	-	1.4	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/dt = 100A/µs	-	300 (typ)	-	300 (typ)	ns

** Pulsed test: Width ≤ 300µs, duty cycle ≤ 2%.

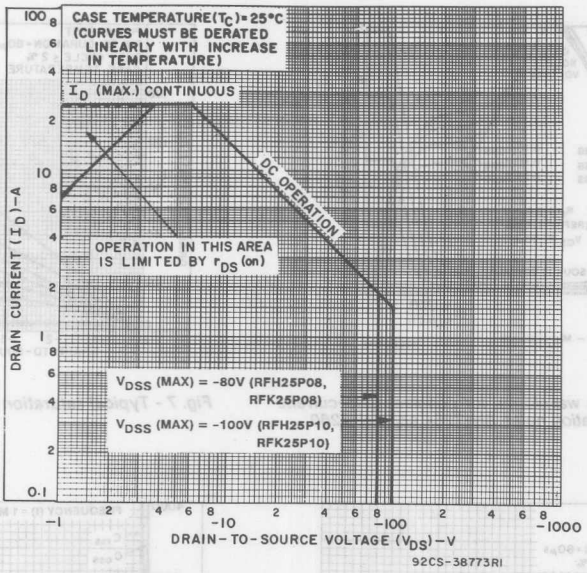


Fig. 1 - Maximum safe operating areas for all types.

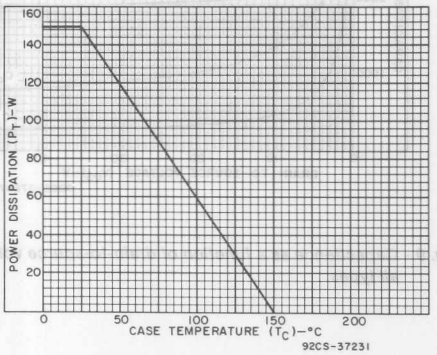


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

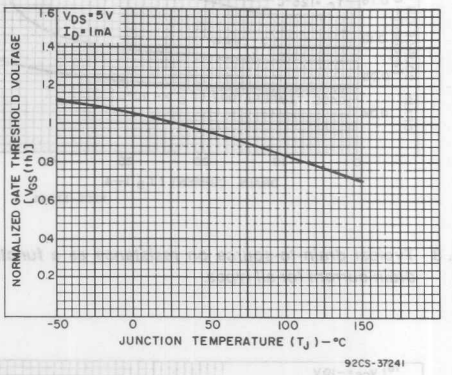


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

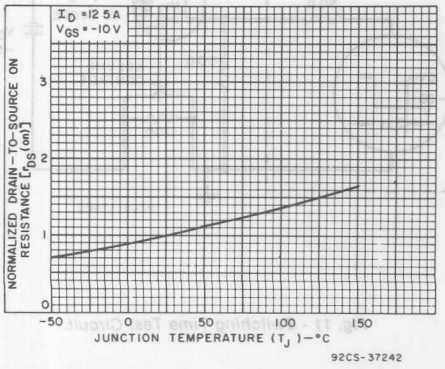


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

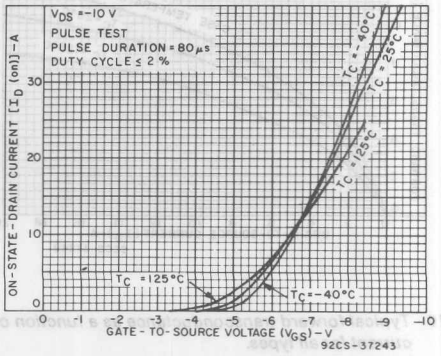


Fig. 5 - Typical transfer characteristics for all types.

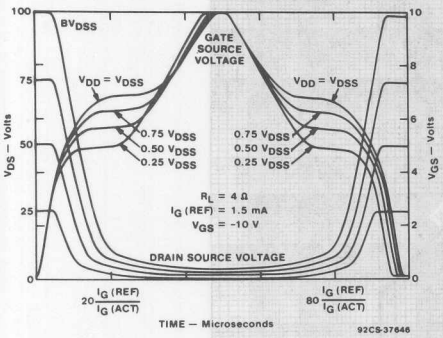


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

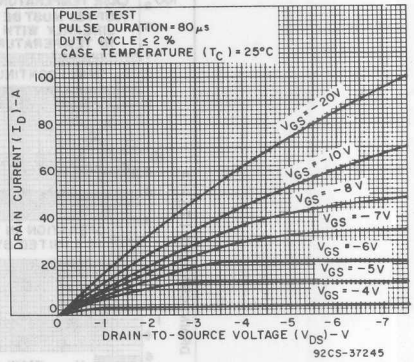


Fig. 7 - Typical saturation characteristics for all types.

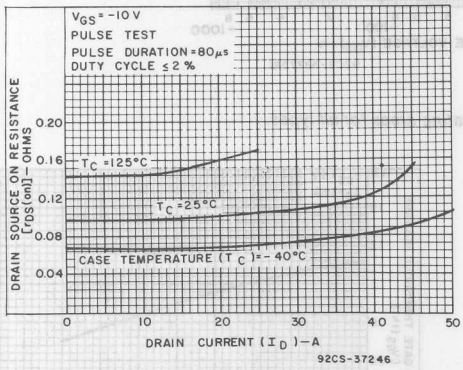


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

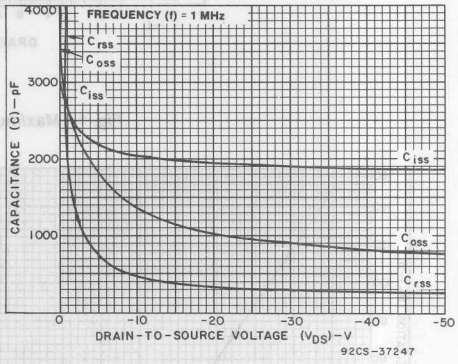


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

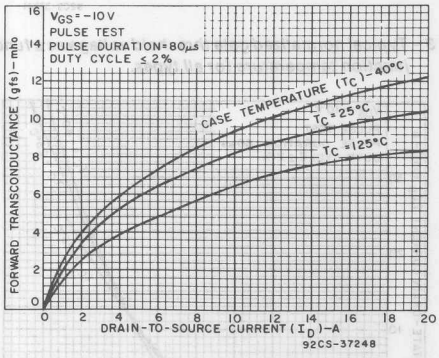


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

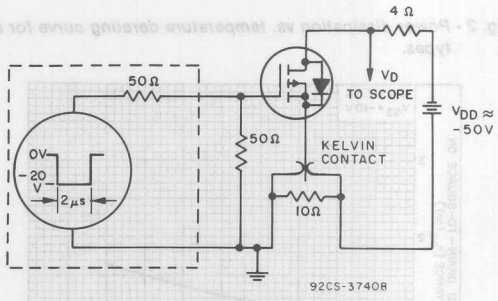


Fig. 11 - Switching Time Test Circuit.

RFG30P05
RFP30P05

P-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

August 1991

Features

- -30A, -50V
- $r_{DS(on)}$ = 0.065 Ω
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 175°C Operating Temperature

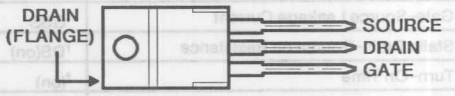
Description

The RFG30P05 and RFP30P05 p-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

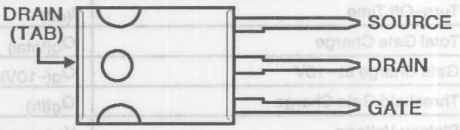
The RFG30P05 is supplied in the JEDEC TO-247 plastic package and the RFP30P05 in the TO-220AB plastic package.

Packages

TO-220AB
TOP VIEW

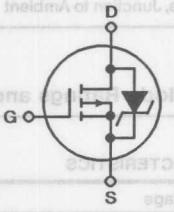


TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS}	-50V
Drain-Gate Voltage, (R_{GS} = 1mΩ), V_{DGR}	-50V
Gate-Source Voltage, V_{GS}	±20V
Drain Current:	
RMS Continuous, I_D	-30A
Pulsed, I_{DM}	-75A
Single Pulse Avalanche Rating, Refer to UIS SOA Curve	
Power Dissipation, P_D:	
T_C = +25°C	120W
Derate Above T_C = +25°C	0.8W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55 to +175°C

5

P-CHANNEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

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File Number 2436

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V		-50	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25 mA		2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V		-	1	µA
		T_C = 150°C			50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V		-	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 30A, V_{GS} = -10V		-	0.0.65	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -25V, I_D = 15A Ig1 = Ig2 = 0.8A V_{GS} (clamp): -10V, +0.6V R_L = 1.67Ω		-	80	ns
Turn-On Delay Time	$t_{d(on)}$			15 (typ)	-	ns
Rise Time	t_r			23 (typ)	-	ns
Turn-Off Delay Time	$t_{d(off)}$			28 (typ)	-	ns
Fall Time	t_f			18 (typ)	-	ns
Turn-Off Time	$t_{(off)}$			-	100	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V	V_{DD} = -40V	-	200	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V	I_D = 40A	-	100	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V	R_L = 1.33Ω	-	2	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 30A, V_{DS} = -15V		-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -25V, I_D = 15A, R_L = 1.67Ω L = 0.2µH, Ig1 = Ig2 = 0.8A V_{GS} (clamp): -10V, +0.6V		-	75	µJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	1.25	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 30A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 30A, d_{ISD}/dt = 100A/µs	-	150	ns

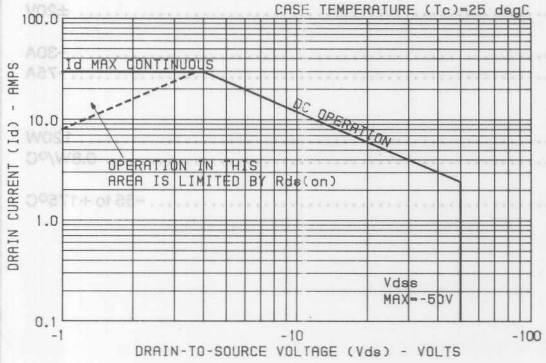


Figure 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

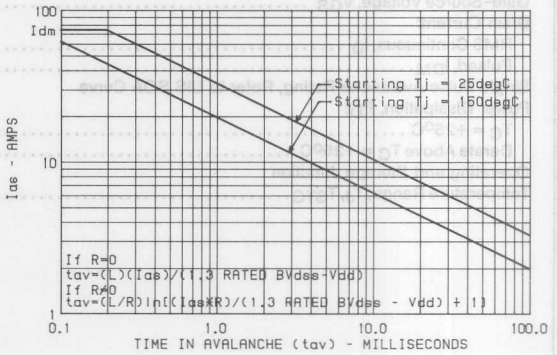


Figure 2 - Unclamped inductive-switching safe-operating-area curve. (Single pulse UIS SOA). See Figure 13 for test circuit.

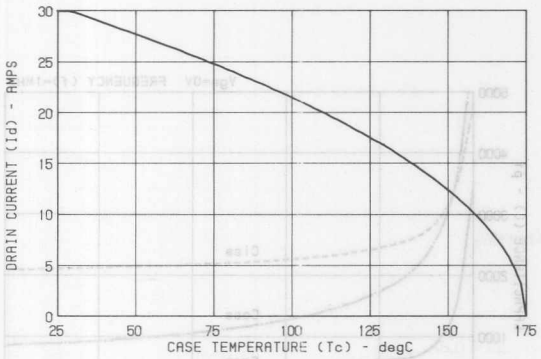


Figure 3 - Maximum continuous drain current vs case temperature.

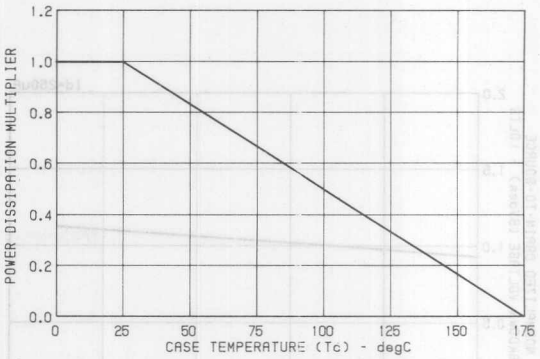


Figure 4 - Normalized power dissipation vs case temperature.



Figure 5 - Typical saturation characteristics.

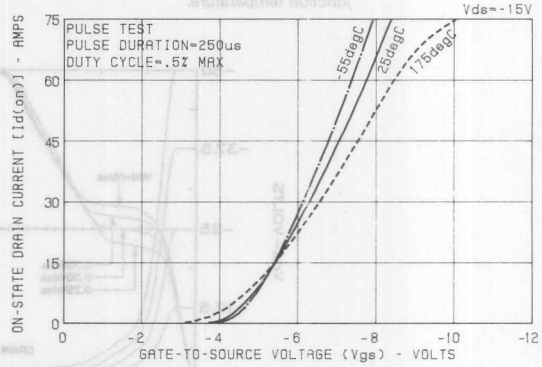


Figure 6 - Typical transfer characteristics.

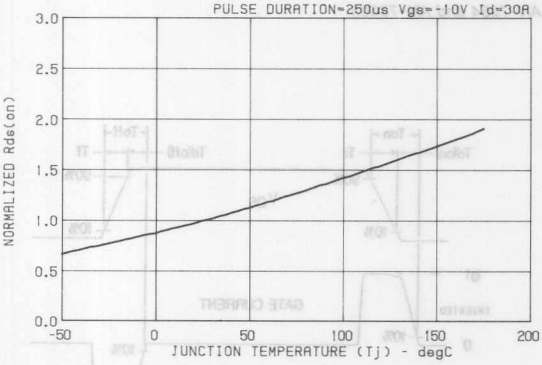


Figure 7 - Normalized on-state resistance vs junction temperature.

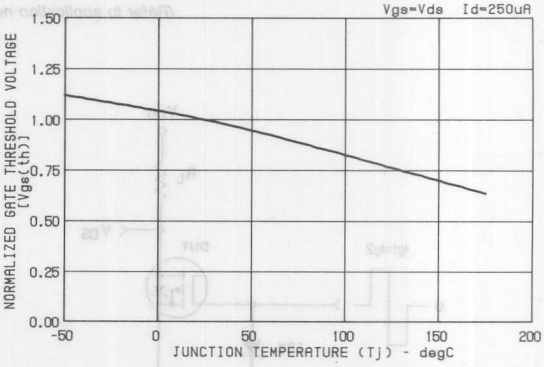


Figure 8 - Normalized gate threshold voltage vs junction temperature.

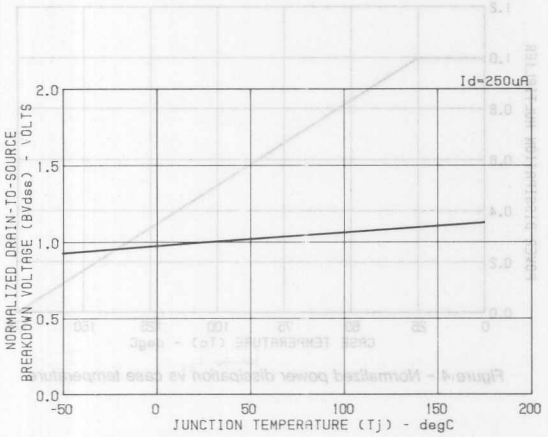


Figure 9 – Normalized drain source breakdown voltage vs junction temperature.

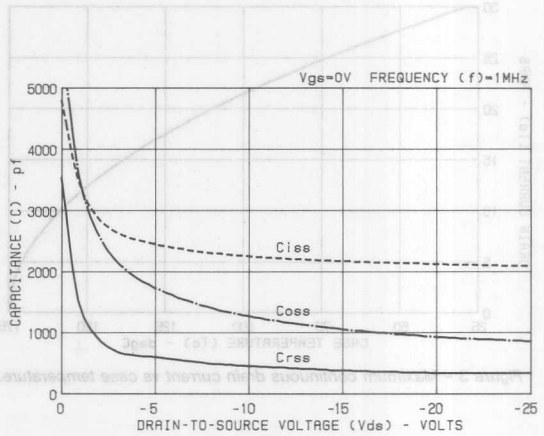


Figure 10 – Typical capacitance vs voltage.

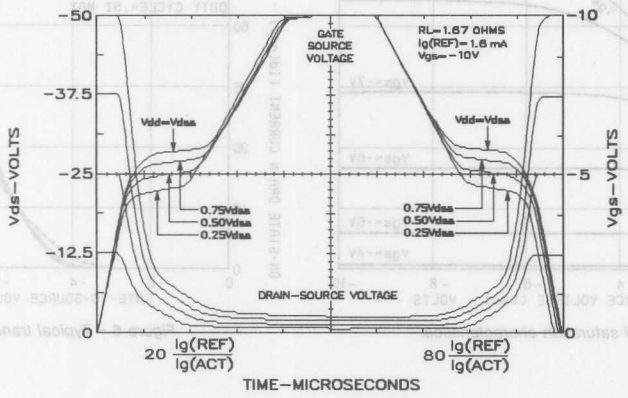
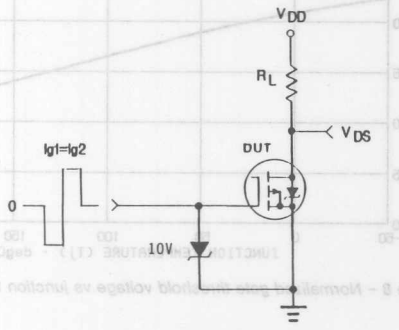
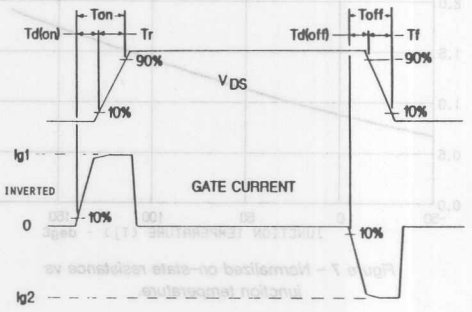


Figure 11 – Normalized switching waveforms for constant gate current.
(Refer to application notes AN-7254 and AN-7260.)

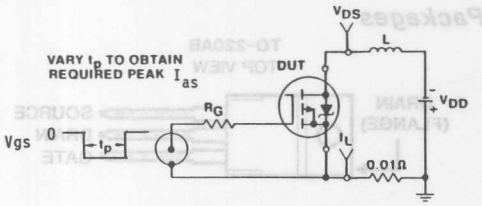


Switching Test Circuit

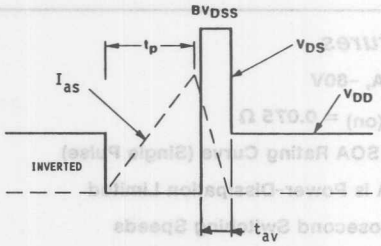


Switching Waveforms

Figure 12 – Resistive switching.



UIS Test Circuit



UIS Waveforms

Figure 13 – Unclamped-inductive-switching test.

HARRIS

RFG30P06
RFP30P06

P-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

August 1991

Features

- -30A, -60V
- $r_{DS(on)} = 0.075\ \Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 175°C Operating Temperature

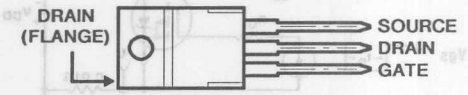
Description

The RFG30P06 and RFP30P06 p-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

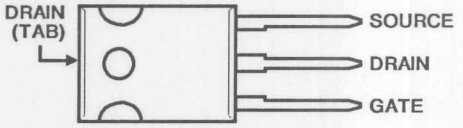
The RFG30P06 is supplied in the JEDEC TO-247 plastic package and the RFP30P06 in the TO-220AB plastic package.

Packages

TO-220AB
TOP VIEW

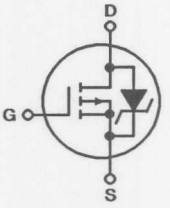


TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS}	-60V
Drain-Gate Voltage, ($R_{GS} = 1m\Omega$), V_{DGR}	-60V
Gate-Source Voltage, V_{GS}	±20V
Drain Current:	
RMS Continuous, I_D	-30A
Pulsed, I_{DM}	-75A
Single Pulse Avalanche Rating, Refer to UIS SOA Curve	
Power Dissipation, P_D:	
$T_C = +25^oC$	135W
Derate Above $T_C = +25^oC$	0.9W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55 to +175°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

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File Number **2437**

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V		-60	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25 mA		-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V		-	1	µA
		T_C = 150°C			50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V		-	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 30A, V_{GS} = -10V		-	0.075	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -30V, I_D = 15A Ig1 = Ig2 = 0.8A V_{GS} (clamp): -10V, +0.6V R_L = 2.0Ω		-	60	ns
Turn-On Delay Time	$t_{d(on)}$			15 (typ)	-	ns
Rise Time	t_r			23 (typ)	-	ns
Turn-Off Delay Time	$t_{d(off)}$			28 (typ)	-	ns
Fall Time	t_f			18 (typ)	-	ns
Turn-Off Time	$t_{(off)}$			-	100	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V	V_{DD} = -48V	-	200	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V	I_D = 30A	-	100	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V	R_L = 1.6Ω	-	7	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 30A, V_{DS} = -15V		-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -30V, I_D = 15A, R_L = 2.0Ω L = 0.2µH, Ig1 = Ig2 = 0.8A V_{GS} (clamp): -10V, +0.6V		-	75	µJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	1.11	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 30A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 30A, d_{ISD}/dt = 100A/µs	-	150	ns

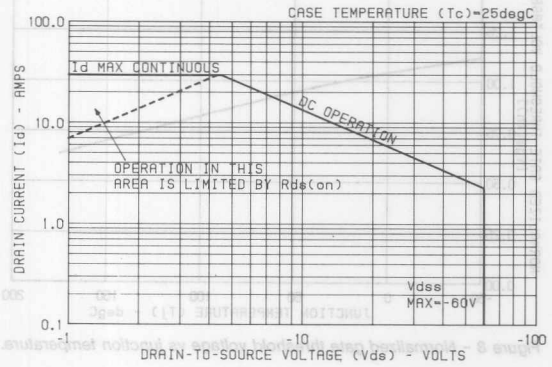


Figure 1 – Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

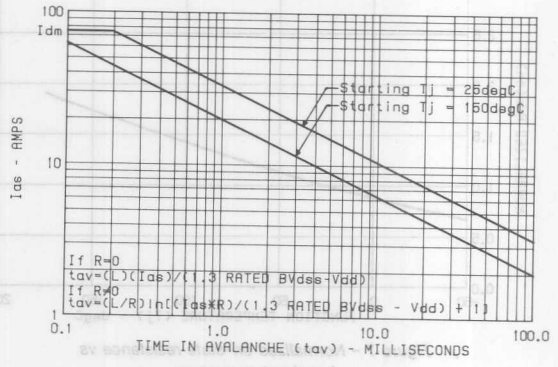


Figure 2 – Unclamped inductive-switching safe-operating-area curve. (Single pulse UIS SOA). See Figure 13 for test circuit.

5 P-CHANNEL POWER MOSFETs

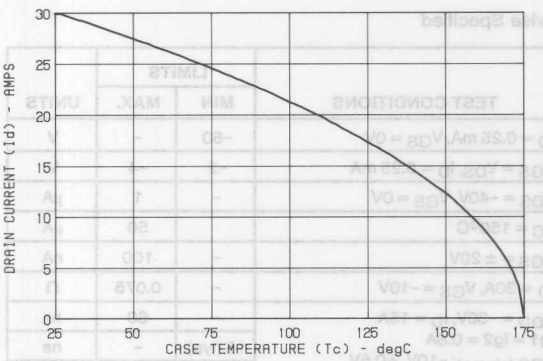


Figure 3 - Maximum continuous drain current vs case temperature.

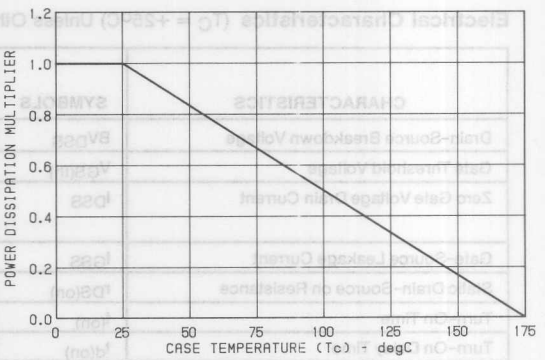


Figure 4 - Normalized power dissipation vs case temperature.

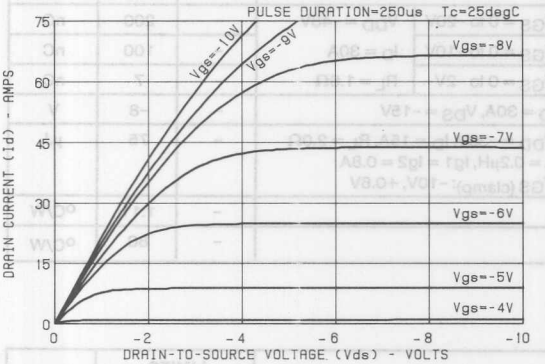


Figure 5 - Typical saturation characteristics.

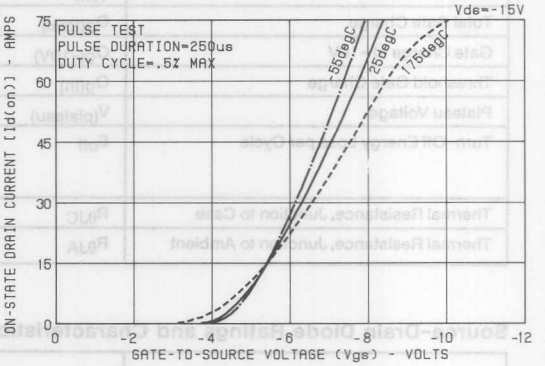


Figure 6 - Typical transfer characteristics.

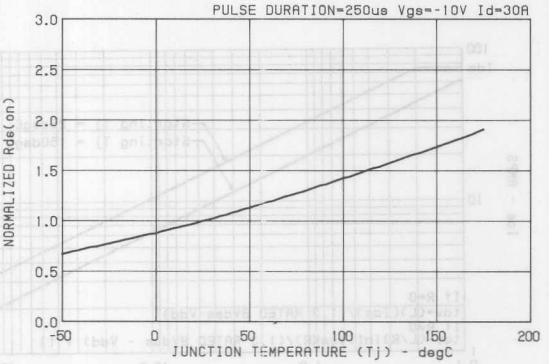


Figure 7 - Normalized on-state resistance vs junction temperature.

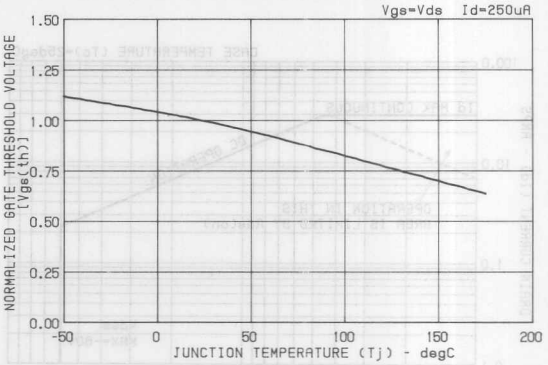


Figure 8 - Normalized gate threshold voltage vs junction temperature.

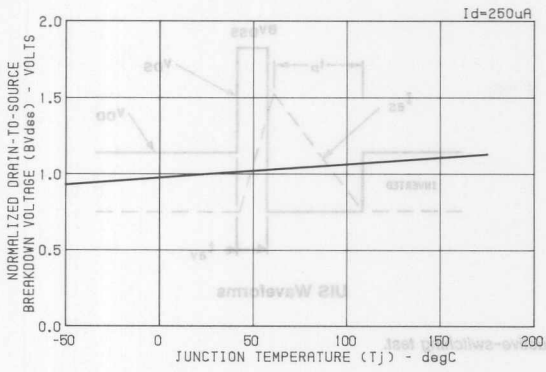


Figure 9 – Normalized drain source breakdown voltage vs junction temperature.

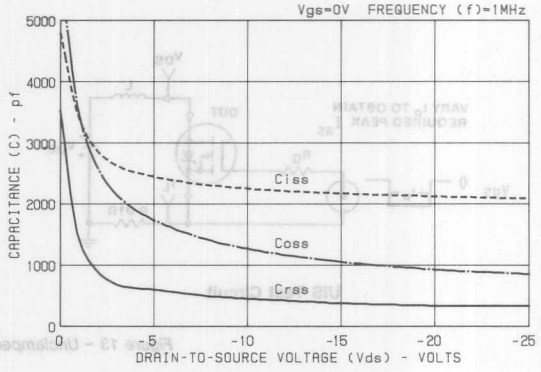


Figure 10 – Typical capacitance vs voltage.

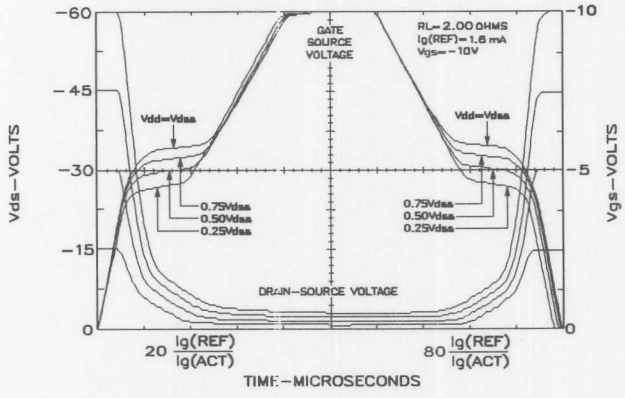


Figure 11 – Normalized switching waveforms for constant gate current. (Refer to application notes AN-7254 and AN-7260.)

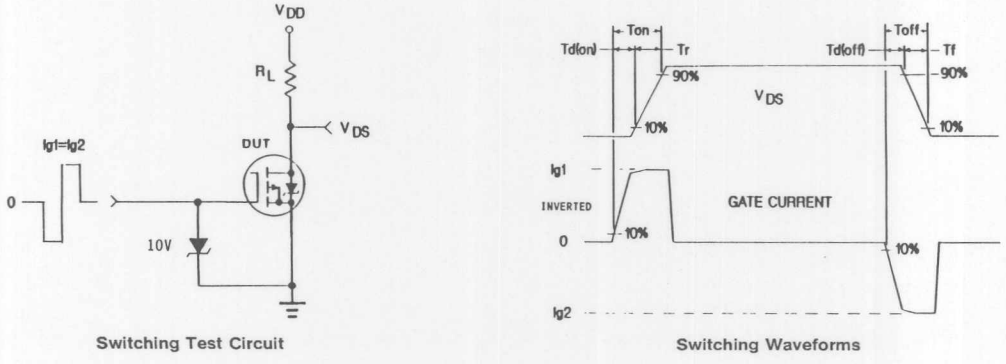
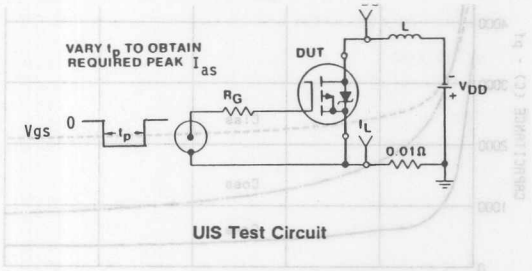
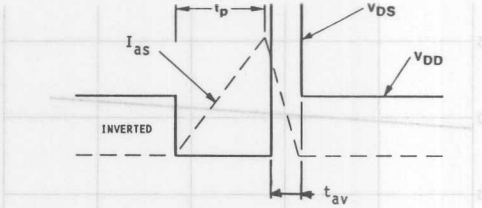


Figure 12 – Resistive switching.



UIS Test Circuit



UIS Waveforms

Figure 13 – Unclamped-inductive-switching test.

HARRIS

RFG60P05E
RFG60P06E

P-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

August 1991

Features

- RFG60P05E = -60A, -50V, $r_{DS(on)}$ = 0.026Ω
- RFG60P05E = -60A, -60V, $r_{DS(on)}$ = 0.030Ω
- Electrostatic Discharge Rated
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 175°C Operating Temperature

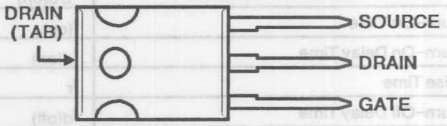
Description

The RFG60P05E and RFG60P06E p-channel ESD rated power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFG60P05E and RFG60P06E are supplied in the JEDEC TO-247 plastic package.

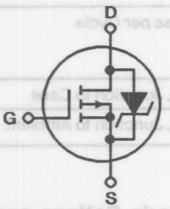
Package

TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		RFG60P05E	RFG60P06E	UNITS
Drain-Source Voltage	V_{DSS}	-50	-60	V
Drain-Gate Voltage (R_{GS} = 1mΩ)	V_{DGR}	-50	-60	V
Continuous Drain Current				
RMS Continuous	I_D	-60	-60	A
Pulsed Drain Current	I_{DM}	-150	-150	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	E_{SD}	2	2	KV
Single Pulse Avalanche Rating (Refer to UIS SOA Curve)				
Maximum Power Dissipation				
T_C = +25°C	P_D	190	215	W
Above T_C = +25°C, Derate Linearly		1.27	1.43	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2745.1

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V		-50	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25 mA		-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V		-	1	µA
		T_C = 150°C		-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V		-	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 60A, V_{GS} = -10V		-	0.026	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -25V, I_D = 30A Ig1 = Ig2 = 2.0A V_{GS} (clamp): -10V, +0.6V R_L = 0.83Ω		-	125	ns
Turn-On Delay Time	$t_{d(on)}$			20 (typ)	-	ns
Rise Time	t_r			70 (typ)	-	ns
Turn-Off Delay Time	$t_{d(off)}$			65 (typ)	-	ns
Fall Time	t_f			20 (typ)	-	ns
Turn-Off Time	$t_{(off)}$			-	125	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V	V_{DD} = -40V	-	450	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V	I_D = 60A	-	225	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V	R_L = 0.67Ω	-	15	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 60A, V_{DS} = -15V		-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -25V, I_D = 30A, R_L = 0.83Ω L = 0.2µH, Ig1 = Ig2 = 2.0A V_{GS} (clamp): -10V, +0.6V		-	300	µJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	0.79	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 60A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 60A, d_{ISD}/dt = 100A/µs	-	200	ns

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V	-60	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48V, V_{GS} = 0V	–	1	µA
		T_C = 150°C	–	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V	–	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 60A, V_{GS} = -10V	–	0.030	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -30V, I_D = 30A Ig1 = Ig2 = 2.0A V_{GS} (clamp): -10V, +0.6V R_L = 1.0Ω	–	125	ns
Turn-On Delay Time	$t_{d(on)}$		20 (typ)	–	ns
Rise Time	t_r		60 (typ)	–	ns
Turn-Off Delay Time	$t_{d(off)}$		65 (typ)	–	ns
Fall Time	t_f		20 (typ)	–	ns
Turn-Off Time	$t_{(off)}$		–	125	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V, V_{DD} = -48V	–	450	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V, I_D = 60A	–	225	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V, R_L = 0.8Ω	–	15	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 60A, V_{DS} = -15V	–	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -30V, I_D = 30A, R_L = 1.0Ω L = 0.2µH, Ig1 = Ig2 = 2.0A V_{GS} (clamp): -10V, +0.6V	–	300	µJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$		–	0.70	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$		–	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 60A	–	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 60A, d_{ISD}/dt = 100A/µs	–	200	ns

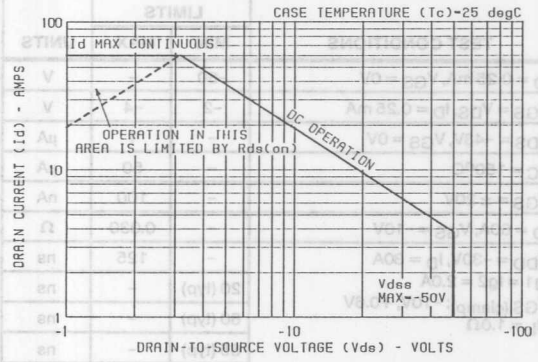


FIGURE 1. RFG60P05E - SAFE OPERATING AREA CURVE

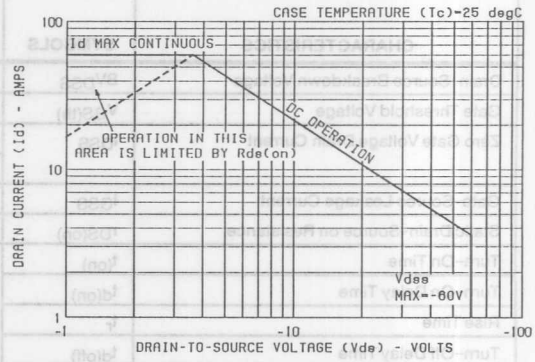


FIGURE 2. RFG60P06E - SAFE OPERATING AREA CURVE

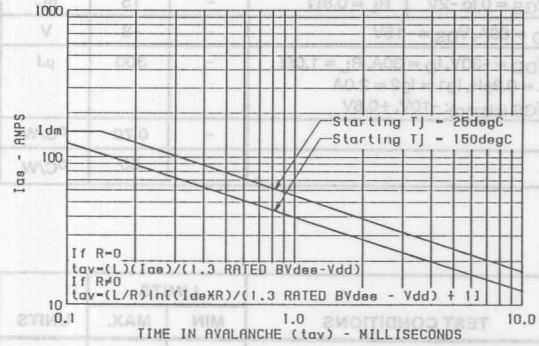


FIGURE 3. RFG60P05E - UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

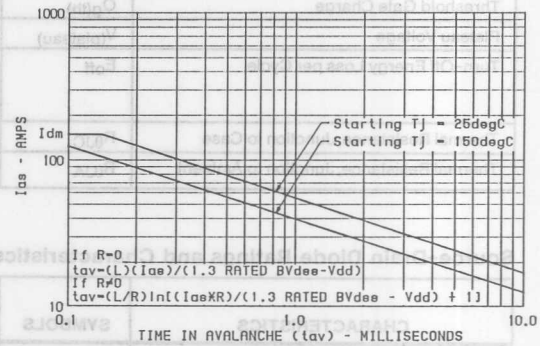


FIGURE 4. RFG60P06E - UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

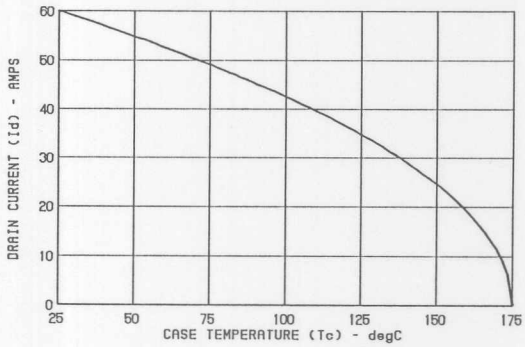


FIGURE 5. MAXIMUM CONTINUOUS DRAIN CURRENT VS TEMPERATURE

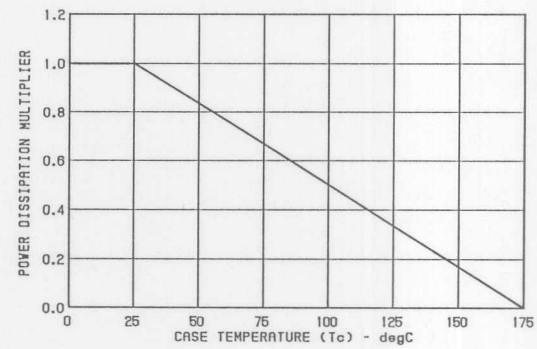


FIGURE 6. NORMALIZED POWER DISSIPATION VS TEMPERATURE

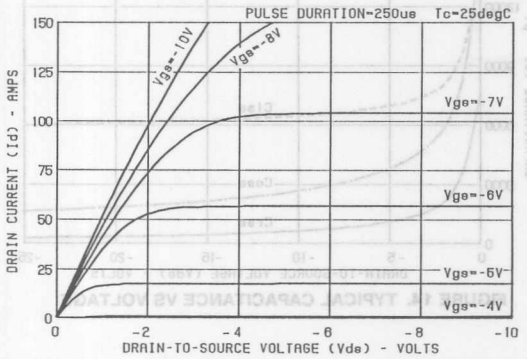


FIGURE 7. RFG60P05E - TYPICAL SATURATION CHARACTERISTICS

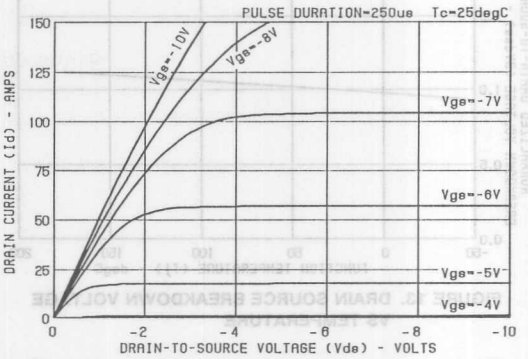


FIGURE 8. RFG60P06E - TYPICAL SATURATION CHARACTERISTICS

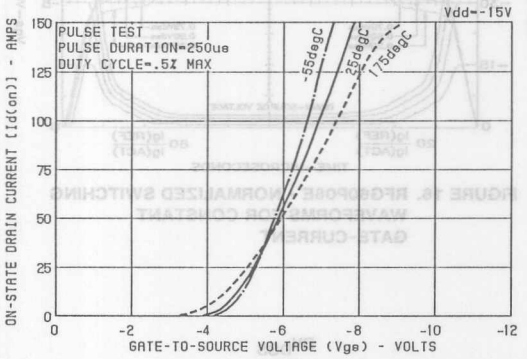


FIGURE 9. RFG60P05E - TYPICAL TRANSFER CHARACTERISTICS

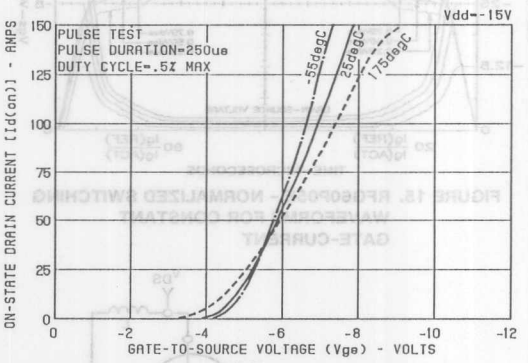


FIGURE 10. RFG60P06E - TYPICAL TRANSFER CHARACTERISTICS

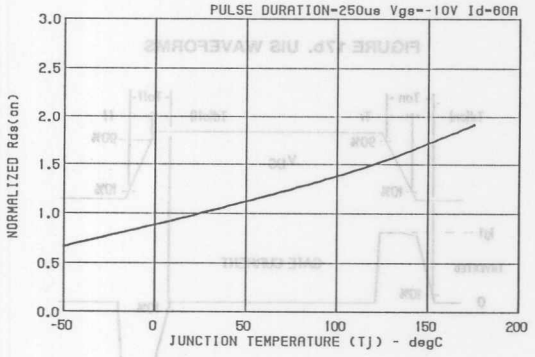


FIGURE 11. NORMALIZED $r_{DS(ON)}$ VS JUNCTION TEMPERATURE

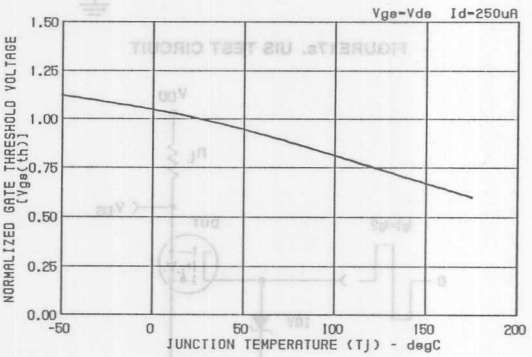


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE

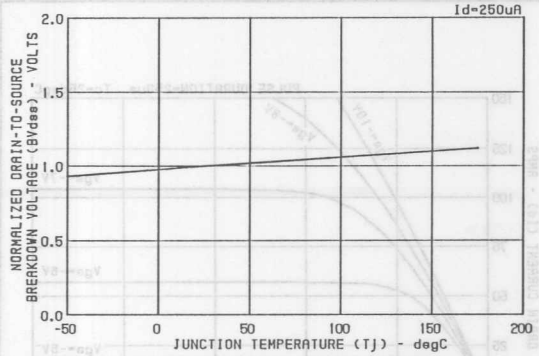


FIGURE 13. DRAIN SOURCE BREAKDOWN VOLTAGE VS TEMPERATURE

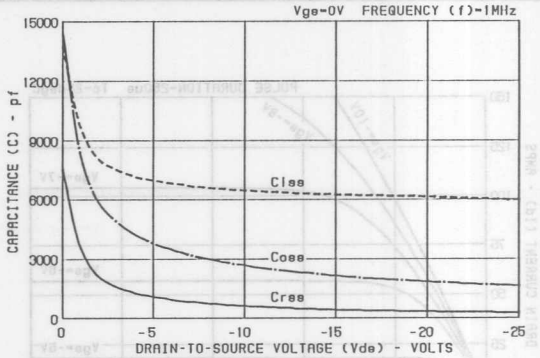


FIGURE 14. TYPICAL CAPACITANCE VS VOLTAGE

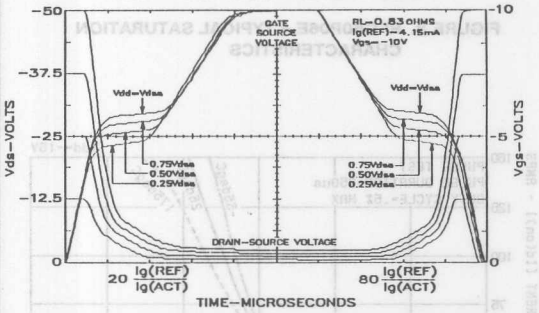


FIGURE 15. RFG60P05E - NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT

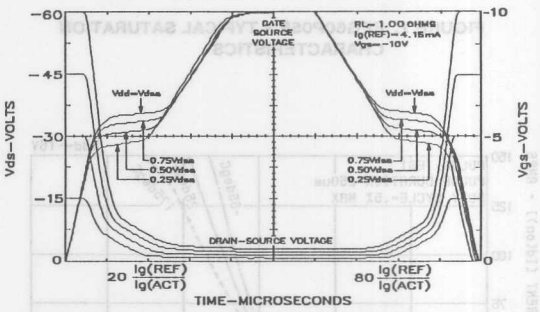


FIGURE 16. RFG60P06E - NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT

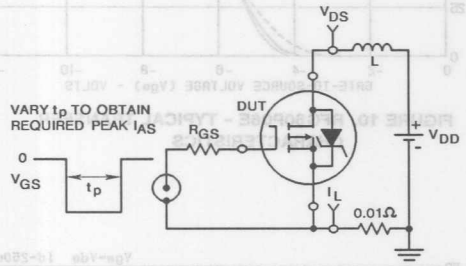


FIGURE17a. UIS TEST CIRCUIT

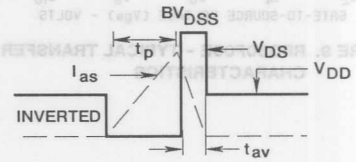


FIGURE 17b. UIS WAVEFORMS

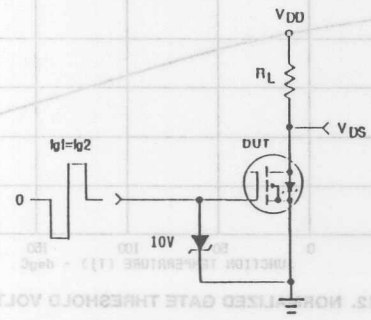


FIGURE 18a. SWITCHING TEST CIRCUIT

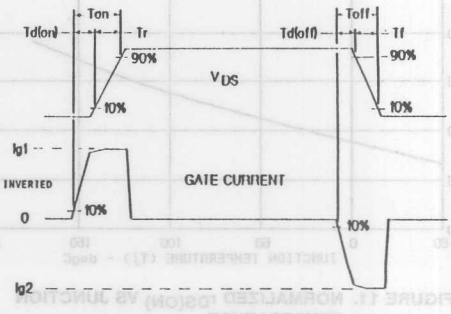


FIGURE 18b. SWITCHING WAVEFORMS

POWER MOSFETs 6

LOGIC LEVEL POWER MOSFETs

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RFD3055RLESM
RFP3055RLE

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2N6901

N-Channel Logic Level Power MOS Field-Effect Transistors (L^2FET)

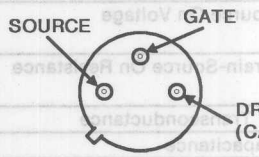
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Features

- 1.69A, 100V
- $r_{DS(on)} = 1.4\Omega$
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

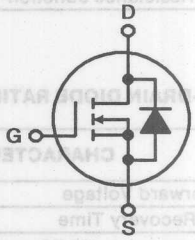
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Description

The 2N6901 is an N-channel enhancement-mode silicon-gate power MOS field-effect transistor specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, therefore facilitating true on-off power control directly from logic circuit supply voltages.

The 2N6901 is supplied in the JEDEC TO-205AF metal package.

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		2N6901	UNITS
Drain-Source Voltage	V_{DS}	100*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	100*	V
Continuous Drain Current			
T_C = +25°C	I_D	1.69*	A
Pulsed Drain Current	I_{DM}	5*	A
Gate-Source Voltage	V_{GS}	±10*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	8.33*	W
Above T_C = +25°C, Derate Linearly		0.0667*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering	T_L	260*	°C
At distance > 1/8 in. (3.17mm) from seating plane for 10s max			

*JEDEC registered values

6 LOGIC LEVEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1877.1

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V	—	1	μA
			T_C = 125°C, V_{DS} = 80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 1.07 A, V_{GS} = 5 V	—	1.5	V
			I_D = 1.69 A, V_{GS} = 5 V	—	2.4	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 1.07 A, V_{GS} = 5 V	—	1.4	Ω
			T_C = 125°C, I_D = 1.07 A, V_{GS} = 5 V	—	2.6	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = 5 V, I_D = 1.07 A	500	2000	mmho
*	Input Capacitance	C_{iss}	V_{DS} = 25 V	50	200	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	20	80	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	5	20	
*	Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	—	25	ns
*	Rise Time	t_r	I_D = 1.07 A	—	45	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	45	
*	Fall Time	t_f	V_{GS} = 5 V	—	80	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1.69 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 1 A, d_{IF}/dt = 50 A/μs	—	250	ns

*In accordance with JEDEC registration data.
[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

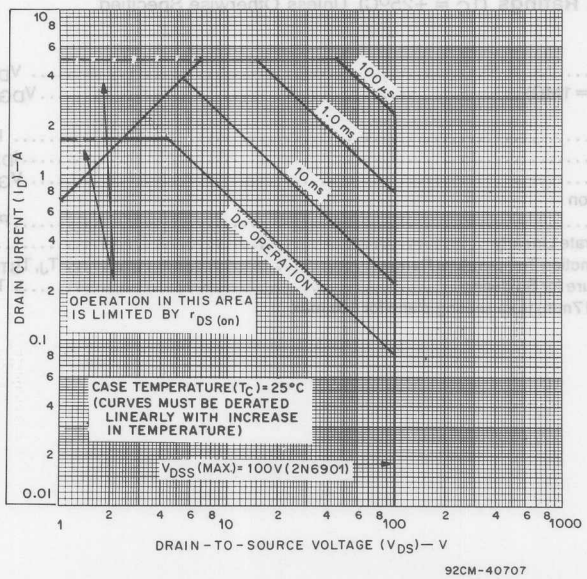


Fig. 1 - Maximum operating areas.

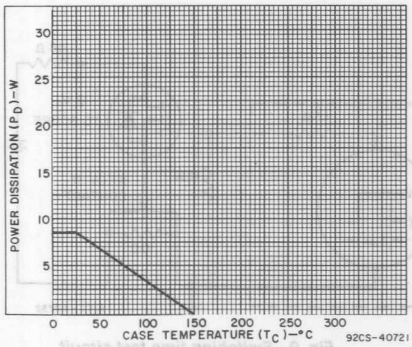


Fig. 2 - Power dissipation vs. temperature derating curve.

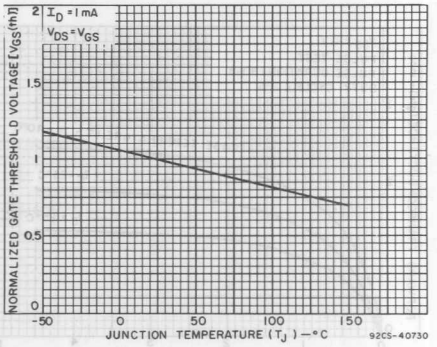


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

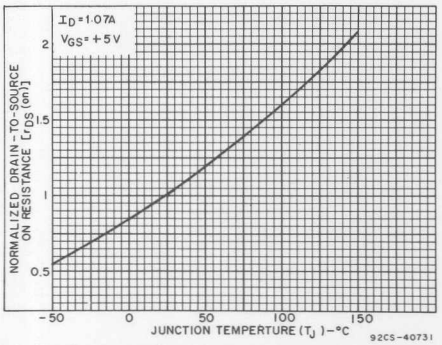


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

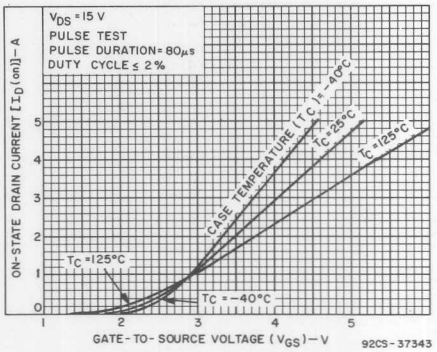


Fig. 5 - Typical transfer characteristics.

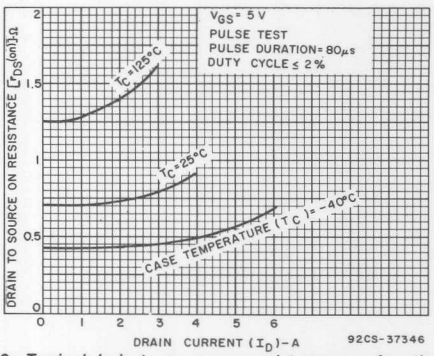


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

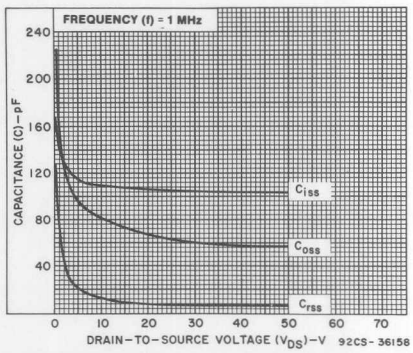


Fig. 7 - Capacitance as a function of drain-to-source voltage.

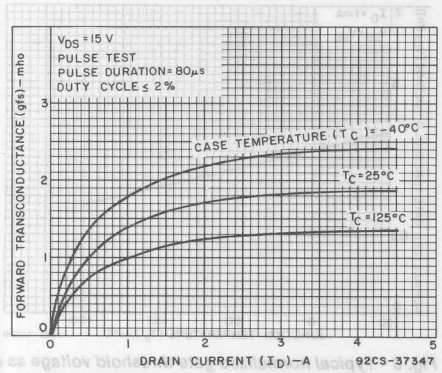


Fig. 8 - Typical forward transconductance as a function of drain current.

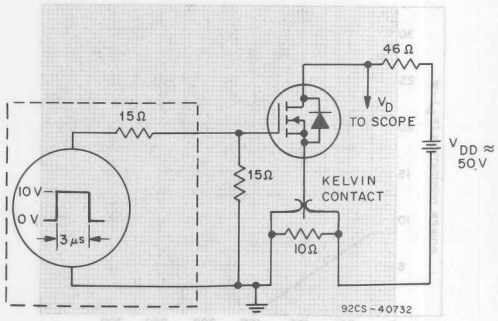


Fig. 9 - Switching time test circuit.

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2N6902

August 1991

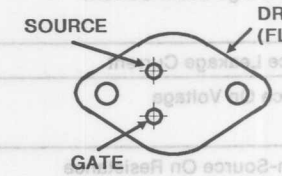
N-Channel Logic Level Power MOS Field-Effect Transistors (L^2FET)

Features

- 12A, 100V
- $r_{DS(on)} = 0.2\Omega$
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

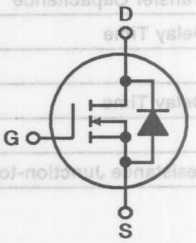
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Description

The 2N6901 is an N-channel enhancement-mode silicon-gate power MOS field-effect transistor specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, therefore facilitating true on-off power control directly from logic circuit supply voltages.

The 2N6902 is supplied in the JEDEC TO-204AA steel package.

Absolute Maximum Ratings ($T_C = +25^oC$), Unless Otherwise Specified

		2N6902	UNITS
Drain-Source Voltage	V_{DS}	100*	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	100*	V
Continuous Drain Current			
$T_C = +25^oC$	I_D	12*	A
Pulsed Drain Current	I_{DM}	30*	A
Gate-Source Voltage	V_{GS}	±10*	V
Maximum Power Dissipation			
$T_C = +25^oC$	P_D	75*	W
Above $T_C = +25^oC$, Derate Linearly		0.6*	$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	^oC
Maximum Lead Temperature for Soldering	T_L	260*	^oC
At distance > 1/8 in. (3.17mm) from seating plane for 10s max			

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1878.1

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C = 25°C) unless otherwise specified

	CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V	—	1	μA
			T_C = 125°C, V_{DS} = 80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 7.6 A, V_{GS} = 5 V	—	1.52	V
			I_D = 12 A, V_{GS} = 5 V	—	3.3	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 7.6 A	—	0.2	Ω
			T_C=125°C, I_D=7.6 A, V_{GS}=5 V	—	0.32	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = 5 V, I_D = 7.6 A	3	12	mho
*	Input Capacitance	C_{iss}	V_{DS} = 25 V	350	900	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	100	325	
*	Reverse-Transfer Capacitance	C_{rss}	f = 0.1 MHz	25	100	
*	Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	—	50	ns
*	Rise Time	t_r	I_D = 7.6 V	—	150	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	130	
*	Fall Time	t_f	V_{GS} = 5 V	—	150	
*	Thermal Resistance Junction-to-Case	$R\theta_{JC}$		—	1.67	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 12 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A d_{IF}/d_t = 100 A/μs	—	375	ns

* In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs, max., duty cycle = 2%.

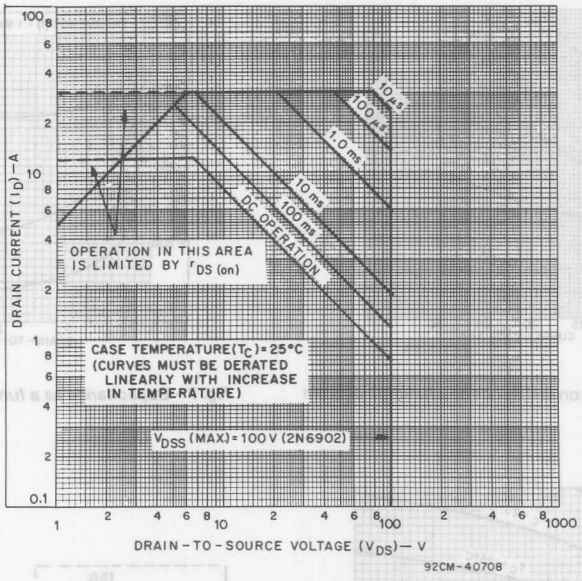


Fig. 1 - Maximum safe operating areas.

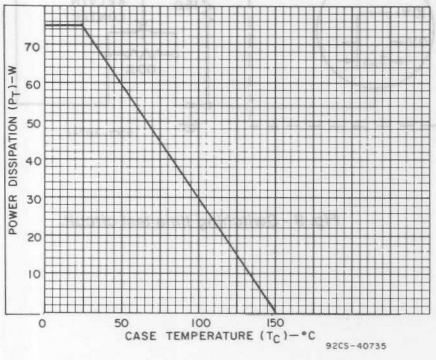


Fig. 2 - Power dissipation vs. temperature derating curve.

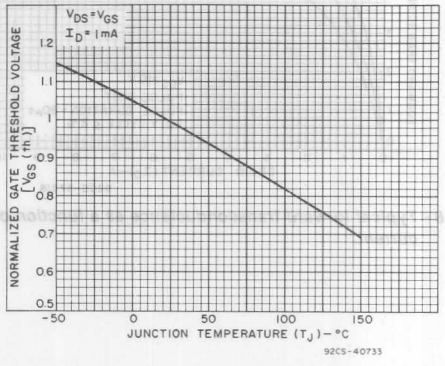


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

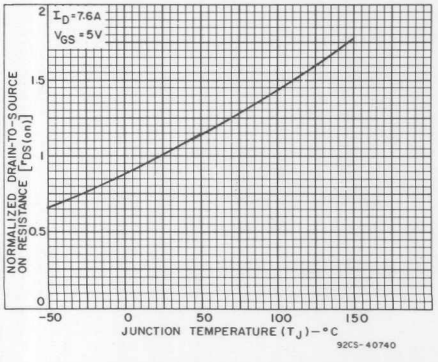


Fig. 4 - Typical normalized drain-to-source on resistance to

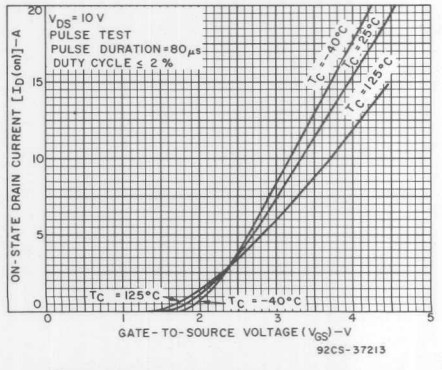


Fig. 5 - Typical transfer characteristics.

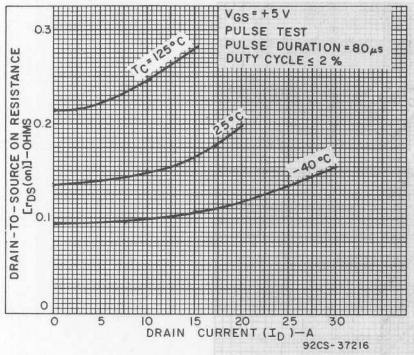


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

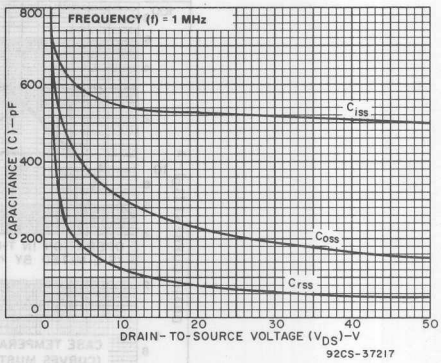


Fig. 7 - Capacitance as a function of drain-to-source voltage.

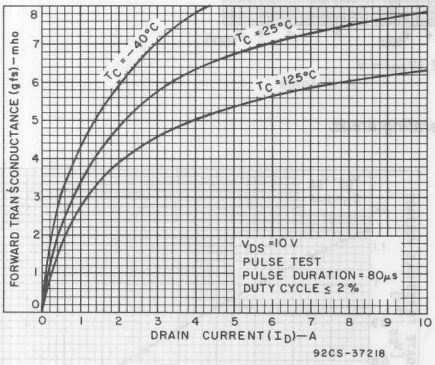


Fig. 8 - Typical forward transconductance as a function of drain current.

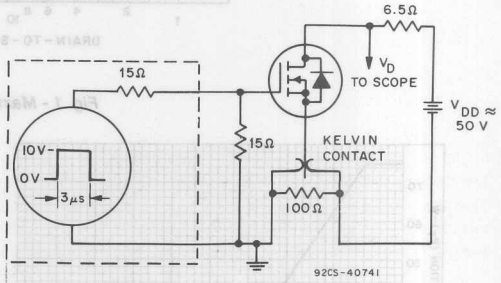


Fig. 9 - Switching time test circuit.

HARRIS

2N6903

N-Channel Logic Level Power MOS Field-Effect Transistors (L^2FET)

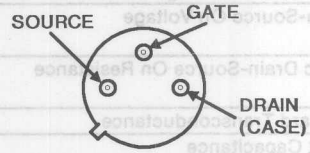
August 1991

Features

- 0.98A, 100V
- $r_{DS(on)} = 3.65\Omega$
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

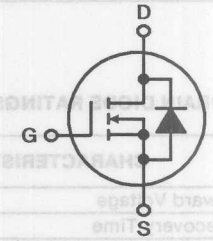
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Description

The 2N6903 is an N-channel enhancement-mode silicon-gate power MOS field-effect transistor specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, therefore facilitating true on-off power control directly from logic circuit supply voltages.

The 2N6903 is supplied in the JEDEC TO-205AF metal package.

Absolute Maximum Ratings ($T_C = +25^oC$), Unless Otherwise Specified

		2N6903	UNITS
Drain-Source Voltage	V_{DS}	200*	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	200*	V
Continuous Drain Current			
$T_C = +25^oC$	I_D	0.98*	A
Pulsed Drain Current	I_{DM}	4*	A
Gate-Source Voltage	V_{GS}	±10*	V
Maximum Power Dissipation			
$T_C = +25^oC$	P_D	8.33*	W
Above $T_C = +25^oC$, Derate Linearly		0.0667*	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	^{o}C
Maximum Lead Temperature for Soldering	T_L	260*	^{o}C
At distance > 1/8 in. (3.17mm) from seating plane for 10s max			

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1879.1

	CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
				Min.	Max.	
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	200	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V	—	1	μA
			T_C = 125°C, V_{DS} = 160 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 0.62 A, V_{GS} = 5 V	—	2.26	V
			I_D = 0.98 A, V_{GS} = 5 V	—	6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 0.62 A, V_{GS} = 5 V	—	3.65	Ω
			T_C = 125°C, I_D = 0.62 A, V_{GS} = 5 V	—	7.7	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = 5 V, I_D = 0.62 A	500	2000	mmho
*	Input Capacitance	C_{iss}	V_{DS} = 25 V	50	200	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	15	60	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	2	20	
*	Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V	—	25	ns
*	Rise Time	t_r	I_D = 0.62 A	—	30	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	40	
*	Fall Time	t_f	V_{GS} = 5 V	—	80	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
				Min.	Max.	
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 0.98 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 1 A, d_{IF}/dt = 50 A/μs	—	500	ns

*In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

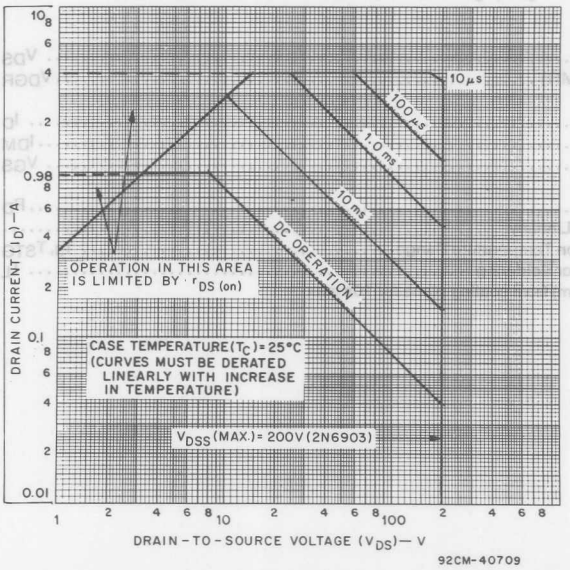


Fig. 1 - Maximum operating areas.

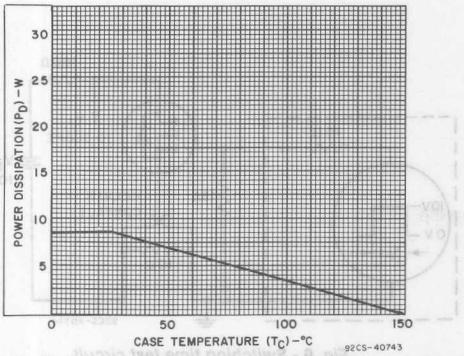


Fig. 2 - Power dissipation vs. temperature derating curve.

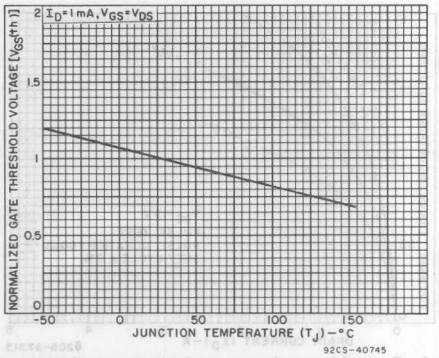


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

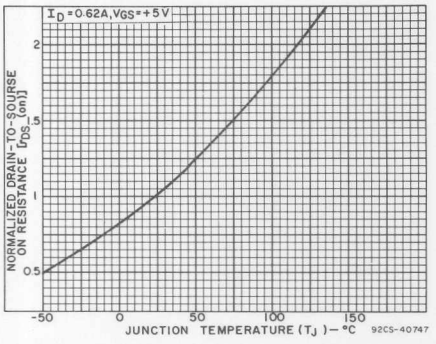


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

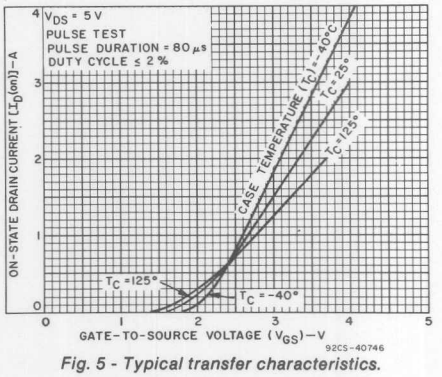


Fig. 5 - Typical transfer characteristics.

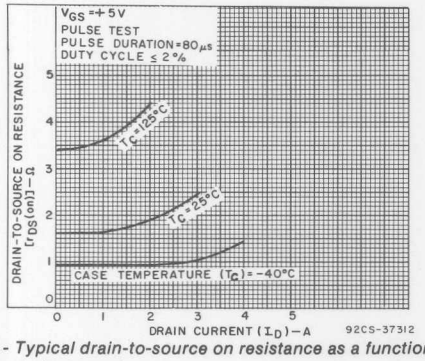


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

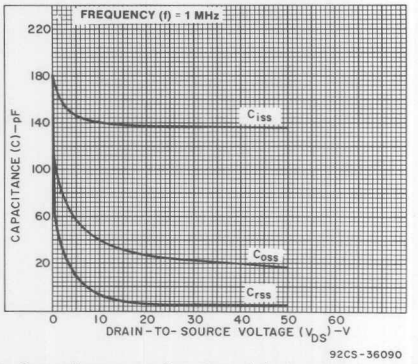


Fig. 7 - Capacitance as a function of drain-to-source voltage.

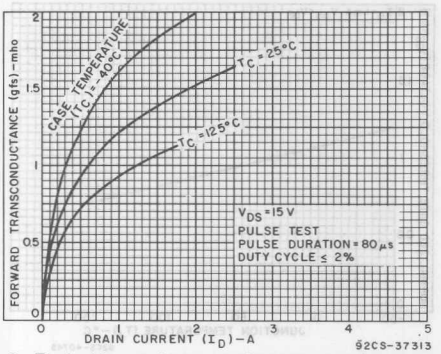


Fig. 8 - Typical forward transconductance as a function of drain current.

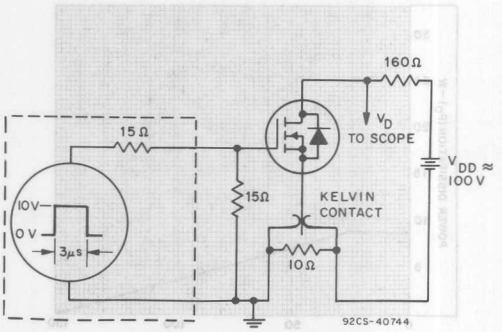


Fig. 9 - Switching time test circuit.

HARRIS

2N6904

N-Channel Logic Level Power MOS Field-Effect Transistors (L^2FET)

August 1991

Features

- 8A, 200V
- $r_{DS(on)} = 0.6\Omega$
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

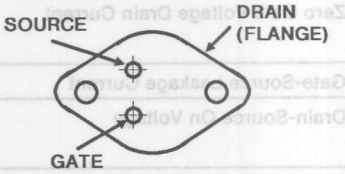
Description

The 2N6904 is an N-channel enhancement-mode silicon-gate power MOS field-effect transistor specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, therefore facilitating true on-off power control directly from logic circuit supply voltages.

The 2N6904 is supplied in the JEDEC TO-204AA steel package.

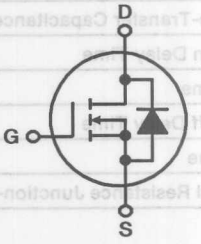
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		2N6904	UNITS
Drain-Source Voltage	V_{DS}	200*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	200*	V
Continuous Drain Current			
T_C = +25°C	I_D	8*	A
Pulsed Drain Current	I_{DM}	20*	A
Gate-Source Voltage	V_{GS}	±10*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	75*	W
Above T_C = +25°C, Derate Linearly		0.6*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering	T_L	260*	°C
At distance > 1/8 in. (3.17mm) from seating plane for 10s max			

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1880.1

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C = 25°C) unless otherwise specified

	CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	200	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V	—	1	μA
			T_C = 125°C, V_{DS} = 160 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5.1 A, V_{GS} = 5 V	—	3.06	V
			I_D = 8 A, V_{GS} = 5 V	—	5.5	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5.1 A	—	0.6	Ω
			T_C=125°C, I_D=5.1 A, V_{GS}=5 V	—	1.11	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = 5 V, I_D = 5.1 A	3	12	mho
*	Input Capacitance	C_{iss}	V_{DS} = 25 V	350	900	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	75	250	
*	Reverse-Transfer Capacitance	C_{rss}	f = 0.1 MHz	20	100	
*	Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V	—	45	ns
*	Rise Time	t_r	I_D = 5.1 A	—	150	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	135	
*	Fall Time	t_f	V_{GS} = 5 V	—	150	
*	Thermal Resistance Junction-to-Case	$R\theta_{JC}$		—	1.67	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 8 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/d_t = 100 A/μs	—	625	ns

* In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs, max., duty cycle = 2%.

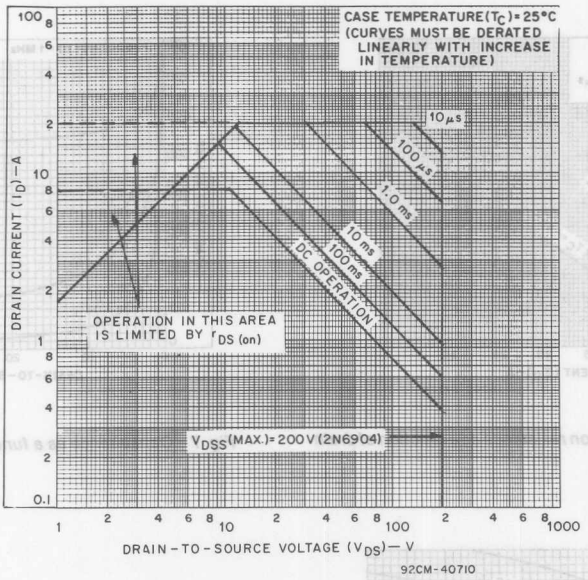


Fig. 1 - Maximum safe operating areas.

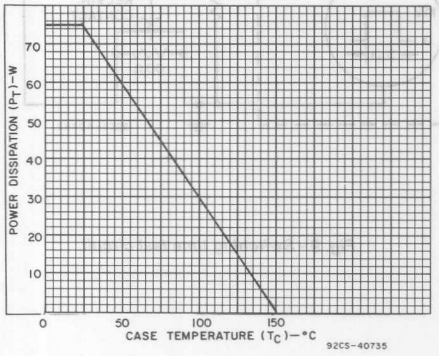


Fig. 2 - Power dissipation vs. temperature derating curve.

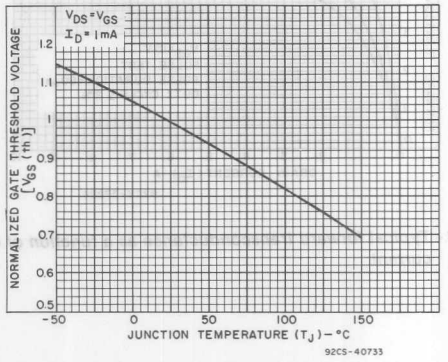
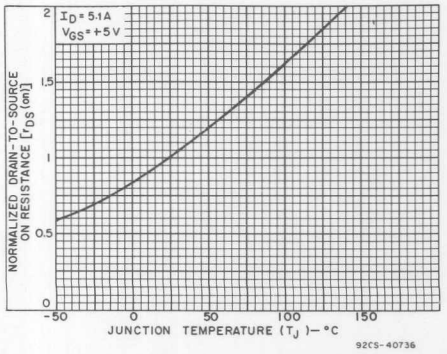
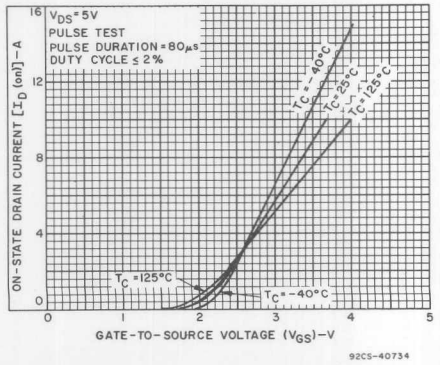


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.





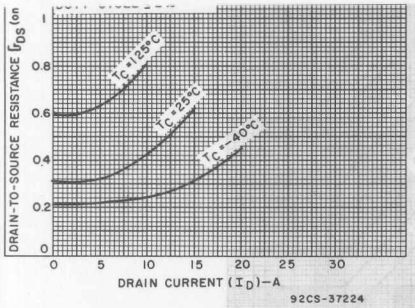


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

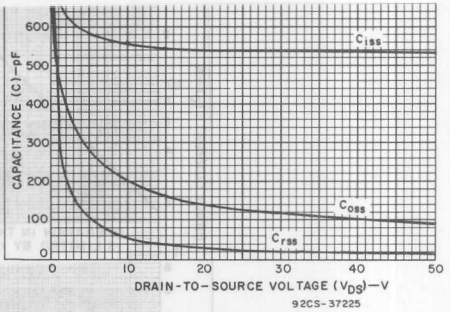


Fig. 7 - Capacitance as a function of drain-to-source voltage.

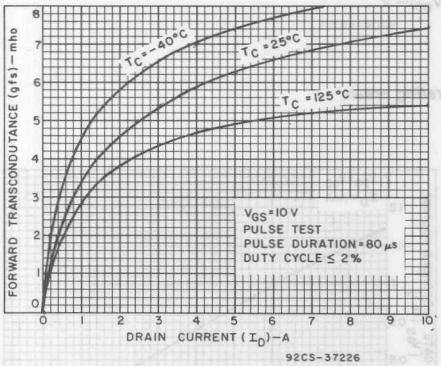


Fig. 8 - Typical forward transconductance as a function of drain current.

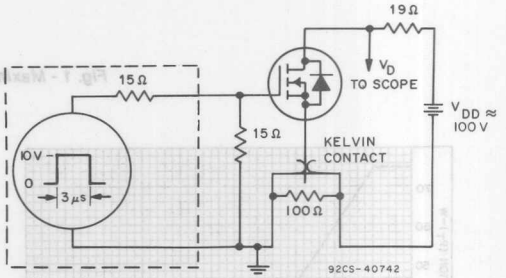


Fig. 9 - Switching time test circuit.

HARRIS

RFL1N08L
RFL1N10L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 1A, 80V and 100V
- $r_{DS(ON)} = 1.2\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

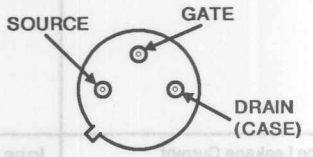
Description

The RFL1N08L and RFL1N10L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL series types are supplied in the JEDEC TO-205AF steel package.

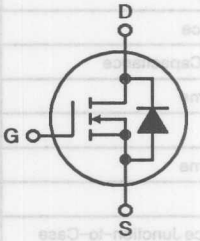
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		RFL1N08L	RFL1N10L	UNITS
Drain-Source Voltage	V_{DS}	80	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	80	100	V
Continuous Drain Current				
RMS Continuous	I_D	1	1	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
T_C = +25°C	P_D	8.33	8.33	W
Above T_C = +25°C, Derate Linearly		0.0667	0.0667	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1510.1

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL1N08L MIN	LIMITS RFL1N08L MAX	LIMITS RFL1N10L MIN	LIMITS RFL1N10L MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	80	–	100	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V	–	1	–	–	µA
		V_{DS} = 80V	–	–	–	1	µA
		T_C = +125°C, V_{DS} = 65V	–	50	–	–	µA
		V_{DS} = 80V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.2	–	1.2	V
		I_D = 2A, V_{GS} = 5V	–	2.9	–	2.9	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.2	–	1.2	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse Transfer Capacitance	C_{RSS}		–	35	–	35	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 50V, R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	25	10 (typ)	25	ns
Rise Time	t_r		15 (typ)	45	15 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		25 (typ)	45	25 (typ)	45	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

* Pulsed: Pulse duration = 300µs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL1N08L MIN	LIMITS RFL1N08L MAX	LIMITS RFL1N10L MIN	LIMITS RFL1N10L MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = –1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/µs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulse Test: Width ≤ 300µs, Duty Cycle ≤ 2%.

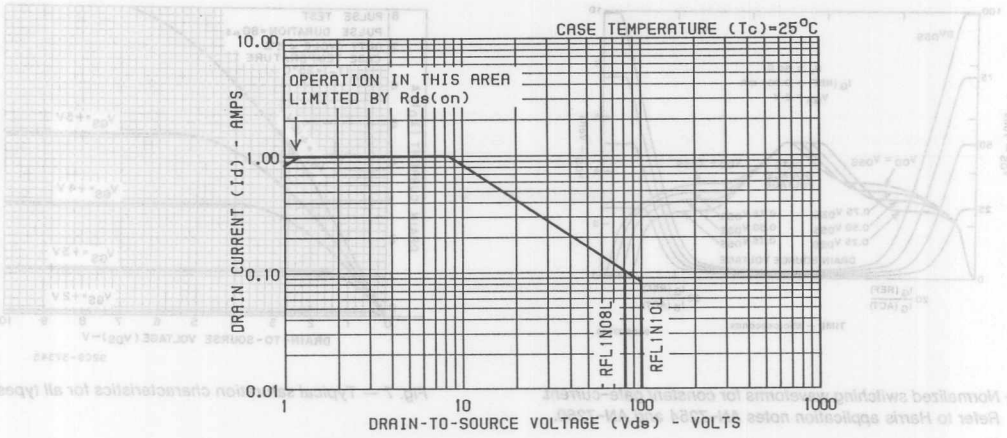


Fig. 1 — Maximum operating areas for all types.

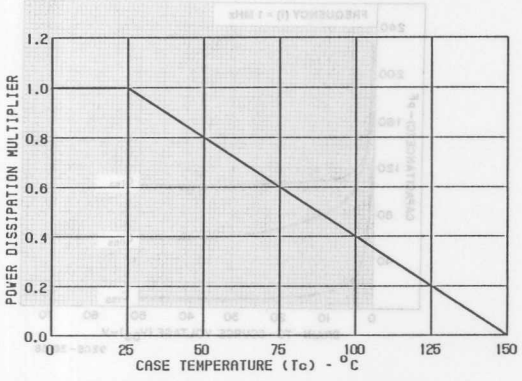


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

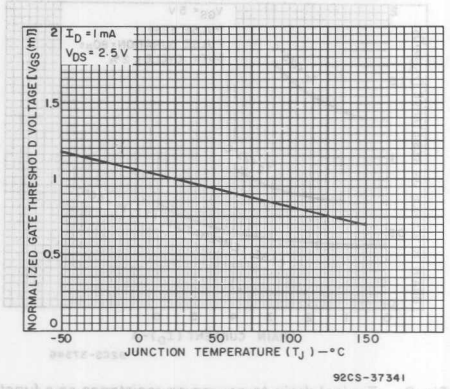


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

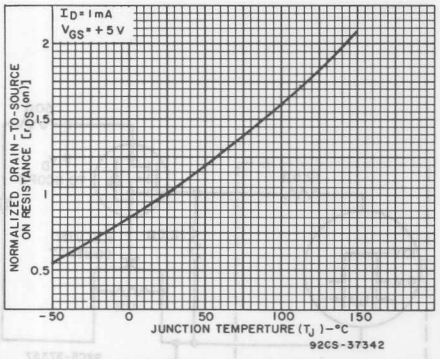


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

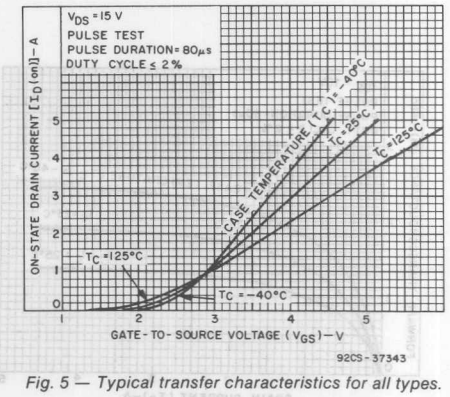


Fig. 5 — Typical transfer characteristics for all types.

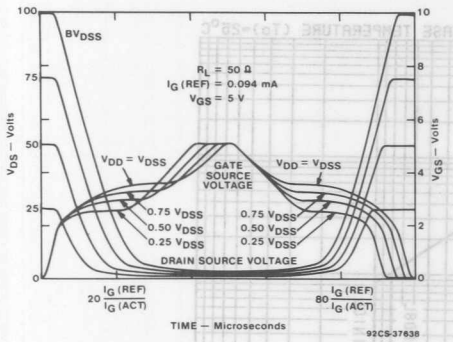


Fig 6. – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

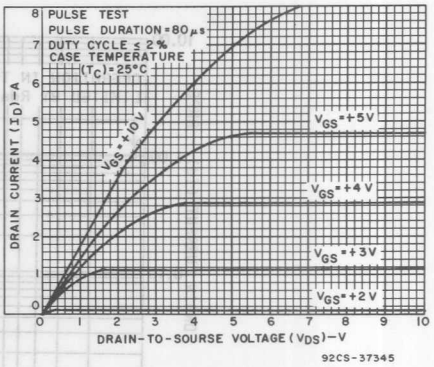


Fig. 7 — Typical saturation characteristics for all types.

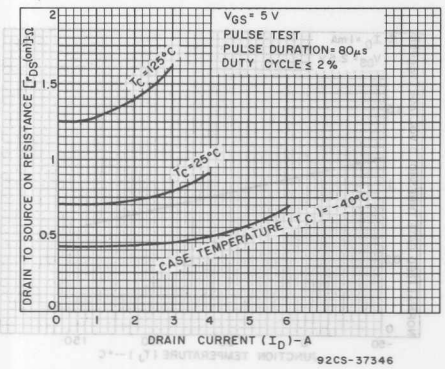


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

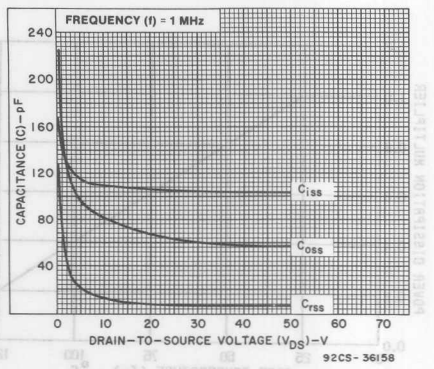


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

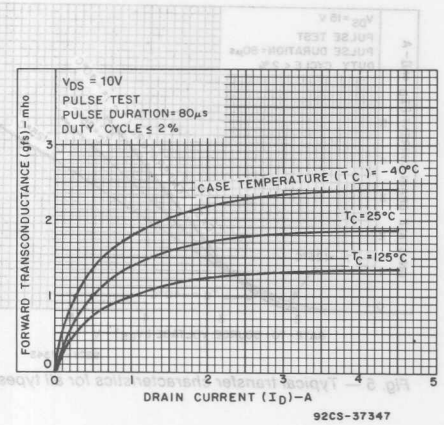


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

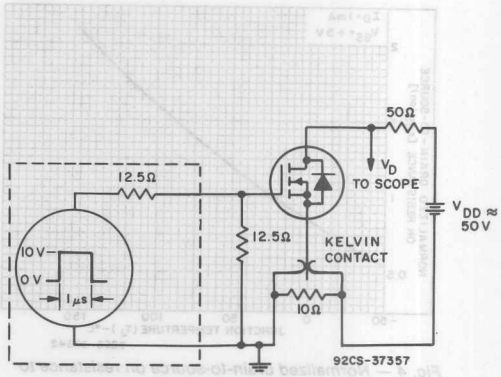


Fig. 11 — Switching Time Test Circuit.

RFL1N12L
RFL1N15L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

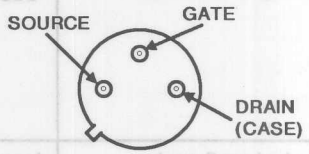
August 1991

Features

- 1A, 120V and 150V
- $r_{DS(ON)} = 1.9\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

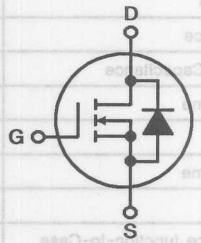
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Description

The RFL1N12L and RFL1N15L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL series types are supplied in the JEDEC TO-205AF metal package.

Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFL1N12L	RFL1N15L	UNITS
Drain-Source Voltage	V_{DS}	120	150	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	120	150	V
Continuous Drain Current				
RMS Continuous	I_D	1	1	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	8.33	8.33	W
Above $T_C = +25^oC$, Derate Linearly		0.0667	0.0667	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1513.1

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL1N12L MIN	LIMITS RFL1N12L MAX	LIMITS RFL1N15L MIN	LIMITS RFL1N15L MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	120	–	150	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V	–	1	–	–	μA
		V_{DS} = 120V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 100V	–	50	–	–	μA
		V_{DS} = 120V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.9	–	1.9	V
		I_D = 2A, V_{GS} = 5V	–	4.6	–	4.6	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.9	–	1.9	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse Transfer Capacitance	C_{RSS}		–	35	–	35	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 75V, R_{GEN} = ∞, R_{GS} = 6.25Ω, V_{GS} = 5V	10 (typ)	25	10 (typ)	25	ns
Rise Time	t_r		10 (typ)	45	10 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		24 (typ)	45	24 (typ)	45	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL1N12L MIN	LIMITS RFL1N12L MAX	LIMITS RFL1N15L MIN	LIMITS RFL1N15L MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, dI_F/dt = 50A/μs	150 (typ)	150 (typ)	150 (typ)	150 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

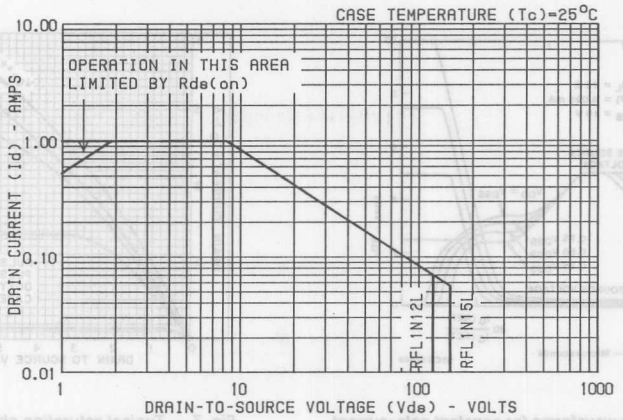


Fig. 1 — Maximum operating areas for all types.

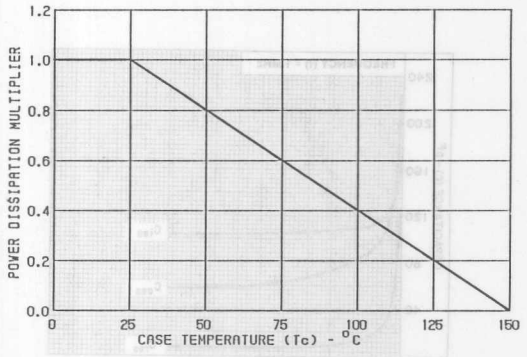


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

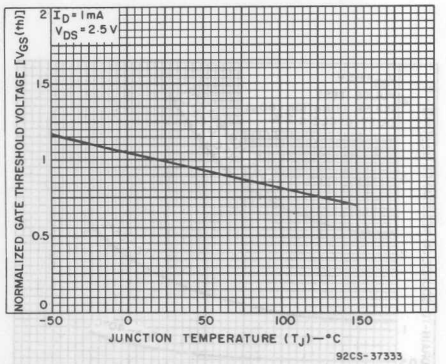


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

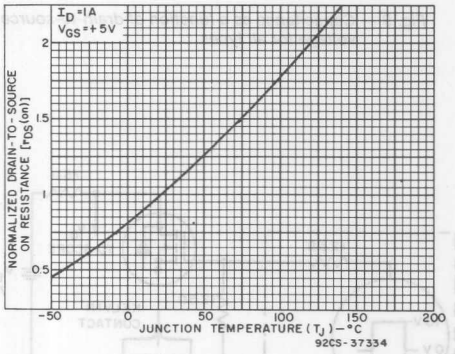


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

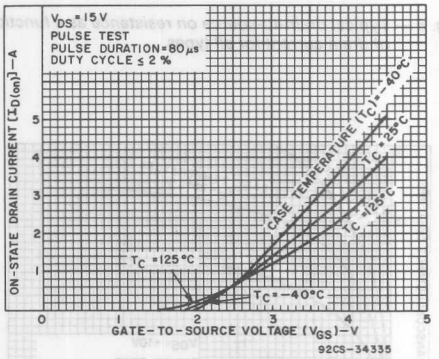


Fig. 5 — Typical transfer characteristics for all types.

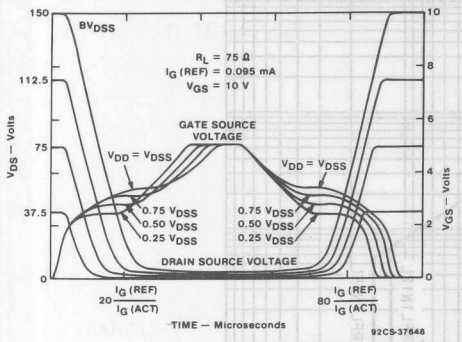


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

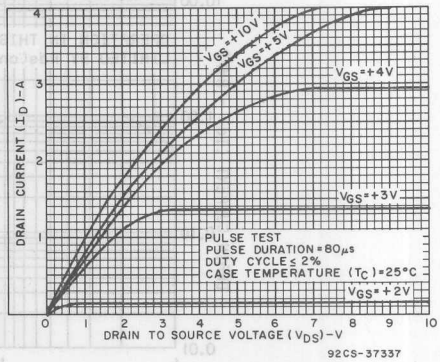


Fig. 7 — Typical saturation characteristics for all types.

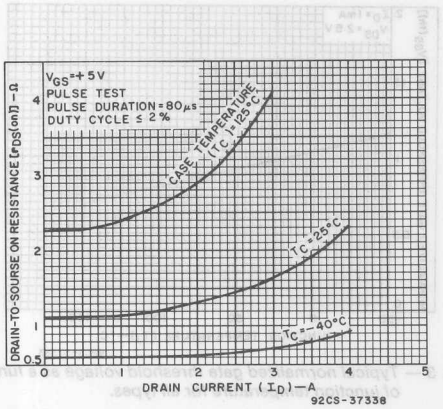


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

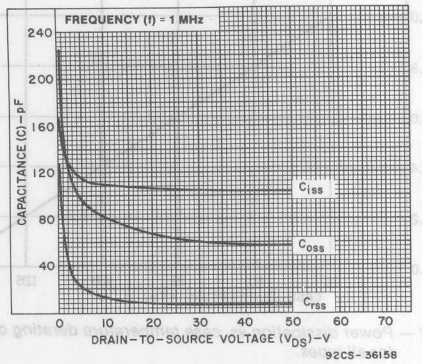


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

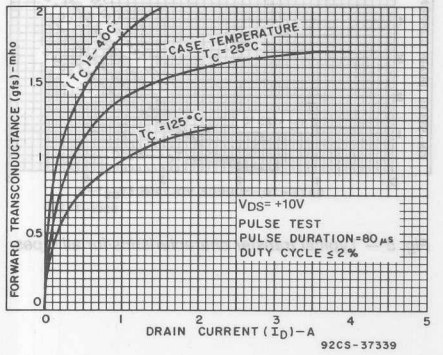


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

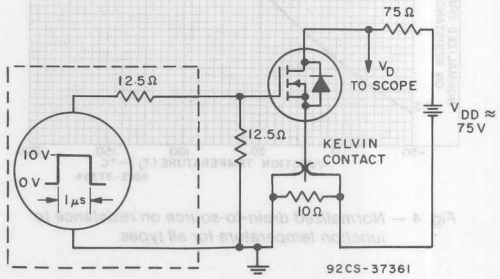


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFL1N18L
RFL1N20L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 1A, 180V and 200V
- $r_{DS(ON)} = 3.65\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

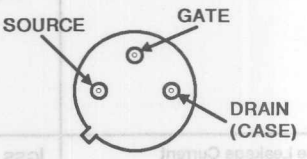
Description

The RFL1N18L and RFL1N20L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL series types are supplied in the JEDEC TO-205AF metal package.

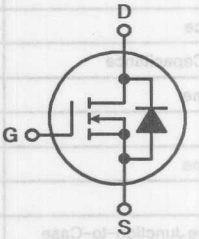
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFL1N18L	RFL1N20L	UNITS
Drain-Source Voltage	V_{DS}	180	200	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	180	200	V
Continuous Drain Current				
RMS Continuous	I_D	1	1	A
Pulsed Drain Current	I_{DM}	4	4	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	8.33	8.33	W
Above $T_C = +25^oC$, Derate Linearly		0.0667	0.0667	W/°C
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1511.1

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL1N18L MIN	LIMITS RFL1N18L MAX	LIMITS RFL1N20L MIN	LIMITS RFL1N20L MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	180	–	200	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145V	–	1	–	–	µA
		V_{DS} = 160V	–	–	–	1	µA
		T_C = +125°C, V_{DS} = 145V	–	50	–	–	µA
		V_{DS} = 160V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	3.65	–	3.65	V
		I_D = 2A, V_{GS} = 5V	–	9.3	–	9.3	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	3.65	–	3.65	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	60	–	60	pF
Reverse Transfer Capacitance	C_{RSS}		–	35	–	35	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 100V, R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	25	10 (typ)	25	ns
Rise Time	t_r		10 (typ)	30	10 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		25 (typ)	40	25 (typ)	40	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

* Pulsed: Pulse duration = 300µs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL1N18L MIN	LIMITS RFL1N18L MAX	LIMITS RFL1N20L MIN	LIMITS RFL1N20L MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/µs	200 (typ)	200 (typ)	200 (typ)	200 (typ)	ns

* Pulse Test: Width ≤ 300µs, Duty Cycle ≤ 2%.

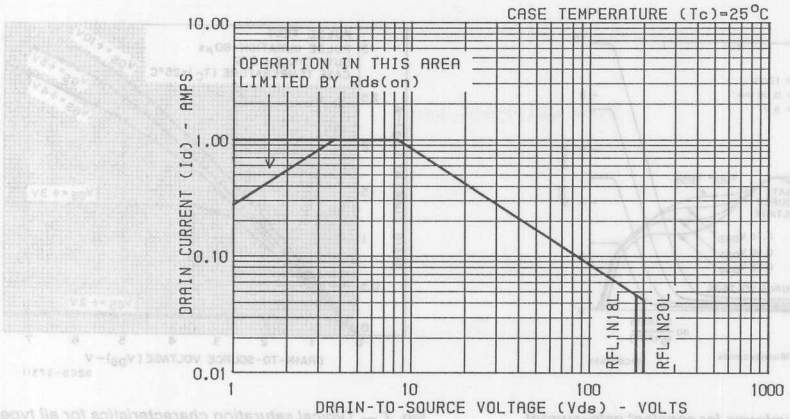


Fig. 1 — Maximum operating areas for all types.

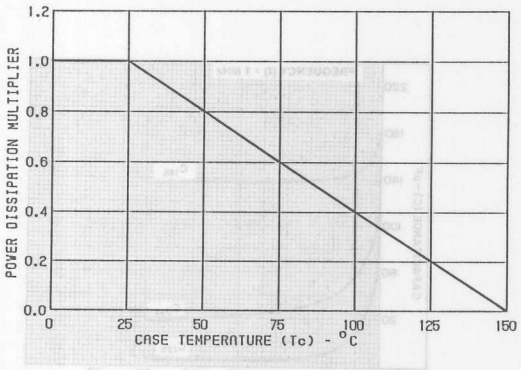


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

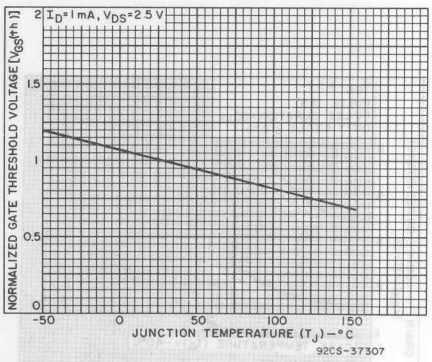


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

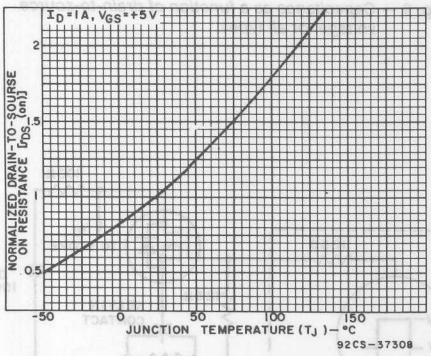


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

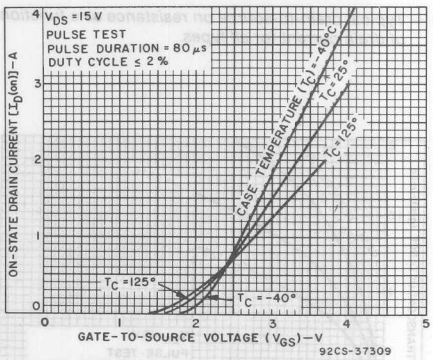


Fig. 5 — Typical transfer characteristics for all types.

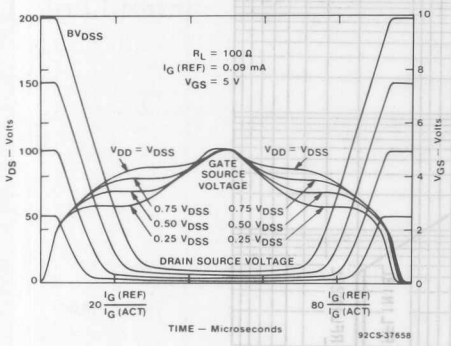


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

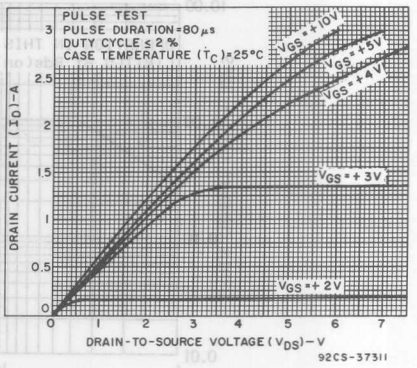


Fig. 7 — Typical saturation characteristics for all types.

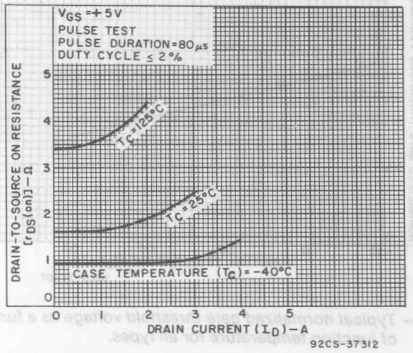


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

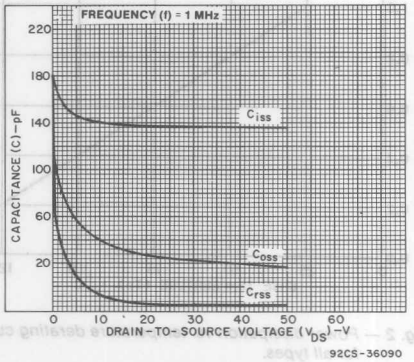


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

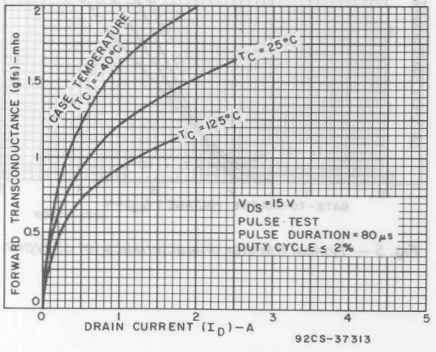


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

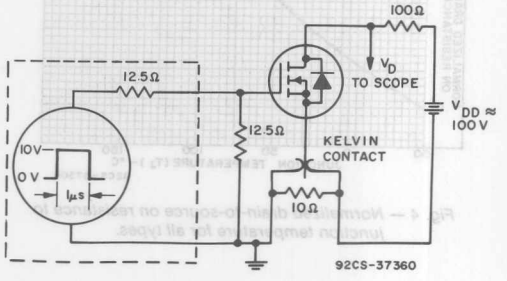


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFL2N05L
RFL2N06L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 2A, 50V and 60V
- $r_{DS(ON)} = 0.95\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

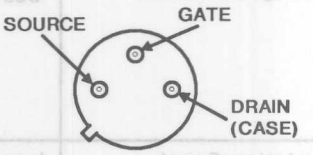
Description

The RFL2N05L and RFL2N06L are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL series types are supplied in the JEDEC TO-205AF metal package.

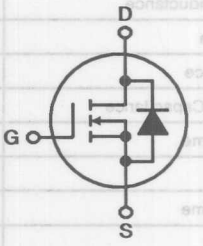
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFL2N05L	RFL2N06L	UNITS
Drain-Source Voltage	V_{DS}	50	50	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	50	60	V
Continuous Drain Current				
RMS Continuous	I_D	2	2	A
Pulsed Drain Current	I_{DM}	10	10	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	8.33	8.33	W
Above $T_C = +25^oC$, Derate Linearly		0.0667	0.0667	W/°C
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1560.1**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL2N05L MIN	LIMITS RFL2N05L MAX	LIMITS RFL2N06L MIN	LIMITS RFL2N06L MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	50	–	60	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V	–	1	–	–	μA
		V_{DS} = 50V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 40V	–	50	–	–	μA
		V_{DS} = 50V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	0.95	–	0.95	V
		I_D = 2A, V_{GS} = 5V	–	2.0	–	2.0	V
		I_D = 4A, V_{GS} = 7.5V	–	4.8	–	4.8	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	0.95	–	0.95	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	225	–	225	pF
Output Capacitance	C_{OSS}		–	100	–	100	pF
Reverse Transfer Capacitance	C_{RSS}		–	40	–	40	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 30V, R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	20	10 (typ)	20	ns
Rise Time	t_r		65 (typ)	130	65 (typ)	130	ns
Turn-Off Delay Time	$t_{d(off)}$		20 (typ)	40	20 (typ)	40	ns
Fall Time	t_f		30 (typ)	60	30 (typ)	60	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFL2N05L MIN	LIMITS RFL2N05L MAX	LIMITS RFL2N06L MIN	LIMITS RFL2N06L MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 100A/μs	150 (typ)	150 (typ)	150 (typ)	150 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

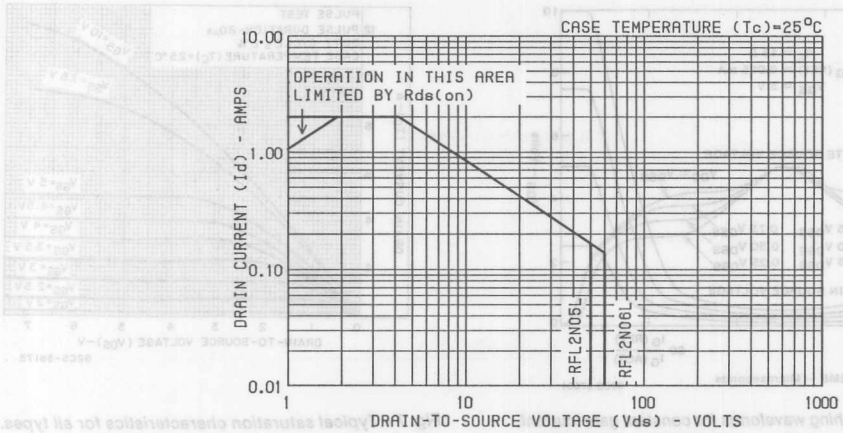


Fig. 1 - Maximum operating areas for all types.

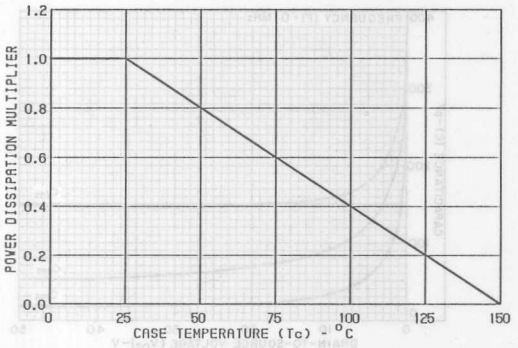


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

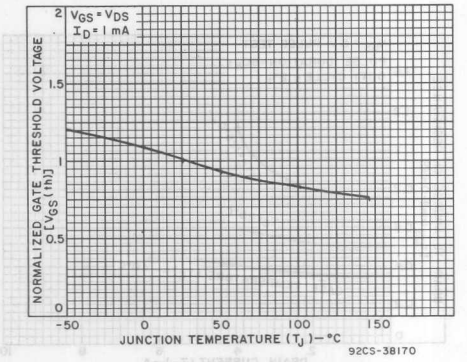


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

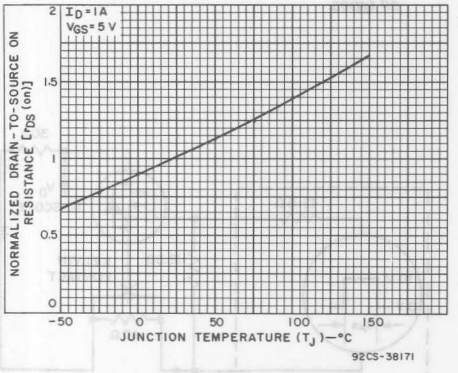


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

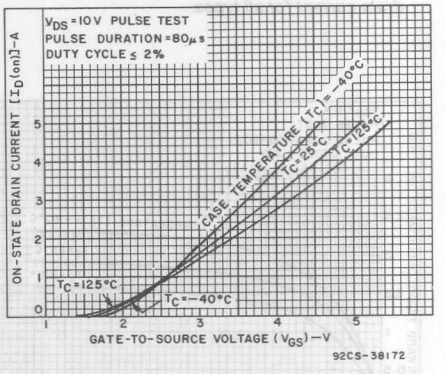


Fig. 5 - Typical transfer characteristics for all types.

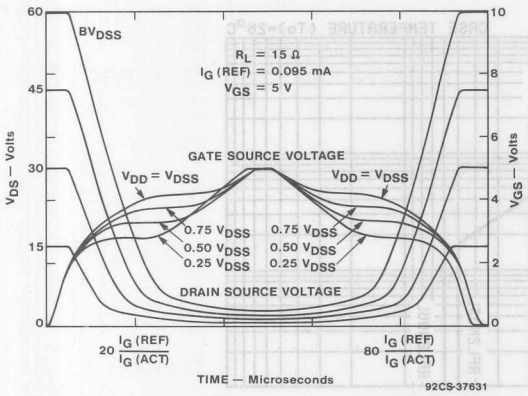


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

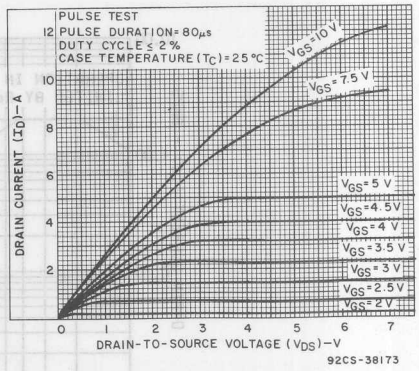


Fig. 7 - Typical saturation characteristics for all types.

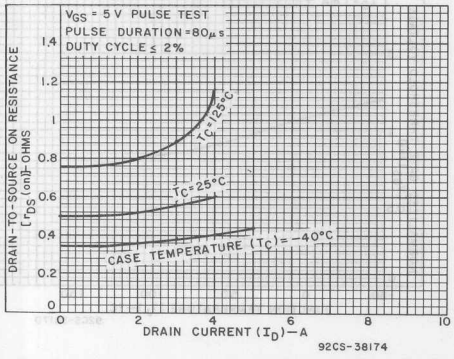


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

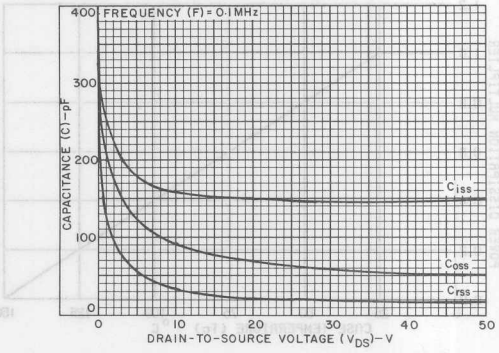


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

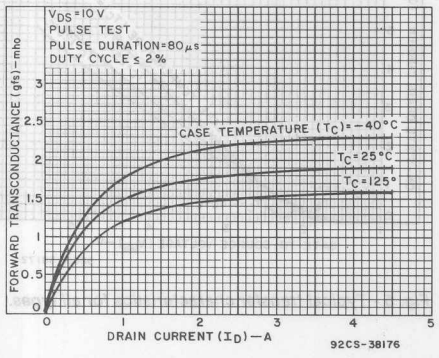


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

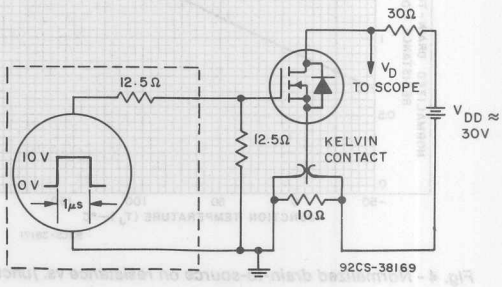


Fig. 11 - Switching Time Test Circuit.

HARRIS SEMICONDUCTOR

RFW2N06RLE

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors

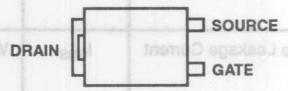
May 1992

Features

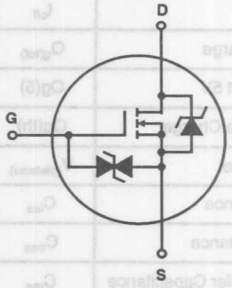
- 2A, 60V
- $r_{DS}(on) = 0.160\Omega$
- UIS Rating Curve (Single Pulse)
- Design Optimized For 5 Volt Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Electrostatic Discharge Protected

Package

4-PIN HEXDIP
TOP VIEW



Terminal Diagram



Description

The RFW2N06RLE (TA9861) N-Channel logic level ESD protected power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. The RFW2N06RLE was designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor and relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFW2N06RLE is supplied in the 4-pin hexdip plastic package. (Similar to JEDEC outline TO-250)

Absolute Maximum Ratings ($T_C = +25°C$)

			UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	+10, -5	V
Drain Current			
RMS Continuous	I_D	2	A
Pulsed Drain Current	I_{DM}	14	A
Single Pulse Avalance Rating	E_{AS}	Refer to UIS Curve	
Electrostatic Discharge Rating, MIL-STD-883, Category B(2)	ESD	2	KV
Power Dissipation			
$T_C = +25°C$	P_D	1.09	W
Derate Above +25°C	P_T	0.009	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2838.1**

Electrical Characteristics Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25mA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25°C	-	-1	1	µA
			T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = +10V, V_{GS} = -5V		-	-	10	µA
				-	-	10	µA
On Resistance	$r_{DS(on)}$	I_D = 2A, V_{GS} = 5.0V, I_D = 2A, V_{GS} = 4.3V		-	-	160	mΩ
				-	-	200	mΩ
Turn-On Time	t_{on}	V_{DD} = 30V, I_D = 2A, R_L = 15, V_{GS} = 5V, R_{GS} = 25Ω		-	-	100	ns
Turn-On Delay Time	$t_{d(on)}$			-	13	-	ns
Rise Time	t_r			-	42	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	95	-	ns
Fall Time	t_f			-	45	-	ns
Turn-Off Time	t_{off}			-	-	200	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0 to 10V	V_{DD} = 48V, I_D = 2A, RL = 24Ω	-	20	30	nC
Gate Charge at 5V	Qg(5)	V_{GS} = 0 to 5V		-	11	16	nC
Threshold Gate Charge	Qg(th)	V_{GS} = 0 to 1V		-	0.6	1.0	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 2A, V_{DS} = 15V		-	-	4.3	V
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	535	-	pF
Output Capacitance	C_{oss}			-	175	-	pF
Reverse Transfer Capacitance	C_{rss}			-	32	-	pF
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 30V, I_D = 2A, L = 0.21µH, R_L = 15Ω, V_{GS} = 5V, R_{GS} = 25Ω		-	-	10	µJ
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	115	°C/W

Source-Drain Diode Ratings And Characteristics

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 2A	-	-	1.2	V
Reverse Recovery Time	t_{rr}	I_{SD} = 2A, dI_{SD}/dt = 100A/µs	-	-	200	ns

Performance Curves

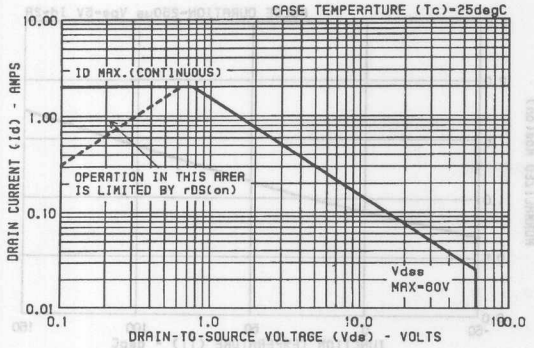


FIGURE 1. SAFE-OPERATING AREA CURVE

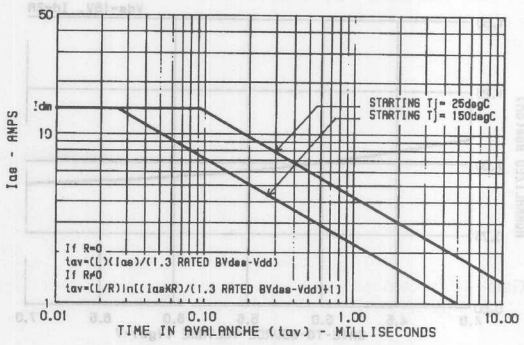


FIGURE 2. UNCLAMPED INDUCTIVE-SWITCHING

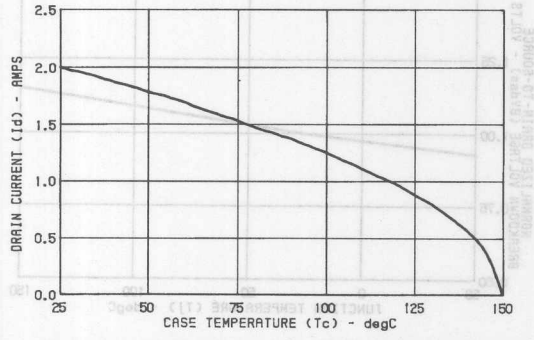


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

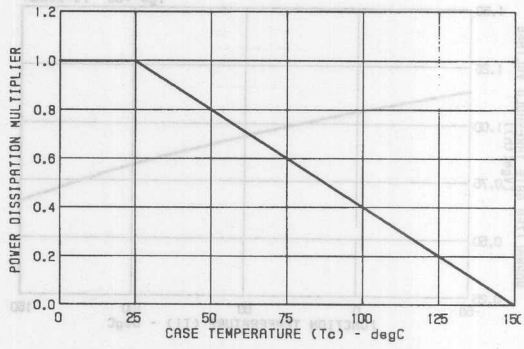


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

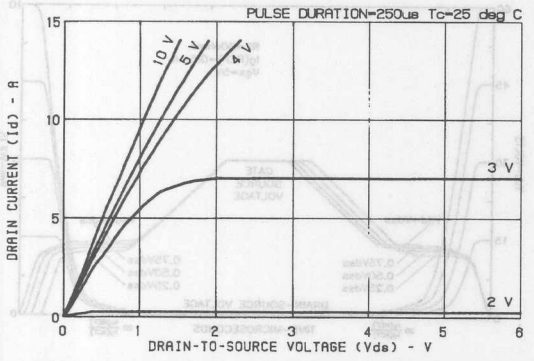


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

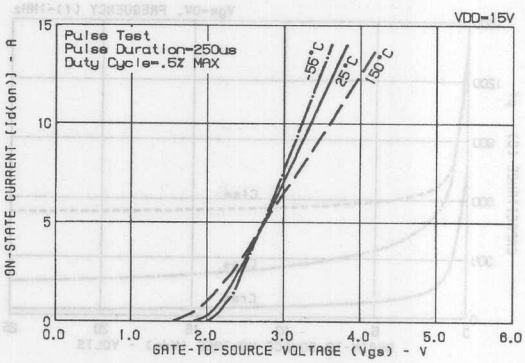


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Performance Curves (Continued)

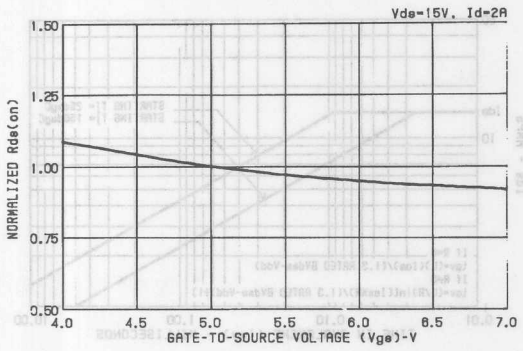


FIGURE 7. NORMALIZED $r_{DS(on)}$ vs V_{gs}

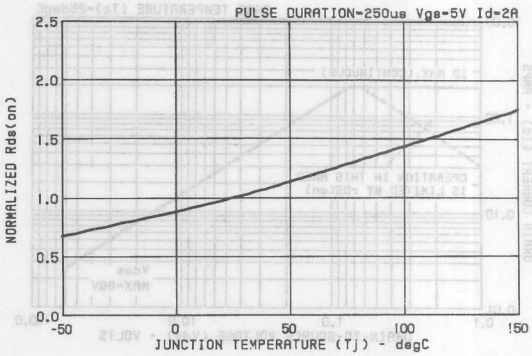


FIGURE 8. NORMALIZED $r_{DS(on)}$ vs JUNCTION TEMPERATURE

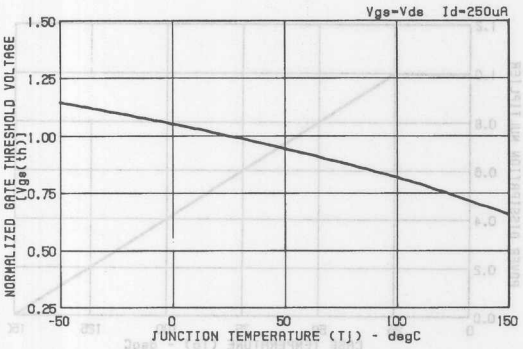


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

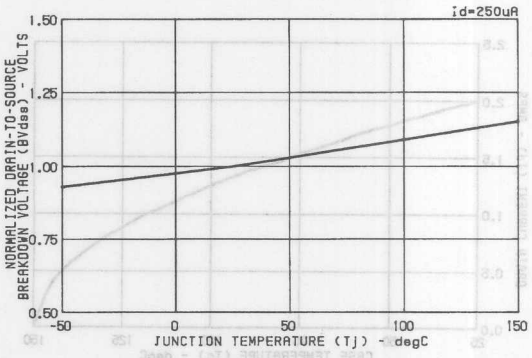


FIGURE 10. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

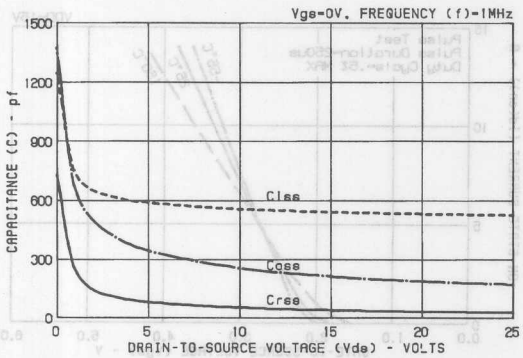


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

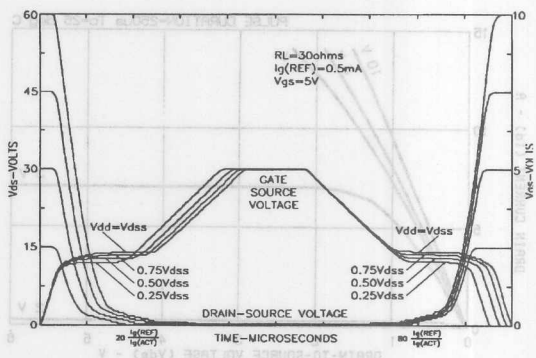


FIGURE 12. TYPICAL SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTES AN7254 AND AN7260

Performance Curves (Continued)

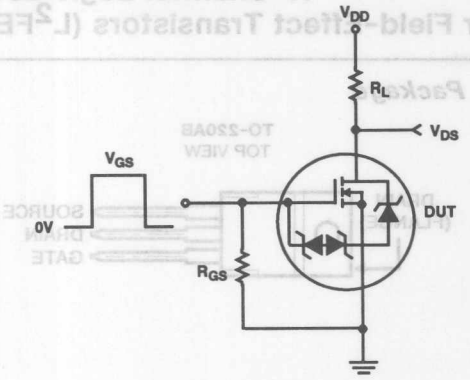


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUITS

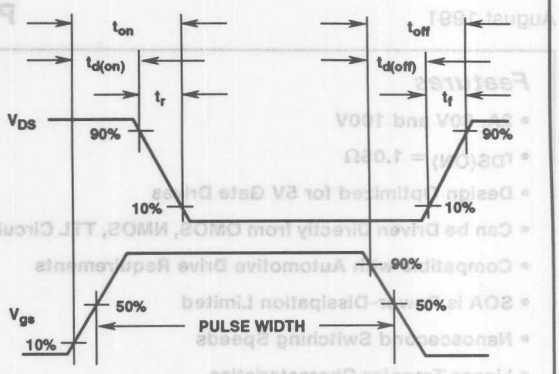


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

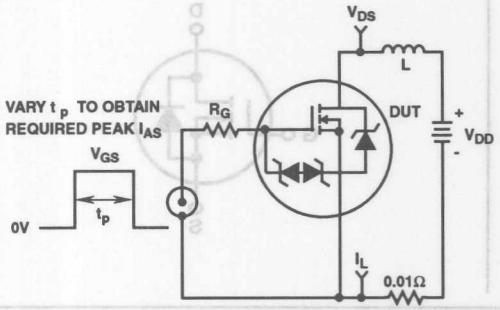


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

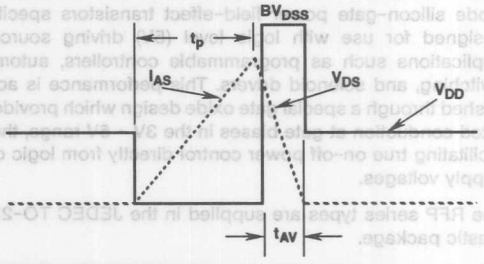


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

HARRIS

RFP2N08L
RFP2N10L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 2A, 80V and 100V
- $r_{DS(ON)} = 1.05\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

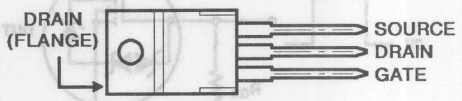
Description

The RFP2N08L and RFP2N10L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

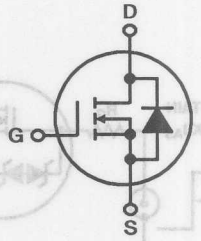
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		RFP2N08L	RFP2N10L	UNITS
Drain-Source Voltage	V_{DS}	80	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	80	100	V
Continuous Drain Current				
RMS Continuous	I_D	2	2	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
T_C = +25°C	P_D	25	25	W
Above T_C = +25°C, Derate Linearly		0.2	0.2	W/°C
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2872

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP2N08L MIN	LIMITS RFP2N08L MAX	LIMITS RFP2N10L MIN	LIMITS RFP2N10L MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	80	–	100	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V	–	1	–	–	μA
		V_{DS} = 80V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 65V	–	50	–	–	μA
		V_{DS} = 80V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.05	–	1.05	V
		I_D = 2A, V_{GS} = 5V	–	2.5	–	2.5	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.05	–	1.05	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse Transfer Capacitance	C_{RSS}		–	35	–	35	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 50V, R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	25	10 (typ)	25	ns
Rise Time	t_r		15 (typ)	45	15 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		25 (typ)	45	25 (typ)	45	ns
Fall Time	t_f		20 (typ)	25	20 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP2N08L MIN	LIMITS RFP2N08L MAX	LIMITS RFP2N10L MIN	LIMITS RFP2N10L MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = −1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

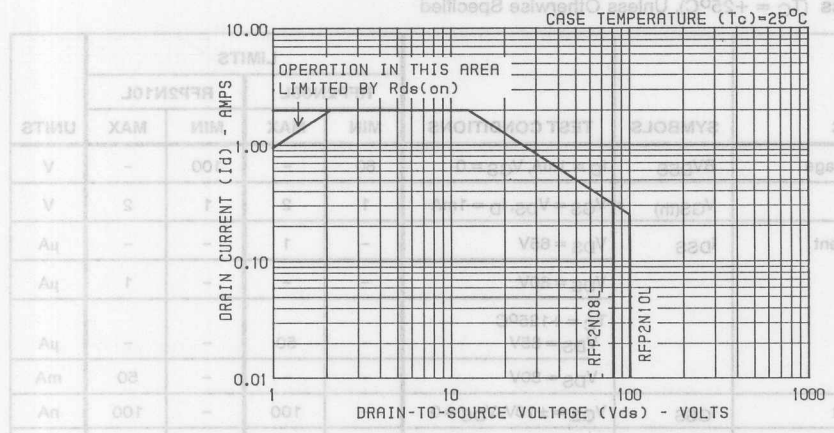


Fig. 1 — Maximum operating areas for all types.

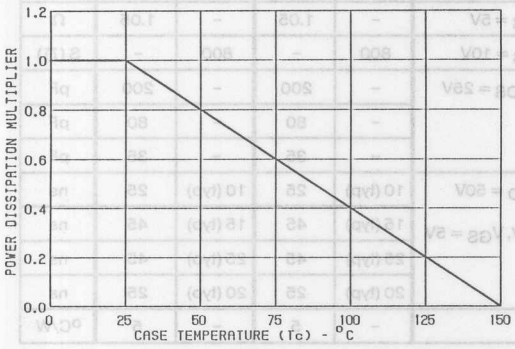


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

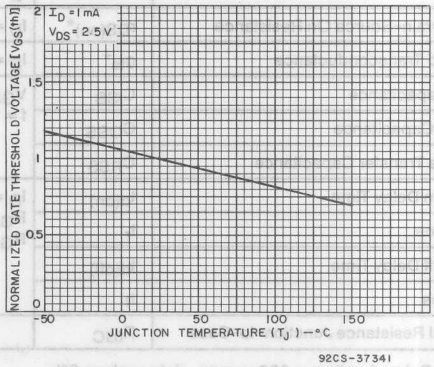


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

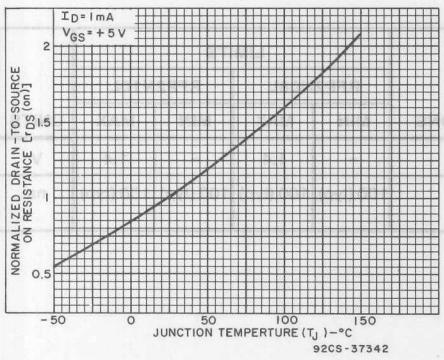


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

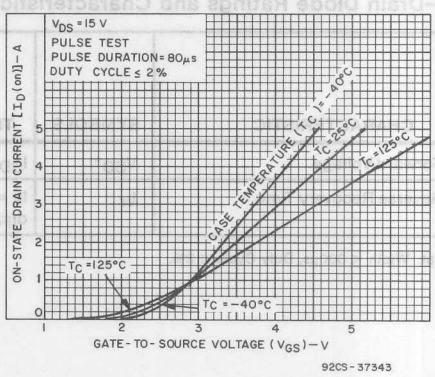


Fig. 5 — Typical transfer characteristics for all types.

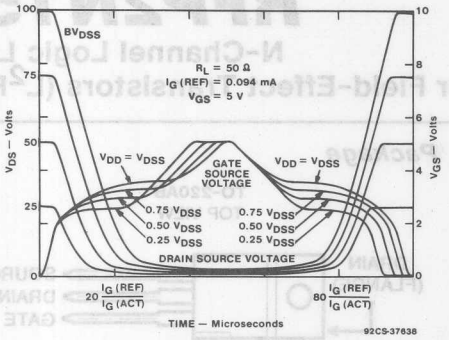


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

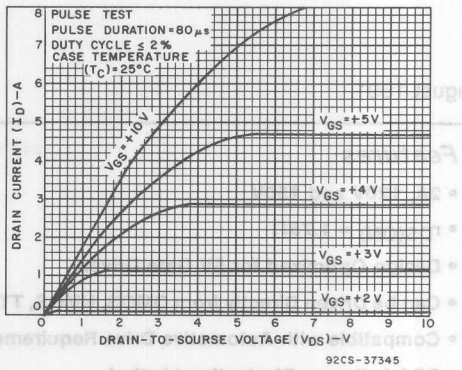


Fig. 7 — Typical saturation characteristics for all types.

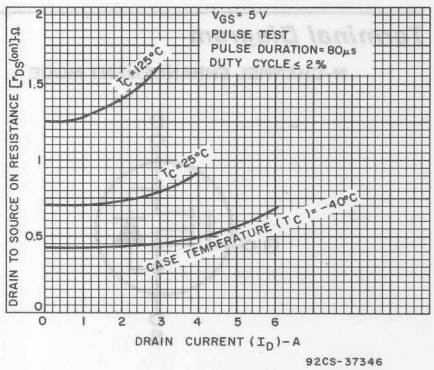


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

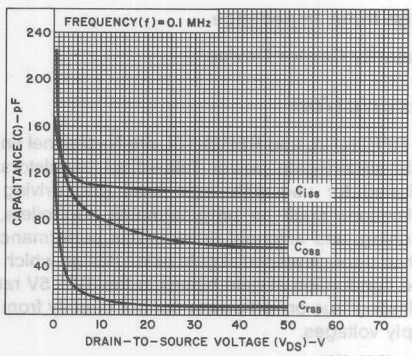


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

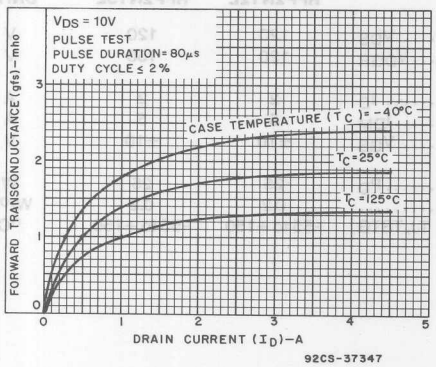


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

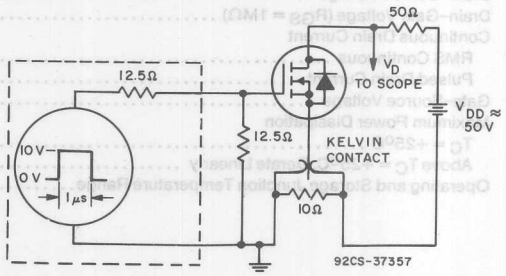


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFP2N12L
RFP2N15L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 2A, 120V and 150V
- $r_{DS(ON)} = 1.75\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

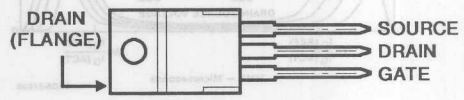
Description

The RFP2N12L and RFP2N15L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

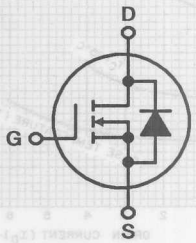
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFP2N12L	RFP2N15L	UNITS
Drain-Source Voltage	V_{DS}	120	120	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	120	150	V
Continuous Drain Current				
RMS Continuous	I_D	2	2	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	25	25	W
Above $T_C = +25^oC$, Derate Linearly		0.2	0.2	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2874

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP2N12L MIN	LIMITS RFP2N12L MAX	LIMITS RFP2N15L MIN	LIMITS RFP2N15L MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	120	–	150	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V	–	1	–	–	μA
		V_{DS} = 120V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 100V	–	50	–	–	μA
		V_{DS} = 120V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.75	–	1.75	V
		I_D = 2A, V_{GS} = 5V	–	4.2	–	4.2	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.75	–	1.75	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse Transfer Capacitance	C_{RSS}		–	35	–	35	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 75V, R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	25	10 (typ)	25	ns
Rise Time	t_r		10 (typ)	45	10 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		24 (typ)	45	24 (typ)	45	ns
Fall Time	t_f		20 (typ)	25	20 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP2N12L MIN	LIMITS RFP2N12L MAX	LIMITS RFP2N15L MIN	LIMITS RFP2N15L MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	150 (typ)	150 (typ)	150 (typ)	150 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

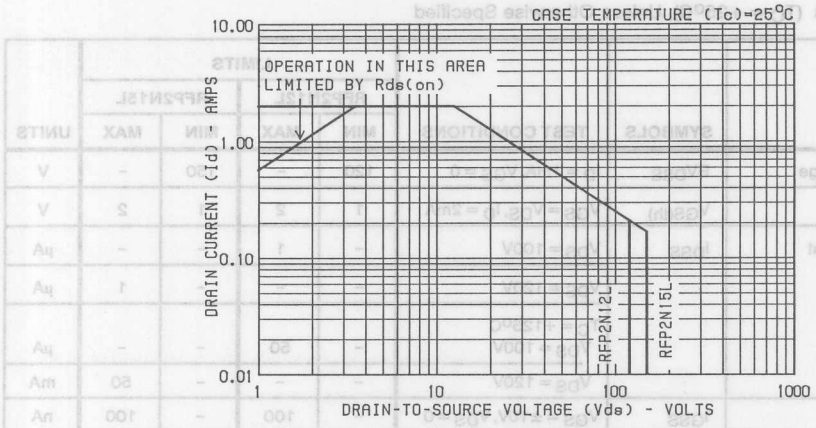


Fig. 1 — Maximum operating areas for all types.

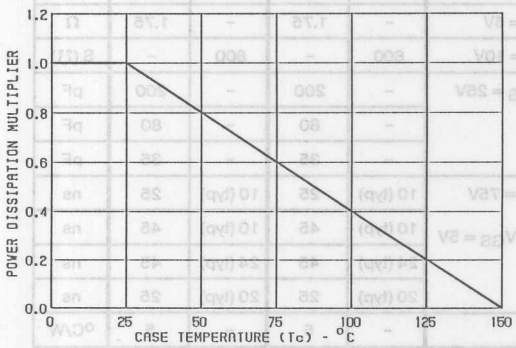


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

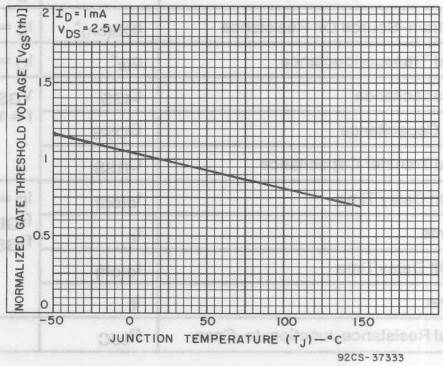


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

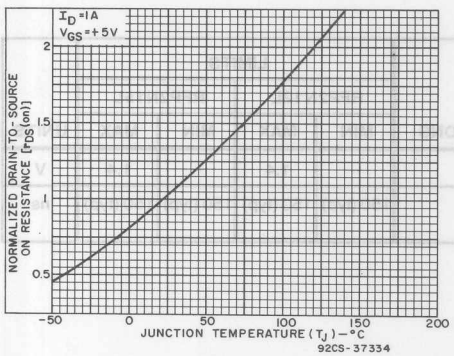


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

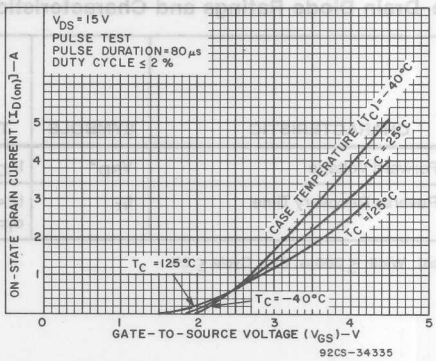


Fig. 5 — Typical transfer characteristics for all types.

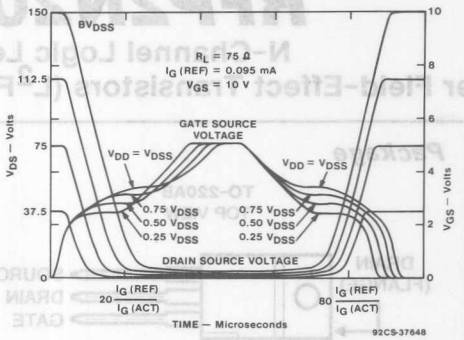


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

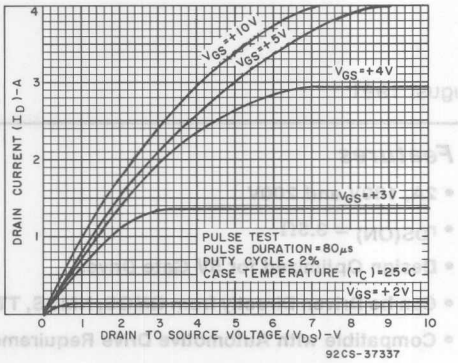


Fig. 7 — Typical saturation characteristics for all types.

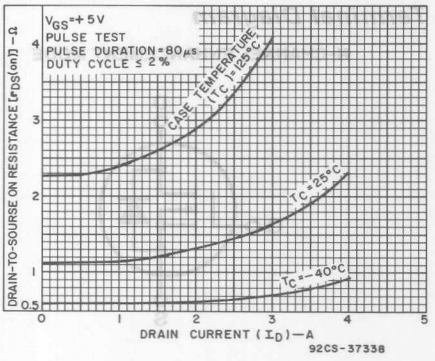


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

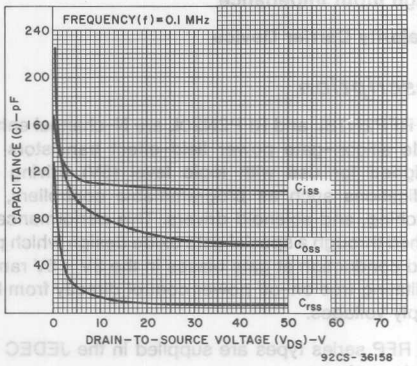


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

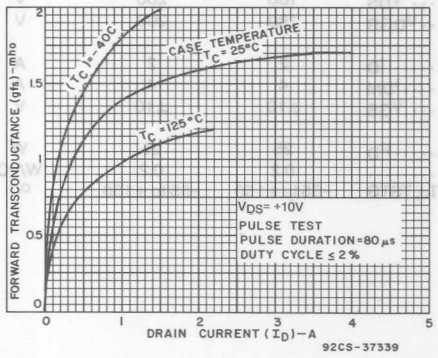


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

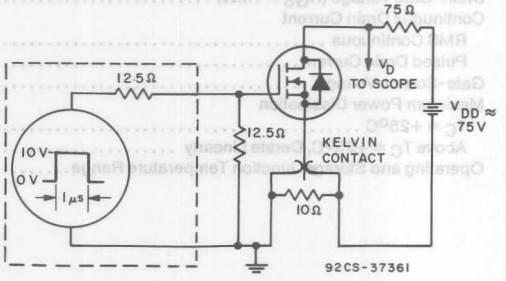


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFP2N18L
RFP2N20L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 2A, 180V and 200V
- $r_{DS(ON)} = 3.5\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

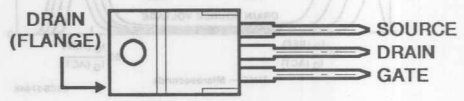
Description

The RFP2N18L and RFP2N20L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

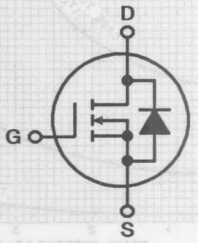
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFP2N18L	RFP2N20L	UNITS
Drain-Source Voltage	V_{DS}	180	200	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	180	200	V
Continuous Drain Current				
RMS Continuous	I_D	2	2	A
Pulsed Drain Current	I_{DM}	4	4	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	25	25	W
Above $T_C = +25^oC$, Derate Linearly		0.2	0.2	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2875

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N18L		RFP2N20L		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	180	–	200	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145V	–	1	–	–	μA
		V_{DS} = 160V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 145V	–	50	–	–	μA
		V_{DS} = 160V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	3.5	–	3.5	V
		I_D = 2A, V_{GS} = 5V	–	9	–	9	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	3.5	–	3.5	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	60	–	60	pF
Reverse Transfer Capacitance	C_{RSS}		–	35	–	35	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 100V, R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	25	10 (typ)	25	ns
Rise Time	t_r		10 (typ)	30	10 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		25 (typ)	40	25 (typ)	40	ns
Fall Time	t_f		20 (typ)	25	20 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N18L		RFP2N20L		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = –1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	200 (typ)	200 (typ)	200 (typ)	200 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

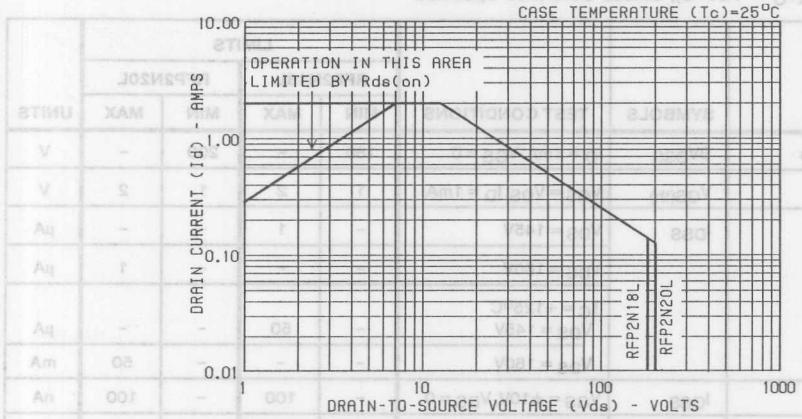


Fig. 1 — Maximum operating areas for all types.

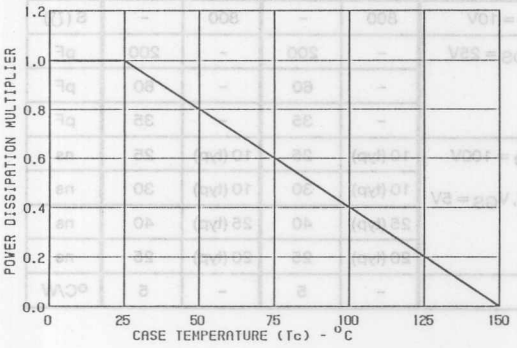


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

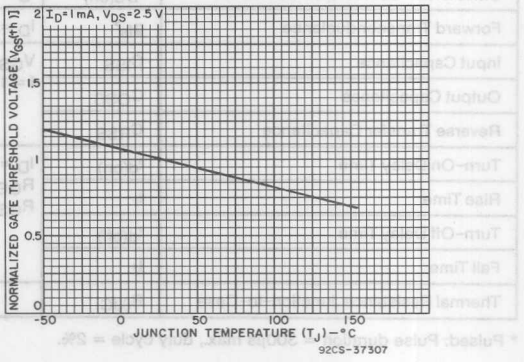


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

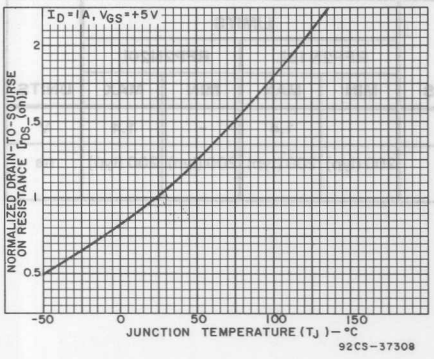


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

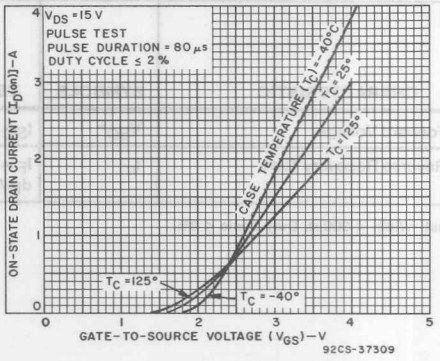


Fig. 5 — Typical transfer characteristics for all types.

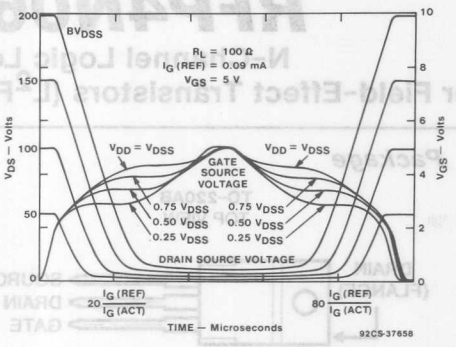


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

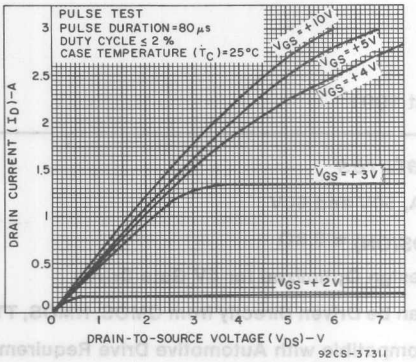


Fig. 7 — Typical saturation characteristics for all types.

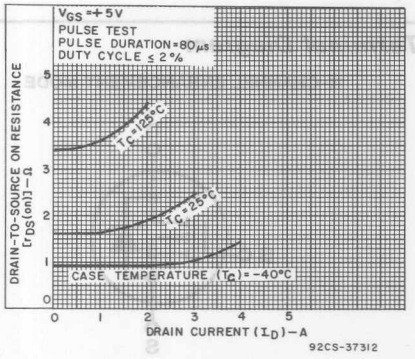


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

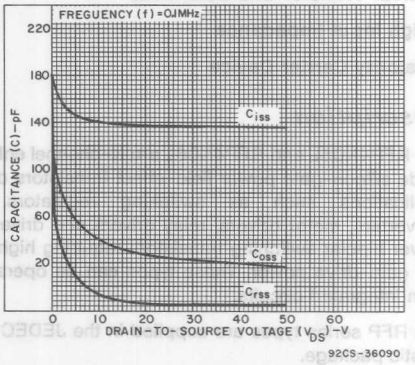


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

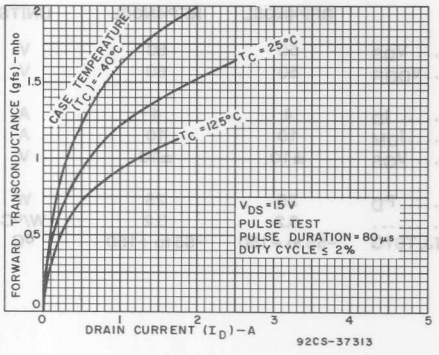


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

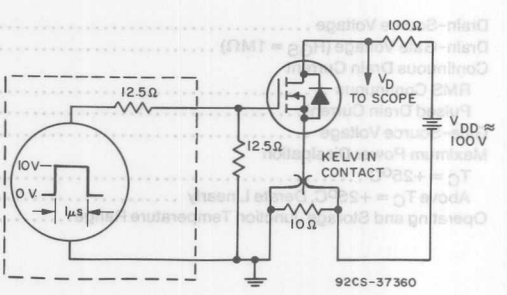


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFP4N05L
RFP4N06L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 4A, 50V and 60V
- $r_{DS(ON)} = 0.8\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

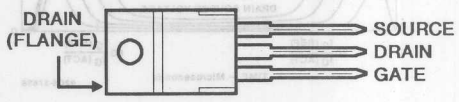
Description

The RFP4N05L and RFP4N06L are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

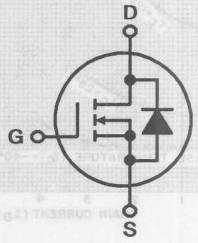
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFP4N05L	RFP4N06L	UNITS
Drain-Source Voltage	V_{DS}	50	60	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	50	60	V
Continuous Drain Current				
RMS Continuous	I_D	4	4	A
Pulsed Drain Current	I_{DM}	10	10	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	25	25	W
Above $T_C = +25^oC$, Derate Linearly		0.2	0.2	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2876**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP4N05L MIN	LIMITS RFP4N05L MAX	LIMITS RFP4N06L MIN	LIMITS RFP4N06L MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	50	–	60	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V	–	1	–	–	μA
		V_{DS} = 50V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 40V	–	50	–	–	μA
		V_{DS} = 50V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	0.8	–	0.8	V
		I_D = 2A, V_{GS} = 5V	–	2.0	–	2.0	V
		I_D = 4A, V_{GS} = 7.5V	–	4.8	–	4.8	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	0.8	–	0.8	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	225	–	225	pF
Output Capacitance	C_{OSS}		–	100	–	100	pF
Reverse Transfer Capacitance	C_{RSS}		–	40	–	40	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 30V, R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	20	10 (typ)	20	ns
Rise Time	t_r		65 (typ)	130	65 (typ)	130	ns
Turn-Off Delay Time	$t_{d(off)}$		20 (typ)	40	20 (typ)	40	ns
Fall Time	t_f		30 (typ)	60	30 (typ)	60	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP4N05L MIN	LIMITS RFP4N05L MAX	LIMITS RFP4N06L MIN	LIMITS RFP4N06L MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 100A/μs	150 (typ)	150 (typ)	150 (typ)	150 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

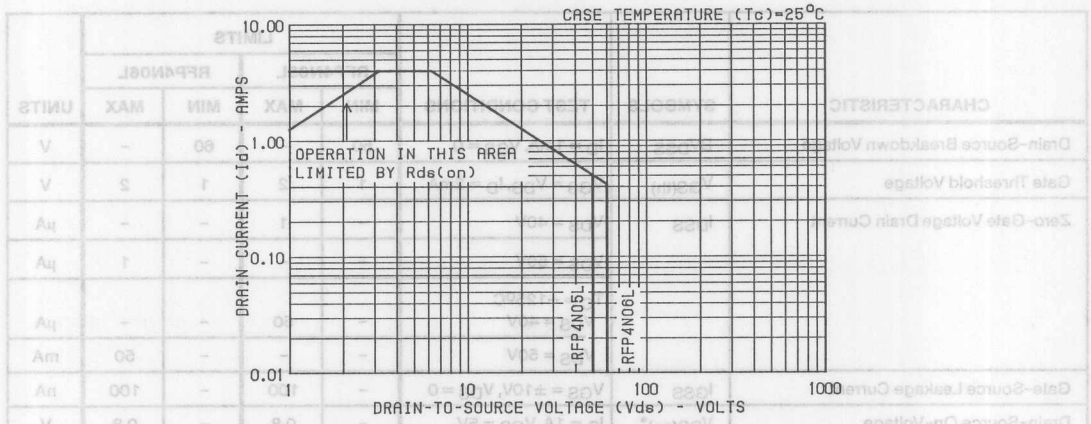


Fig. 1 - Maximum operating areas for all types.

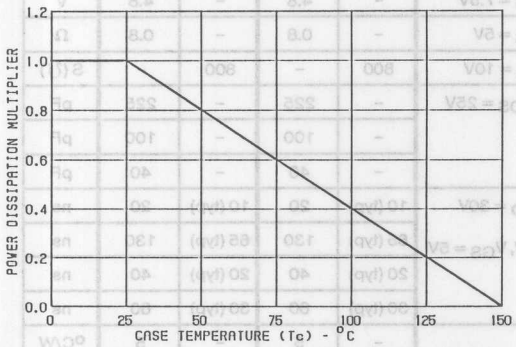


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

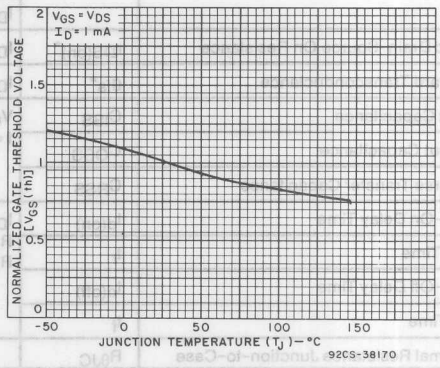


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

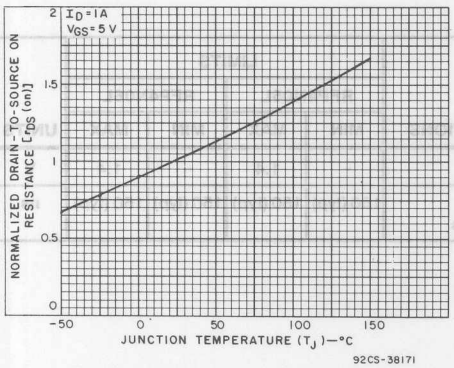


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

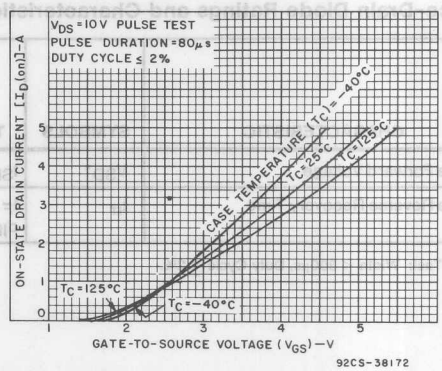


Fig. 5 - Typical transfer characteristics for all types.

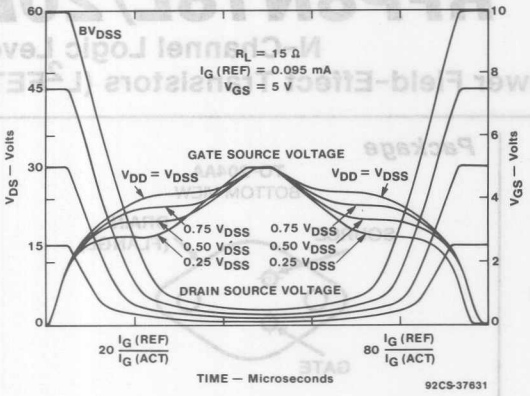


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

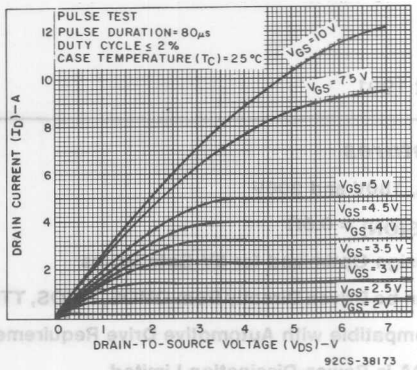


Fig. 7 - Typical saturation characteristics for all types.

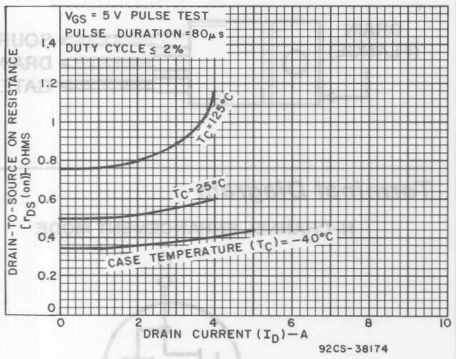


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

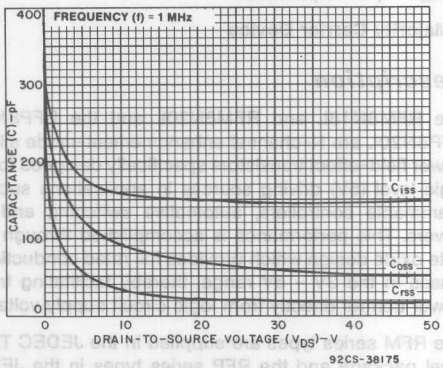


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

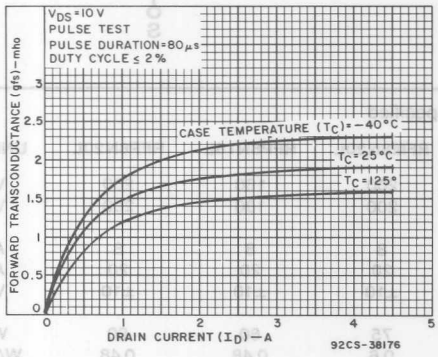


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

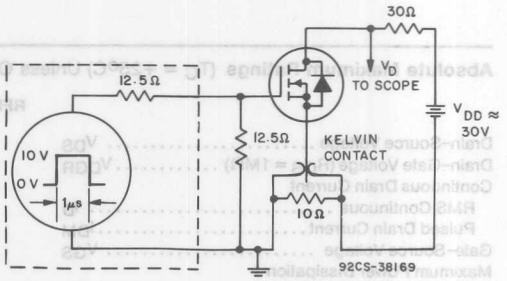


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFM8N18L/20L
RFP8N18L/20L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 8A, 180V and 200V
- $r_{DS(ON)} = 0.5\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

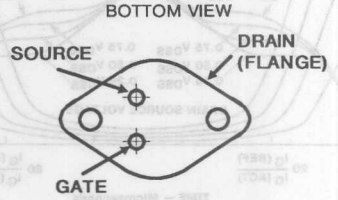
Description

The RFM8N18L and RFM8N20L and the RFP8N18L and RFP8N20L are N-channel enhancmement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

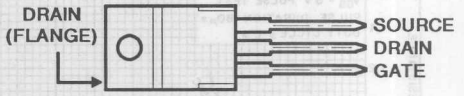
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Package

TO-204AA
BOTTOM VIEW

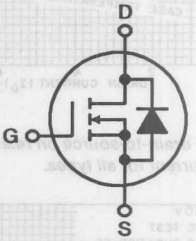


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFM8N18L	RFM8N20L	RFP8N18L	RFP8N20L	UNITS
Drain-Source Voltage	V_{DS}	180	200	180	200	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	180	200	180	200	V
Continuous Drain Current						
RMS Continuous	I_D	8	8	8	8	A
Pulsed Drain Current	I_{DM}	20	20	20	20	A
Gate-Source Voltage	V_{GS}	±10	±10	±10	±10	V
Maximum Power Dissipation						
$T_C = +25^oC$	P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly		0.6	0.6	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1514.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V V_{DS}=160 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=145 V V_{DS}=160 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm$10 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=4 A V_{GS}=5 V	—	2.0	—	2.0	V
		I_D=8 A V_{GS}=5 V	—	4.6	—	4.6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=4 A V_{GS}=5 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=4 A	3.0	—	3.0	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1MHz	—	900	—	900	pF
Output Capacitance	C_{oss}		—	250	—	250	pF
Reverse-Transfer Capacitance	C_{rss}		—	120	—	120	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=4A $R_{gen}=\infty$ R_{gs}=6.25 Ω V_{GS}=5 V	15(typ)	45	15(typ)	45	ns
Rise Time	t_r		45(typ)	150	45(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		100(typ)	135	100(typ)	135	ns
Fall Time	t_f		60(typ)	105	60(typ)	105	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM8N18L, RFM8N20L	—	1.67	—	1.67	°C/W
		RFP8N18L, RFP8N20L	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=4 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	250(typ)		250(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

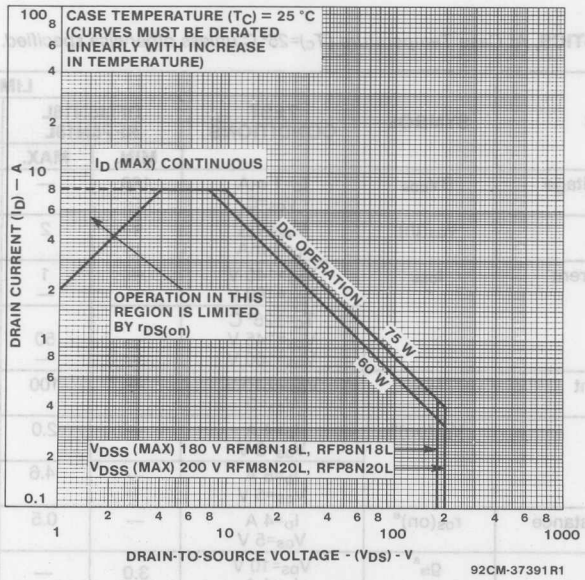


Fig. 1 — Maximum safe operating areas for all types.

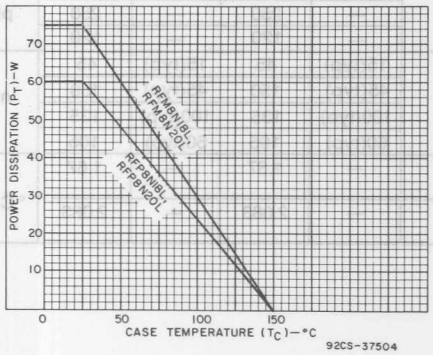


Fig. 2 — Power vs. temperature derating curve for all types.

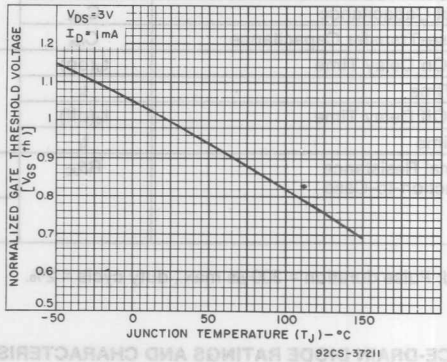


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

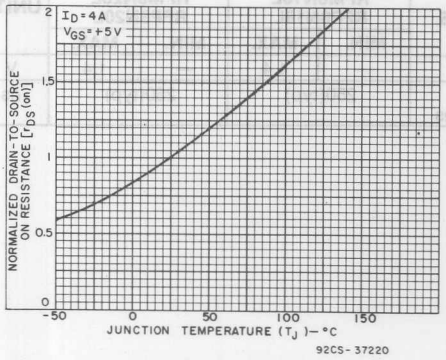


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

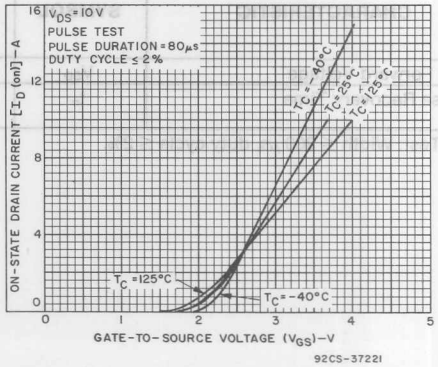


Fig. 5 — Typical transfer characteristics for all types.

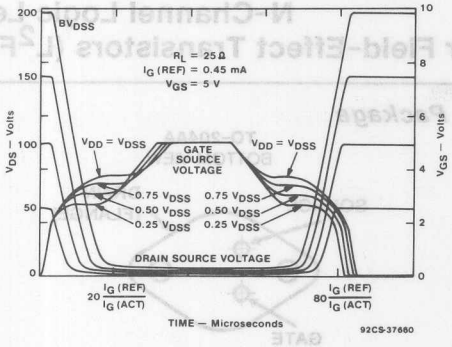


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

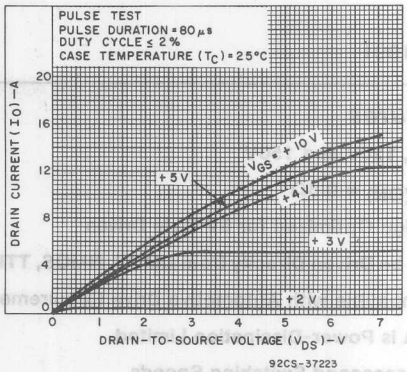


Fig. 7 — Typical saturation characteristics for all types.

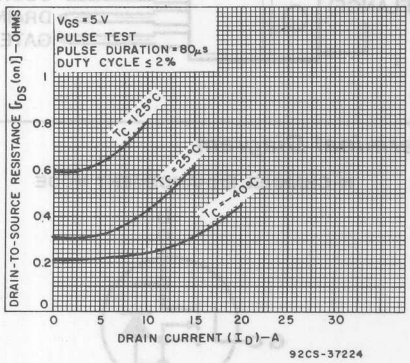


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

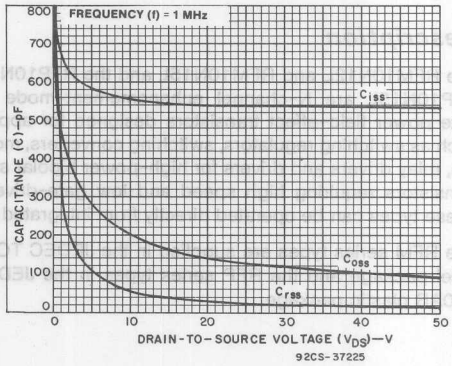


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

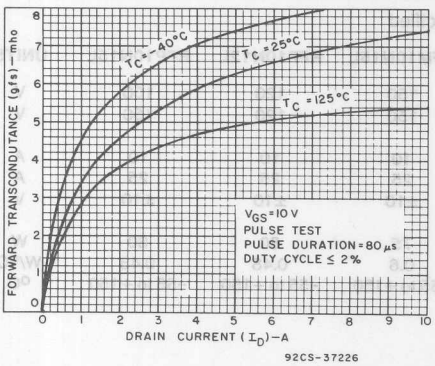


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

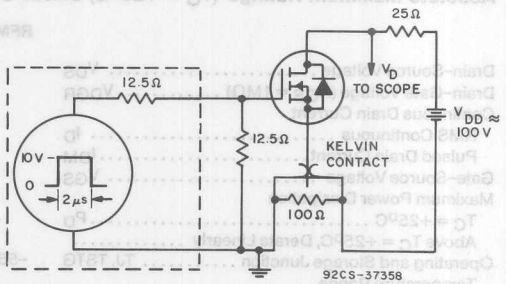


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFM10N12L/15L
RFP10N12L/15L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 10A, 120V and 150V
- $r_{DS(ON)} = 0.3\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

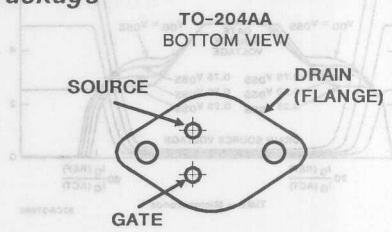
Description

The RFM10N12L and RFM10N15L and the RFP10N12L and RFP10N15L are N-channel enhancmement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

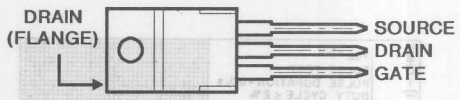
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Package

TO-204AA
BOTTOM VIEW

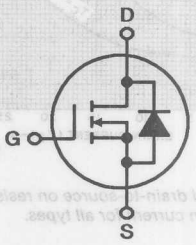


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	RFM10N12L	RFM10N15L	RFP10N12L	RFP10N15L	UNITS
Drain-Source Voltage ..... V_{DS}	120	150	120	150	V
Drain-Gate Voltage (R_{GS} = 1MΩ) ..... V_{DGR}	120	150	120	150	V
Continuous Drain Current					
RMS Continuous ..... I_D	10	10	10	10	A
Pulsed Drain Current ..... I_{DM}	25	25	25	25	A
Gate-Source Voltage ..... V_{GS}	±10	±10	±10	±10	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	60	60	W
Above T_C = +25°C, Derate Linearly	0.6	0.6	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1559.1

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12L RFP10N12L		RFM10N15L RFP10N15L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	120	—	150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 2 mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V	—	1	—	—	μA
		V_{DS} = 120 V	—	—	—	1	
		T_C = 125° C V_{DS} = 100 V	—	50	—	—	
		V_{DS} = 120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 5 A V_{GS} = 5 V	—	1.5	—	1.5	V
		I_D = 10 A V_{GS} = 5 V	—	4	—	4	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 5 A V_{GS} = 5 V	—	0.3	—	0.3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 5 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	1200	—	1200	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	250	—	250	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	120	—	120	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 75 V	15(typ)	60	15(typ)	60	ns
Rise Time	t_r	I_D = 5 A	50(typ)	135	50(typ)	135	
Turn-Off Delay Time	$t_{d(off)}$	R_{gen} = ∞ R_{gs} = 6.25 Ω	90(typ)	135	90(typ)	135	
Fall Time	t_f	V_{GS} = 5 V	90(typ)	135	90(typ)	135	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10N12L, RFM10N15L	—	1.67	—	1.67	°C/W
		RFP10N12L, RFP10N15L	—	2.083	—	2.083	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12L RFP10N12L		RFM10N15L RFP10N15L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	150 (typ.)		150 (typ.)		ns

[a] Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%

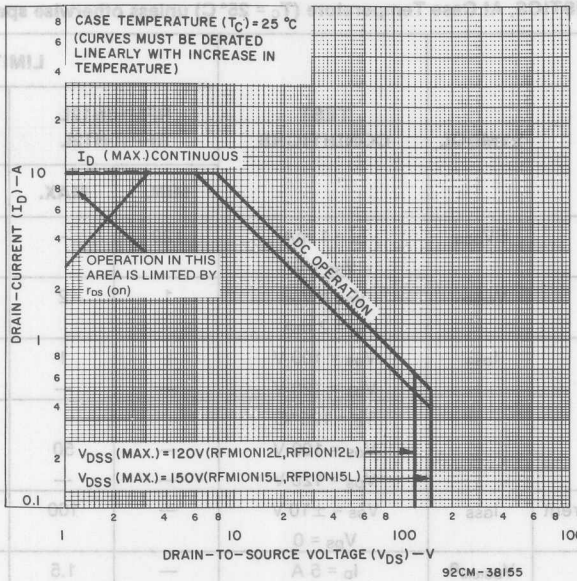


Fig. 1 - Maximum safe operating areas for all types.

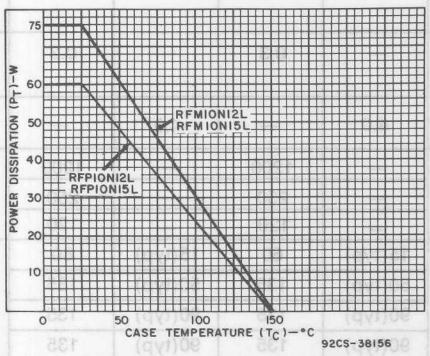


Fig. 2 - Power vs. temperature derating curve for all types.

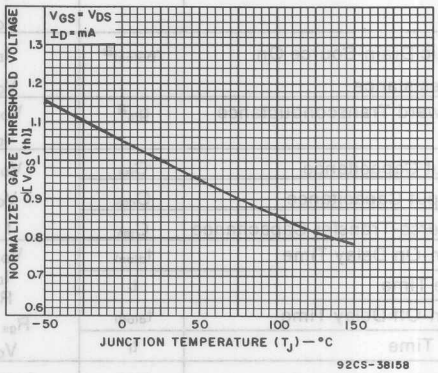


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

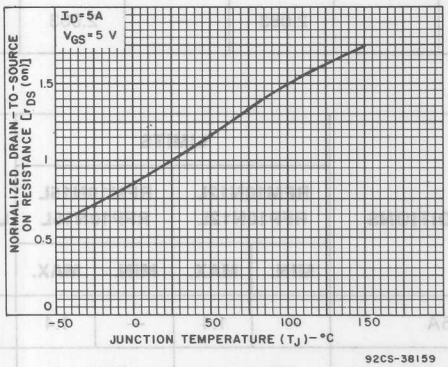


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

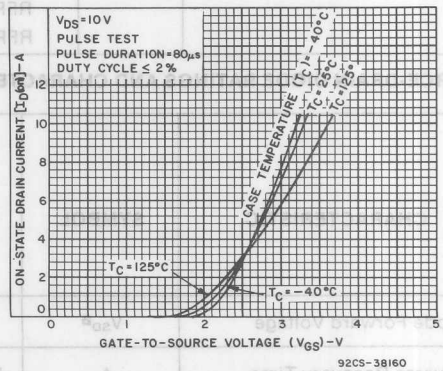


Fig. 5 - Typical transfer characteristics for all types.

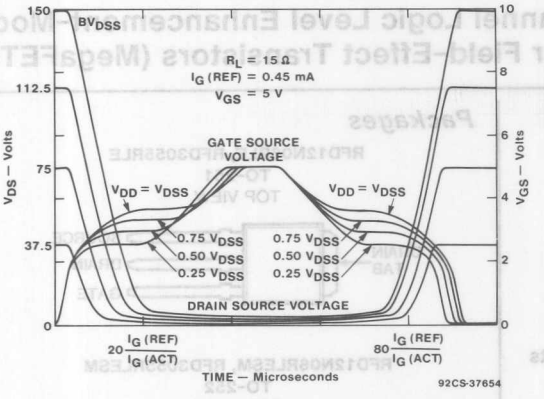


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

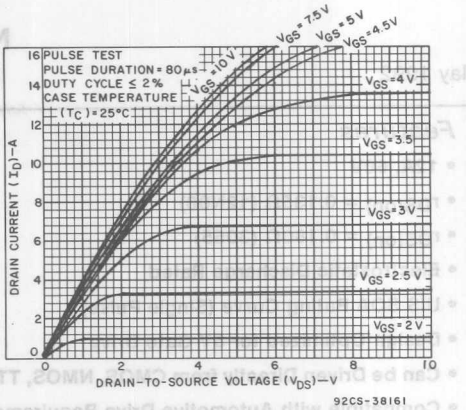


Fig. 7 - Typical saturation characteristics for all types.

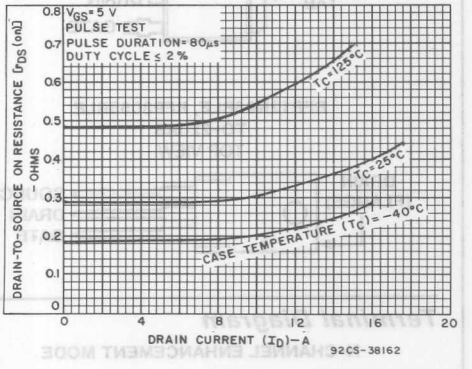


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

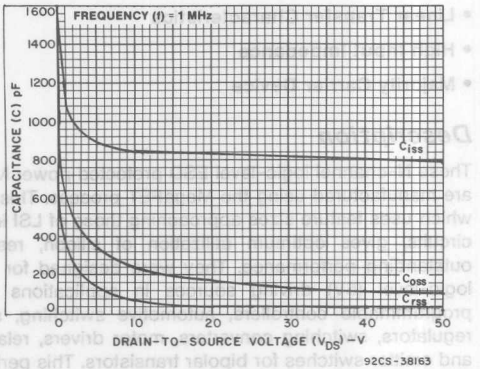


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

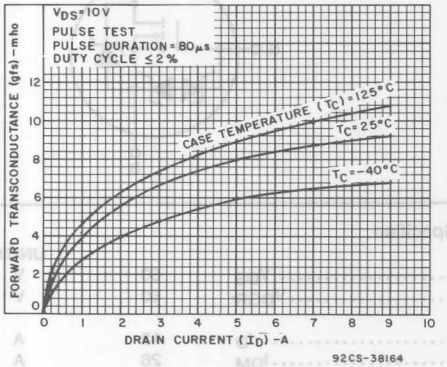


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

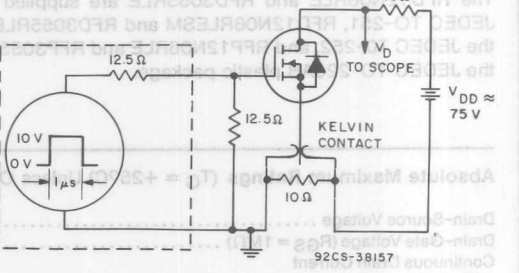


Fig. 11 - Switching Time Test Circuit.

RFD12N06RLE, RFD12N06RLESM
RFP12N06RLE, RFD3055RLE
RFD3055RLESM, RFP3055RLE

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

May 1992

Features

- 12A, 60V
- $r_{DS(on)} = 0.135\Omega$ (12N06)
- $r_{DS(on)} = 0.180\Omega$ (3055)
- Electrostatic Discharge Rated
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

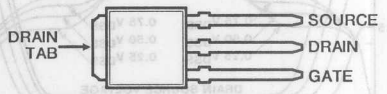
Description

These N-channel logic-level ESD protected power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic-level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

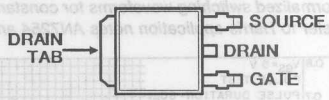
The RFD12N06RLE and RFD3055RLE are supplied in the JEDEC TO-251, RFD12N06RLESM and RFD3055RLESM in the JEDEC T0-252, and RFP12N06RLE and RFP3055RLE in the JEDEC TO-220AB plastic package.

Packages

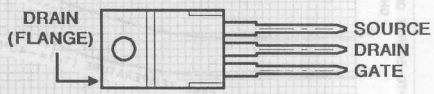
RFD12N06RLE, RFD3055RLE
TO-251
TOP VIEW



RFD12N06RLESM, RFD3055RLESM
TO-252
TOP VIEW

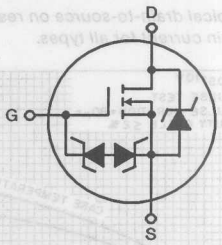


RFP12N06RLE, RFP3055RLE
TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	60	V
Continuous Drain Current			
RMS Continuous	I_D	12	A
Pulsed Drain Current	I_{DM}	26	A
Gate-Source Voltage	V_{GS}	+10	-5V
Maximum Power Dissipation			
$T_C = +25^oC$	P_D	40	W
Above $T_C = +25^oC$, Derate Linearly		0.32	W/^{o}C
Single Pulse Avalanche Rating, Refer to UIS SOA Curve Electrostatic Discharge Rating, ESD, MIL-STD-883, Category B(2)		2	KV
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	^{o}C

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File Number **2407.1**

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS		LIMITS RFD12N06RLE RFD12N06RLESM RFP12N06RLE Min	LIMITS RFD12N06RLE RFD12N06RLESM RFP12N06RLE Max	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA V_{GS} = 0 V		60	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 0.25 mA		1	2	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V T_C = 150° C		— —	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = +10 V V_{GS} = -5 V		— —	10 10	
On Resistance	$r_{DS(on)}$	V_{GS} = 5.0 V, I_D = 12 A V_{GS} = 4.0 V, I_D = 12 A		— —	0.135 0.160	Ω
Turn-On Time	$t_{(on)}$	See Fig. 13		—	60	ns
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 6 A		12 (typ)	—	
Rise Time	t_r	R_L = 5.0 Ω		20 (typ)	—	
Turn-Off Delay Time	$t_{d(off)}$	Ig1 = Ig2 = 0.4 A		24 (typ)	—	
Fall Time	t_f	$V_{GS(clamp)}$ = +5 V, -0.6 V		12 (typ)	—	
Turn-Off Time	$t_{(off)}$			—	60	
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0-10 V	V_{DD} = 48 V I_D = 12 A R_L = 4.0 Ω	—	40	nC
Gate Charge at 5 Volts	$Q_{g(5)}$	V_{GS} = 0-5 V		—	20	
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0-1 V		—	1.5	
Plateau Voltage	$V_{(plateau)}$	I_D = 12 A, V_{DS} = 15 V		—	4.0	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 30 V, I_D = 6 A L = 0.2 uH, Ig1 = Ig2 = 0.4 A $V_{GS(clamp)}$ = +5.0 V, -0.6 V R_L = 5.0 Ω		—	10	μJ
Thermal Resistance Junction to Case	RθJC			—	3.125	°C/W
Thermal Resistance Junction to Ambient	RθJA	TO-251 & TO-252 packages TO-220 package		— —	100 80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Forward Voltage	V_{SD}	I_{SD} = 12A	—	1.2	V
Reverse Recovery Time	t_{rr}	I_F = 12 A dI_F/dt = 100 A/μs	—	200	ns

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS RFD3055RLE RFD3055RLESM RFP3055RLE		UNITS
			Min	Max	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA V_{GS} = 0 V	60	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25 mA T_j = 150°C	1 0.6	2 1.6	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V T_C = 150°C	— —	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = +10 V V_{GS} = -5 V	— —	10 10	
On Resistance	$r_{DS(on)}$	V_{GS} = 5.0 V, I_D = 6 A	—	0.180	Ω
Turn-On Delay Time	$t_{d(on)}$	See Fig. 14	15 (typ)	—	ns
Rise Time	t_r	V_{DD} = 25 V, I_D = 6 A	55 (typ)	—	
Turn-Off Delay Time	$t_{d(off)}$	V_{GS} = 5.0 V, R_L = 4.17 Ω	80 (typ)	—	
Fall Time	t_f	R_{gen} = R_{GS} = 50 Ω	50 (typ)	—	
Total Gate Charge	Q_g	V_{DS} = 48 V, I_D = 12 A	11 (typ)	17	nC
Gate Source Charge	Q_{gs}	V_{GS} = 5 V	4 (typ)	—	
Gate Drain Charge	Q_{gd}	R_L = 4.0 Ω	7 (typ)	—	
Plateau Voltage	$V_{(plateau)}$	I_D = 12 A, V_{DS} = 15 V	—	5.0	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 30 V, I_D = 6 A L = 0.2 uH, Ig1 = Ig2 = 0.4 A $V_{GS(clamp)}$ = +5.0 V, -0.6 V R_L = 5.0 Ω	—	10	μJ
Thermal Resistance Junction to Case	RθJC		—	3.125	°C/W
Thermal Resistance Junction to Ambient	RθJA	TO-251 & TO-252 packages TO-220 package	— —	100 80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Forward Voltage	V_{SD}	I_{SD} = 12 A	—	1.2	V
Reverse Recovery Time	t_{rr}	I_F = 12 A dI_F/dt = 100 A/μs	—	200	ns

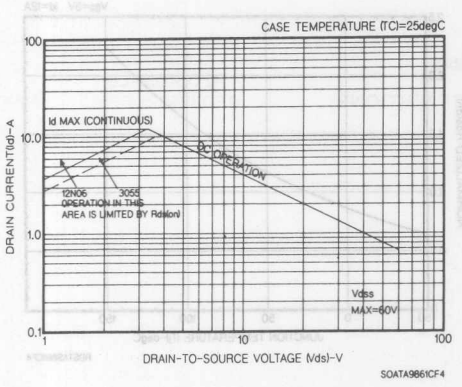


Fig. 1 - Safe-operating area curve. (Curves must be derated linearly with increase in case temperature.)

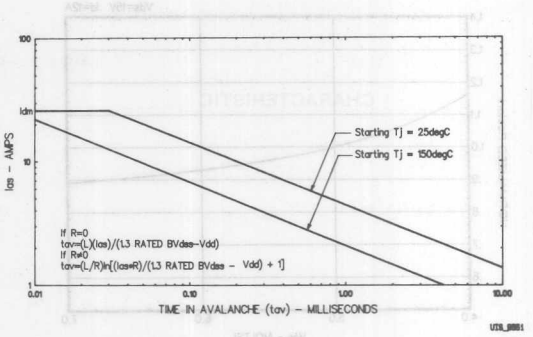


Fig. 2 - Unclamped-inductive-switching. Safe-operating-area. (Single pulse UIS SOA.)

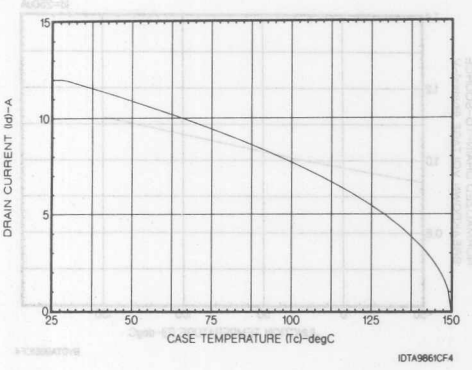


Fig. 3 - Maximum continuous drain current vs. temperature.

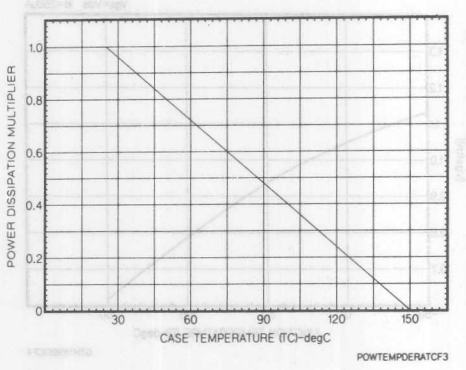


Fig. 4 - Normalized power dissipation vs. temperature derating curve.

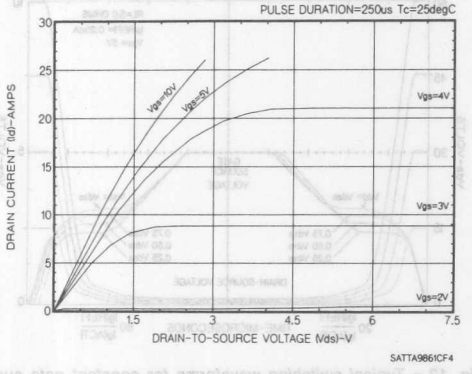


Fig. 5 - Typical saturation characteristics.

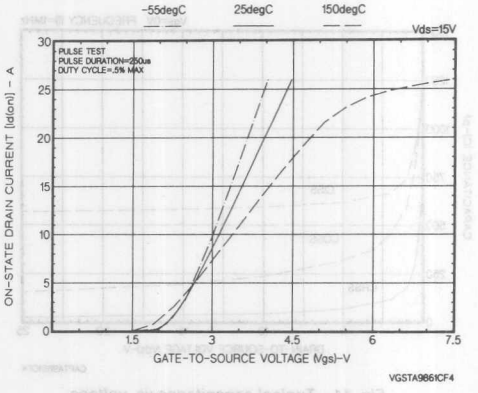


Fig. 6 - Typical transfer characteristics.

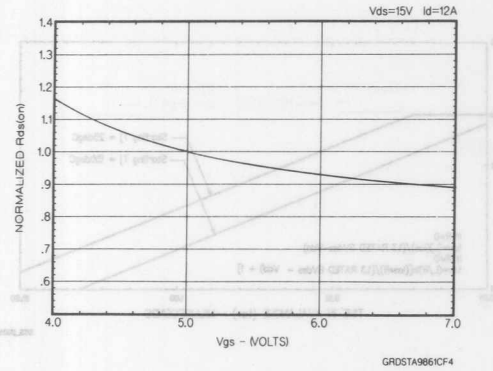


Fig. 7 - Normalized $r_{DS}(on)$ vs. V_{gs}.

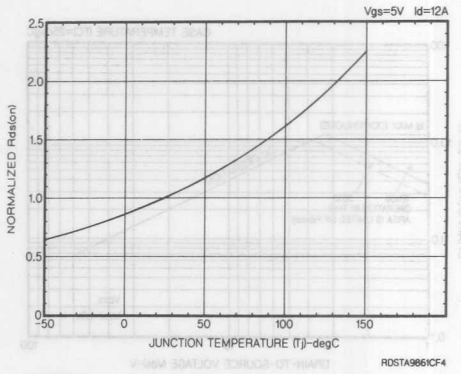


Fig. 8 - Normalized $r_{DS(on)}$ vs. junction temperature.

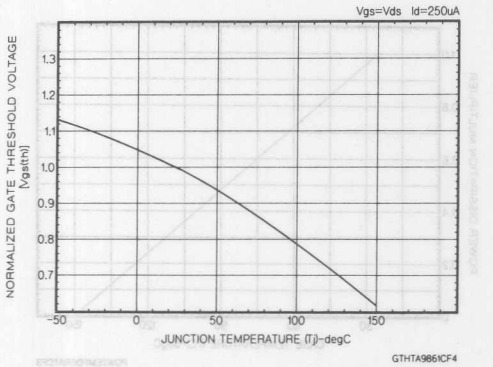


Fig. 9 - Normalized gate threshold voltage vs. temperature.

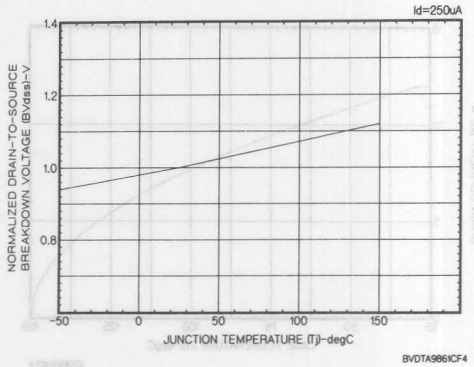


Fig. 10 - Normalized drain source breakdown voltage vs. temperature.

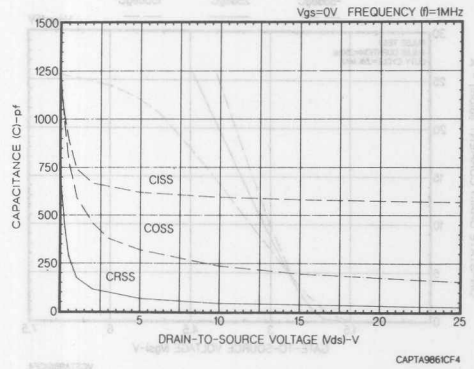


Fig. 11 - Typical capacitance vs. voltage.

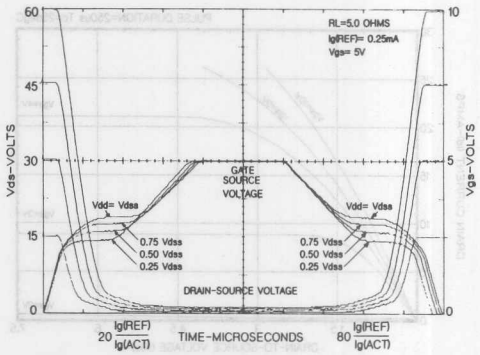


Fig. 12 – Typical switching waveforms for constant gate current. Refer to Harris application notes AN7254 and AN-7260.

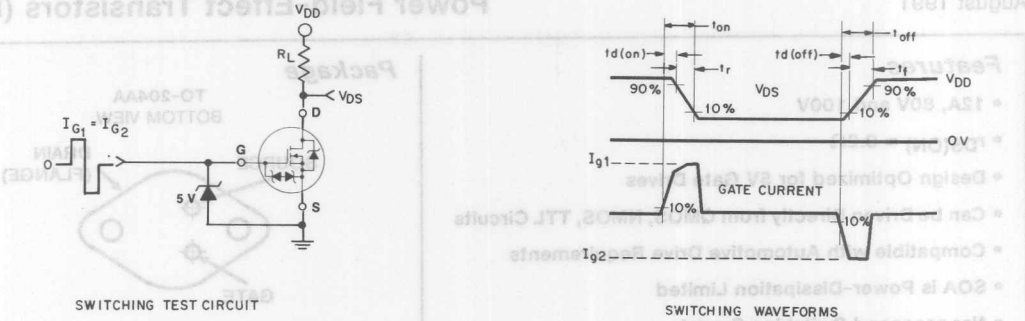


Fig. 13 - Resistive switching.

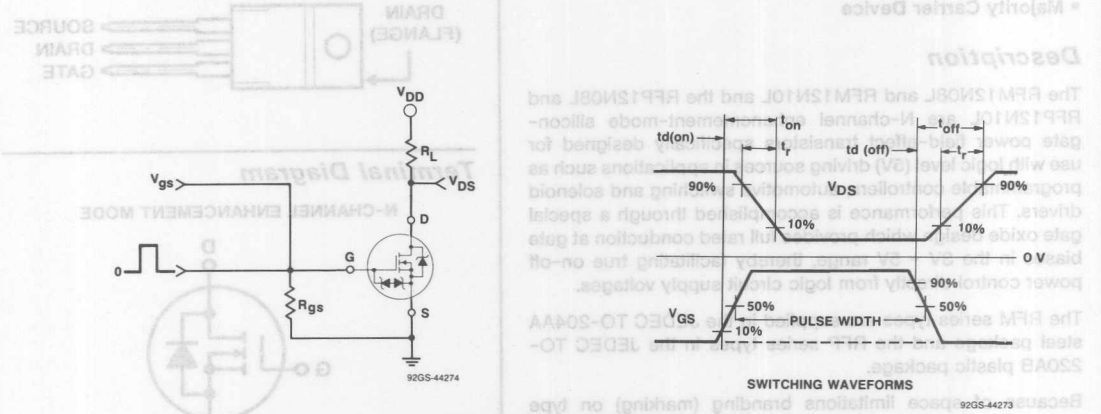


Fig. 14 - Resistive switching.

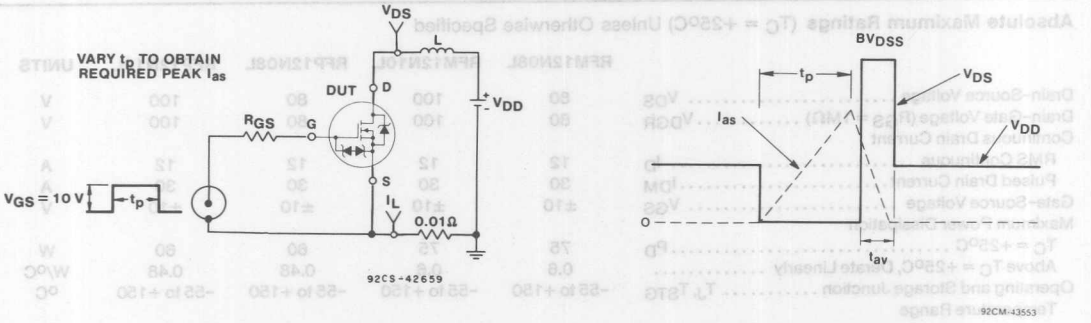


Fig. 15 - Unclamped inductive switching test.

RFM12N08L/10L
RFP12N08L/10L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 12A, 80V and 100V
- $r_{DS(ON)} = 0.2\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

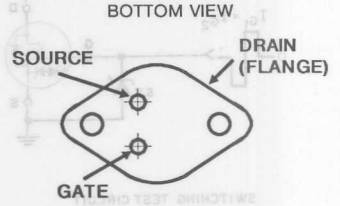
The RFM12N08L and RFM12N10L and the RFP12N08L and RFP12N10L are N-channel enhancmement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

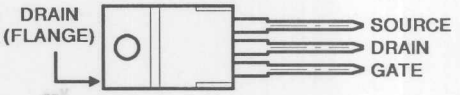
Because of space limitations branding (marking) on type RFP12N08L is F12N08L and on type RFP12N10L is F12N10L.

Package

TO-204AA
BOTTOM VIEW

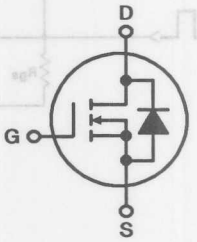


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

	RFM12N08L	RFM12N10L	RFP12N08L	RFP12N10L	UNITS
Drain-Source Voltage ..... V_{DS}	80	100	80	100	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$) ..... V_{DGR}	80	100	80	100	V
Continuous Drain Current					
RMS Continuous ..... I_D	12	12	12	12	A
Pulsed Drain Current ..... I_{DM}	30	30	30	30	A
Gate-Source Voltage ..... V_{GS}	±10	±10	±10	±10	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1512.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08L RFP12N08L		RFM12N10L RFP12N10L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V V_{DS}=80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=65 V V_{DS}=80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=5 V	—	1.2	—	1.2	V
		I_D=12 A V_{GS}=5 V	—	3.3	—	3.3	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=5 V	—	0.2	—	0.2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1MHz	—	900	—	900	pF
Output Capacitance	C_{oss}		—	325	—	325	pF
Reverse-Transfer Capacitance	C_{rss}		—	170	—	170	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=6 A R_{gen}=∞ R_{gs}=6.25 Ω V_{GS}=5 V	15(typ)	50	15(typ)	50	ns
Rise Time	t_r		70(typ)	150	70(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		100(typ)	130	100(typ)	130	ns
Fall Time	t_f		80(typ)	150	80(typ)	150	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM12N08L, RFM12N10L	—	1.67	—	1.67	°C/W
		RFP12N08L, RFP12N10L	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08L RFP12N08L		RFM12N10L RFP12N10L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

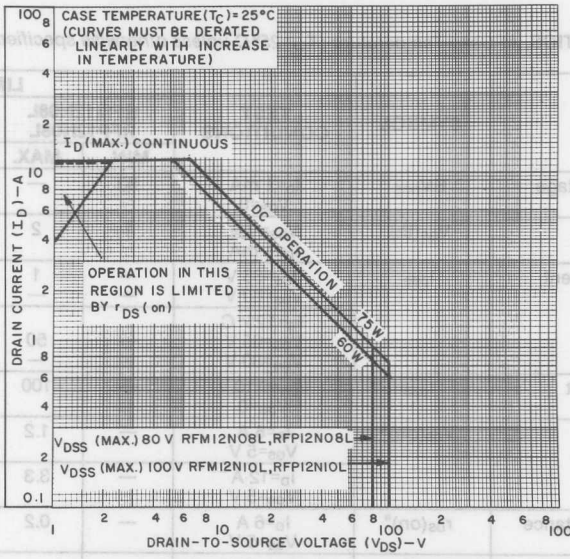


Fig. 1 — Maximum operating areas for all types.

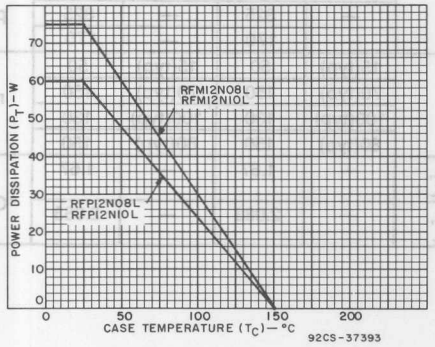


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

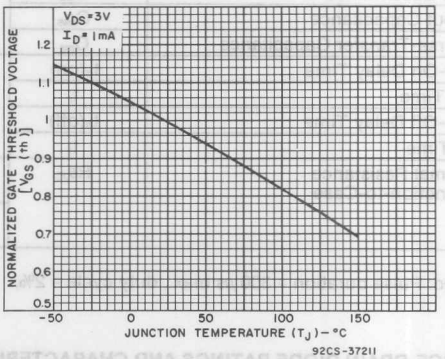


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

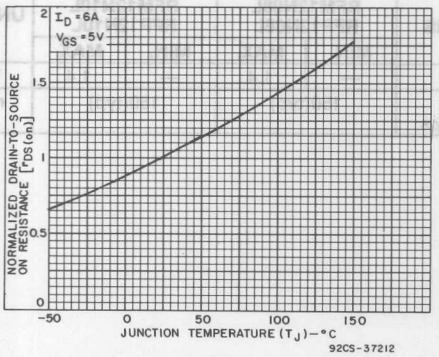


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

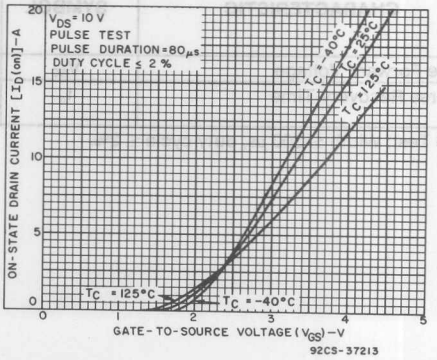


Fig. 5 — Typical transfer characteristics for all types.

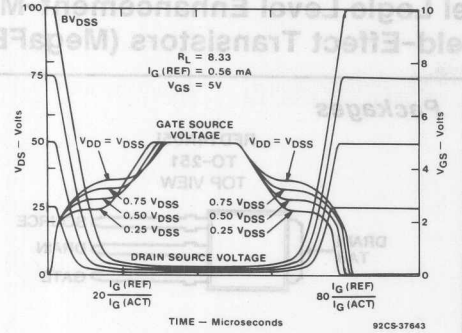


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

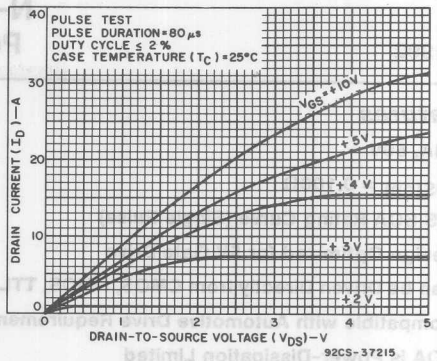


Fig. 7 — Typical saturation characteristics for all types.

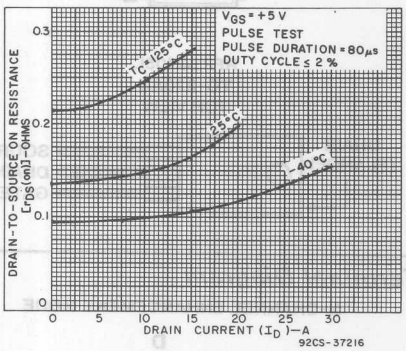


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

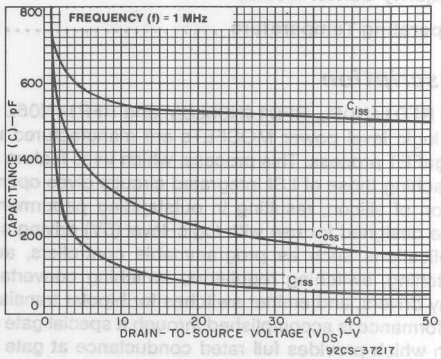


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

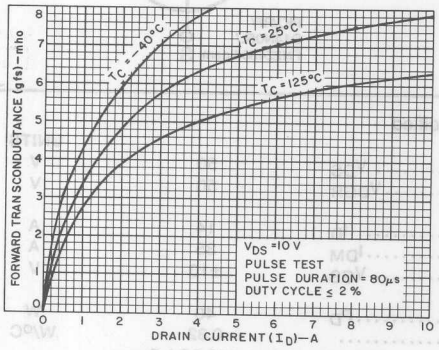


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

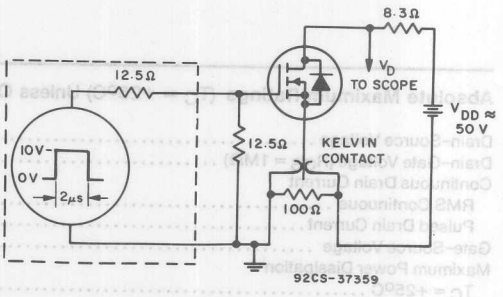


Fig. 11 — Switching Time Test Circuit.

HARRIS RFD14N05L/05LSM RFP14N05L

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

June 1992

Features

- 14A, 50V
- $r_{DS(on)} = 0.100\Omega$
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Operating Temperature ..... +150°C

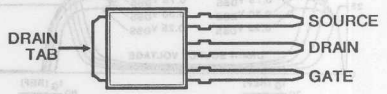
Description

The RFD14N05L, RFD14N05LSM and RFP14N05L N-Channel logic level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic-level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers, and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

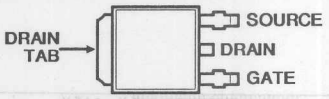
The RFD14N05L is supplied in the JEDEC TO-251 plastic package, the RFD14N05LSM in the JEDEC TO-252 plastic package and the RFP14N05L in the JEDEC TO-220AB plastic package.

Packages

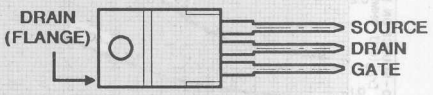
RFD14N05L
TO-251
TOP VIEW



RFD14N05LSM
TO-252
TOP VIEW

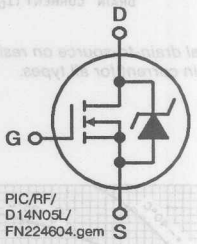


RFP14N05L
TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	V
Continuous Drain Current			
RMS Continuous	I_D	14	A
Pulsed Drain Current	I_{DM}	35	A
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
T_C = +25°C	P_D	40	W
Above T_C = +25°C, Derate Linearly		0.32	W/°C
Single Pulse Avalanche Rating		Refer to UIS SOA Curve	
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2246.1

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25° C Unless Otherwise Specified.

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		1	2	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V		—	1	μA
		T_C = 150° C		—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On-Resistance	$r_{DS}(on)$	I_D = 14 A, V_{GS} = 5 V		—	0.1	Ω
		I_D = 14 A, V_{GS} = 4 V		—	0.12	
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 7 A		—	60	ns
Turn-On Delay Time	$t_d(on)$	I_{g1} = I_{g2} = 0.4 A		—	13 (typ.)	
Rise Time	t_r	V_{GS}(clamp) +5 V, -0.6 V		—	24 (typ.)	
Turn-Off Delay Time	$t_d(off)$	R_L = 3.57 Ω		—	42 (typ.)	
Fall Time	t_f	(See Figs. 10 & 11)		—	16 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	Q_g(total)	V_{DD} = 40 V	V_{GS} = 0-10 V	—	40	nC
Gate Charge at 5 V	$Q_g(5)$	I_D = 14 A	V_{GS} = 0-5 V	—	25	
Threshold Gate Charge	$Q_g(th)$	R_L = 2.86 Ω	V_{GS} = 0-1 V	—	1.5	
Plateau Voltage	V(plateau)	I_D = 14 A, V_{DS} = 15 V		—	4	V
Turn-Off Energy Loss Per Cycle	E_{off}	V_{DD} = 25 V, I_D = 7 A, L = 0.2 μH, R_L = 3.57 Ω, I_{g1} = I_{g2} = 0.2 A, V_{GS}(clamp) +5 V, -0.6 V		—	14	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	3.125	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	TO-251 & TO-252		—	100	
		TO-220		—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 14 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, dI_F/d_t = 100 A/μs	—	125	ns

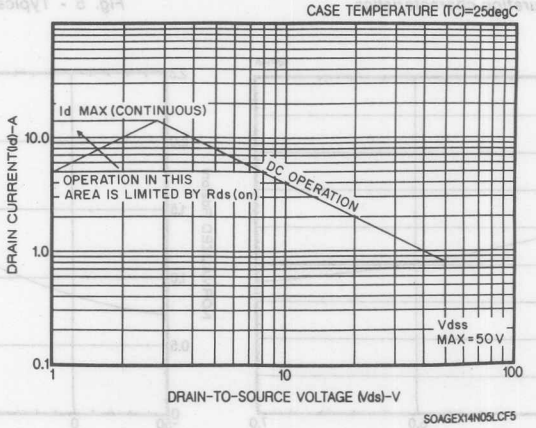


Fig. 1 - Safe-operating-area curve. (Curves must be derated linearly with increase in case temperature.)

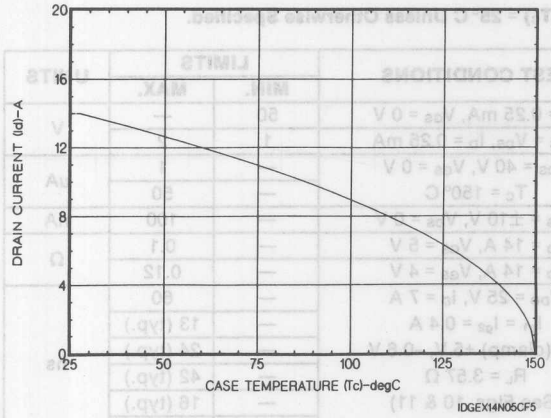


Fig. 2 - Maximum continuous drain current vs. temperature.

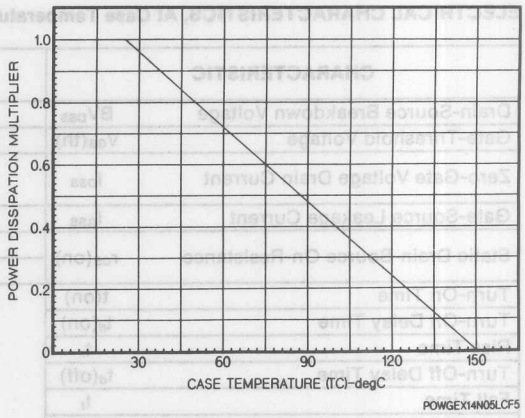


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

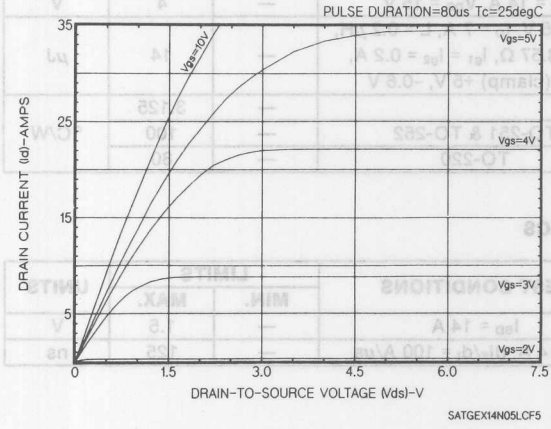


Fig. 4 - Typical saturation characteristics.

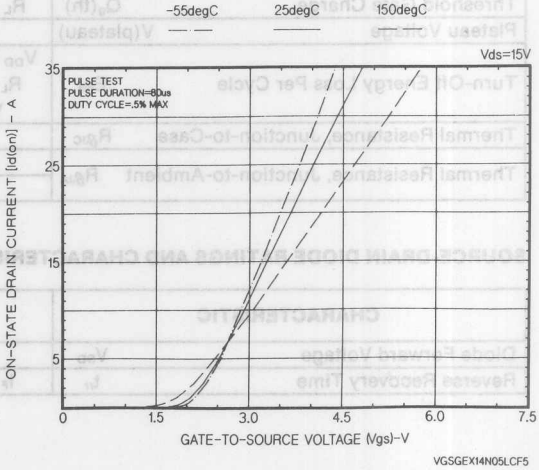


Fig. 5 - Typical transfer characteristics.

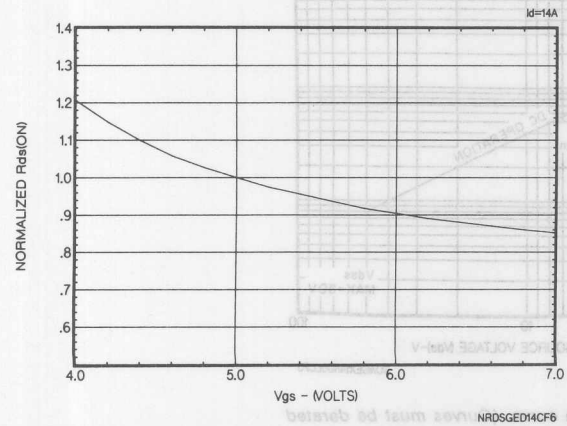


Fig. 6 - Normalized $r_{DS}(on)$ vs. V_{gs}.

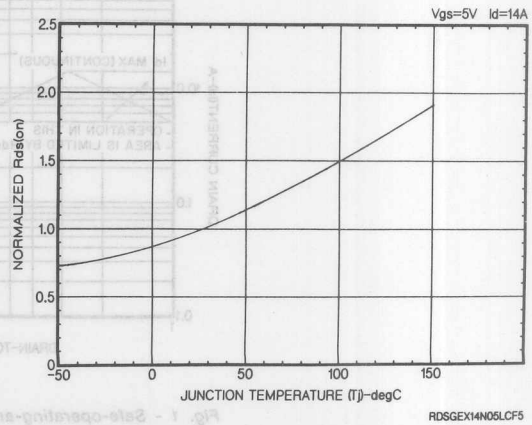


Fig. 7 - Normalized $r_{DS}(on)$ vs. junction temperature.

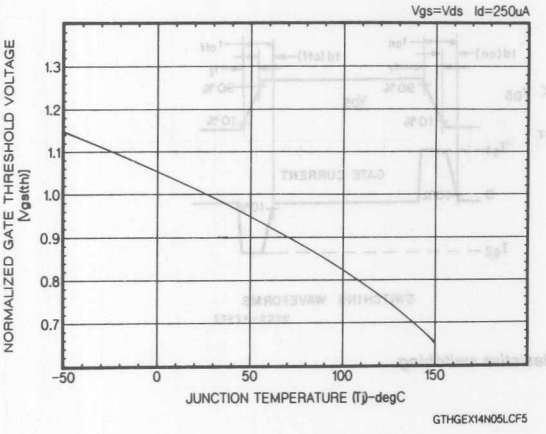


Fig. 8 - Gate threshold voltage vs. temperature.

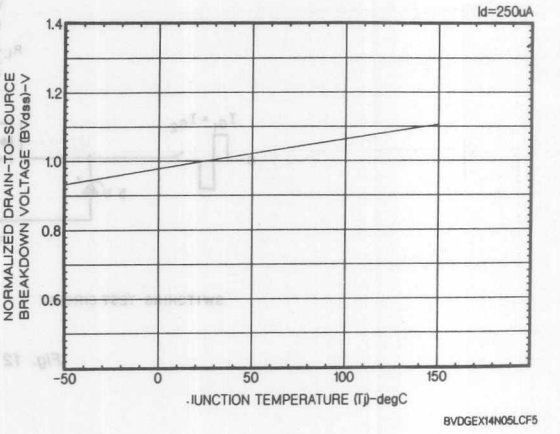


Fig. 9 - Drain source breakdown voltage vs. temperature.

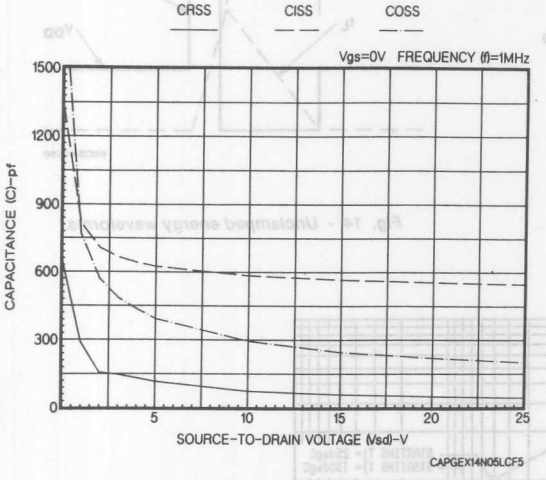


Fig. 10 - Typical capacitance vs. voltage.

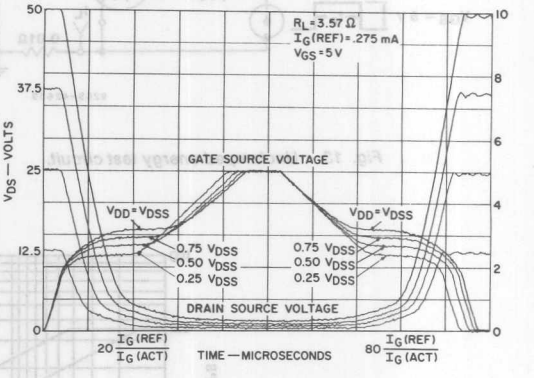


Fig. 11 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

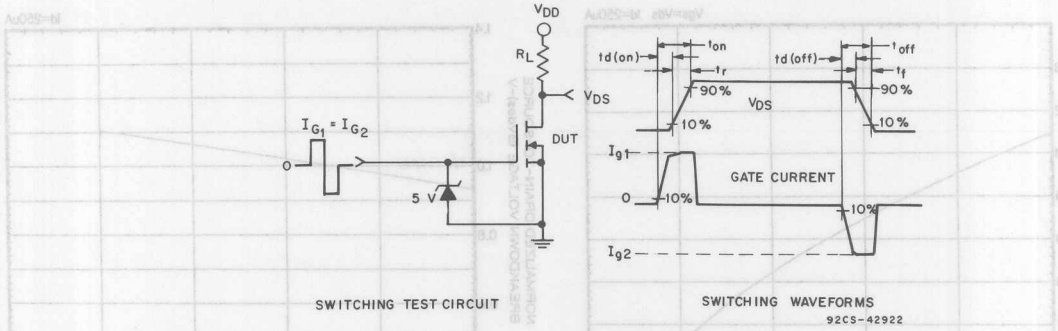


Fig. 12 - Resistive switching.

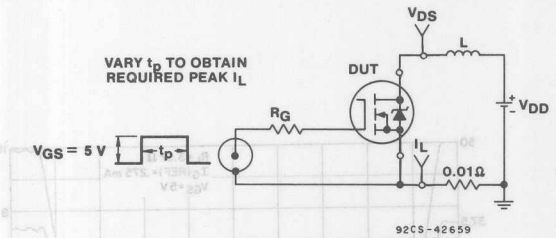


Fig. 13 - Unclamped energy test circuit.

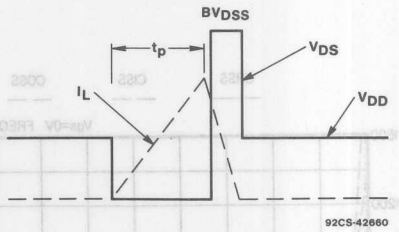


Fig. 14 - Unclamped energy waveforms.

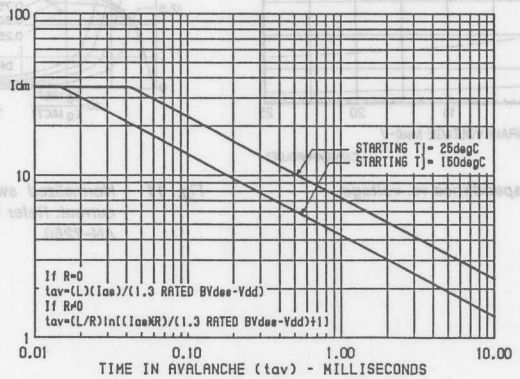


Fig. 15 - Unclamped inductive switching.

RFM15N05L/06L
RFP15N05L/06L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 15A, 50V and 60V
- $r_{DS(ON)} = 0.14\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

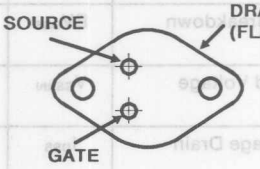
The RFM15N05L and RFM15N06L and the RFP15N05L and RFP15N06L are N-channel enhancmement-mode silicon-gate power field-effect transistors specifically designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

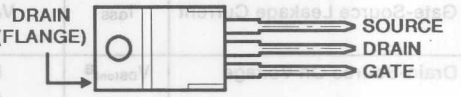
Because of space limitations branding (marking) on type RFP15N05L is F15N05L and on type RFP15N06L is F15N06L.

Package

TO-204AA
BOTTOM VIEW

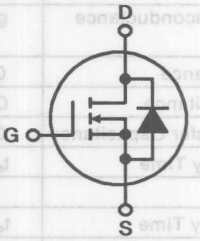


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFM15N05L	RFM15N06L	RFP15N05L	RFP15N06L	UNITS
Drain-Source Voltage	V_{DS}	50	60	50	60	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	50	60	50	60	V
Continuous Drain Current						
RMS Continuous	I_D	15	15	15	15	A
Pulsed Drain Current	I_{DM}	40	40	40	40	A
Gate-Source Voltage	V_{GS}	±10	±10	±10	±10	V
Maximum Power Dissipation						
$T_C = +25^oC$	P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly		0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1558.1**

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05L RFP15N05L		RFM15N06L RFP15N06L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	50	—	60	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V	—	1	—	—	μA
		V_{DS} = 50 V	—	—	—	1	
		T_C = 125° C, V_{DS} = 40 V	—	50	—	—	
		T_C = 125° C, V_{DS} = 50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 7.5 A, V_{GS} = 5 V	—	1.05	—	1.05	V
		I_D = 15 A, V_{GS} = 5 V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 7.5 A, V_{GS} = 5 V	—	0.14	—	0.14	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 7.5 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	—	900	—	900	pF
Output Capacitance	C_{oss}		—	450	—	450	
Reverse-Transfer Capacitance	C_{rss}		—	200	—	200	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 7.5 A, R_{gen} = ∞, R_{gs} = 6.25 Ω, V_{GS} = 5 V	16(typ)	40	16(typ)	40	ns
Rise Time	t_r		250(typ)	325	250(typ)	325	
Turn-Off Delay Time	$t_{d(off)}$		200(typ)	325	200(typ)	325	
Fall Time	t_f		225(typ)	325	225(typ)	325	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM15N05L, RFM15N06L	—	1.67	—	1.67	°C/W
		RFP15N05L, RFP15N06L	—	2.083	—	2.083	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05L RFP15N05L		RFM15N06L RFP15N06L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 7.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100A/μs	225 (typ.)		225 (typ.)		ns

[a] Pulsed: Pulse duration = 300 μs, duty cycle = 2%.

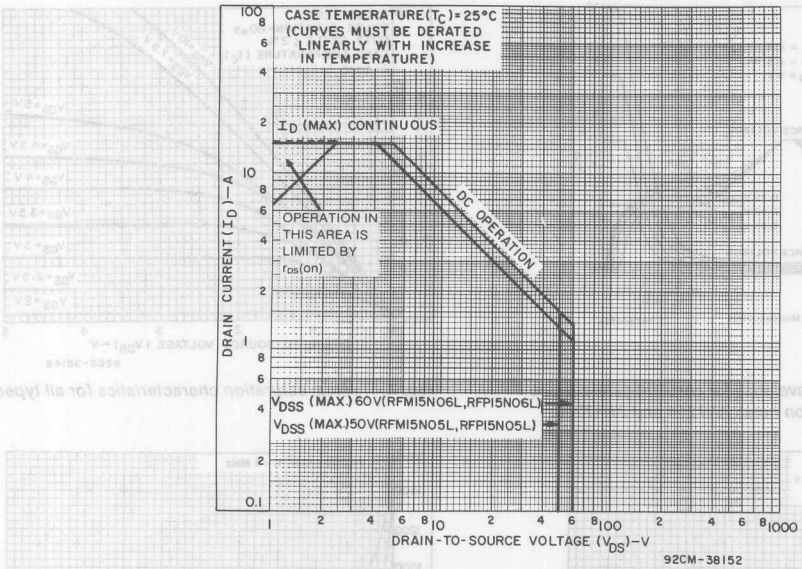


Fig. 1 - Maximum safe operating areas for all types.

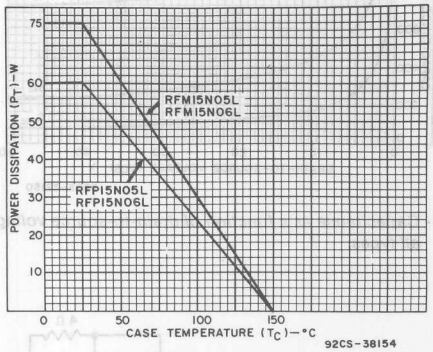


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

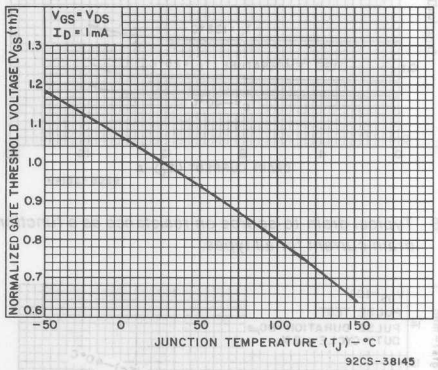


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

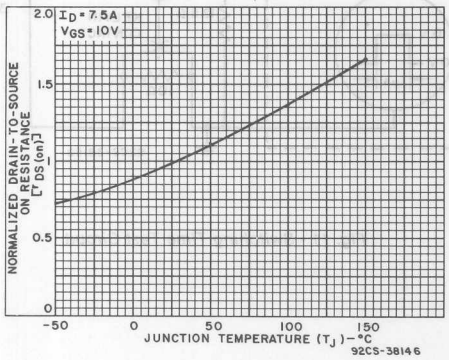


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

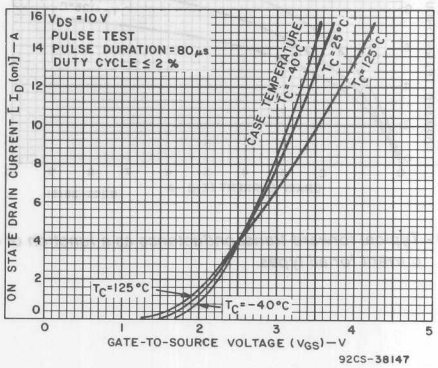


Fig. 5 - Typical transfer characteristics for all types.

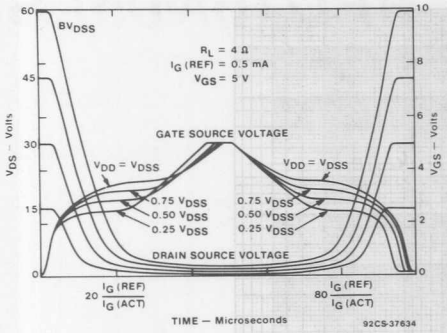


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

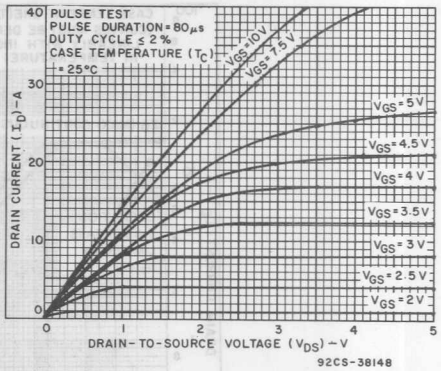


Fig. 7 - Typical saturation characteristics for all types.

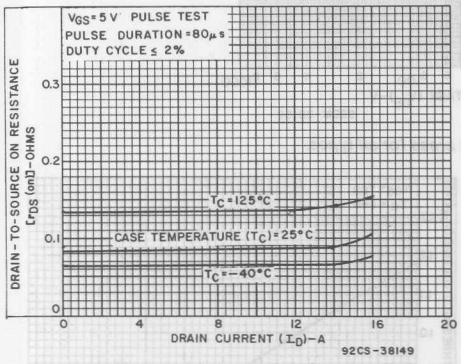


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

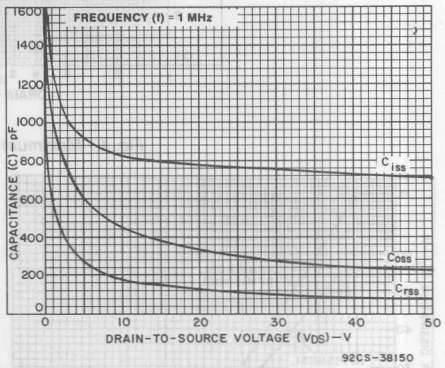


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

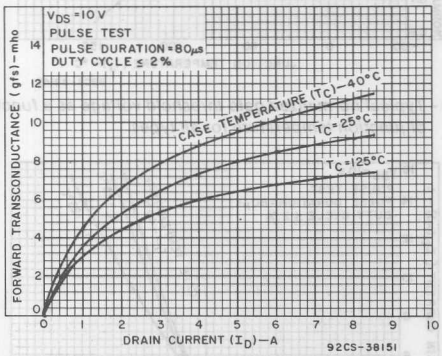


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

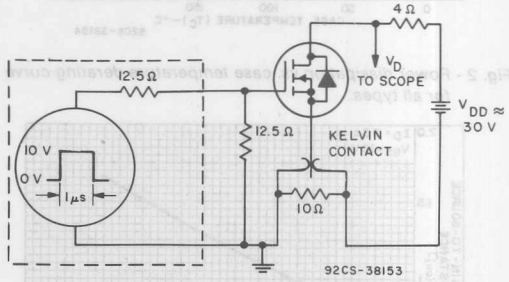


Fig. 11 - Switching Time Test Circuit.

HARRIS SEMICONDUCTOR

RFD16N05L
RFD16N05LSM

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

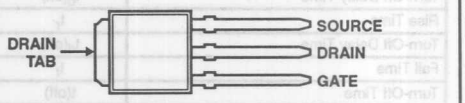
June 1992

Features

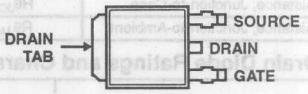
- 16A, 50V
- $r_{DS}(ON) = 0.047\Omega$
- UIS SOA Rating Curves (Single Pulse)
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Operating Temperature +150°C

Package

TO-251AA
TOP VIEW



TO-252AA
TOP VIEW



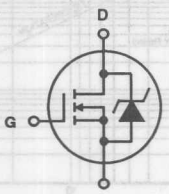
Description

The RFD16N05L and RFD16N05LSM N-channel logic level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. The RFD16N05L and RFD16N05LSM were designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFD16N05L is supplied in the JEDEC TO-251 plastic package and the RFD16N05LSM in the JEDEC TO-252 plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25°C$), Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	50	V
Continuous Drain Current			
RMS Continuous	I_D	16	A
Pulsed Drain Current	I_{DM}	45	A
Single Pulse Avalance Rating		Refer to UIS SOA Curve	
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
$T_C = +25°C$	P_D	60	W
Above $T_C = +25°C$, Derate Linearly		0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

6
LOGIC LEVEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2269.1**

Electrical Characteristics At Case Temperature (Tc) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 2.05mA, V_{GS} = 0V		50	-	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS} = V_{DS}$, I_D = 2.05mA		1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V T_C = 150°C		-	1 50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GC} = ±10V, V_{DS} = 0V		-	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D = 16A, V_{GS} = 5V I_D = 16A, V_{GS} = 4V		- -	0.047 0.056	W
Turn-On Time	t(on)	V_{DD} = 25V, I_D = 8A, $I_{G1} = I_{G2}$ = 0.4A, V_{GS} (clamp) + 5V, -0.6V, R_L = 3.125Ω		-	60	ns
Turn-On Delay Time	$t_d(on)$			-	14(typ)	ns
Rise Time	t_r			-	30 (typ)	ns
Turn-Off Delay Time	$t_d(off)$			-	42 (typ)	ns
Fall Time	t_f			-	14 (typ)	ns
Turn-Off Time	t(off)			-	100	ns
Total Gate Charge	Q_g(total)	V_{GS} = 0-10V	V_{DD} = 40V, I_D = 16A, R_L = 2.5Ω	-	80	nC
Gate Charge at 5V	Qg(5)	V_{GS} = 0-5V		-	45	nC
Threshold Gate Charge	Qg(th)	V_{GS} = 0-1V		-	3	nC
Plateau Voltage	V(plateau)	I_D = 16A, V_{DS} = 15V		-	4	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 8A, R_L = 3.125Ω, L = 0.2µH, $I_{g1} = I_{g2}$ = 0.8A, V_{GS}(clamp) +5V, -0.6V		-	19	µJ
Thermal Resistance, Junction-to-Case	$R\theta_{JC}$			-	2.083	°C/W
Thermal Resistance, Junction-to-Ambient	$R\theta_{JA}$			-	100	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 16A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 16A, dI_F/d_t = 100A/µs	-	125	ns

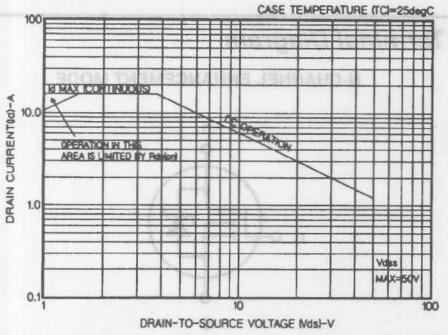


FIGURE 1. SAFE OPERATING AREA CURVE. (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN TEMP.)

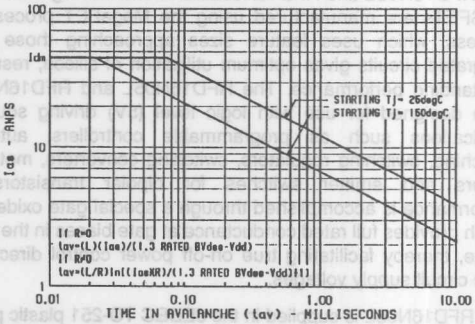


FIGURE 2. UNCLAMPED INDUCTIVE SWITCHING SOA. (SINGLE PULSE UIS SOA

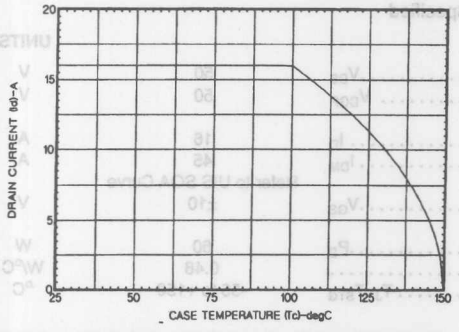


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

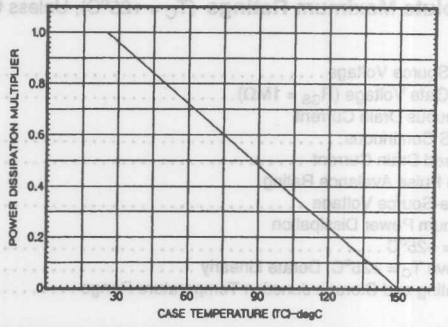


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

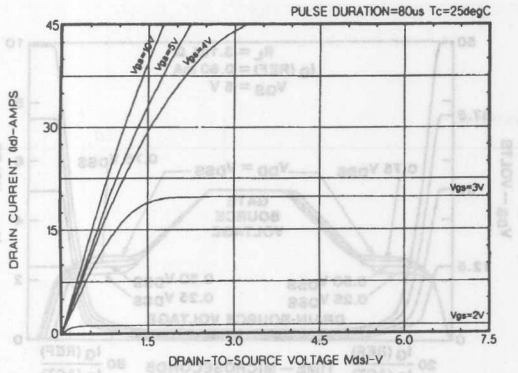


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

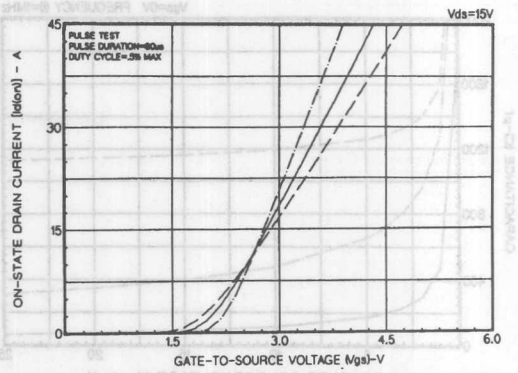


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

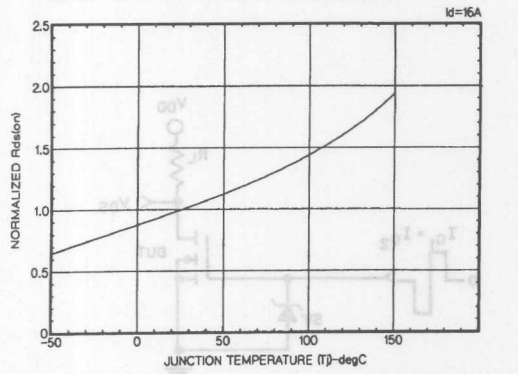


FIGURE 7. NORMALIZED $r_{DS}(on)$ vs JUNCTION TEMPERATURE

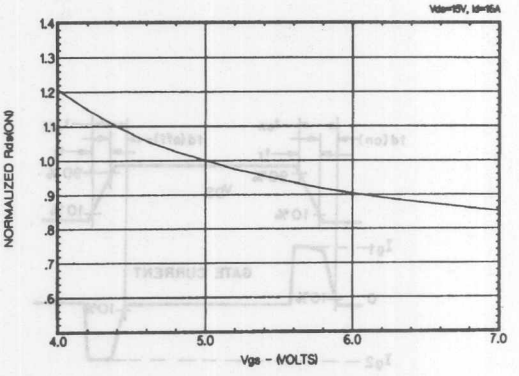


FIGURE 8. NORMALIZED $r_{DS}(on)$ vs V_{GS}

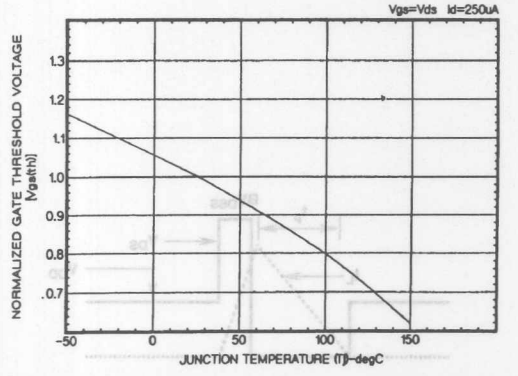


FIGURE 9. TYPICAL NORMALIZED GATE THRESHOLD VOLTAGE

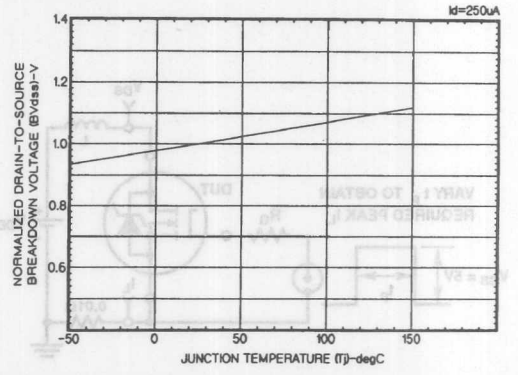


FIGURE 10. DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

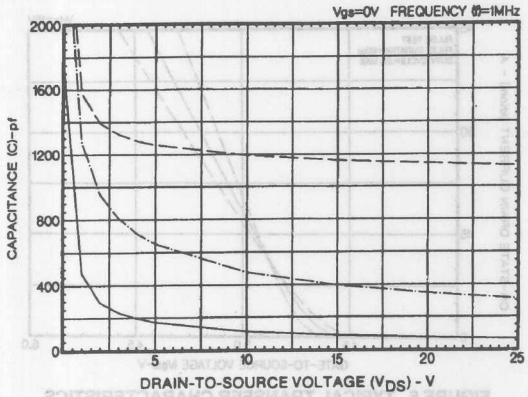


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

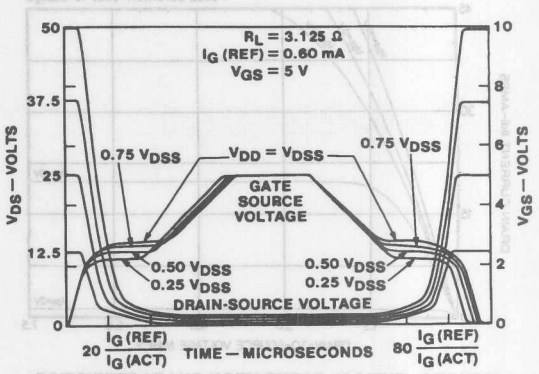
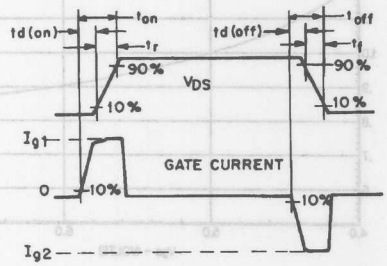
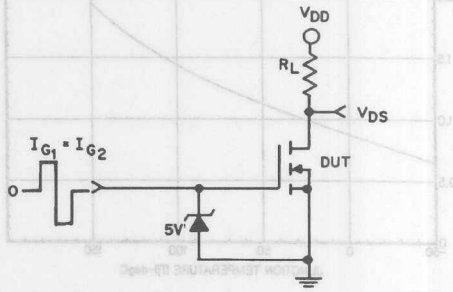


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260.



SWITCHING WAVEFORMS



SWITCHING TEST CIRCUIT

FIGURE 13. RESISTIVE SWITCHING

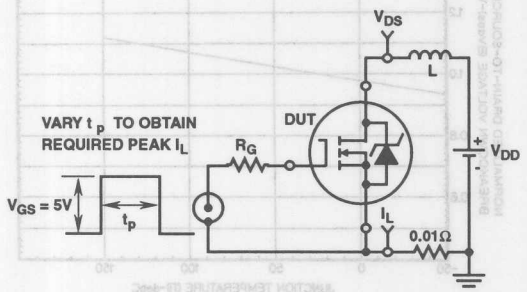


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

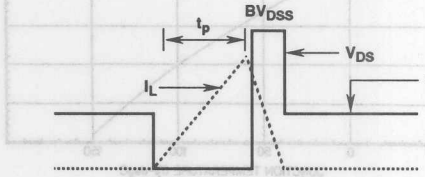


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

Spice Model (RFD16N05L)

```
.SUBCKT RFD16N05L  2  1  3;  rev 04/08/92
*Nominal Temperature = 25°C
.MODEL MOSMOD NMOS (VTO=2.054  KP=24.73  IS=1e-30  N=10  TOS=1  L=1u  W=1u)
Vto  21  6  0.448
Rsource  8  7  RDSMOD  0.614E-3
Rdrain  5  16  RDSMOD  27.38E-3
.MODEL RDSMOD RES (TC1=3.66E-3  TC2=1.46E-5)
.MODEL RVTOMOD RES (TC1=-1.81E3  TC2=1.41E-6)
.MODEL RVTOMOD2 RES (TC1=0  TC2=0)
Ebreak 11  7  17  18  70.9
.MODEL RBKMOD RES (TC1=1.01E-3  TC2=5.21E-8)
.MODEL DBKMOD D (RS=8.82E-2  TRS1=-2.01E-3  TRS2=7.32E-10)
.MODEL DBDMOD D (IS=1.34E-13  RS=1.21E-2  TRS1=1.64E-3  TRS2=2.59E-6  +CJO=1.13E-9  TT=4.14E-8)
Cin  6  8  1.21E-9
Ca  12  8  3.33E-9
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-4.25  VOFF=-2.25)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-2.25  VOFF=-4.25)
.MODEL DPLCAPMOD D (CJO=5.22E-10  IS=1e-30  N=10)
Cb  12  14  3.11E-9
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-0.65  VOFF=4.35)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=4.35  VOFF=-0.65)
Rgate  9  20  2.98
Lgate  1  9  1.38E-9
Ldrain  2  5  1.0E-12
Lsource  3  7  1.0E-9
Dbody  7  5  DBDMOD
Dbreak  5  11  DBKMOD
Dplcap  10  5  DPLCAPMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Evto  20  6  18  8  1
It  8  17  1
MOS1  16  6  8  8  MOSMOD  M=0.99
MOS2  16  21  8  8  MOSMOD  M=0.01
Rbreak  17  18  RBKMOD  1
Rin  6  8  1e9
Rvto  18  19  RVTOMOD  1
S1a  6  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
.ENDS
```

HARRIS

RFP17N06L

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 17A, 60V
- $r_{DS(ON)} = 0.100\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

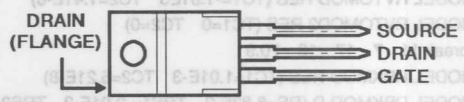
Description

The RFP17N06L is an N-Channel enhancement mode silicon-gate power field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP17N06L is supplied in the JEDEC TO-220AB plastic package.

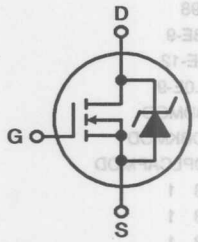
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	60	V
Continuous Drain Current			
RMS Continuous	I_D	17	A
Pulsed Drain Current	I_{DM}	50	A
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
T_C = +25°C	P_D	60	W
Above T_C = +25°C, Derate Linearly		0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2272.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified.*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1.0 mA, V_{GS} = 0 V	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1.0 mA	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48V, V_{GS} = 0 V	—	1	μA
		T_C = 150°C		50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V	—	100	nA
On Resistance	$R_{DS}(on)$	I_D = 8.5 A, V_{GS} = 4.0 V	—	0.150	Ω
		I_D = 8.5 A, V_{GS} = 5.0 V	—	0.100	Ω
		I_D = 17.0 A, V_{GS} = 5.0 V	—	0.130	Ω
Forward Transconductance	g_{FS}	I_D = 8.5 A, V_{DS} = 5.0 V	6.0	—	S
Turn-On Delay Time	$T_d(on)$	V_{DD} = 30 V, I_D = 8.5 A	—	40	ns
Rise Time	T_R	R_{GEN} = 12.5 ohms	—	150	ns
Turn-Off Delay Time	$T_d(off)$	R_{GS} = 12.5 ohms	—	240	ns
Fall Time	T_F	V_{GS} = +5 V	—	110	ns
Total Gate Charge	$Q_g(total)$	I_D = 8.5 A, V_{DD} = 30 V	—	45	nC
		V_{GS} = 10 V, R_L = 3.5 ohms			
Gate Charge at 5 volts	$Q_g(5)$	V_{GS} = 5 V	—	25	nC
Threshold Gate Charge	$Q_g(th)$	V_{GS} = 1 V	—	2.0	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		—	2.083	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		—	80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Forward Voltage	V_{SD}	I_{SD} = 17 A	—	1.2	V
Reverse Recovery Time	t_{rr}	I_F = 17 A, dI_F/d_t = 100 A/μs	115 (typ)		ns

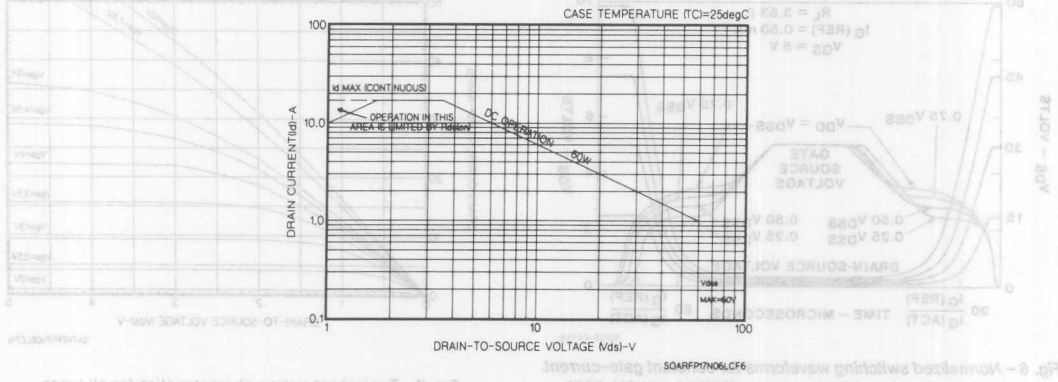


Fig. 1 - Maximum safe operating areas for all types.

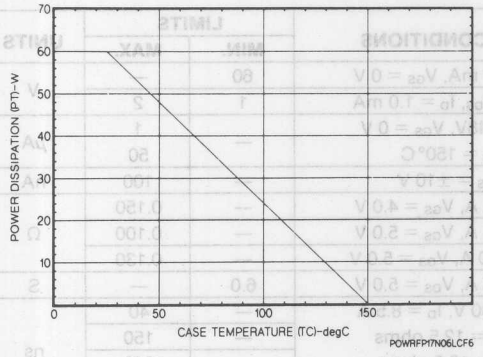


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

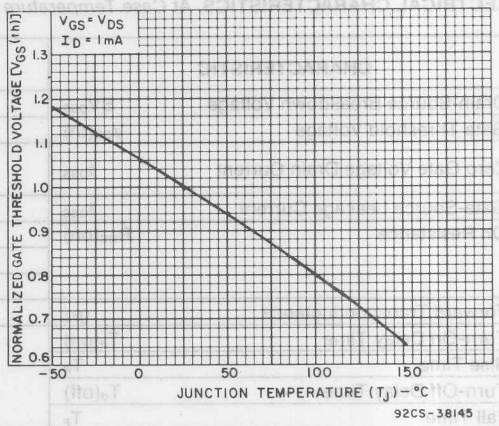


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

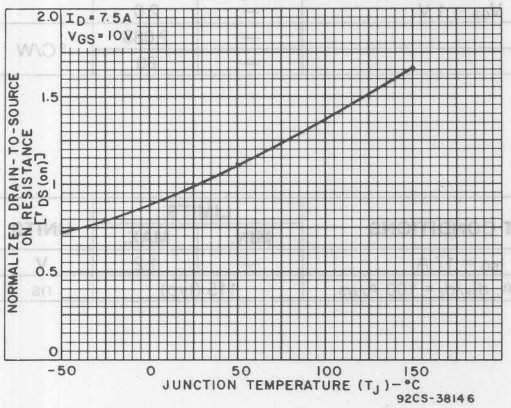


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

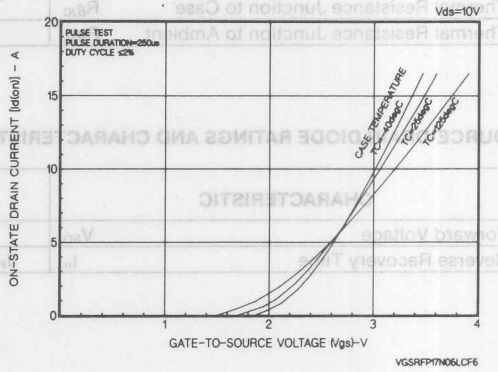


Fig. 5 - Typical transfer characteristics for all types.

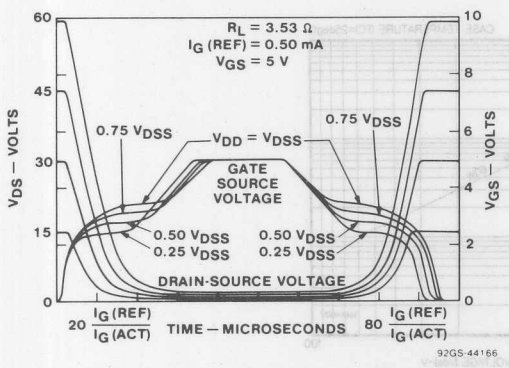


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

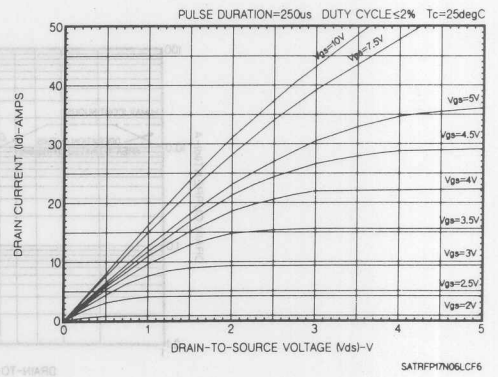


Fig. 7 - Typical saturation characteristics for all types.

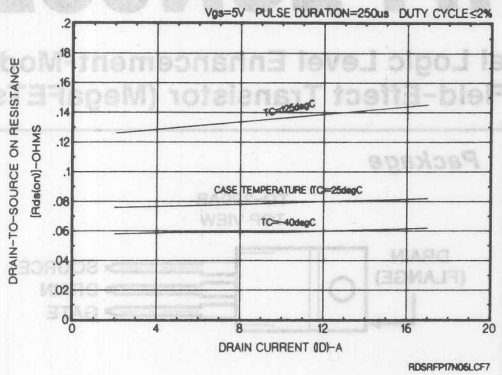


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

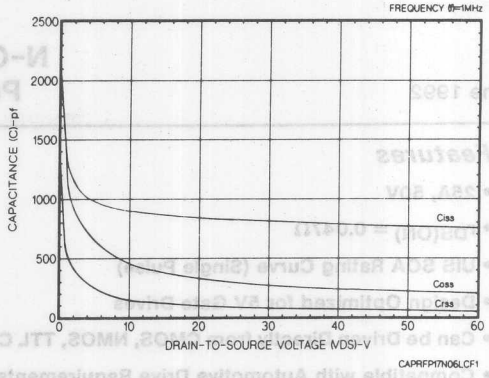


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

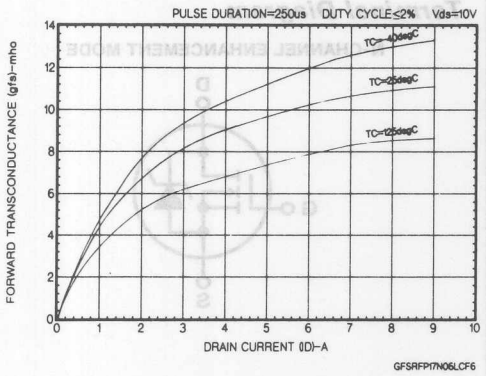


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

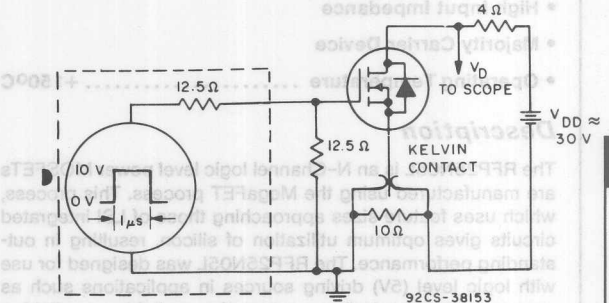


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFP25N05L

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistor (MegaFETs)

June 1992

Features

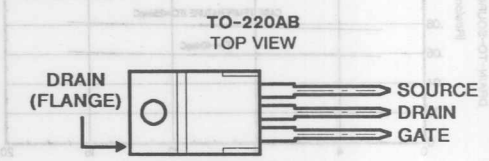
- 25A, 50V
- $r_{DS(ON)} = 0.047\Omega$
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Operating Temperature ..... +150°C

Description

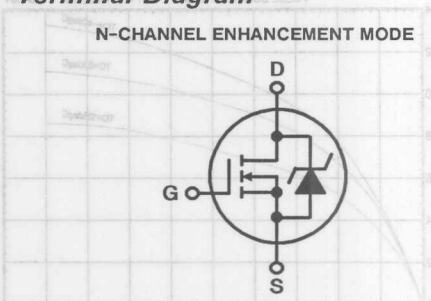
The RFP25N05L is an N-Channel logic level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. The RFP25N05L was designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP25N05L is supplied in the JEDEC TO-220AB plastic package.

Package



Terminal Diagram



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	V
Continuous Drain Current			
RMS Continuous	I_D	25	A
Pulsed Drain Current	I_{DM}	65	A
Single Pulse Avalanche Energy Rating		Refer to UIS SOA Curve*	
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
T_C = +25°C	P_D	60	W
Above T_C = +25°C, Derate Linearly		0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

* See Figures 13, 14 and 15

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2270.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified:*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V T_C = 150°C		—	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D = 25 A, V_{GS} = 5 V I_D = 25 A, V_{GS} = 4 V		—	0.047 0.056	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 12.5 A I_{g1} = I_{g2} = 1 A V_{GS} (clamp) + 5 V, −0.6 V R_L = 2 Ω		—	60	ns
Turn-On Delay Time	$t_d(on)$			—	15 (typ.)	
Rise Time	t_r			—	35 (typ.)	
Turn-Off Delay Time	$t_d(off)$			—	40 (typ.)	
Fall Time	t_f			—	14 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	Q_g(total)	V_{GS} = 0-10 V	V_{DD} = 40 V	—	80	nC
Gate Charge at 5 V	$Q_g(5)$	V_{GS} = 0-5 V	I_D = 25 A	—	45	
Threshold Gate Charge	$Q_g(th)$	V_{GS} = 0-1 V	R_L = 1.6 Ω	—	3	
Plateau Voltage	V(plateau)	I_D = 25 A, V_{DS} = 15 V		—	4	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 12.5 A, R_L = 2 Ω L = 0.2 μH, I_{g1} = I_{g2} = 1 A V_{GS} (clamp) + 5 V, −0.6 V		—	30	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	2.083	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 25 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 25 A, dI_F/d_t = 100 A/μs	—	125	ns

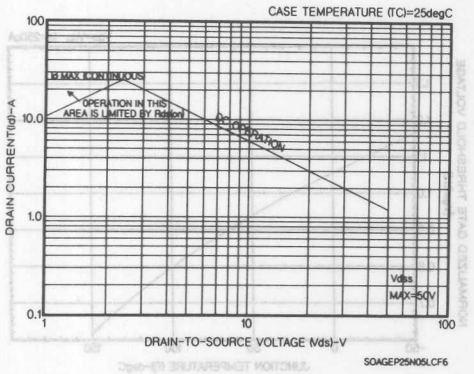


Fig. 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

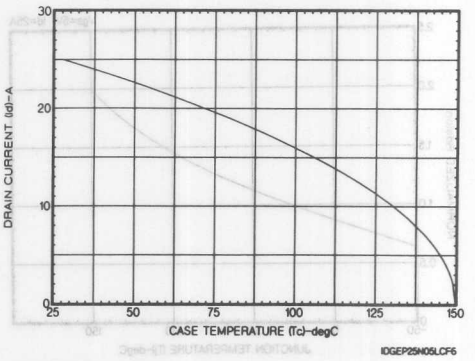


Fig. 2 - Maximum continuous drain current vs. temperature.

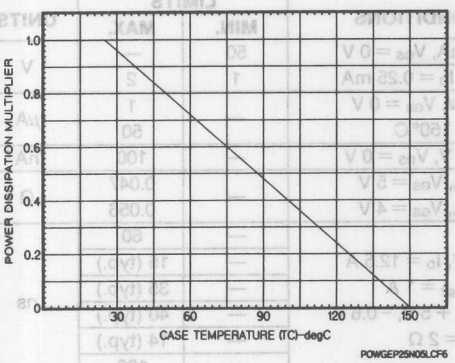


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

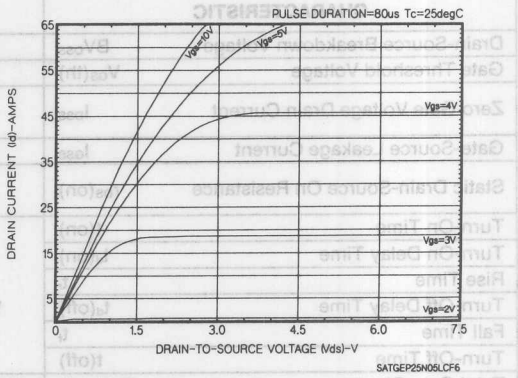


Fig. 4 - Typical saturation characteristics.

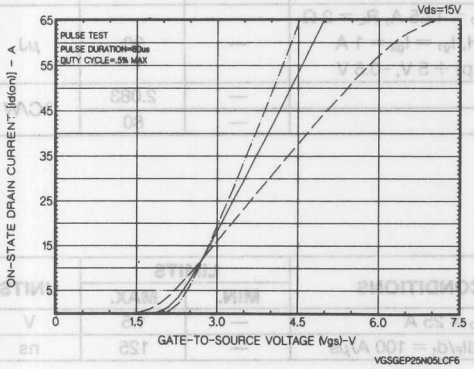


Fig. 5 - Typical transfer characteristics.

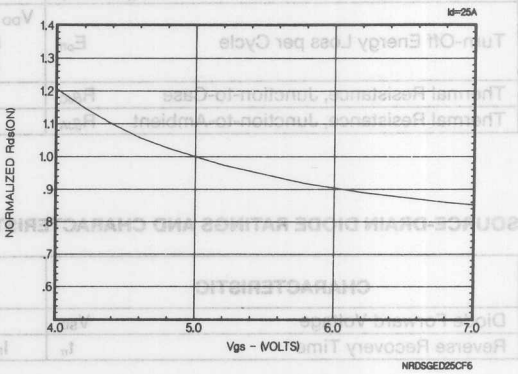


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

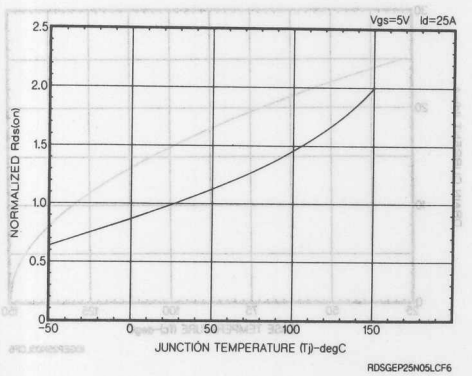


Fig. 7 - Normalized $r_{ds}(on)$ vs. junction temperature.

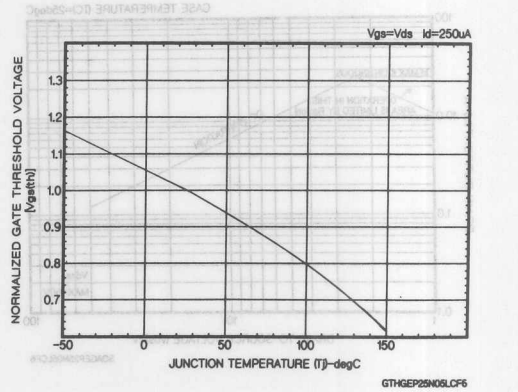


Fig. 8 - Typical normalized gate threshold voltage.

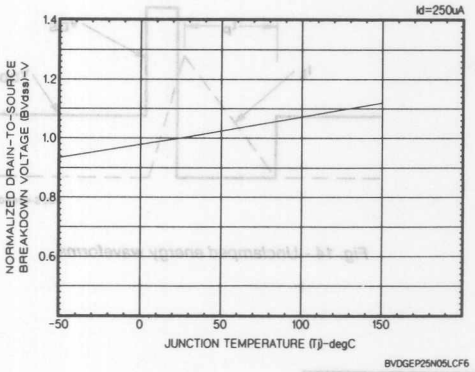


Fig. 9 - Drain source breakdown voltage vs. temperature.

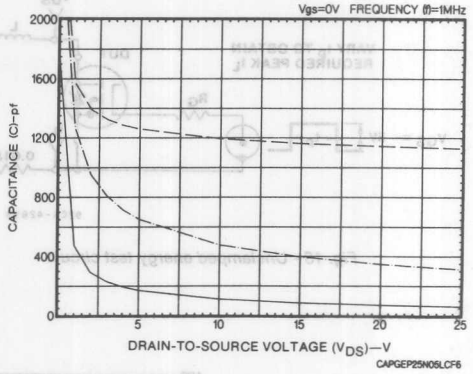


Fig. 10 – Typical capacitance vs. voltage

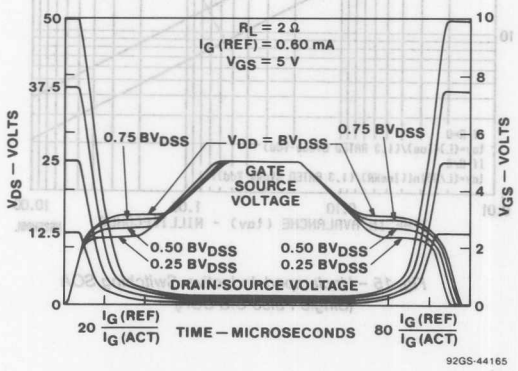


Fig. 11 – Normalized switching waveforms for constant gate-current
(Refer to Harris application notes AN-7254 and AN-7260)

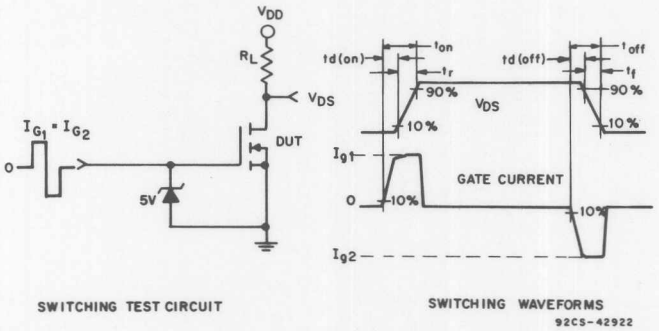


Fig. 12 - Resistive switching.

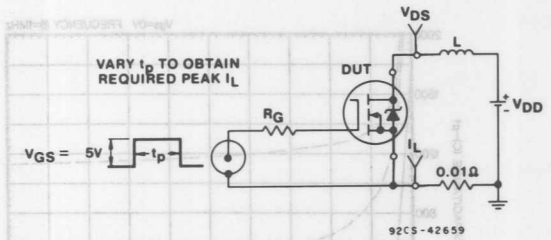


Fig. 13 - Unclamped energy test circuit.

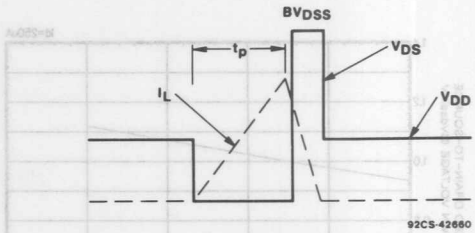


Fig. 14 - Unclamped energy waveforms.

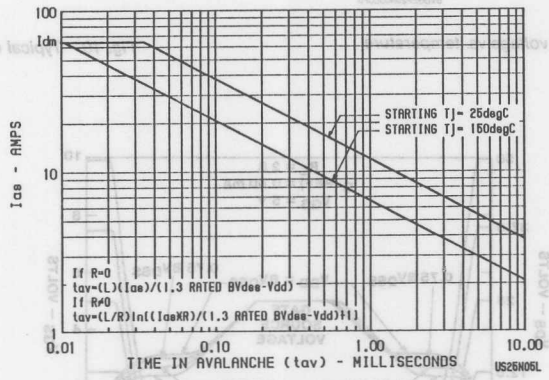


Fig. 15 – Unclamped-Inductive-Switching SOA
(Single Pulse UIS SOA)

HARRIS

RFP25N06L

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistor (L^2FET)

August 1991

Features

- 25A, 60V
- $r_{DS(ON)} = 0.085\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

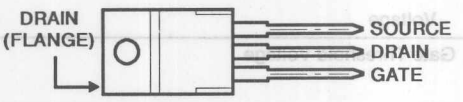
The RFP25N06L is an N-Channel enhancement-mode silicon-gate power field-effect transistor specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP25N06L is supplied in the JEDEC TO-220AB plastic package.

Because of space limitations branding (marking) on type RFP25N06L is F25N06L.

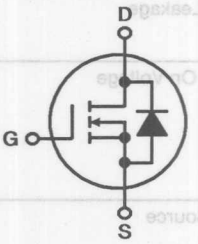
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	60	V
Continuous Drain Current			
RMS Continuous	I_D	25	A
RMS Continuous @ $T_C = +85^oC$		18	A
Pulsed Drain Current	I_{DM}	60	A
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
$T_C = +25^oC$	P_D	75	W
Above $T_C = +25^oC$ Derate Linearly		0.6	$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	^oC

6 LOGIC LEVEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2044.1**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTICS		TEST CONDITIONS	LIMITS RFP25N06L MIN.	LIMITS RFP25N06L MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1$ mA, $V_{GS} = 0$	60	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 1$ mA	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40$ V	—	—	μA
		$V_{DS} = 50$ V	—	1	
		$T_c = 125$ °C			
		$V_{DS} = 40$ V	—	—	
		$V_{DS} = 50$ V	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 10$ V, $V_{DS} = 0$	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	$I_D = 12.5$ A, $V_{GS} = 5$ V	—	1.06	V
		$I_D = 25$ A, $V_{GS} = 5$ V	—	2.5	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	$I_D = 12.5$ A, $V_{GS} = 5$ V	—	0.085	Ω
Forward Transconductance	g_{fs}[a]	$V_{DS} = 5$ V, $I_D = 12.5$ A	5	—	mho
Input Capacitance	C_{iss}	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1 MHz	—	2000	pF
Output Capacitance	C_{oss}		—	900	
Reverse Transfer Capacitance	C_{rss}		—	400	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = 30$ V, $I_D = 12.5$ A, $R_{gen} = \infty$, $R_{gs} = 6.25\ \Omega$, $V_{GS} = 5$ V	18 (typ.)	60	ns
Rise Time	t_r		120 (typ.)	225	
Turn-Off Delay Time	$t_{d(off)}$		123 (typ.)	225	
Fall Time	t_f		123 (typ.)	200	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFP25N06L	—	1.67	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

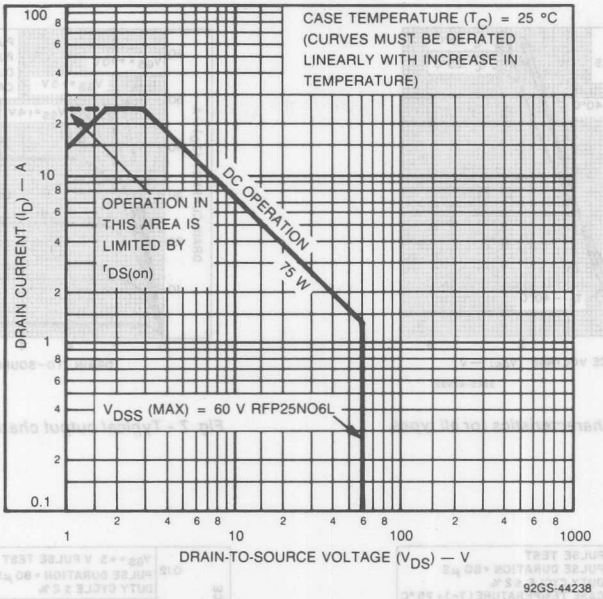


Fig. 1 - Maximum operating areas for all types.

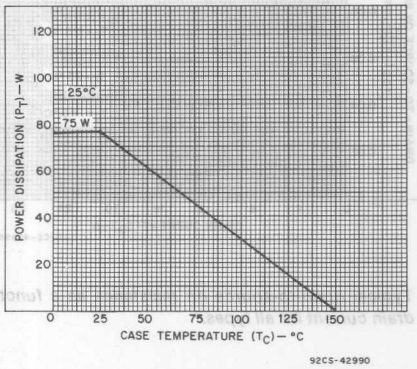


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

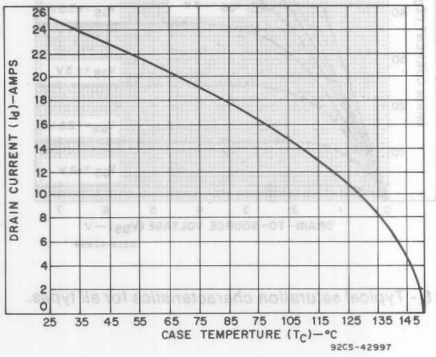


Fig. 3 - Maximum continuous drain current vs. case temperature.

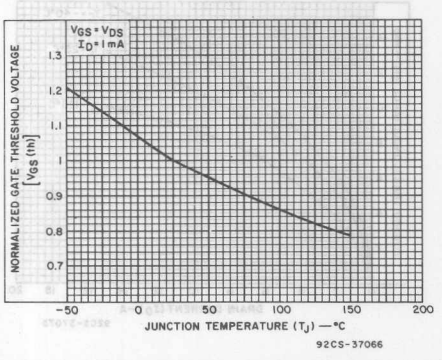


Fig. 4 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

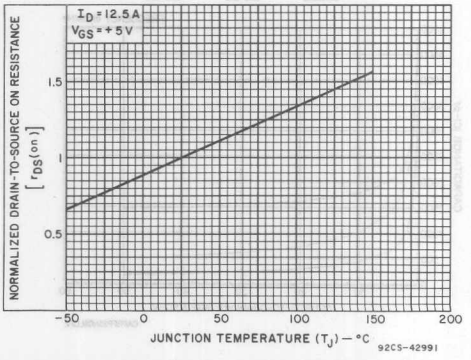


Fig. 5 - Normalized drain-to-source on resistance to junction temperature for all types.

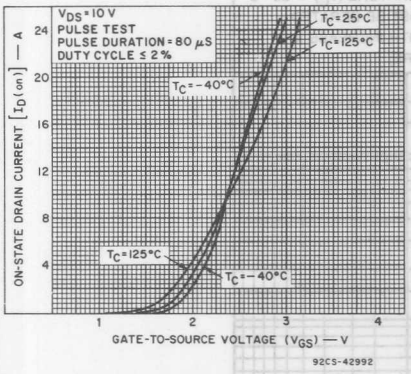


Fig. 6 - Typical transfer characteristics for all types.

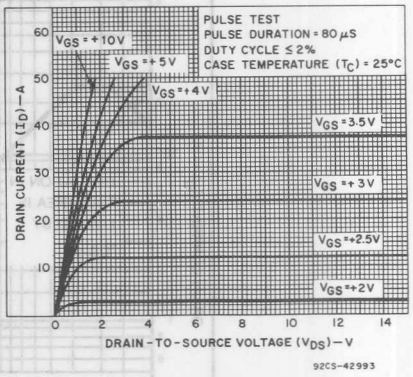


Fig. 7 - Typical output characteristics for all types.

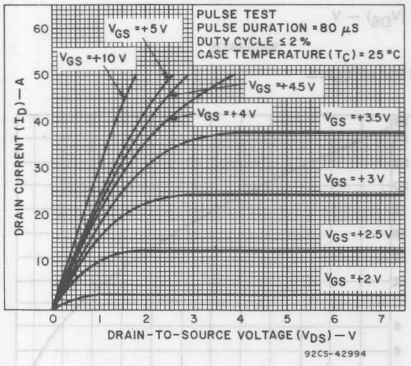


Fig. 8 - Typical saturation characteristics for all types.

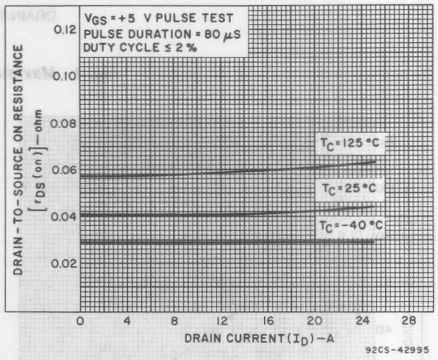


Fig. 9 - Typical drain-to-source on resistance as a function of drain current for all types.

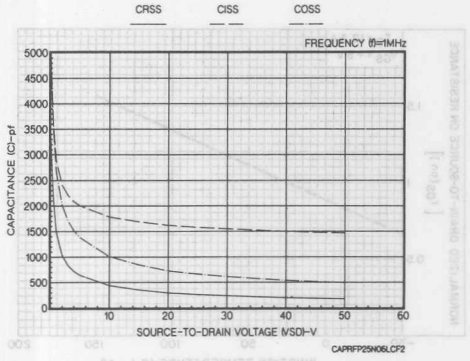


Fig. 10 - Typical capacitance vs. voltage.

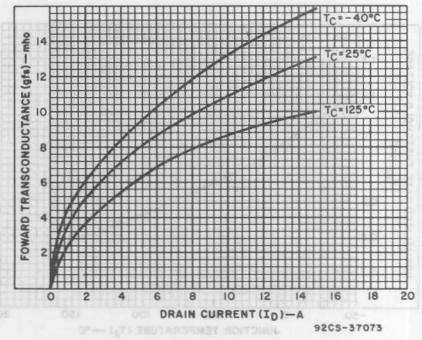


Fig. 11 - Typical forward transconductance as a function of drain current for all types.

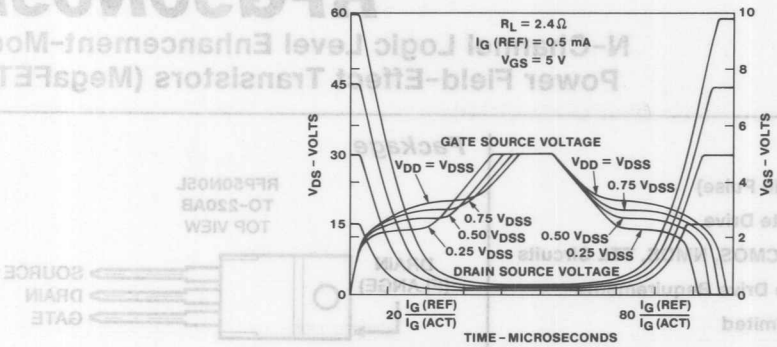


Fig. 12 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.





HARRIS

RFP50N05L
RFG50N05L

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

May 1992

Features

- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

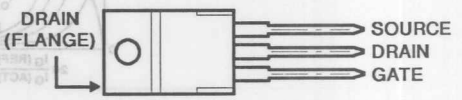
Description

The RFP50N05L and RFG50N05L N-channel logic-level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic-level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers, and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from integrated circuit supply voltages.

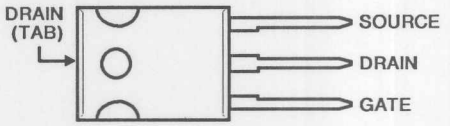
The RFP50N05L is supplied in the JEDEC TO-220AB plastic package and the RFG50N05L is supplied in the TO-247 plastic package.

Package

RFP50N05L
TO-220AB
TOP VIEW

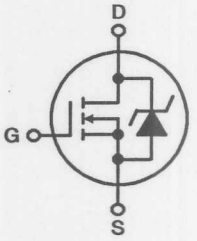


RFG50N05L
TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Maximum Ratings, Absolute-Maximum Values (T_C = +25°C)

			UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	V
Continuous Drain Current			
RMS Continuous	I_D	50	A
Pulsed Drain Current	I_{DM}	130	A
Single Pulse Avalance Rating, Refer to UIS SOA Curve			
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
T_C = +25°C	P_D	110	W
Above T_C = +25°C, Derate Linearly		0.88	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2424.1

ELECTRICAL CHARACTERISTICS *At Case Temperature (Tc) = 25°C unless otherwise specified.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	ID = 0.25 mA, VGS = 0 V		50	–	V
Gate Threshold Voltage	VGS(th)	VGS = VDS, ID = 0.25 mA		1	2	V
Zero Gate Voltage Drain Current	IDSS	VDS = 40 V, VGS = 0 V Tc = 150°C		–	1 50	µA
Gate-Source Leakage Current	IGSS	VGS = ±10 V, VDS = 0 V		–	100	nA
Static Drain-Source on Resistance	rDS(on)	ID = 50 A, VGS = 5 V ID = 50 A, VGS = 4 V		– –	0.022 0.027	Ω
Turn-On Time	t(on)	VDD = 25 V, ID = 25 A Ig1 = Ig2 = 2 A VGS (clamp): +5 V, -0.6 V RL = 1 Ω		–	100	ns
Turn-On Delay Time	td(on)			15 (typ)	–	
Rise Time	tr			50 (typ)	–	
Turn-Off Delay Time	td(off)			50 (typ)	–	
Fall Time	tr			15 (typ)	–	
Turn-Off Time	t(off)			–	100	
Total Gate Charge	Qg(total)	VGS = 0 to 10 V	VDD = 40 V	–	140	nC
Gate Charge at 5V	Qg(5)	VGS = 0 to 5 V	ID = 50 A	–	80	
Threshold Gate Charge	Qg(th)	VGS = 0 to 1 V	RL = 0.8 Ω	–	6	
Plateau Voltage	V(plateau)	ID = 50 A, VDS = 15 V		–	4	V
Turn-Off Energy Loss per Cycle	Eoff	VDD = 25 V, ID = 25 A, RL = 1 Ω L = 0.2 µH, Ig1 = Ig2 = 2 A VGS (clamp): +5 V, -0.6 V		–	150	µJ
Thermal Resistance, Junction to Case	RθJC			–	1.14	°C/W
Thermal Resistance, Junction to Ambient	RθJA			–	80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	VSD	ISD = 50 A	–	1.5	V
Reverse Recovery Time	trr	ISD = 50 A, dISD/dt = 100 A/µs	–	1.25	ns

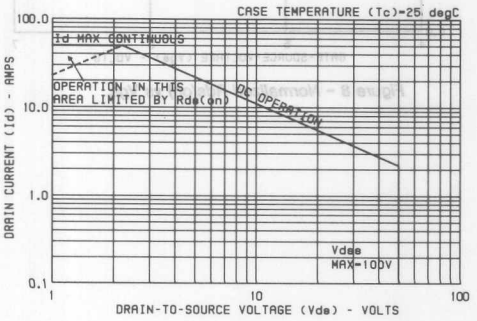


Figure 1 – Safe operating area curve.
(Curves must be derated linearly with increase in temperature.)

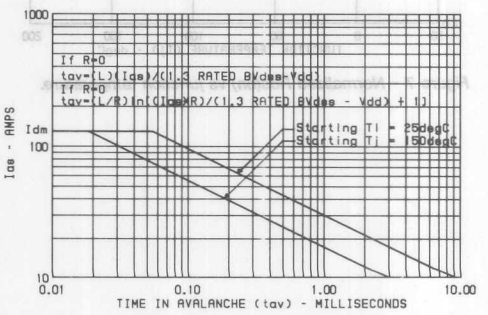


Figure 2 – Unclamped-inductive-switching safe-operating-area (single pulse UIS SOA). See Figure 14 for test circuit.

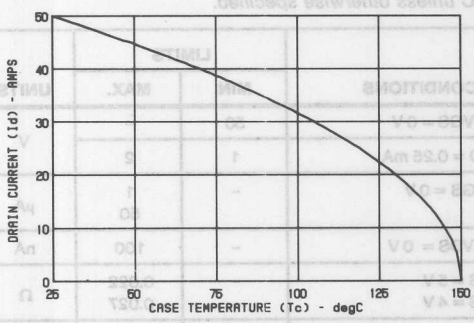


Figure 3 – Maximum continuous drain current vs. temperature.

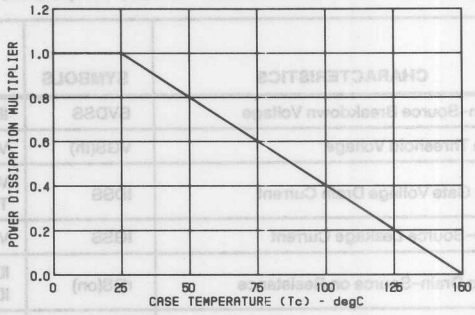


Figure 4 – Normalized power dissipation vs temperature derating curve.

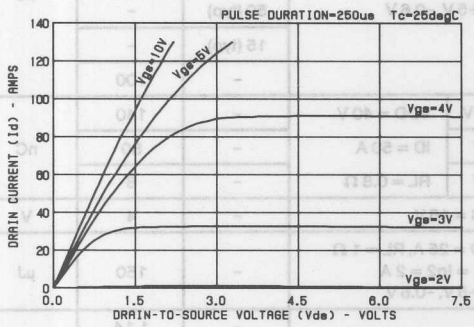


Figure 5 – Typical saturation characteristics.

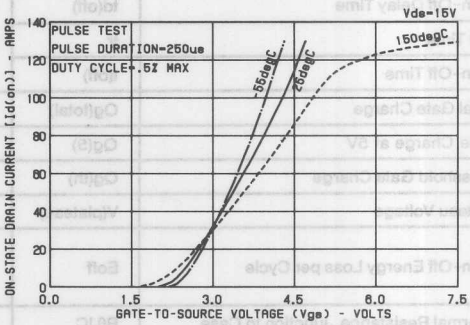


Figure 6 – Typical transfer characteristics.

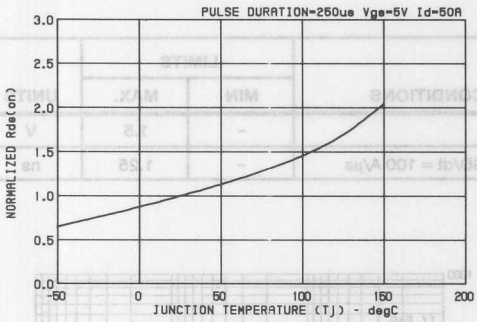


Figure 7 – Normalized Rds(on) vs junction temperature.

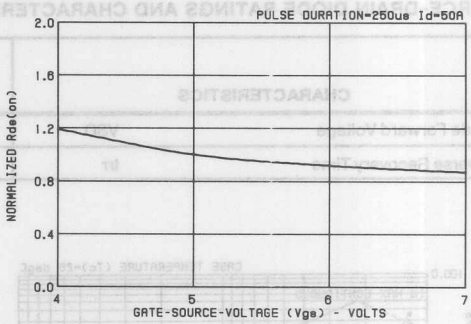


Figure 8 – Normalized Rds(on) vs Vgs.

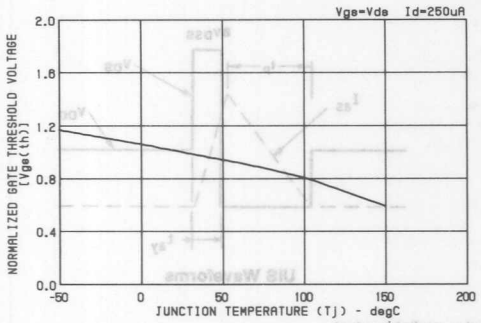


Figure 9 – Normalized gate threshold voltage.

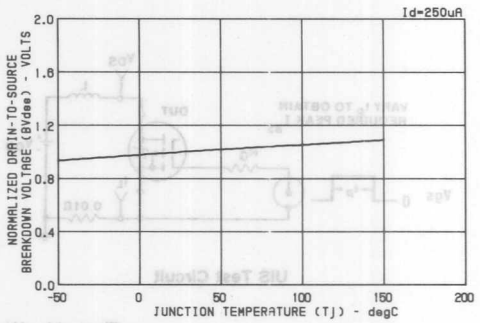


Figure 10 – Normalized drain source breakdown voltage vs temperature.

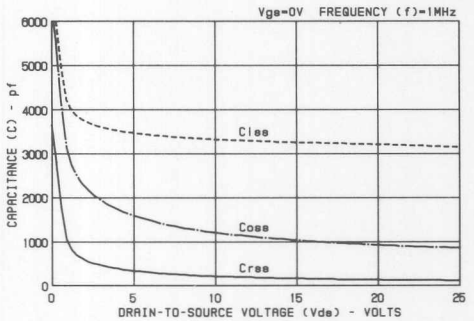


Figure 11 – Typical capacitance vs voltage.

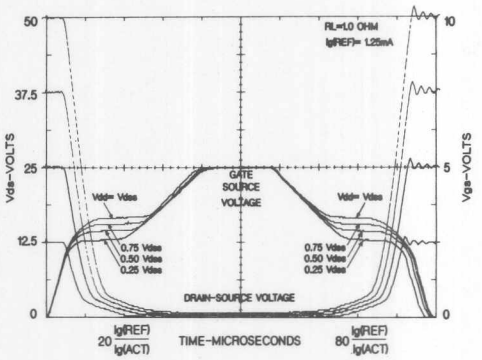
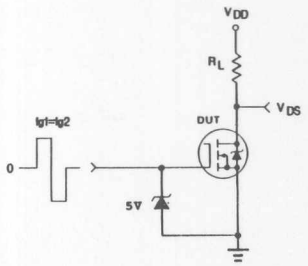
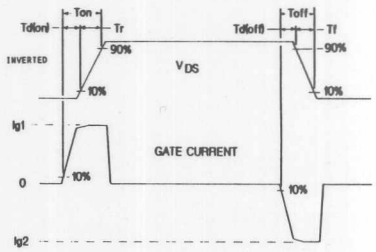


Fig. 12 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

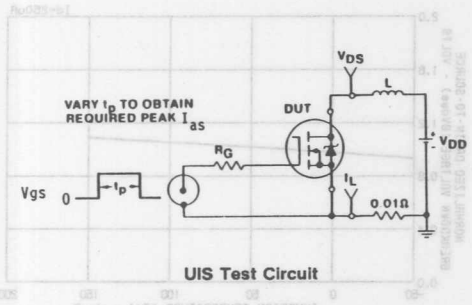


Switching Test Circuit

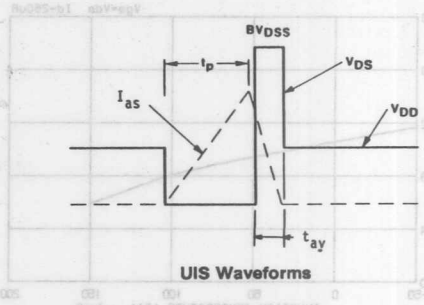


Switching Waveforms

Figure 13 – Resistive switching.



UIS Test Circuit



UIS Waveforms

Figure 14 – Unclamped-inductive-switching test.

POWER MOSFETs
LOGIC LEVEL

POWER MOSFETs 7

INSULATED GATE BIPOLAR TRANSISTORS

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2N6976	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)	7-5
2N6977	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)	7-5
2N6978	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)	7-5
HGTD6N40E1, S, HGTD6N50E1, S	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs)	7-9
HGTP6N40E1D, HGTP6N50E1D	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs) with Anti-Parallel Ultra-Fast Diode	7-13
HGTD10N40F1, S, HGTD10N50F1, S	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs)	7-18
HGTP10N40C1, E1, HGTP10N50C1, E1	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs)	7-22
HGTP10N40C1D, E1D, HGTP10N50C1D, E1D	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs) with Anti-Parallel Ultra-Fast Diode	7-27
HGTP10N40F1D, HGTP10N50F1D	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs) with Anti-Parallel Ultra-Fast Diode	7-32
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HGTH12N40C1D, E1D, HGTH12N50C1D, E1D	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs) with Anti-Parallel Ultra-Fast Diode	7-37
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HGTG12N60D1D	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT) with Anti-Parallel Ultra-Fast Diode	7-42

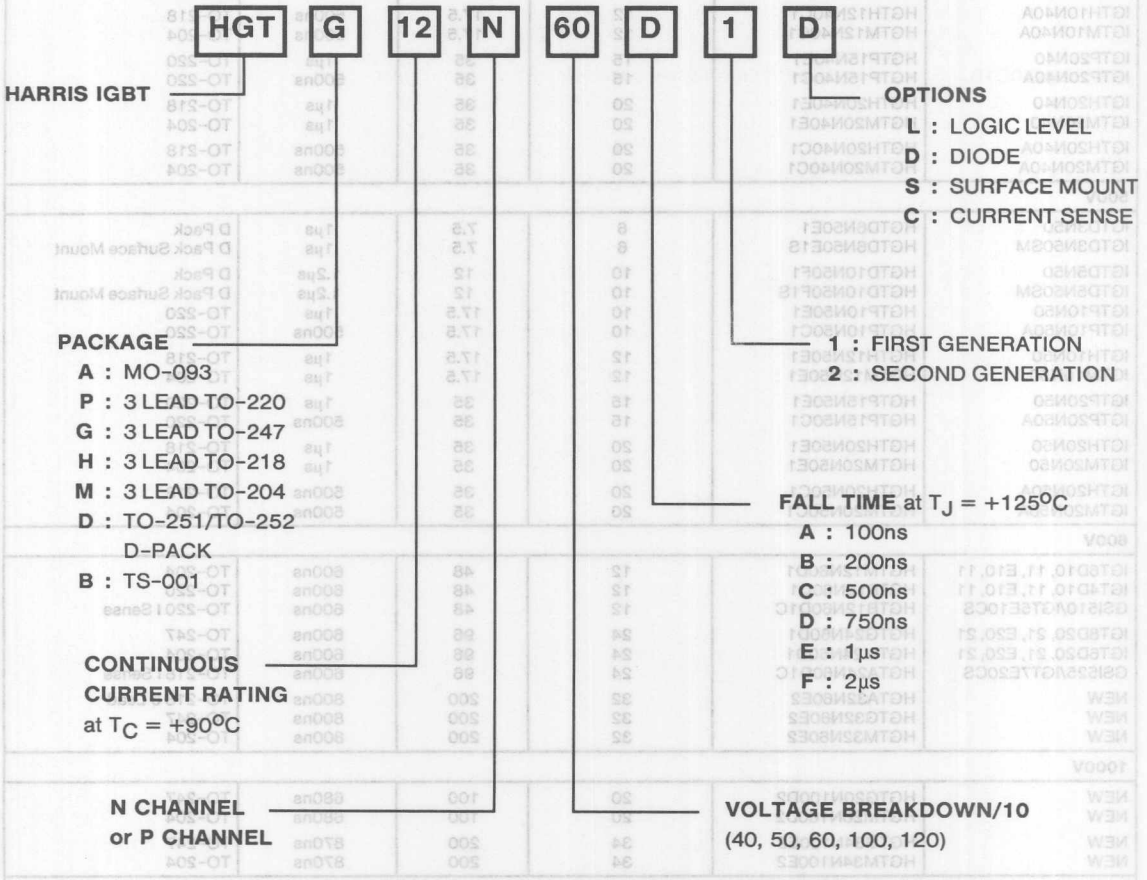
INSULATED-GATE BIPOLAR TRANSISTORS (Continued)

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HGTH20N40C1D, E1D HGTH20N50C1D, E1D	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs) with Anti-Parallel Ultra-Fast Diode	7-60
HGTM20N40C1, E1 HGTM20N50C1, E1	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs)	7-55
HGTG20N50C1D	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT) with Anti-Parallel Ultra-Fast Diode	7-65
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HGTG34N100E2	N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)	7-95

HARRIS

IGBT

PART NUMBERING SYSTEM AND PRODUCT OFFERINGS



HARRIS IGBT PRODUCT OFFERINGS

OLD NUMBER	NEW NUMBER	I CONTINUOUS T_C = +90°C (AMP)	I PEAK (AMP)	T FALL AT T_J = +125°C	PACKAGE
400 VOLTS					
IGTD3N40	HGTD6N40E1	6	7.5	1µs	D Pack
IGTD3N40SM	HGTD6N40E1S	6	7.5	1µs	D Pack Surface Mount
IGTD5N40	HGTD10N40F1	10	12	1.2µs	D Pack
IGTD5N40SM	HGTD10N40F1S	10	12	1.2µs	D Pack Surface Mount
IGTP10N40	HGTP10N40E1	10	17.5	1µs	TO-220
IGTP10N40A	HGTP10N40C1	10	17.5	500ns	TO-220
IGTH10N40	HGTH12N40E1	12	17.5	1µs	TO-218
IGTM10N40	HGTM12N40E1	12	17.5	1µs	TO-204
IGTH10N40A	HGTH12N40C1	12	17.5	500ns	TO-218
IGTM10N40A	HGTM12N40C1	12	17.5	500ns	TO-204
IGTP20N40	HGTP15N40E1	15	35	1µs	TO-220
IGTP20N40A	HGTP15N40C1	15	35	500ns	TO-220
IGTH20N40	HGTH20N40E1	20	35	1µs	TO-218
IGTM20N40	HGTM20N40E1	20	35	1µs	TO-204
IGTH20N40A	HGTH20N40C1	20	35	500ns	TO-218
IGTM20N40A	HGTM20N40C1	20	35	500ns	TO-204
500V					
IGTD3N50	HGTD6N50E1	6	7.5	1µs	D Pack
IGTD3N50SM	HGTD6N50E1S	6	7.5	1µs	D Pack Surface Mount
IGTD5N50	HGTD10N50F1	10	12	1.2µs	D Pack
IGTD5N50SM	HGTD10N50F1S	10	12	1.2µs	D Pack Surface Mount
IGTP10N50	HGTP10N50E1	10	17.5	1µs	TO-220
IGTP10N50A	HGTP10N50C1	10	17.5	500ns	TO-220
IGTH10N50	HGTH12N50E1	12	17.5	1µs	TO-218
IGTM10N50	HGTM12N50E1	12	17.5	1µs	TO-204
IGTP20N50	HGTP15N50E1	15	35	1µs	TO-220
IGTP20N50A	HGTP15N50C1	15	35	500ns	TO-220
IGTH20N50	HGTH20N50E1	20	35	1µs	TO-218
IGTM20N50	HGTM20N50E1	20	35	1µs	TO-204
IGTH20N50A	HGTH20N50C1	20	35	500ns	TO-218
IGTM20N50A	HGTM20N50C1	20	35	500ns	TO-204
600V					
IGT6D10, 11, E10, 11	HGTM12N60D1	12	48	600ns	TO-204
IGT4D10, 11, E10, 11	HGTP12N60D1	12	48	600ns	TO-220
GSI510/IGT5E10CS	HGTB12N60D1C	12	48	600ns	TO-220 I Sense
IGT8D20, 21, E20, 21	HGTG24N60D1	24	96	600ns	TO-247
IGT6D20, 21, E20, 21	HGTM24N60D1	24	96	600ns	TO-204
GSI525/IGT7E20CS	HGTA24N60D1C	24	96	600ns	TO-218 I Sense
NEW	HGTA32N60E2	32	200	800ns	TO-218 5 Lead
NEW	HGTG32N60E2	32	200	800ns	TO-247
NEW	HGTM32N60E2	32	200	800ns	TO-204
1000V					
NEW	HGTG20N100D2	20	100	680ns	TO-247
NEW	HGTM20N100D2	20	100	680ns	TO-204
NEW	HGTG34N100E2	34	200	870ns	TO-247
NEW	HGTM34N100E2	34	200	870ns	TO-204
400V "IGBT PLUS DIODE COMBINATIONS"					
NEW	HGTP6N40E1D	6	7.5	1µs	TO-220 With Diode
NEW	HGTP10N40F1D	10	12	1.2µs	TO-220 With Diode
IGTP10N40D	HGTP10N40E1D	10	17.5	1µs	TO-220 With Diode
IGTP10N40AD	HGTP10N40C1D	10	17.5	500ns	TO-220 With Diode
500V "IGBT PLUS DIODE COMBINATIONS"					
NEW	HGTP6N50E1D	6	7.5	1µs	TO-220 With Diode
NEW	HGTP10N50F1D	10	12	1.2µs	TO-220 With Diode
IGTP10N50D	HGTP10N50E1D	10	17.5	1µs	TO-220 With Diode
IGTP10N50AD	HGTP10N50C1D	10	17.5	500ns	TO-220 With Diode
NEW	HGTG20N50C1D	20	35	500ns	TO-247 With Diode
600V "IGBT PLUS DIODE COMBINATIONS"					
NEW	HGTG12N60D1D	12	48	600ns	TO-247 With Diode
NEW	HGTG24N60D1D	24	96	600ns	TO-247 With Diode

HARRIS 2N6975, 2N6976, 2N6977, 2N6978

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs)

August 1991

Features

- 5A, 400V and 500V
- $V_{CE(ON)}$: 2V
- T_{fi}: 1μs, 0.5μs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance

Applications

- Power Supplies
- Motor Drives
- Protection Circuits

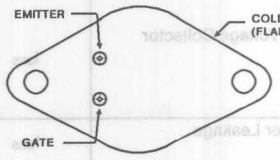
Description

The 2N6975, 2N6976, 2N6977 and the 2N6978 are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high-voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low-power integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

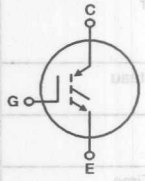
Package

JEDEC TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



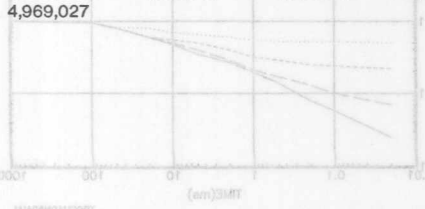
Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified.

		2N6975/2N6977	2N6976/2N6978	UNITS
Collector-Emitter Voltage	V_{CES}	400*	500*	V
Collector-Gate Voltage (R_{GE} = 1MΩ)	V_{CGR}	400*	500*	V
Reverse Collector-Emitter Voltage	$V_{CES(rev.)}$	5*	5*	V
Gate-Emitter Voltage	V_{GE}	±20*	±20*	V
Collector Current Continuous	I_C	5*	5*	A
Collector Current Pulsed	I_{CM}	10*	10*	A
Power Dissipation Total @ T_C = 25°C	P_D	100*	100*	W
Power Dissipation Derating Above T_C = 25°C		0.8*	0.8*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C

* JEDEC registered value.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2297

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			2N6975 2N6977		2N6976 2N6978		
			Min.	Max.	Min.	Max.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1 mA V_{GE} = 0	400*	—	500*	—	V
Gate Threshold Voltage	$V_{GE(th)}$	V_{GE} = V_{CE} I_C = 1 mA	2*	4.5*	2*	4.5*	V
Zero-Gate Voltage Collector Current	I_{CES}	V_{CE} = 400 V V_{CE} = 500 V	— —	250* —	— —	— 250*	μA
		T_C = 125° C V_{CE} = 400 V V_{CE} = 500 V	— — —	— 1000* —	— — —	— — 1000*	
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V V_{CE} = 0	—	100*	—	100*	nA
Reverse Collector-Emitter Leakage Current	I_{ECS}	R_{GE} = 0 Ω V_{EC} = 5 V	—	5*	—	5*	mA
Collector-Emitter On Voltage	$V_{CE(on)}$	I_C = 5 A V_{GE} = 10 V	—	2*	—	2*	V
		I_C = 10 A V_{GE} = 20V	—	2.5	—	2.5	
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 5 A V_{CE} = 10 V	3.4*	6.8*	3.4*	6.8*	V
On-State Gate Charge	$Q_{g(on)}$	I_C = 5 A V_{CE} = 10 V	12*	25*	12*	25*	nC
Turn-On Delay Time	$t_{d(on)}$	I_C = 5 A	50 max				ns
Rise Time	t_r	$V_{CE(CLP)}$ = 300 V	50 max				
Turn-Off Delay Time	$t_{d(off)}$	L = 50 μH	400 max *				
Fall Time	t_{fi}	T_J = 125° C V_{GE} = 10 V R_G = 50 Ω	2N6975 2N6976	1000 max*			
			2N6977 2N6978	500 max *			
Turn-Off Energy Loss per Cycle (off switching dissipation = E_{off} x frequency)	E_{off}	I_C = 5 A $V_{CE(CLP)}$ = 300 V L = 50 μH T_J = 125° C V_{GE} = 10 V R_G = 50 Ω	2N6975 2N6977	1000 max*			μJ
			2N6976 2N6978	500 max*			
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		1.25*				°C/W

*JEDEC registered value.

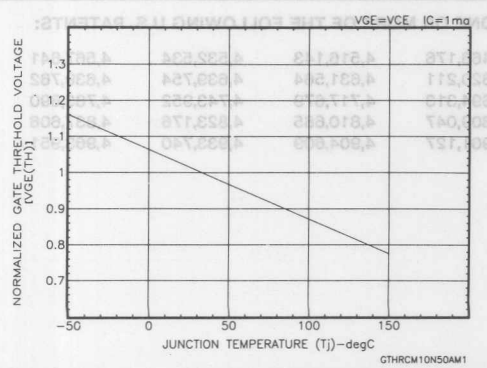


Fig. 1 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

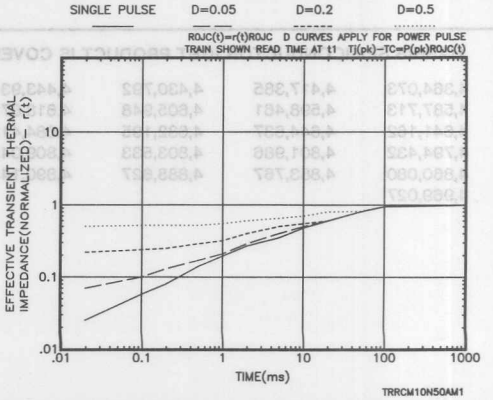


Fig. 2 - Normalized thermal response characteristics for all types.

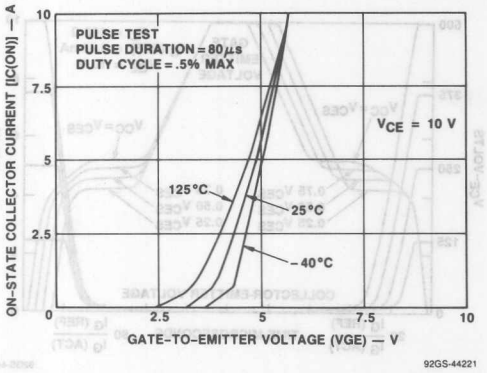


Fig. 3 - Typical transfer characteristics for all types.

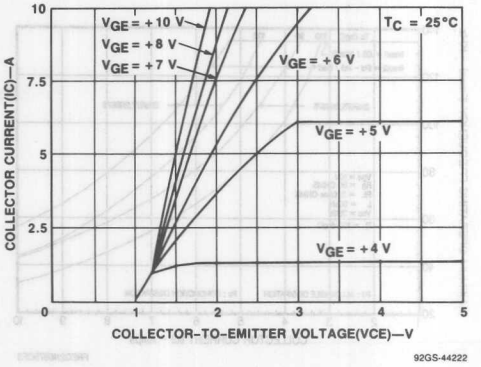


Fig. 4 - Typical saturation characteristics for all types.

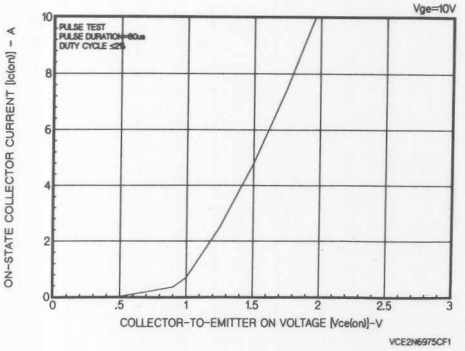


Fig. 5 - Typical collector-to-emitter on-voltage as a function of collector current for all types.

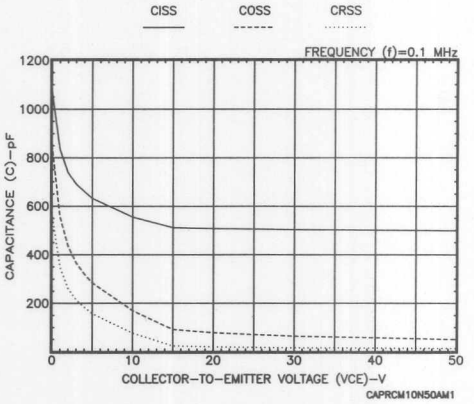


Fig. 6 - Capacitance as a function of collector-to-emitter voltage fo all types.

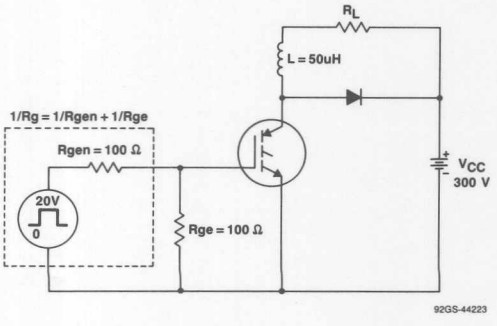


Fig. 7 - Inductive switching test circuit.

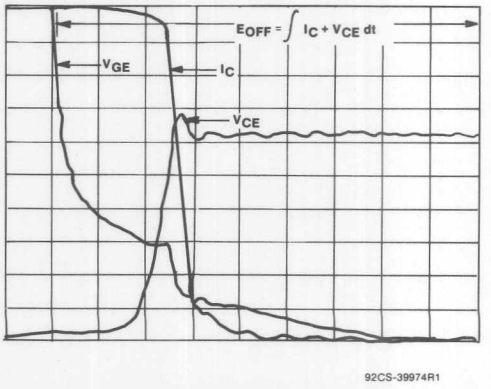


Fig. 8 - Typical inductive switching waveforms.

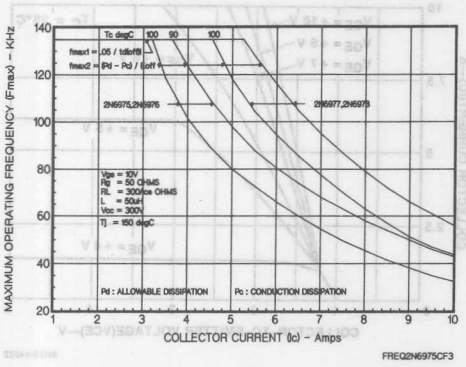


Fig. 9 - Maximum operating frequency vs collector current (typical).

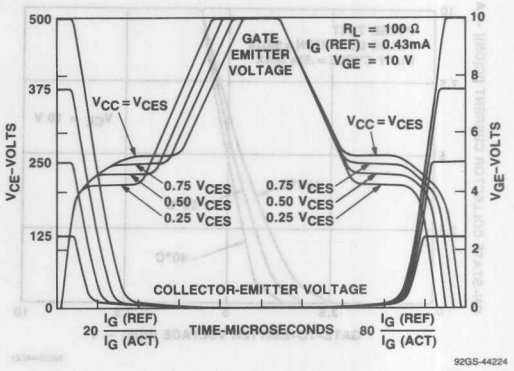


Fig. 10 – Normalized switching waveforms at constant gate current. (Refer to Harris application notes AN-7254 and AN-7260.)

HARRIS HGTD6N40E1/E1S HGTD6N50E1/E1S

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs)

August 1991

Features

- 6 Amp, 400 and 500 Volt
- $V_{CE(ON)}$: 2.5V Max.
- T_{Fall}: 1μs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance

Applications

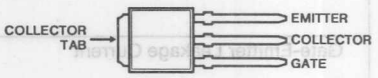
- Power Supplies
- Motor Drives
- Protective Circuits

Description

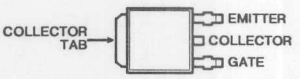
The HGTD6N40E1, HGTD6N40E1S, HGTD6N50E1, and HGTD6N50E1S are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low power integrated circuits. The HGTD6N40E1 and the HGTD6N50E1 are supplied in the JEDEC TO-251AA plastic package. The HGTD6N40E1S and the HGTD6N50E1S are supplied in the JEDEC TO-252AA surface-mount plastic package.

Package

HGTD6N40E1, HGTD6N50E1
TO-251AA
TOP VIEW

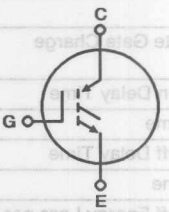


HGTD6N40E1S, HGTD6N50E1S
TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		HGTD6N40E1 HGTD6N40E1S	HGTD6N50E1 HGTD6N50E1S	UNITS
Collector-Emitter Voltage	V_{CES}	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	V_{CGR}	400	500	V
Gate-Emitter Voltage	V_{GE}	±20	±20	V
Collector Current Continuous				
at T_C = 25°C	I_{C25}	7.5	7.5	A
at T_C = 90°C	I_{C90}	6	6	A
Power Dissipation Total @ T_C = 25°C	P_D	60	60	W
Power Dissipation Derating T_C = 25°C		0.48	0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2413.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C = 25° C) Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			HGTD6N40E1 HGTD6N40E1S		HGTD6N50E1 HGTD6N50E1S		
			MIN.	MAX.	MIN.	MAX.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA V_{GE} = 0	400	—	500	—	V
Gate Threshold Voltage	$V_{GE(th)}$	V_{GE} = V_{CE} I_C = 1 mA	2	4.5	2	4.5	V
Zero-Gate Voltage Collector Current	I_{CES}	T_J = 150° C V_{CE} = 400 V V_{CE} = 500 V	— —	250 —	— —	— 250	μA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V V_{CE} = 0	—	100	—	100	nA
Collector-Emitter On-Voltage	$V_{CE(on)}$	I_C = 3 A V_{GE} = 10 V T_j = 150° C	—	2.9	—	2.9	V
		I_C = 3 A V_{GE} = 15 V T_J = 150° C	—	2.5	—	2.5	
		I_C = 3 A V_{GE} = 10 V T_J = 25° C	—	2.5	—	2.5	
		I_C = 3 A V_{GE} = 15 V T_J = 25° C	—	2.4	—	2.4	
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 3 A V_{CE} = 10 V	6.5 (typ)				V
On-State Gate Charge	$Q_{G(on)}$	I_C = 3 A V_{CE} = 10 V	6.9 (typ)				nC
Turn-On Delay Time	$t_{d(on)}$	Resistive Load	90 (typ)				ns
Rise Time	t_r	I_C = 3 A	32 (typ)				
Turn-Off Delay Time	$t_{d(off)}$	R_L = 133 Ω	24 (typ)				
Fall Time	t_{fi}	V_{CE} = 400 V	1100 (typ)				
Turn-Off Energy Loss per Cycle (off switching dissipation = W_{off} x frequency)	W_{off}	T_J = 150° C V_{GE} = 10 V R_g = 25 Ω	0.29 (typ)				mJ
Turn-Off Delay Time	$t_{d(off)}$	Inductive Load	—	190	—	190	ns
Fall Time	t_{fi}	(see Fig. 6)	—	1	—	1	μs
Turn-Off Energy Loss per Cycle (off switching dissipation = W_{off} x frequency)	W_{off}	I_C = 3 A $V_{CE(clp)}$ = 400 V R_L = 133 Ω L = 50 μH T_J = 150° C V_{GE} = 10 V R_g = 25 Ω	—	0.43	—	0.43	mJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	2.08	—	2.08	°C/W

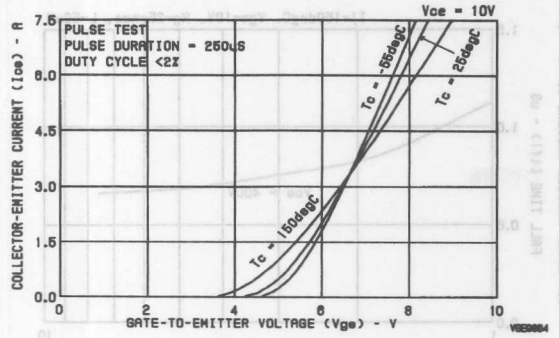


Fig. 1 - Typical transfer characteristics.

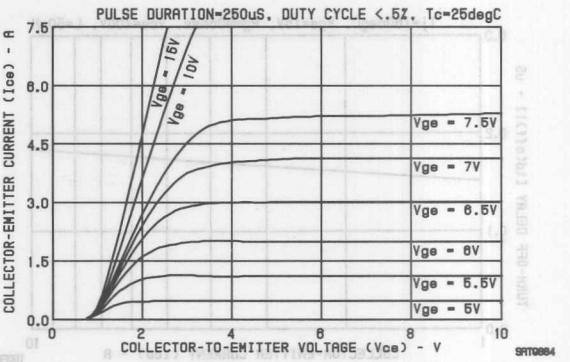


Fig. 2 - Typical saturation characteristics.

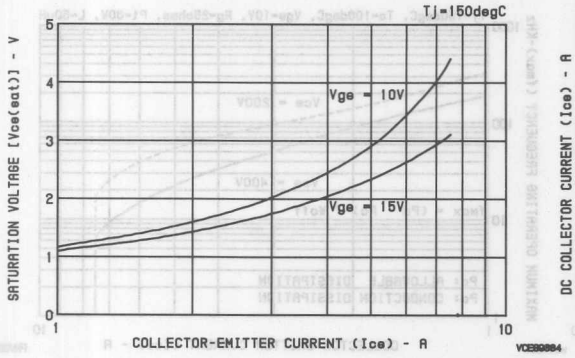


Fig. 3 - Saturation voltage as a function of collector-emitter current. (Typical)

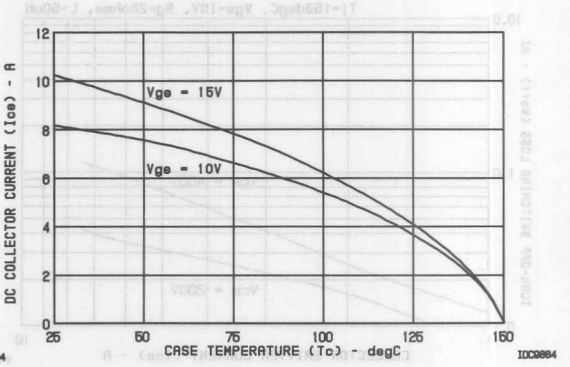


Fig. 4 - DC collector current as a function of case temperature.

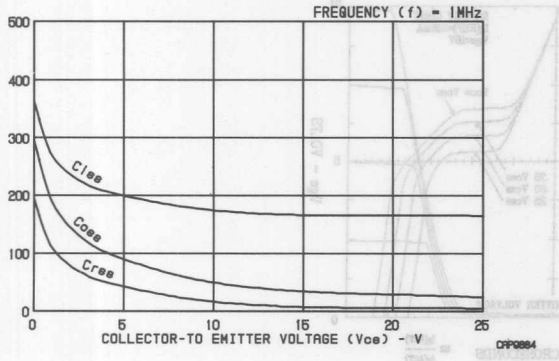


Fig. 5 - Capacitance as a function of collector-to-emitter voltage. (Typical)

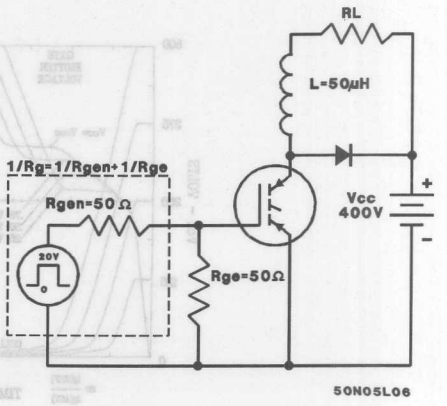


Fig. 6 - Inductive switching test circuit.

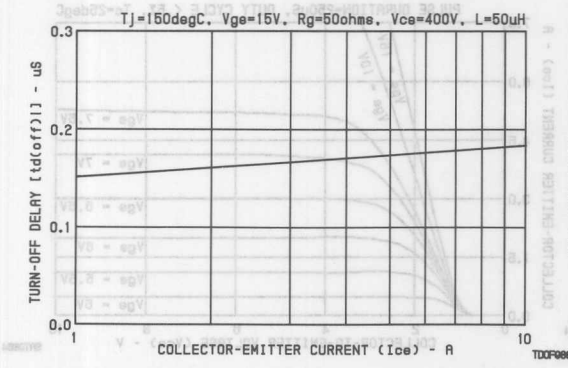


Fig. 7 - Turn-off delay as a function of collector-to-emitter current. (Typical)

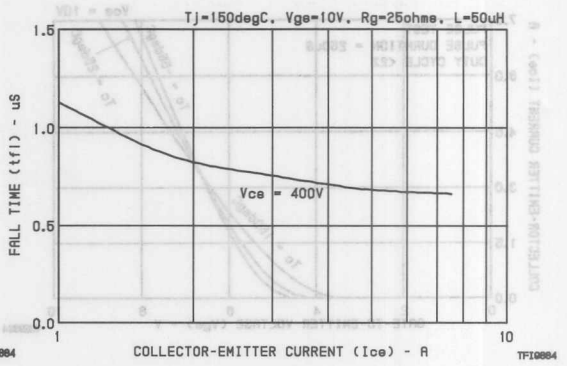


Fig. 8 - Fall time as a function of collector-to-emitter current. (Typical)

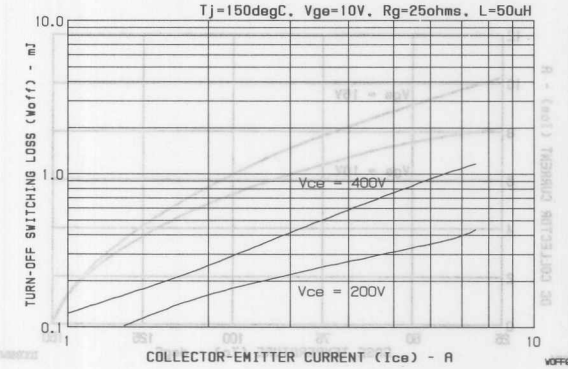


Fig. 9 - Turn-off switching loss as a function of collector-emitter current. (Typical)

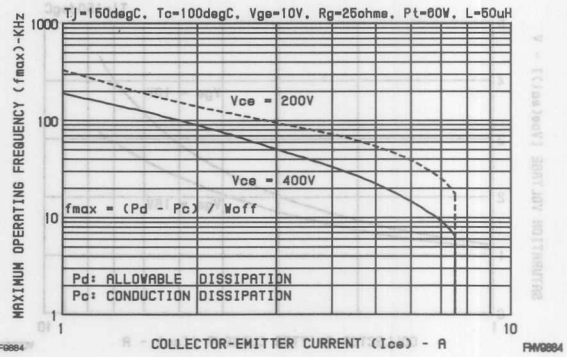


Fig. 10 - Maximum operating frequency as a function of collector current and voltage. (Typical)

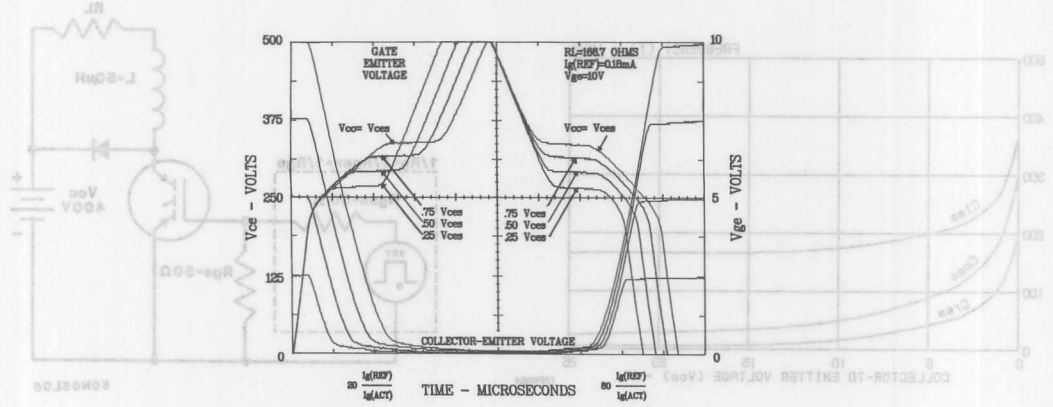


Fig. 11 - Normalized switching waveforms at constant gate current.

HARRIS HGTP6N40E1D HGTP6N50E1D

May 1991

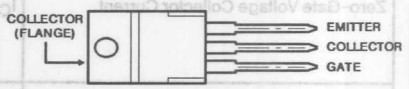
N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs) with Anti-Parallel Ultra-Fast Diode

Features

- 6 Amp, 400 and 500 Volt
- Latch Free Operation
- Typical Fall Time < 1.1μs
- High Input Impedance
- Low Conduction Loss
- With Anti-Parallel Diode
- t_{rr} < 60ns

Package

TO-220AB
TOP VIEW



Description

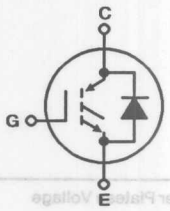
The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C. The diode used in parallel with the IGBT is an ultrafast (t_{rr} < 60ns) with soft recovery characteristic.

The IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

These devices are supplied in the JEDEC TO-220 package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		HGTP6N40E1D	HGTP6N50E1D	UNITS
Collector-Emitter Voltage	BV_{CES}	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	400	500	V
Collector Current Continuous				
at T_C = 25°C	I_{C25}	7.5	7.5	A
at T_C = 90°C	I_{C90}	6	6	A
Collector Current Pulsed (Note 1)	I_{CM}	7.5	7.5	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	±20	V
Diode Forward Current				
at T_C = 25°C	I_{f25}	10	10	A
at T_C = 90°C	I_{f90}	6	6	A
Power Dissipation Total @ T_C = 25°C	P_D	75	75	W
Power Dissipation Derating T_C > 25°C		0.6	0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	260	°C

Note 1. T_J = 150°C, Min. R_{GE} = 25Ω w/o latch

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2795

Electrical Characteristics At Case Temperature (T_C = 25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS HGTP6N40E1D MIN.	LIMITS HGTP6N40E1D MAX.	LIMITS HGTP6N50E1D MIN.	LIMITS HGTP6N50E1D MAX.	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1.25mA, V_{GE} = 0	400	–	500	–	V
Gate Threshold Voltage	$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 1mA	2	4.5	2	4.5	V
Zero-Gate Voltage Collector Current	I_{CES}	T_J = 150°C, V_{CE} = 400V	–	1.25	–	–	mA
		T_J = 150°C, V_{CE} = 500V	–	–	–	1.25	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V, V_{CE} = 0	–	100	–	100	nA
Collector-Emitter On-Voltage	$V_{CE(on)}$	I_C = 3A, V_{GE} = 10V, T_J = 150°C	–	2.9	–	2.9	V
		I_C = 3A, V_{GE} = 15V, T_J = 150°C	–	2.5	–	2.5	V
		I_C = 3A, V_{GE} = 10V, T_J = 25°C	–	2.5	–	2.5	V
		I_C = 3A, V_{GE} = 15V, T_J = 25°C	–	2.4	–	2.4	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 3A, V_{CE} = 10V	6.5 (typ.)				V
On-State Gate Charge	$Q_{G(on)}$	I_C = 3A, V_{CE} = 10V	6.9 (typ)				nC
Turn-On Delay Time	$t_{d(on)}$	Resistive Load, I_C = 3A, R_L = 133Ω, V_{CE} = 400V, T_J = 150°C, V_{GE} = 10V, R_g = 25Ω	90 (typ)				ns
Rise Time	t_r		32 (typ)				ns
Turn-Off Delay Time	$t_{d(off)}$		24 (typ)				ns
Fall Time	t_f		1100 (typ)				ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{off} x frequency)	W_{off}		0.29 (typ)				mJ
Turn-Off Delay Time	$t_{d(off)i}$	Inductive Load (See Figure 6), I_C = 3A, R_L = 133Ω, L = 50μH, R_g = 25Ω, $V_{CE(clp)}$ = 400V, T_J = 150°C, V_{GE} = 10V	–	190	–	190	ns
Fall Time	t_{fi}		–	1	–	1	μs
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{off} x frequency)	W_{off}		–	0.43	–	0.43	mJ
Thermal Resistance Junction-to-Case (IGBT)	$R_{\theta JC}$		–	2.08	–	2.08	°C/W
Thermal Resistance of Diode	$R_{\theta JC}$		–	2	–	2	°C/W
Diode Forward Voltage	V_{EC}	I_{EC} = 6A	–	1.6	–	1.6	V
Diode Reverse Recovery Time	T_{rr}	I_{EC} = 6A, di/dt = 100A/μs	–	60	–	60	ns

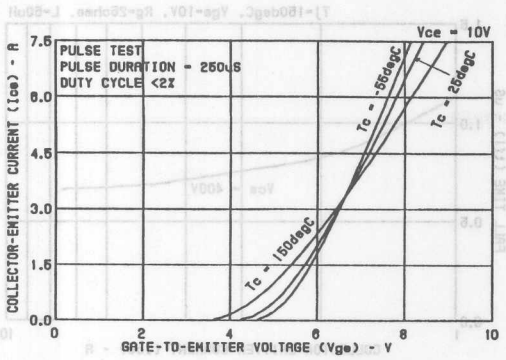


FIGURE 1. TYPICAL TRANSFER CHARACTERISTICS

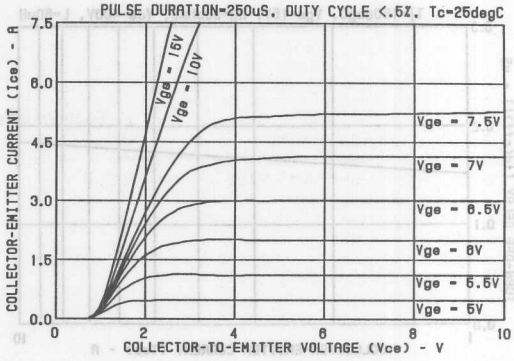


FIGURE 2. TYPICAL SATURATION CHARACTERISTICS

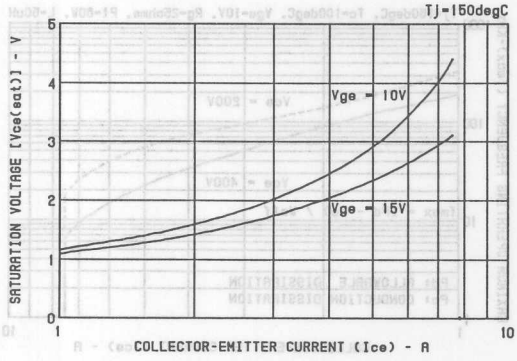


FIGURE 3. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT (TYPICAL)

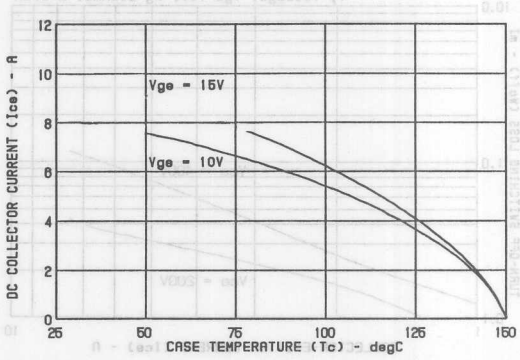


FIGURE 4. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

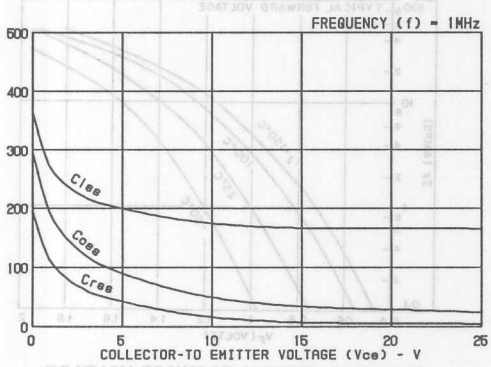


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-TO-EMITTER VOLTAGE (TYPICAL)

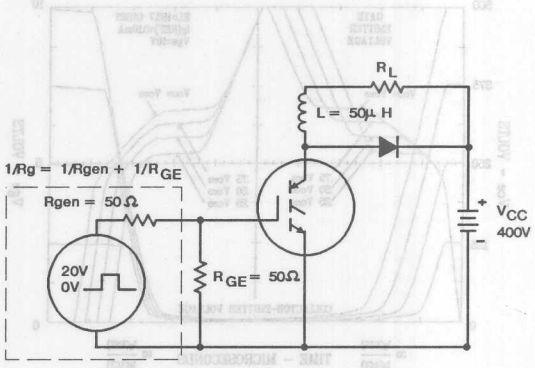


FIGURE 6. INDUCTIVE SWITCHING TEST CIRCUIT

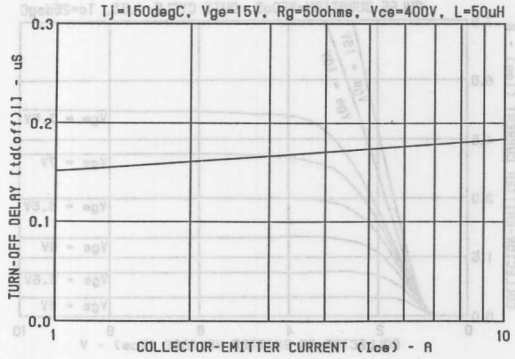


FIGURE 7. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

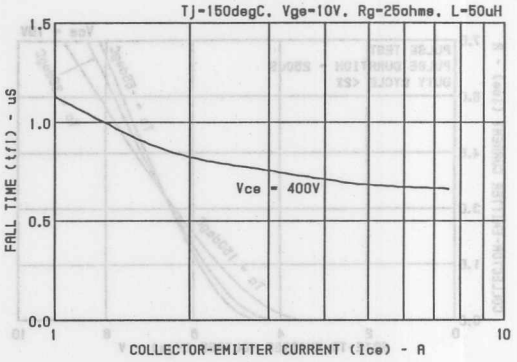


FIGURE 8. FALL TIME AS A FUNCTION OF COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

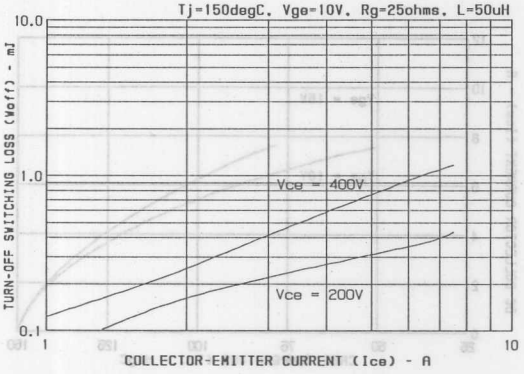


FIGURE 9. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT (TYPICAL)

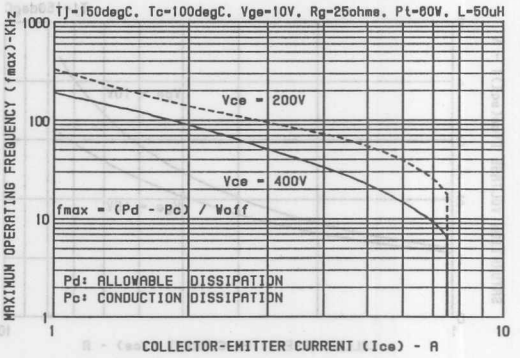


FIGURE 10. MAXIMUM OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR CURRENT AND VOLTAGE (TYPICAL)

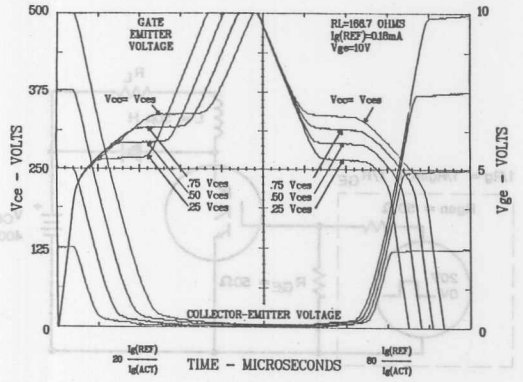


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT

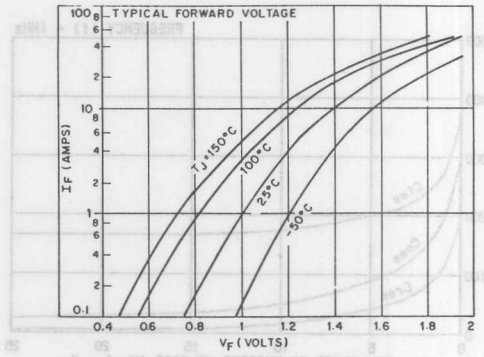


FIGURE 12. TYPICAL FORWARD VOLTAGE

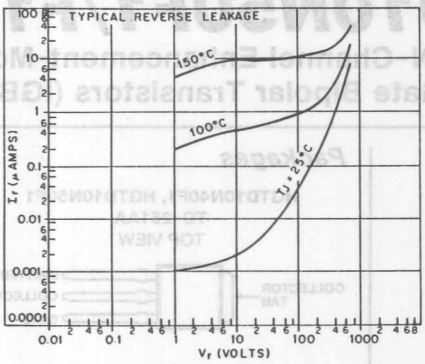


FIGURE 13. TYPICAL REVERSE LEAKAGE

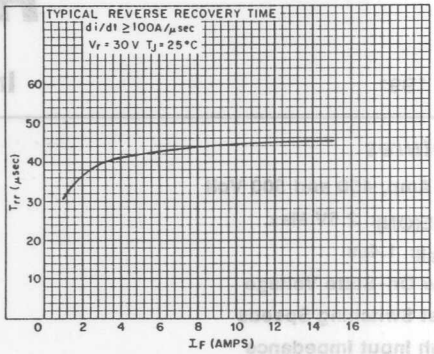


FIGURE 14. TYPICAL REVERSE RECOVERY TIME

HARRIS HGTD10N40F1/F1S HGTD10N50F1/F1S

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs)

August 1991

Features

- 10 Amp, 400 and 500 Volt
- $V_{CE(ON)}$: 2.5V Max.
- T_{Fall}: 1.4μs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance

Applications

- Power Supplies
- Motor Drives
- Protective Circuits

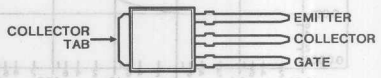
Description

The HGTD10N40F1, HGTD10N40F1S, HGTD10N50F1, and HGTD10N50F1S are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low power integrated circuits.

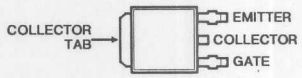
The HGTD10N40F1 and the HGTD10N50F1 are supplied in the JEDEC TO-251AA plastic package. The HGTD10N40F1S and the HGTD10N50F1S are supplied in the JEDEC TO-252AA surface-mount plastic package.

Packages

HGTD10N40F1, HGTD10N50F1
TO-251AA
TOP VIEW

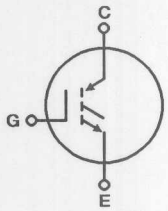


HGTD10N40F1S, HGTD10N50F1S
TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		HGTD10N40F1 HGTD10N40F1S	HGTD10N50F1 HGTD10N50F1S	UNITS
Collector-Emitter Voltage	V_{CES}	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	V_{CGR}	400	500	V
Gate-Emitter Voltage	V_{GE}	±20	±20	V
Collector Current Continuous				
at T_C = 25°C	I_{C25}	12	12	A
at T_C = 90°C	I_{C90}	10	10	A
Power Dissipation Total @ T_C = 25°C	P_D	75	75	W
Power Dissipation Derating T_C = 25°C		0.6	0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2425.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C = 25°C) Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			HGTD10N40F1 HGTD10N40F1S		HGTD10N50F1 HGTD10N50F1S		
			MIN.	MAX.	MIN.	MAX.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA V_{GE} = 0	400	—	500	—	V
Gate Threshold Voltage	$V_{GE(th)}$	V_{GE} = V_{CE} I_C = 1 mA	2	4.5	2	4.5	V
Zero-Gate Voltage Collector Current	I_{CES}	T_J = 150°C V_{CE} = 400 V V_{CE} = 500 V	— —	250 —	— —	— 250	μA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V V_{CE} = 0	—	100	—	100	nA
Collector-Emitter On-Voltage	$V_{CE(on)}$	I_C = 5 A V_{GE} = 10 V T_j = 150°C	—	2.5	—	2.5	V
		I_C = 5 A V_{GE} = 15 V T_J = 150°C	—	2.2	—	2.2	
		I_C = 5 A V_{GE} = 10 V T_J = 25°C	—	2.5	—	2.5	
		I_C = 5 A V_{GE} = 15 V T_J = 25°C	—	2.2	—	2.2	
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 5 A V_{CE} = 10 V	5.3 (typ)				V
On-State Gate Charge	$Q_{G(on)}$	I_C = 5 A V_{CE} = 10 V	13.4 (typ)				nC
Turn-On Delay Time	$t_{d(on)}$	Resistive Load	45 (typ)				ns
Rise Time	t_r	I_C = 5 A	35 (typ)				
Turn-Off Delay Time	$t_{d(off)}$	R_L = 80 Ω	130 (typ)				
Fall Time	t_{fi}	V_{CE} = 400 V	1400 (typ)				
Turn-Off Energy Loss per Cycle (off switching dissipation = W_{off} x frequency)	W_{off}	T_J = 150° C V_{GE} = 10 V R_g = 25 Ω	0.64 (typ)				mJ
Turn-Off Delay Time	$t_{d(off)}$	Inductive Load	—	375	—	375	ns
Fall Time	t_{fi}	(see Fig. 6)	—	1200	—	1200	
Turn-Off Energy Loss per Cycle (off switching dissipation = W_{off} x frequency)	W_{off}	I_C = 5 A $V_{CE(clp)}$ = 400 V R_L = 80 Ω L = 50 μH T_J = 150°C V_{GE} = 10 V R_g = 25 Ω	—	1.2	—	1.2	mJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	1.67	—	1.67	°C/W

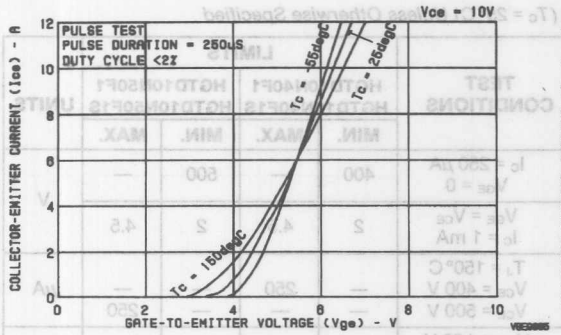


Fig. 1 - Typical transfer characteristics.

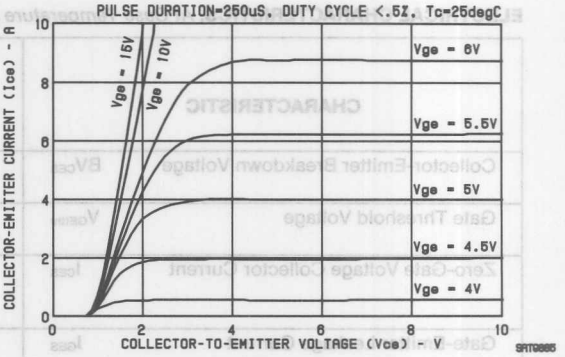


Fig. 2 - Typical saturation characteristics.

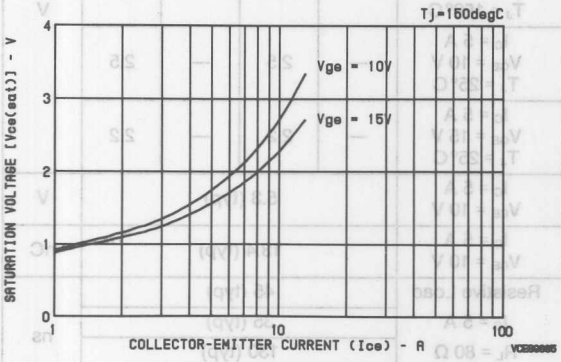


Fig. 3 - Saturation voltage as a function of collector-emitter current. (Typical)

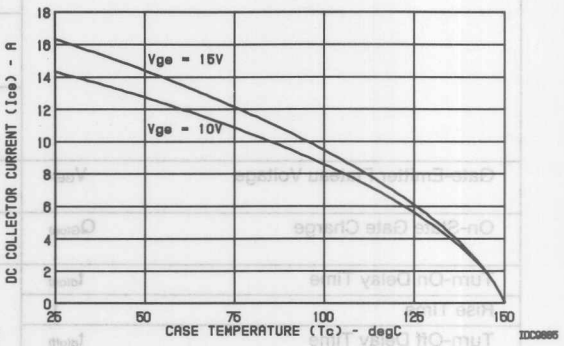


Fig. 4 - DC collector current as a function of case temperature.

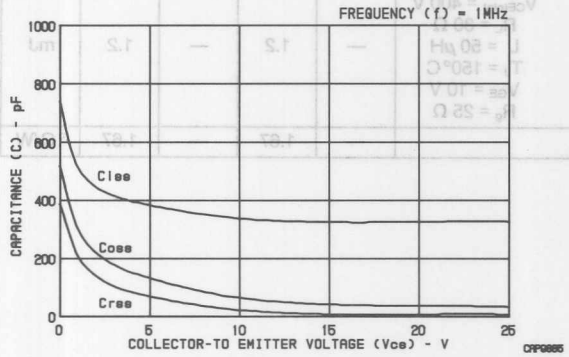


Fig. 5 - Capacitance as a function of collector-to-emitter voltage. (Typical)

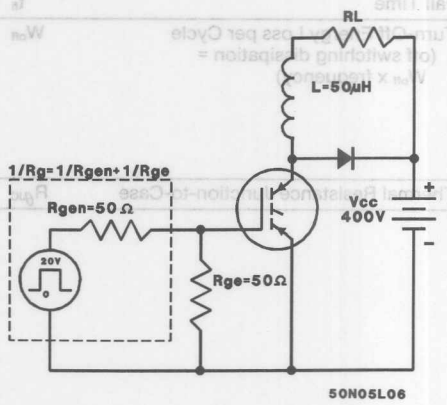


Fig. 6 - Inductive switching test circuit.

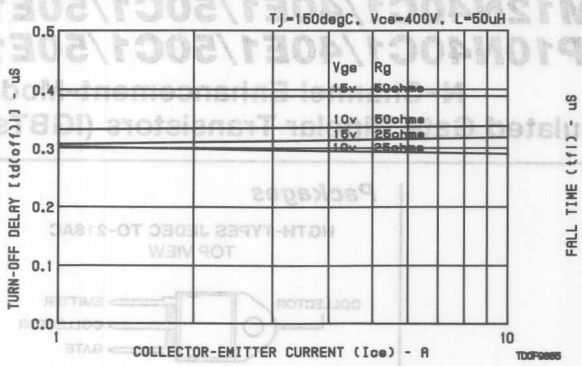


Fig. 7 - Turn-off delay as a function of collector-to-emitter current. (Typical)

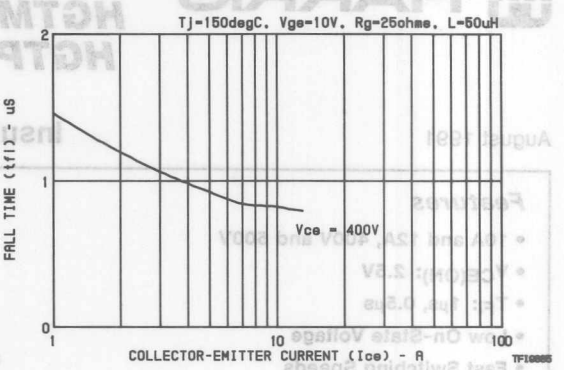


Fig. 8 - Fall time as a function of collector-to-emitter current. (Typical)

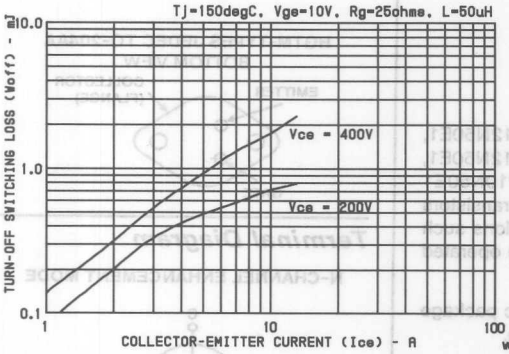


Fig. 9 - Turn-off switching loss as a function of collector-emitter current. (Typical)

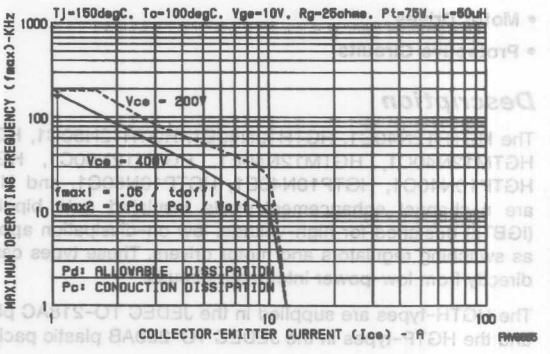


Fig. 10 - Maximum operating frequency as a function of collector current and voltage. (Typical)

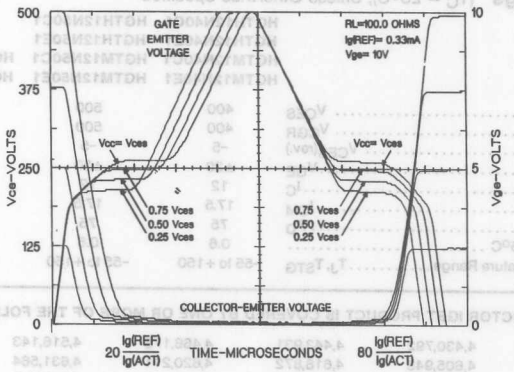


Fig. 11 - Normalized switching waveforms at constant gate current.

HGTH12N40C1/40E1/50C1/50E1
HGTM12N40C1/40E1/50C1/50E1
HGTP10N40C1/40E1/50C1/50E1

N-Channel Enhancement-Mode
Insulated Gate Bipolar Transistors (IGBTs)

August 1991

Features

- 10A and 12A, 400V and 500V
- $V_{CE(ON)}$: 2.5V
- T_{Fi}: 1μs, 0.5μs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance
- No Anti-Parallel Diode

Applications

- Power Supplies
- Motor Drives
- Protective Circuits

Description

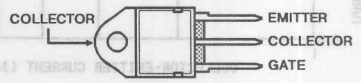
The HGTH12N40C1, HGTH12N40E1, HGTH12N50C1, HGTH12N50E1, HGTM12N40C1, HGTM12N40E1, HGTM12N50C1, HGTM12N50E1, HGTP10N40C1, HGTP10N40E1, HGTP10N50C1, and HGTP10N50E1 are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high-voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low-power integrated circuits.

The HGTH-types are supplied in the JEDEC TO-218AC plastic package and the HGTP-types in the JEDEC TO-220AB plastic package.

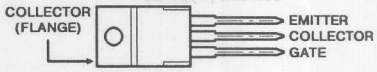
The HGTM-types are supplied in the JEDEC TO-204AA steel package.

Packages

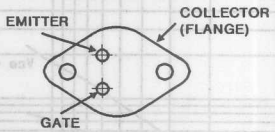
HGTH-TYPES JEDEC TO-218AC
TOP VIEW



HGTP-TYPES JEDEC TO-220AB
TOP VIEW

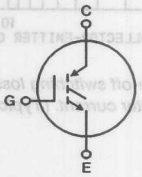


HGTM-TYPES JEDEC TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		HGTH12N40C1 HGTH12N40E1 HGTM12N40C1 HGTM12N40E1	HGTH12N50C1 HGTH12N50E1 HGTM12N50C1 HGTM12N50E1	HGTP10N40C1 HGTP10N40E1	HGTP10N50C1 HGTP10N50E1	UNITS
Collector-Emitter Voltage	V_{CES}	400	500	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	V_{CGR}	400	500	400	500	V
Reverse Collector-Emitter Voltage	$V_{CES(rev.)}$	-5	-5	-5	-5	V
Gate-Emitter Voltage	V_{GE}	±20	±20	±20	±20	V
Collector Current Continuous	I_C	12	12	10	10	A
Collector Current Pulsed	I_{CM}	17.5	17.5	17.5	17.5	A
Power Dissipation @ T_C = 25°C	P_D	75	75	60	60	W
Power Dissipation Derate Above T_C = 25°C		0.6	0.6	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

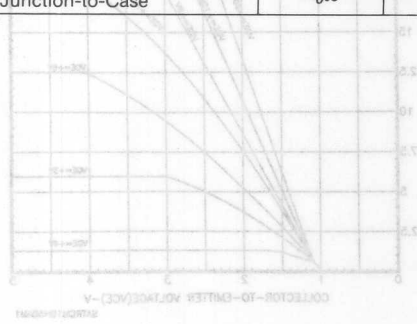
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

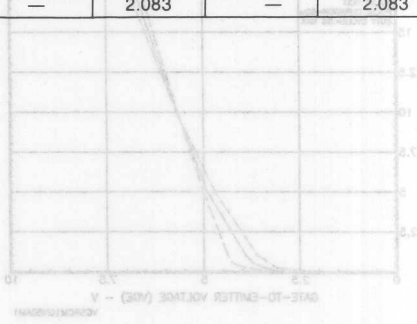
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File Number **1697.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C = 25° C) unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			HGTH12N40C1 HGTH12N40E1 HGTM12N40C1 HGTM12N40E1 HGTP10N40C1 HGTP10N40E1		HGTH12N50C1 HGTH12N50E1 HGTM12N50C1 HGTH12N50E1 HGTP10N50C1 HGTP10N50E1		
			Min.	Max.	Min.	Max.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1 mA V_{GE} = 0	400	—	500	—	V
Gate Threshold Voltage	$V_{GE}(th)$	V_{GE} = V_{CE} I_C = 1 mA	2	4.5 3 (typ.)	2	4.5 3 (typ.)	V
Zero-Gate Voltage Collector Current	I_{CES}	V_{CE} = 400 V V_{CE} = 500 V	— —	250 —	— —	— 250	μA
		T_C = 125° C V_{CE} = 400 V V_{CE} = 500 V	— — —	— 1000 —	— — —	— — 1000	
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V V_{CE} = 0	—	100	—	100	nA
Collector-Emitter On Voltage	$V_{CE}(on)$	I_D = 10 A V_{GE} = 10 V	—	2.5	—	2.5	V
		I_C = 17.5 A V_{GE} = 20 V	—	3.2	—	3.2	
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 5 A V_{CE} = 10 V	—	6 (typ.)	—	6 (typ.)	V
On-State Gate Charge	$Q_g(on)$	I_C = 5 A V_{CE} = 10 V	—	19 (typ.)	—	19 (typ.)	nC
Turn-On Delay Time	$t_d(on)$	I_C = 10 A $V_{CE(CLP)}$ = 300 V L = 50 μH T_J = 100° C V_{GE} = 10 V R_g = 50 Ω	—	50	—	50	ns
Rise Time	t_r		—	50	—	50	
Turn-Off Delay Time	$t_d(off)$		—	400	—	400	
Fall Time	t_{fi} 40E1 50E1		Typ. 680	1000	Typ. 680	1000	
	40C1 50C1		400	500	400	500	
Turn-Off Energy Loss per Cycle (off switching dissipation = E_{off} x frequency)	E_{off} 40E1 50E1	I_C = 10 A $V_{CE(CLP)}$ = 300 V L = 50 μH T_J = 100° C V_{GE} = 10 V R_g = 50 Ω	680 (typ.)				μJ
	40C1 50C1		400 (typ.)				
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	HGTH/HGTM	—	1.67	—	1.67	°C/W
		HGTP	—	2.083	—	2.083	





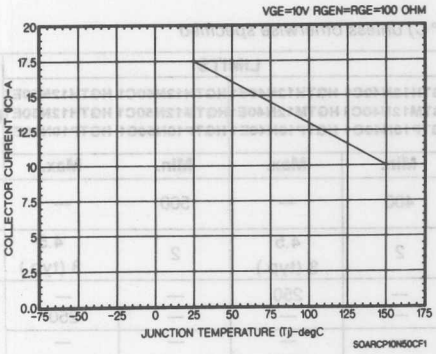


Fig. 1 - Maximum switching current level for all types. $R_g = 50\ \Omega$, $V_{GE} = 0$ V are the minimum allowable values.

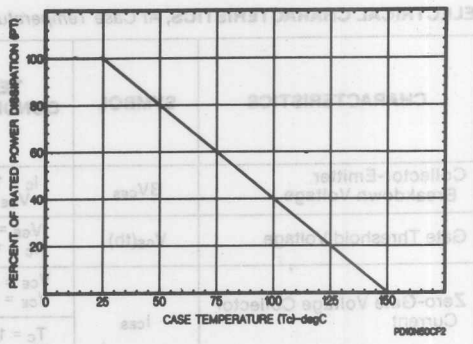


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

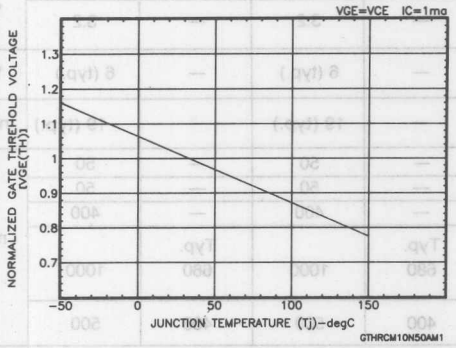


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

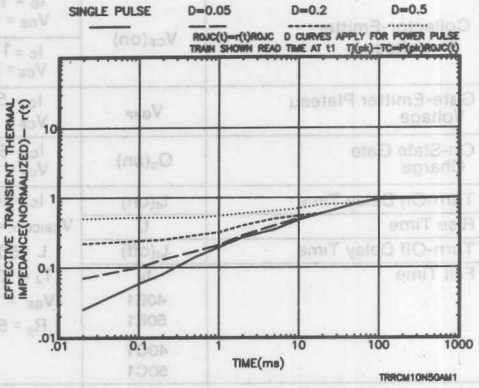


Fig. 4 - Normalized thermal response characteristics for all types.

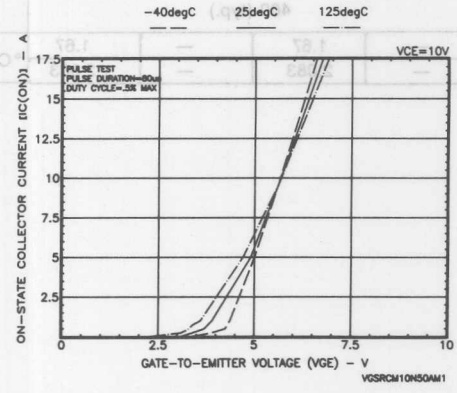


Fig. 5 - Typical transfer characteristics for all types.

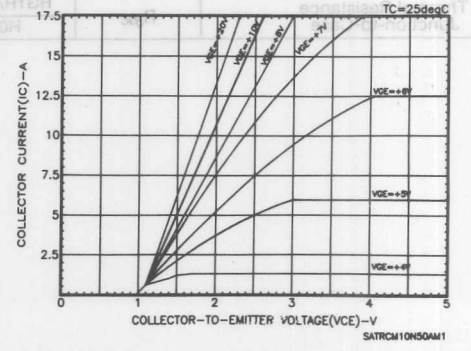


Fig. 6 - Typical saturation characteristics for all types.

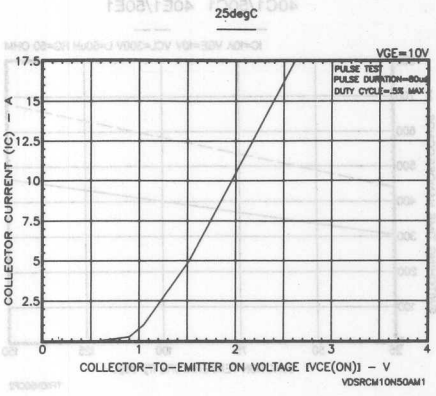


Fig. 7 - Typical collector-to-emitter on-voltage as a function of collector current for all types.

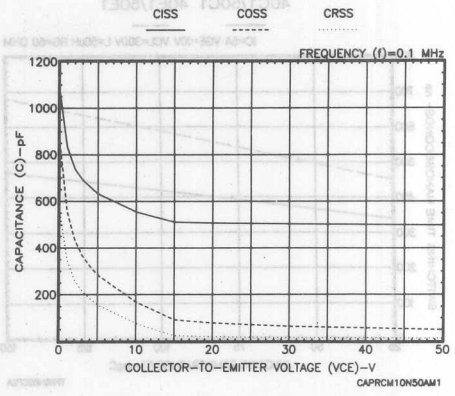


Fig. 8 - Capacitance as a function of collector-to-emitter voltage for all types.

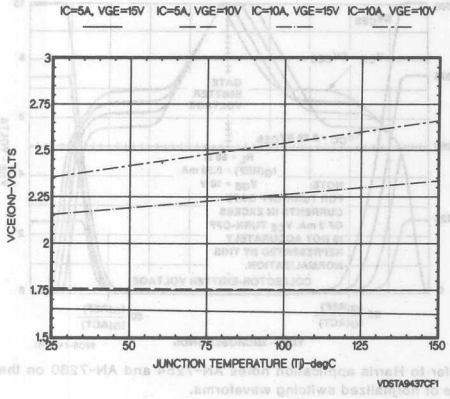


Fig. 9 - Typical $V_{CE}(on)$ vs. temperature for all types.

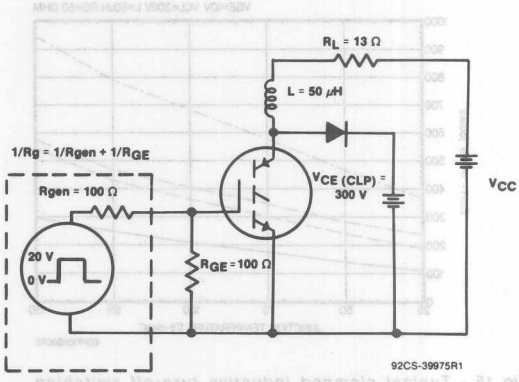


Fig. 10 - Inductive switching test circuit.

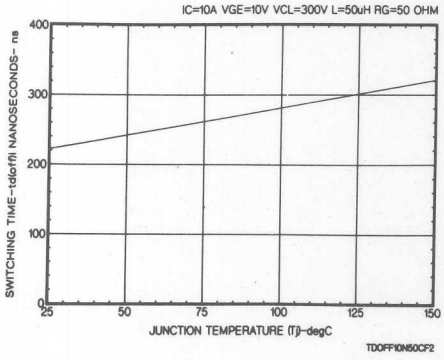


Fig. 11 - Typical turn-off delay time for all types.

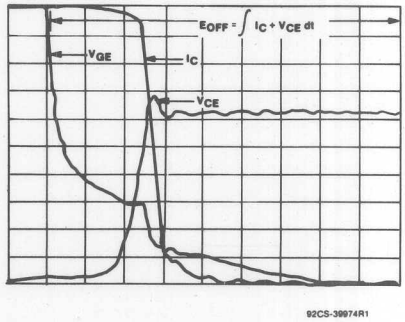


Fig. 12 - Typical inductive switching waveforms.

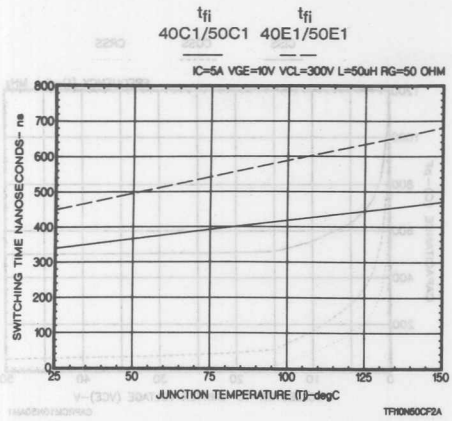


Fig. 13 - Typical fall time for all types ($I_C = 5$ A).

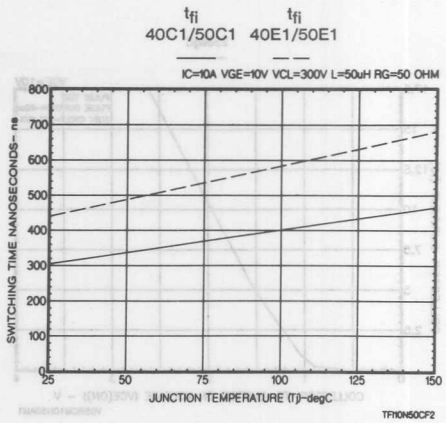


Fig. 14 - Typical fall time for all types ($I_C = 10$ A).

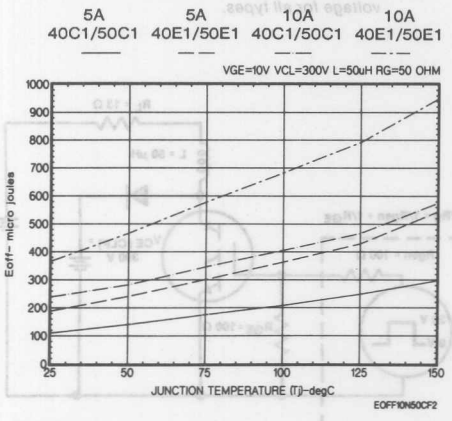
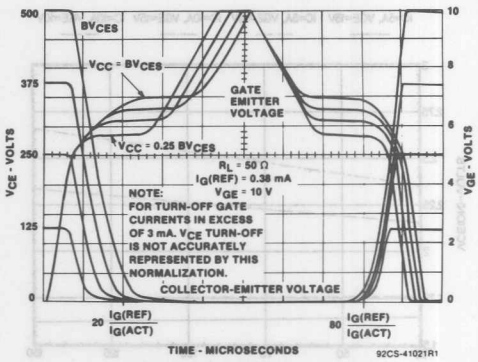


Fig. 15 - Typical clamped inductive turn-off switching loss/cycle.



Refer to Harris application notes AN-7254 and AN-7260 on the use of normalized switcing waveforms.

Fig. 16 - Normalized switching waveforms at constant gate current.

HGTP10N40C1D, E1D
HGTP10N50C1D, E1D

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs) with Anti-Parallel Ultra-Fast Diode

May 1992

Features

- 10 Amp, 400 and 500 Volt
- $V_{CE(ON)}$: 2.5V Max.
- T_{Fall}: 1μs, 0.5μs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance
- Anti-Parallel Diode

Applications

- Power Supplies
- Motor Drives
- Protective Circuits

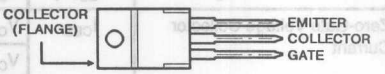
Description

The HGTP10N40C1D, HGTP10N40E1D, HGTP10N50C1D, and HGTP10N50E1D are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. They feature a discrete anti-parallel diode that shunts current around the IGBT in the reverse direction without introducing carriers into the depletion region. These types can be operated directly from low power integrated circuits.

They are supplied in the JEDEC TO-220AB plastic package.

Package

JEDEC TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		HGTP10N40C1D HGTP10N40E1D	HGTP10N50C1D HGTP10N50E1D	UNITS
Collector-Emitter Voltage	V_{CES}	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	V_{CGR}	400	500	V
Gate-Emitter Voltage	V_{GE}	±20	±20	V
Collector Current Continuous				
at T_C = 25°C	I_{C25}	17.5	17.5	A
at T_C = 90°C	I_{C90}	10	10	A
Power Dissipation Total @ T_C = 25°C	P_D	75	75	W
Power Dissipation Derating T_C = 25°C		0.6	0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2405.2

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25°C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS HGTP10N40C1D HGTP10N40E1D MIN	LIMITS HGTP10N40C1D HGTP10N40E1D MAX	LIMITS HGTP10N50C1D HGTP10N50E1D MIN	LIMITS HGTP10N50C1D HGTP10N50E1D MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1mA, V_{GE} = 0		400	-	500	-	V
Gate Threshold Voltage	$V_{GE}(th)$	V_{GE} = V_{CE}, I_C = 1mA		2	4.5	2	4.5	V
Zero-Gate Voltage Collector Current	I_{CES}	V_{CE} = 400V		-	250	-	-	µA
		V_{CE} = 500V		-	-	-	250	µA
		T_C = +125°C	V_{CE} = 400V	-	1000	-	-	µA
			V_{CE} = 500V	-	-	-	1000	µA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V, V_{CE} = 0		-	100	-	100	nA
Collector-Emitter On-Voltage	$V_{CE}(on)$	I_C = 10A, V_{GE} = 10V		-	2.5	-	2.5	V
		I_C = 17.5A, V_{GE} = 20V		-	3.2	-	3.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 5A, V_{CE} = 10V		-	6 (typ)	-	6 (typ)	V
On-State Gate Charge	$Q_G(on)$	I_C = 5A, V_{CE} = 10V		-	19 (typ)	-	19 (typ)	nC
Turn-On Delay Time	$t_d(on)$	I_C = 10A, $V_{CE}(clp)$ = 300V, L = 50µH, T_J = 100°C, V_{GE} = 10V, R_G = 50Ω		-	50	-	50	ns
Rise Time	t_r			-	50	-	50	ns
Turn-Off Delay Time	$t_d(off)$			-	400	-	400	ns
Fall Time	t_{fi}		HGTP10N40E1D, HGTP10N50E1D	680 (typ)	1000	680 (typ)	1000	ns
			HGTP10N40C1D, HGTP10N50C1D	400 (typ)	500	400 (typ)	500	ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = E_{off} x Frequency)	E_{off}	I_C = 10A, $V_{CE}(clp)$ = 300V, L = 50µH, T_J = 100°C, V_{GE} = 10V, R_G = 50Ω	HGTP10N40E1D, HGTP10N50E1D	1810 (typ)				µJ
			HGTP10N40C1D, HGTP10N50C1D	1070 (typ)				µJ
Thermal Resistance	$R_{\theta JC}$			-	1.67	-	1.67	°C/W
Diode Forward Voltage	V_{EC}	I_{EC} = 10A		-	2	-	2	V
Diode Reverse Recovery Time	T_{rr}	I_{EC} = 10A, di/dt = 100A/µs		-	100	-	100	ns

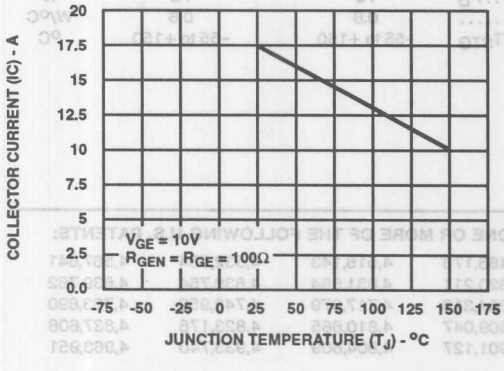


Fig. 1 - Maximum switching current level for all types. Minimum allowable values are R_g = 50Ω, V_{GE} = 0V

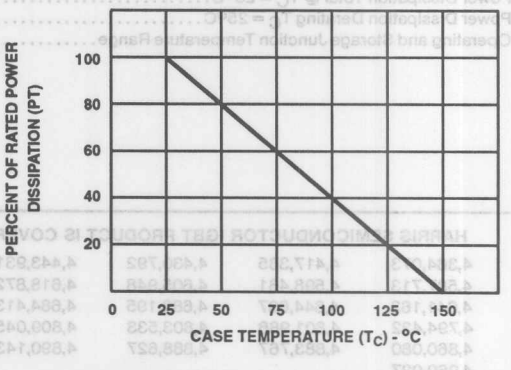


Fig. 2 - Power dissipation vs. temperature derating curve for all types

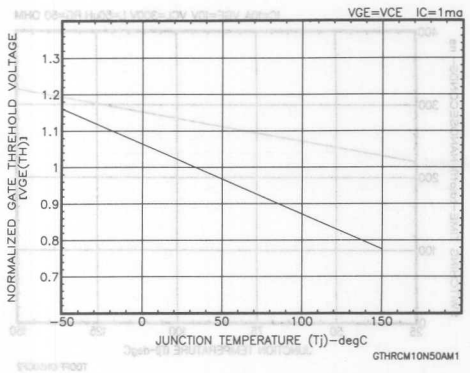


Fig. 3 - Typical normalized gate-threshold voltage as a function of junction temperature for all types.

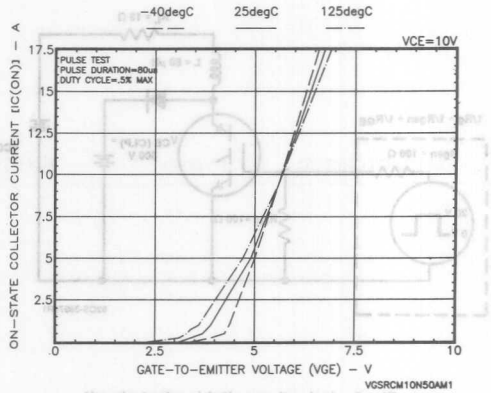


Fig. 4 - Typical transfer characteristics for all types.

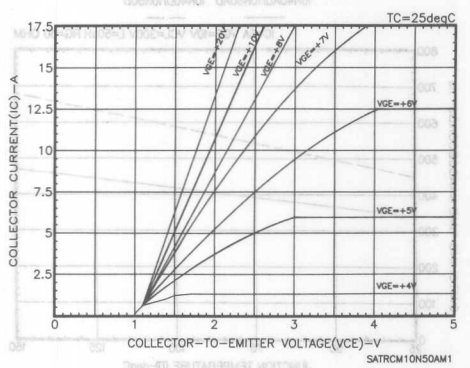


Fig. 5 - Typical saturation characteristics for all types.

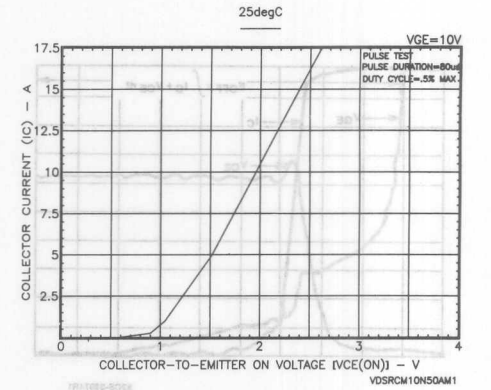


Fig. 6 - Typical collector-to-emitter on-voltage as a function of collector current for all types.

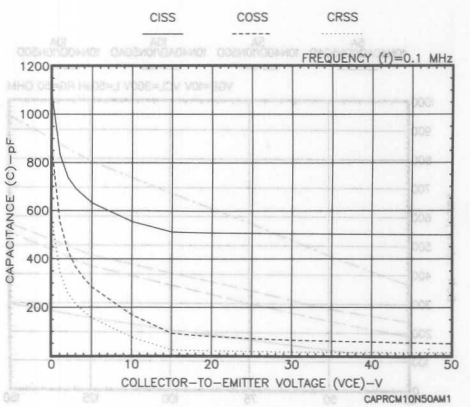


Fig. 7 - Capacitance as a function of collector-to-emitter voltage for all types.

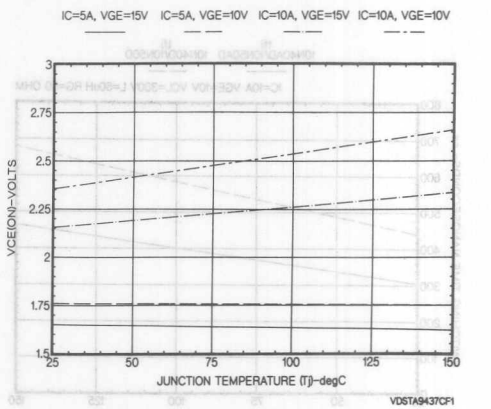


Fig. 8 - Typical $V_{CE}(on)$ vs. temperature for all types.

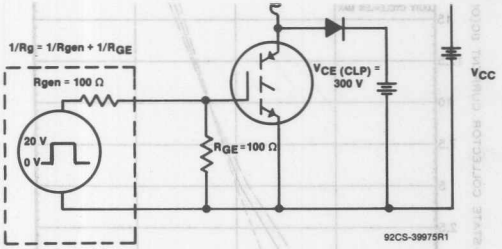


Fig. 9 - Inductive switching test circuit.

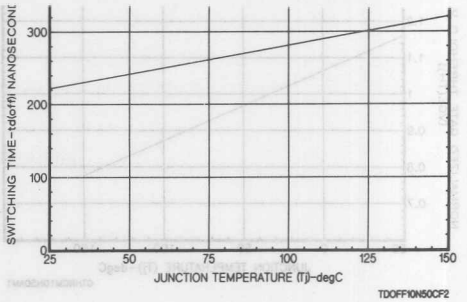


Fig. 10 - Typical turn-off delay time for all types.

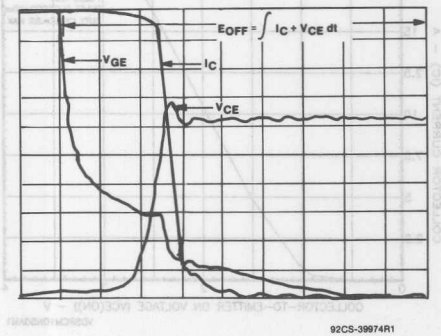


Fig. 11 - Typical inductive switching waveforms.

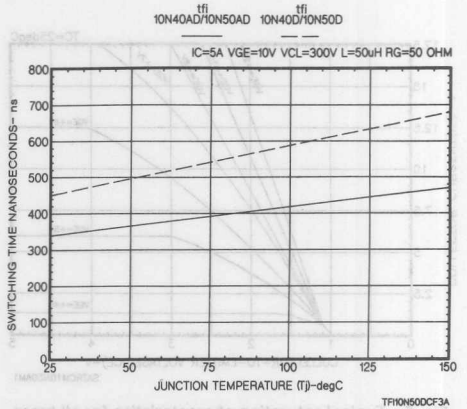


Fig. 12 - Typical fall time for all types ($I_C = 5$ A).

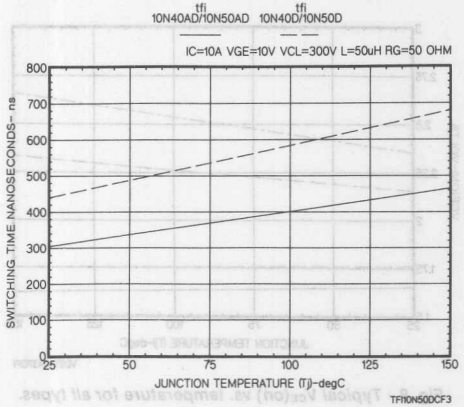


Fig. 13 - Typical fall time for all types ($I_C = 10$ A).

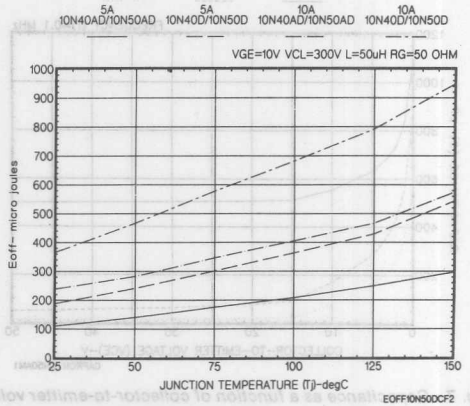


Fig. 14 - Typical clamped inductive turn-off switching loss/cycle.

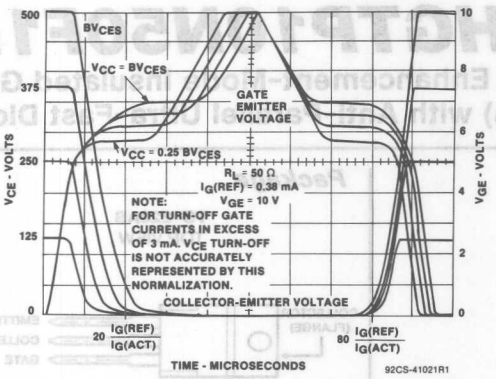


Fig. 15 – Normalized switching waveforms at constant gate current (Refer to Harris application notes AN-7254 and AN-7260.)

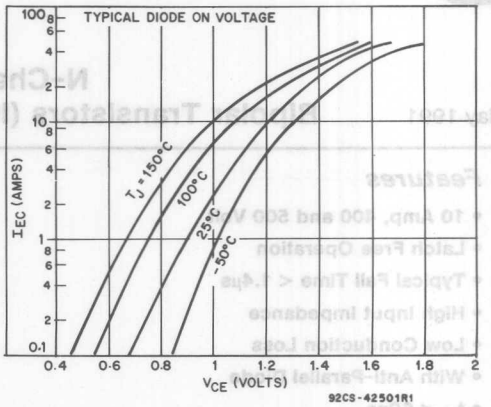


Fig. 16 - Typical diode collector-to-emitter voltage vs. current for all types.

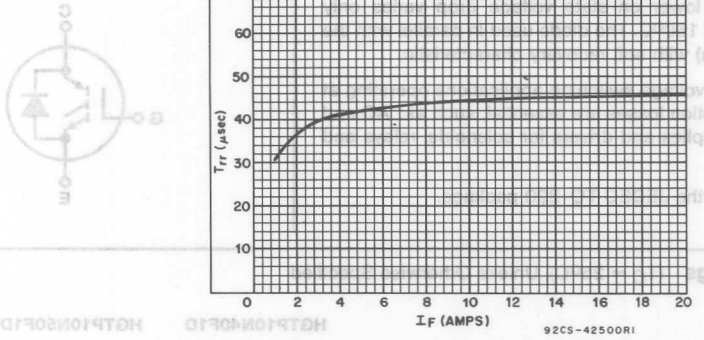


Fig. 17 - Typical diode reverse-recovery time for all types.

HGTP10N40F1D
HGTP10N50F1D

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs) with Anti-Parallel Ultra-Fast Diode

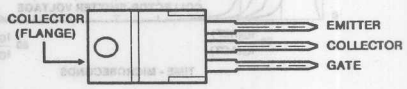
May 1991

Features

- 10 Amp, 400 and 500 Volt
- Latch Free Operation
- Typical Fall Time < 1.4μs
- High Input Impedance
- Low Conduction Loss
- With Anti-Parallel Diode
- t_{rr} < 60ns

Package

TO-220AB
TOP VIEW



Description

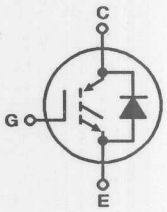
The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C. The diode used in parallel with the IGBT is an ultrafast (t_{rr} < 60ns) with soft recovery characteristic.

IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

These devices are supplied in the JEDEC TO-220 package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		HGTP10N40F1D	HGTP10N50F1D	UNITS
Collector-Emitter Voltage	BV_{CES}	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	400	500	V
Collector Current Continuous				
at T_C = 25°C	I_{C25}	12	12	A
at T_C = 90°C	I_{C90}	10	10	A
Collector Current Pulsed (Note 1)	I_{CM}	12	12	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	±20	V
Diode Forward Current				
at T_C = 25°C	I_{f25}	16	16	A
at T_C = 90°C	I_{f90}	10	10	A
Power Dissipation Total @ T_C = 25°C	P_D	75	75	W
Power Dissipation Derating T_C > 25°C		0.6	0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	260	°C

Note 1. T_J = 150°C, Min. R_{GE} = 25Ω w/o latch

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2751**

Electrical Characteristics At Case Temperature (T_C = 25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS HGTP10N40F1D MIN.	HGTP10N40F1D MAX.	HGTP10N50F1D MIN.	HGTP10N50F1D MAX.	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1.25mA, V_{GE} = 0	400	–	500	–	V
Gate Threshold Voltage	$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 1mA	2	4.5	2	4.5	V
Zero-Gate Voltage Collector Current	I_{CES}	T_J = 150°C, V_{CE} = 400V	–	1.25	–	–	mA
		V_{CE} = 500V	–	–	–	1.25	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V, V_{CE} = 0	–	100	–	100	nA
Collector-Emitter On-Voltage	$V_{CE(on)}$	I_C = 5A, V_{GE} = 10V, T_J = 150°C	–	2.5	–	2.5	V
		I_C = 5A, V_{GE} = 15V, T_J = 150°C	–	2.2	–	2.2	V
		I_C = 5A, V_{GE} = 10V, T_J = 25°C	–	2.5	–	2.5	V
		I_C = 5A, V_{GE} = 15V, T_J = 25°C	–	2.2	–	2.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 5A, V_{CE} = 10V	5.3 (typ.)				V
On-State Gate Charge	$Q_{G(on)}$	I_C = 5A, V_{CE} = 10V	13.4 (typ)				nC
Turn-On Delay Time	$t_{d(on)i}$	Resistive Load, I_C = 5A, R_L = 80Ω, V_{CE} = 400V, T_J = 150°C, V_{GE} = 10V, R_g = 25Ω	45 (typ)				ns
Rise Time	t_{ri}		35 (typ)				ns
Turn-Off Delay Time	$t_{d(off)i}$		130 (typ)				ns
Fall Time	t_f		1400 (typ)				ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{off} x frequency)	W_{off}		0.64 (typ)				mJ
Turn-Off Delay Time	$t_{d(off)i}$	Inductive Load (See Figure 6), I_C = 5A, R_L = 80Ω, L = 50μH, R_g = 25Ω, $V_{CE(clp)}$ = 400V, T_J = 150°C, V_{GE} = 10V	–	375	–	375	ns
Fall Time	t_{fi}		–	1200	–	1200	ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{off} x frequency)	W_{off}		–	1.2	–	1.2	mJ
Thermal Resistance Junction-to-Case (IGBT)	$R_{\theta JC}$		–	1.67	–	1.67	°C/W
Thermal Resistance of Diode	$R_{\theta JC}$		–	2	–	2	°C/W
Diode Forward Voltage	V_{EC}	I_{EC} = 10A	–	1.7	–	1.7	V
Diode Reverse Recovery Time	T_{rr}	I_{EC} = 10A, di/dt = 100A/μs	–	60	–	60	ns

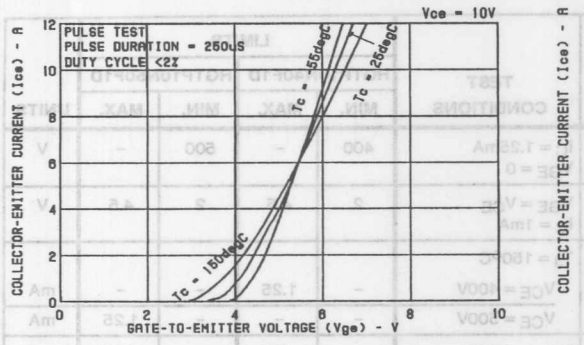


FIGURE 1. TYPICAL TRANSFER CHARACTERISTICS

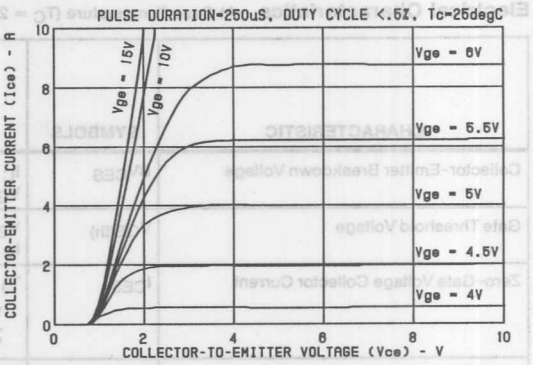


FIGURE 2. TYPICAL SATURATION CHARACTERISTICS

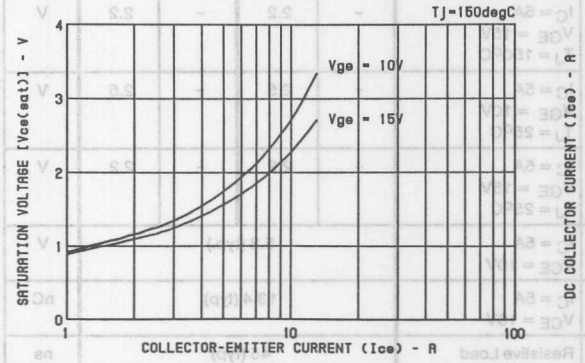


FIGURE 3. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT (TYPICAL)

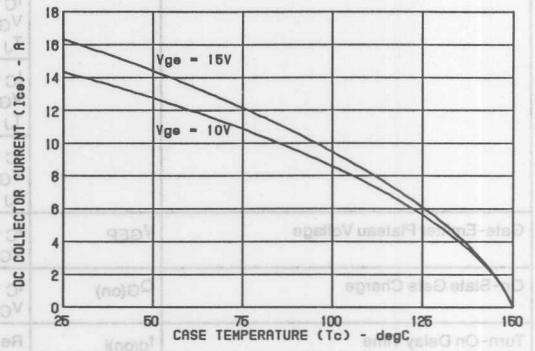


FIGURE 4. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

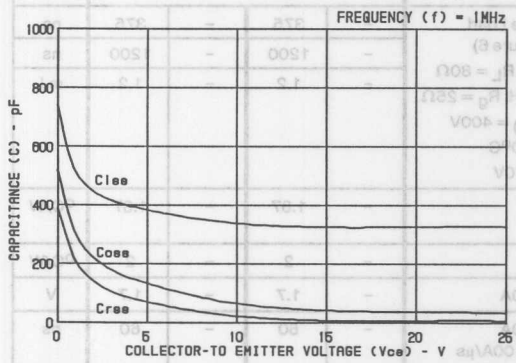


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-TO-EMITTER VOLTAGE (TYPICAL)

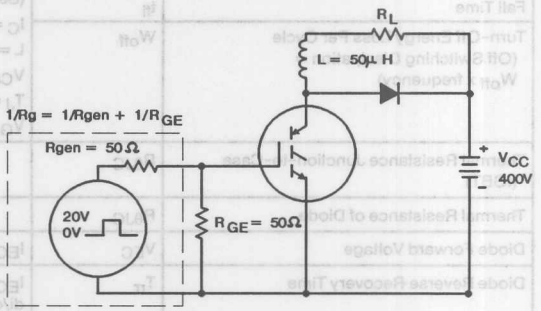


FIGURE 6. INDUCTIVE SWITCHING TEST CIRCUIT

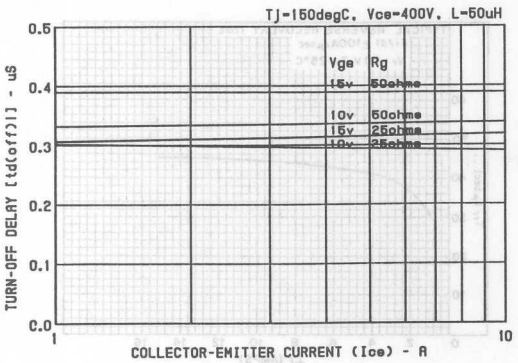


FIGURE 7. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

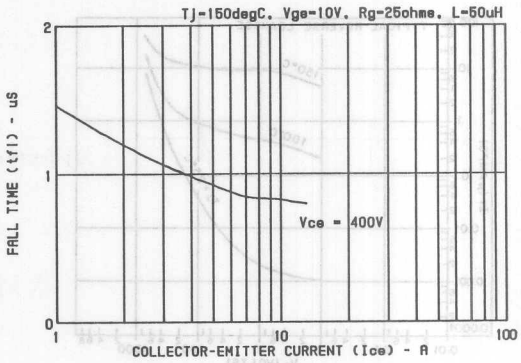


FIGURE 8. FALL TIME AS A FUNCTION OF COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

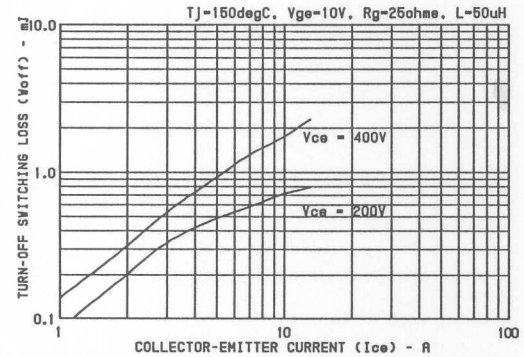


FIGURE 9. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT (TYPICAL)

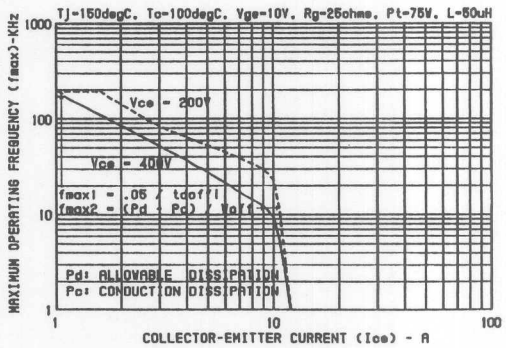


FIGURE 10. MAXIMUM OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR CURRENT AND VOLTAGE (TYPICAL)

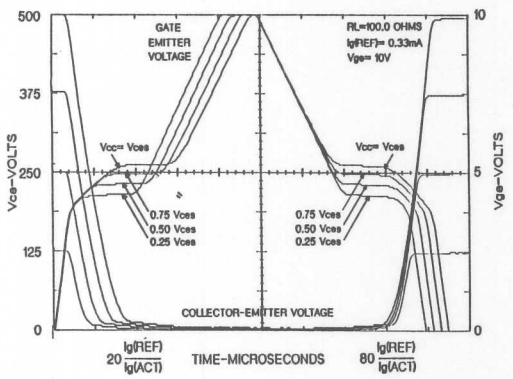


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT

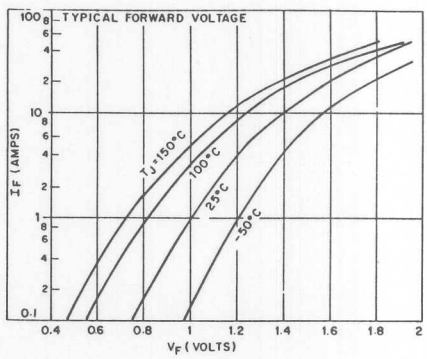


FIGURE 12. TYPICAL FORWARD VOLTAGE

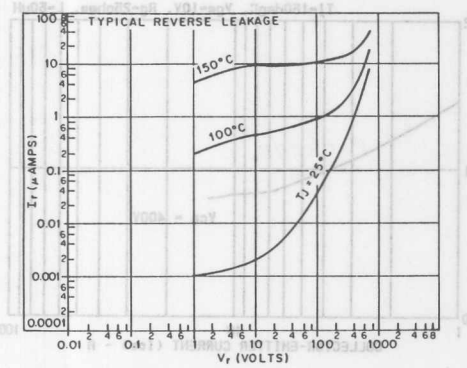


FIGURE 13. TYPICAL REVERSE LEAKAGE

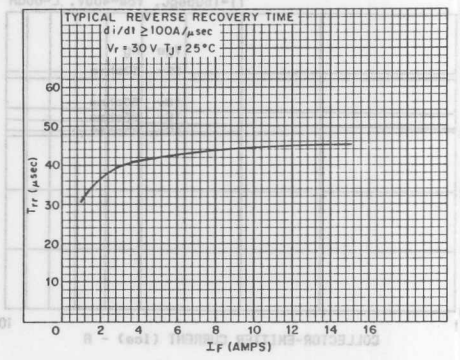


FIGURE 14. TYPICAL REVERSE RECOVERY TIME

HGTH12N40C1D, E1D
HGTH12N50C1D, E1D

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs) with Anti-Parallel Ultra-Fast Diode

August 1991

Features

- 12 Amp, 400 and 500 Volt
- $V_{CE(ON)}$: 2.5V Max.
- T_{Fall}: 1μs, 0.5μs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance
- Anti-Parallel Diode

Applications

- Power Supplies
- Motor Drives
- Protective Circuits

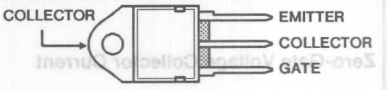
Description

The HGTH12N40C1D, HGTH12N40E1D, HGTH12N50C1D, and HGTH12N50E1D are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. They feature a discrete anti-parallel diode that shunts current around the IGBT in the reverse direction without introducing carriers into the depletion region. These types can be operated directly from low power integrated circuits.

They are supplied in the JEDEC TO-218AC plastic package.

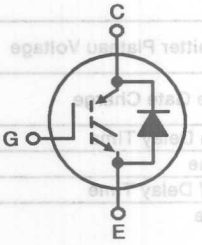
Package

JEDEC TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		HGTH12N40C1D HGTH12N40E1D	HGTH12N50C1D HGTH12N50E1D	UNITS
Collector-Emitter Voltage	V_{CES}	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	V_{CGR}	400	500	V
Gate-Emitter Voltage	V_{GE}	±20	±20	V
Collector Current Continuous	I_C	12	12	A
Collector Current Pulsed	I_{CM}	17.5	17.5	A
Power Dissipation Total @ T_C = 25°C	P_D	75	75	W
Power Dissipation Derating T_C = 25°C		0.6	0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2273.1

CHARACTERISTIC		TEST CONDITIONS	HGTH12N40C1D HGTH12N40E1D		HGTH12N50C1D HGTH12N50E1D		UNITS
			MIN.	MAX.	MIN.	MAX.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1 mA V_{GE} = 0	400	—	500	—	V
Gate Threshold Voltage	$V_{GE}(th)$	V_{GE} = V_{CE} I_C = 1 mA	2	4.5	2	4.5	V
Zero-Gate Voltage Collector Current	I_{CES}	V_{CE} = 400 V	—	250	—	—	μA
		V_{CE} = 500 V	—	—	—	250	μA
		T_C = 125° C V_{CE} = 400 V	—	1000	—	—	μA
		T_C = 125° C V_{CE} = 500 V	—	—	—	1000	μA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V V_{CE} = 0	—	100	—	100	nA
Collector-Emitter On-Voltage	$V_{CE}(on)$	I_C = 10 A V_{GE} = 10 V	—	2.5	—	2.5	V
		I_C = 17.5 A V_{GE} = 20 V	—	3.2	—	3.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 5 A V_{CE} = 10 V	—	6 (typ)	—	6 (typ)	V
On-State Gate Charge	$Q_G(on)$	I_C = 5 A V_{CE} = 10 V	—	19(typ)	—	19(typ)	nC
Turn-On Delay Time	$t_d(on)$	I_C = 10 A $V_{CE}(clp)$ = 300 V L = 50 μH T_J = 100° C V_{GE} = 10 V R_g = 50 Ω	—	50	—	50	ns
Rise Time	t_r		—	50	—	50	ns
Turn-Off Delay Time	$t_d(off)$		—	400	—	400	ns
Fall Time	t_{fi}						ns
40E1D 50E1D			TYP 680	1000	TYP 680	1000	ns
40C1D 50C1D			TYP 400	500	TYP 400	500	ns
Turn-Off Energy Loss per Cycle (off switching dissipation = E_{off} x frequency)	E_{off}	I_C = 10 A $V_{CE}(clp)$ = 300 V L = 50 μH T_J = 100° C V_{GE} = 10 V R_g = 50 Ω					μJ
40E1D 50E1D			1810 (typ)				μJ
40C1D 50C1D			1070 (typ)				μJ
Thermal Resistance Junction-to-Case	$R\theta_{JC}$		—	1.67	—	1.67	°C/W
Diode Forward Voltage	V_{EC}	I_{EC} = 10 A	—	2	—	2	V
Diode Reverse Recovery Time	T_{rr}	I_{EC} = 10 A di/dt = 100 A/μs	—	100	—	100	ns

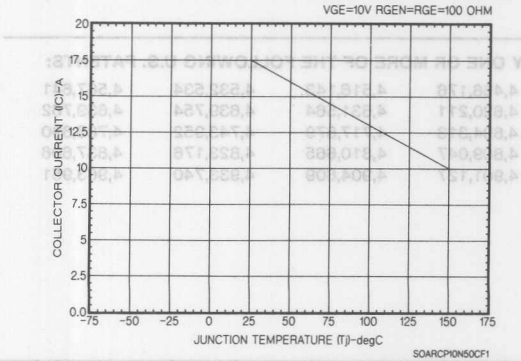


Fig. 1 - Maximum switching current level for all types. Minimum allowable values are R_g = 50 Ω, V_{GE} = 0 V.

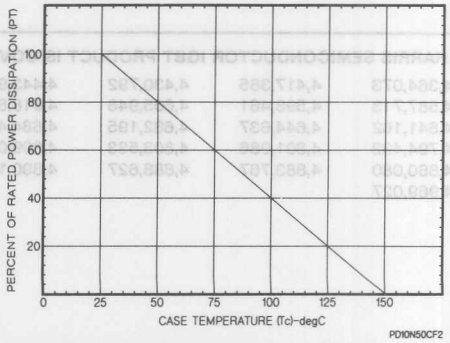


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

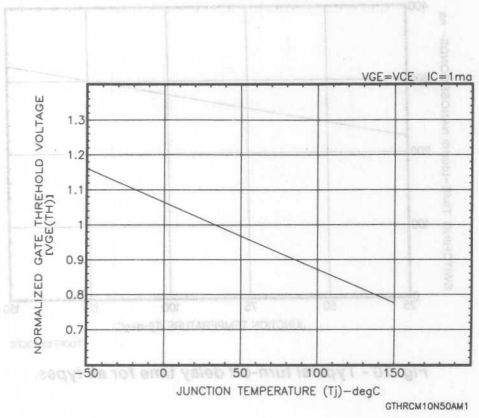


Fig. 3 - Typical normalized gate-threshold voltage as a function of junction temperature for all types.

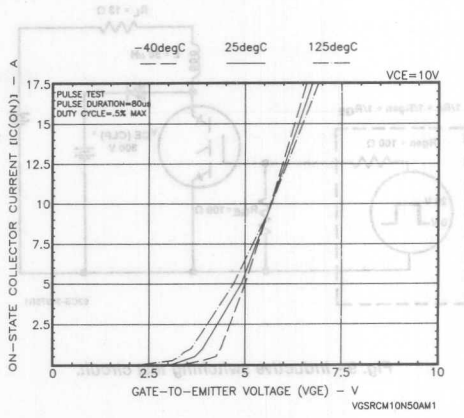


Fig. 4 - Typical transfer characteristics for all types.

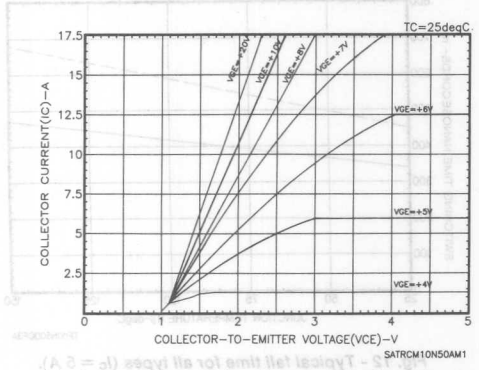


Fig. 5 - Typical saturation characteristics for all types.

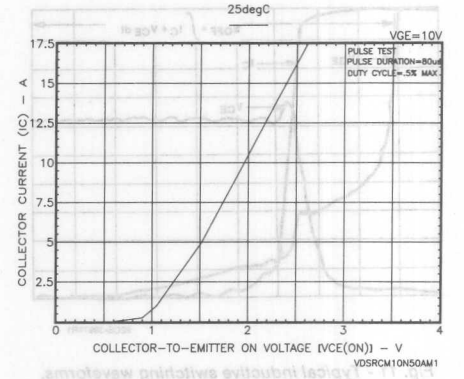


Fig. 6 - Typical collector-to-emitter on-voltage as a function of collector current for all types.

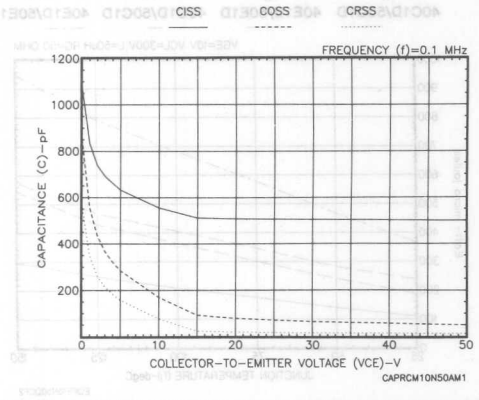


Fig. 7 - Capacitance as a function of collector-to-emitter voltage for all types.

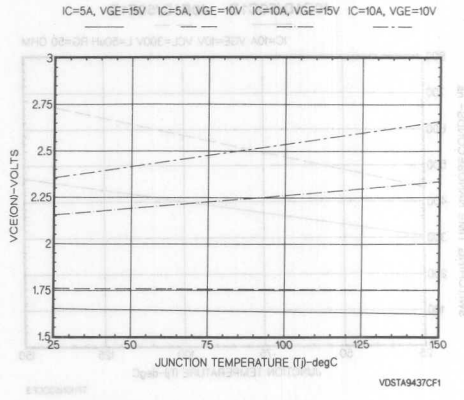


Fig. 8 - Typical $V_{CE}(on)$ vs. temperature for all types.

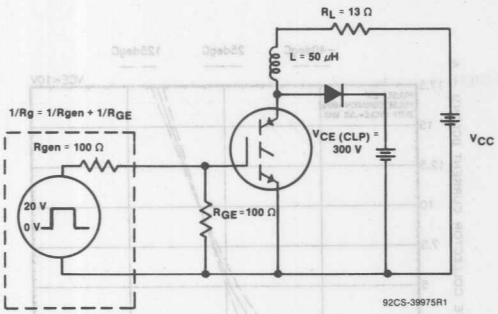


Fig. 9 - Inductive switching test circuit.

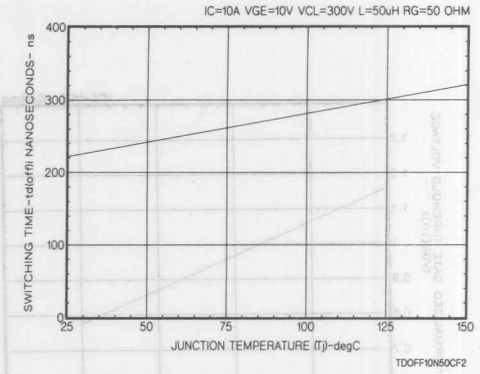


Fig. 10 - Typical turn-off delay time for all types.

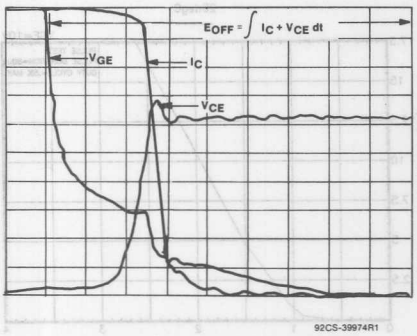


Fig. 11 - Typical inductive switching waveforms.

t_{fi} 40C1D/50C1D — t_{fi} 40E1D/50E1D —

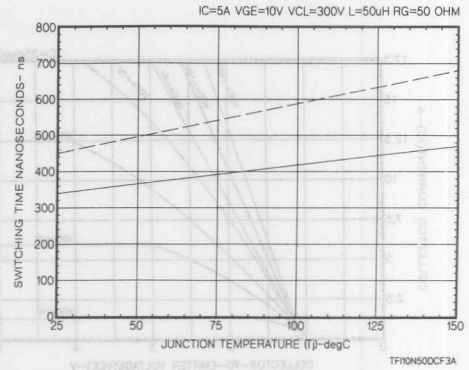


Fig. 12 - Typical fall time for all types (I_C = 5 A).

t_{fi} 40C1D/50C1D — t_{fi} 40E1D/50E1D —

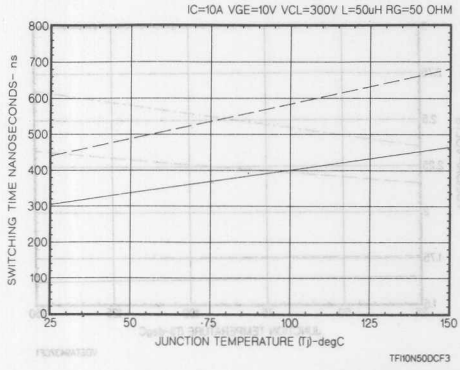


Fig. 13 - Typical fall time for all types (I_C = 10 A).

t_{fi} 40C1D/50C1D — t_{fi} 40E1D/50E1D — 5A 40C1D/50C1D — 5A 40E1D/50E1D —

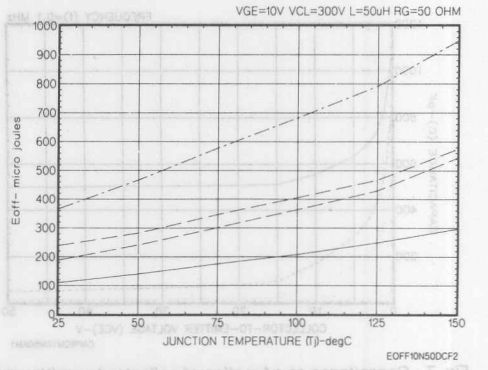


Fig. 14 - Typical clamped inductive turn-off switching loss/cycle.

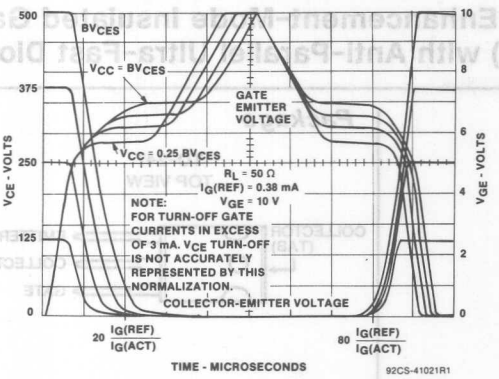


Fig. 15 – Normalized switching waveforms at constant gate current. (Refer to Harris application notes AN7254 and AN7260.)

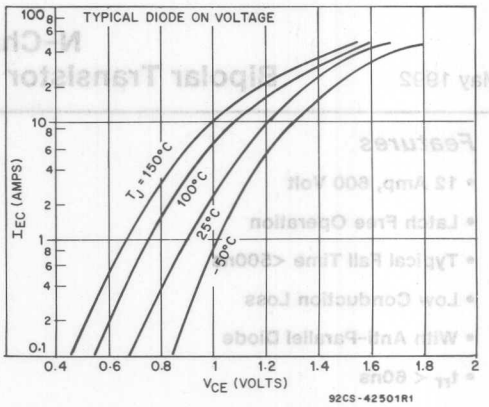


Fig. 16 - Typical diode collector-to-emitter voltage vs. current for all types.

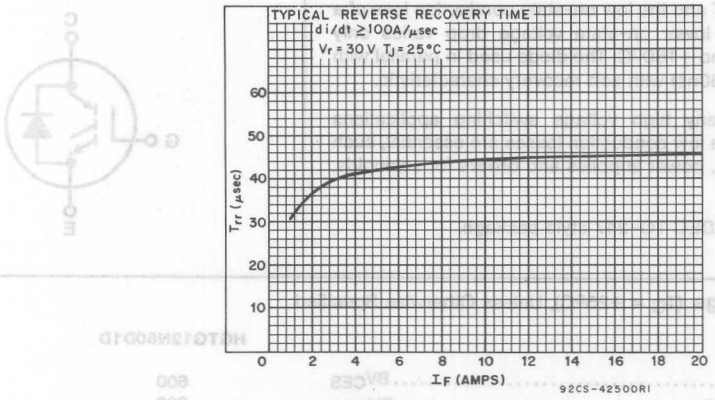


Fig. 17 - Typical diode reverse-recovery time for all types.

HARRIS HGTG12N60D1D

May 1992

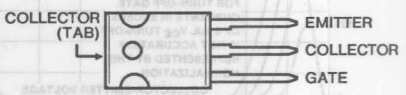
N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT) with Anti-Parallel Ultra-Fast Diode

Features

- 12 Amp, 600 Volt
- Latch Free Operation
- Typical Fall Time <500ns
- Low Conduction Loss
- With Anti-Parallel Diode
- t_{rr} < 60ns

Package

TO-247
TOP VIEW



Description

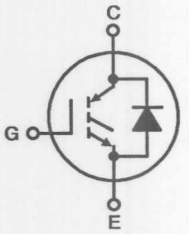
The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C. The diode used in parallel with the IGBT is an ultrafast (t_{rr} < 60ns) with soft recovery characteristic.

The IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

This type is supplied in the JEDEC TO-247 style package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		HGTG12N60D1D	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	600	V
Collector Current Continuous			
@ T_C = +25°	I_{C25}	21	A
@ T_C = +90°	I_{C90}	12	A
Collector Current Pulsed (1)	I_{CM}	48	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Switching Safe Operating Area at T_J = +150°C	SSOA	30A @ 0.8BV_{CES}	-
Diode Forward Current			
@ T_C = +25°	I_{f25}	21	A
@ T_C = +90°	I_{f90}	12	A
Power Dissipation Total @ T_C = +25°C	P_D	75	W
Power Dissipation Derating T_C > +25°C		0.8	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.125" from case for 5 seconds)	T_L	260	°C

(1) Repetitive Rating: Pulse width limited by maximum junction temperature.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2800.1**

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 280μA, V_{GE} = 0V		600	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	V_{CE} = BV_{CES}	T_C = +25°C	-	-	280	μA
		V_{CE} = 0.8 BV_{CES}	T_C = +125°C	-	-	5.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C90}, V_{GE} = 15V	T_C = +25°C	-	1.9	2.5	V
			T_C = +125°C	-	2.1	2.7	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}	T_C = +25°C	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}		-	7.2	-	V
On-State Gate Charge	$Q_{G(on)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	-	45	60	nC
			V_{GE} = 20V	-	70	90	nC
Current Turn-On Delay Time	$t_{d(on)i}$	L = 500μH, I_C = I_{C90}, R_g = 25Ω, V_{GE} = 15V, T_J = 150°C, V_{CE} = 0.8 BV_{CES}		-	100	-	ns
Current Rise Time	t_{ri}			-	150	-	ns
Current Turn-Off	$t_{d(off)i}$			-	430	600	ns
Current Fall Time	t_{fi}			-	430	600	ns
Turn-Off Energy(1)	W_{off}			-	1.8	-	mJ
Thermal Resistance IGBT	$R_{\theta JC}$			-	-	1.67	°C/W
Thermal Resistance Diode	$R_{\theta JC}$			-	-	1.5	°C/W
Diode Forward Voltage	V_{EC}	I_{EC} = 12A				1.50	V
Diode Reverse Recovery Time	t_{rr}	I_{EC} = 12A, di/dt = 100A/μs				60	ns

(1) Turn-off Energy Loss (W_{off}) is defined as the integral of the instantaneous power loss starting at the trailing idge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A) The HGTG12N60D1D was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

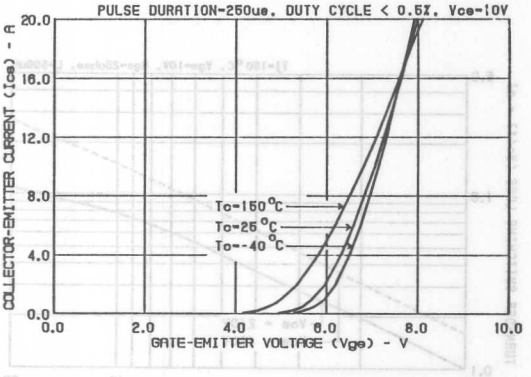


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

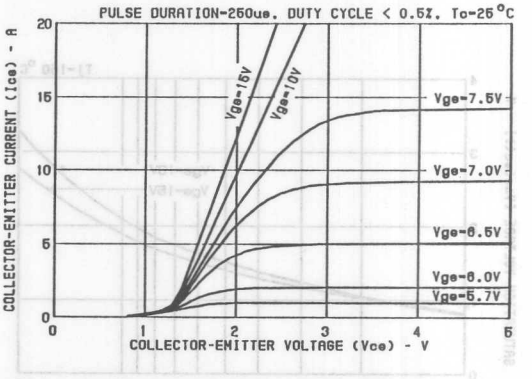


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

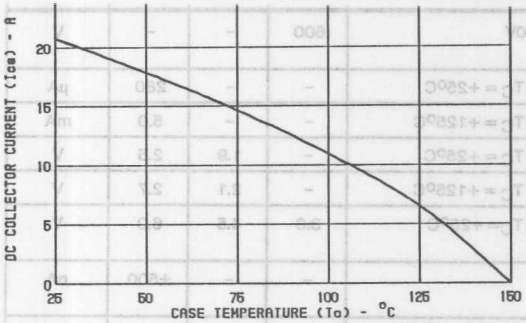


FIGURE 3. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

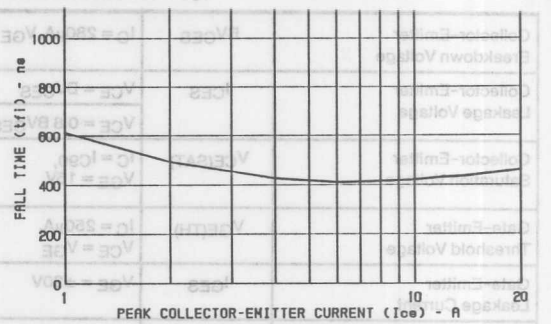


FIGURE 4. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

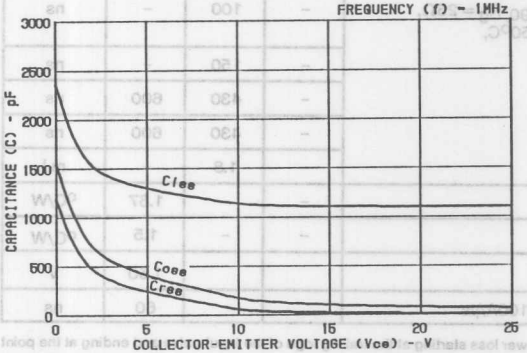


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

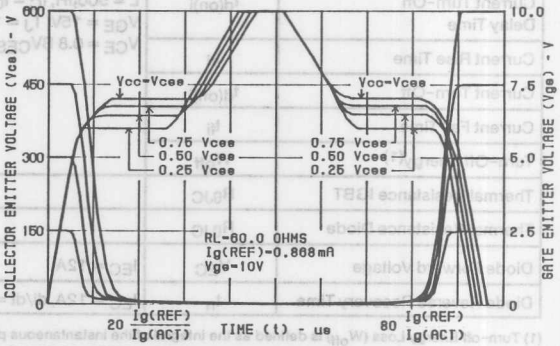


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260.)

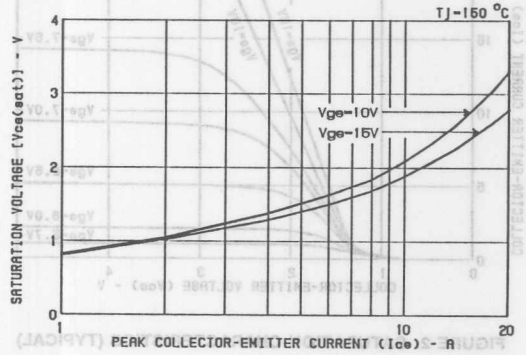


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

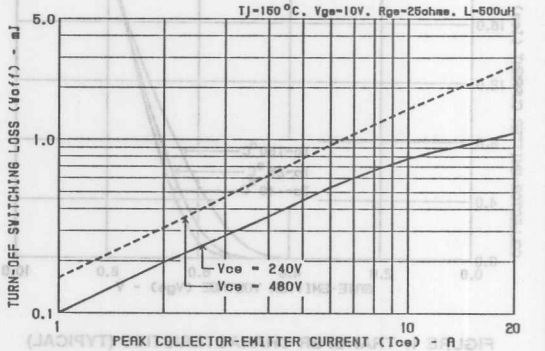


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

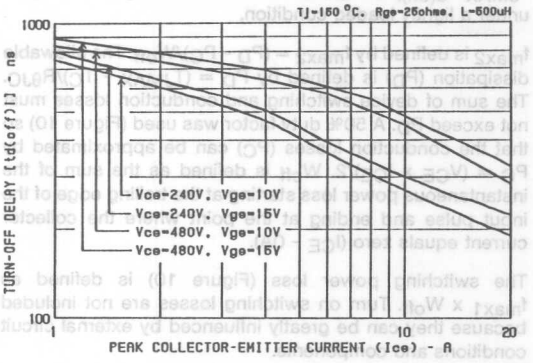


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMMITER CURRENT.

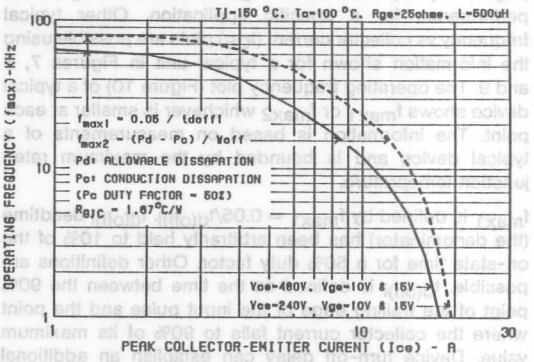


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE.

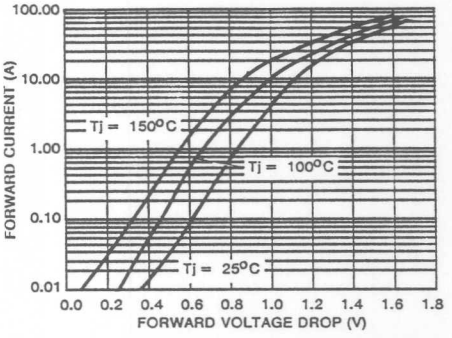


FIGURE 11. TYPICAL DIODE COLLECTOR-TO-EMITTER VOLTAGE.

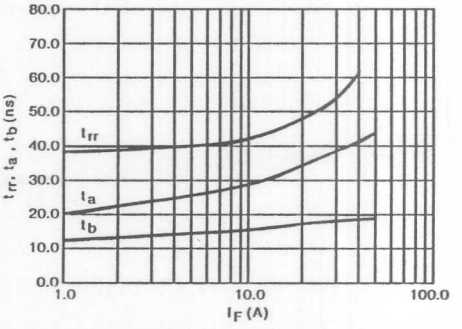


FIGURE 12. TYPICAL t_{rr}, t_a, t_b vs FORWARD CURRENT.

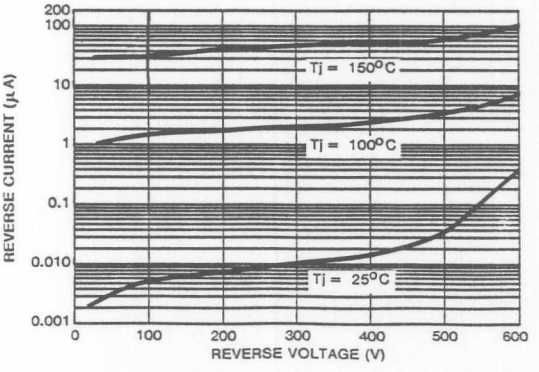


FIGURE 13. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC.

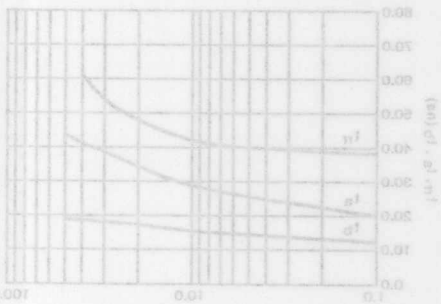
Operating Frequency Information

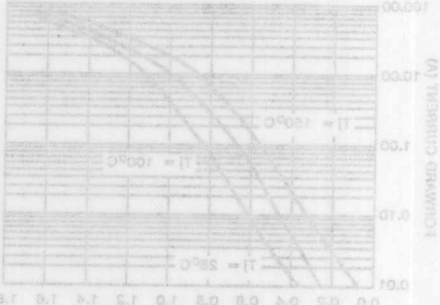
Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{max1} or f_{max2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temeprature.

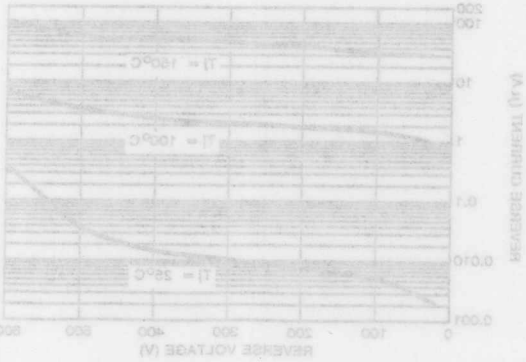
f_{max1} is defined by $f_{max1} = 0.05/t_{d(off)i}$. $t_{d(off)i}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(off)i}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(off)i}$ is important when controlling output ripple under a lightly loaded condition.

f_{max2} is defined by $f_{max2} = (P_D - P_C)/W_{off}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} \times I_{CE})/2$. W_{off} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} - 0A).

The switching power loss (Figure 10) is defined as $f_{max1} \times W_{off}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.







HARRIS HGTM12N60D1

May 1992

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)

Features

- 12 Amp, 600 Volt
- Latch Free Operation
- Typical Fall Time <500ns
- High Input Impedance
- Low Conduction Loss

Description

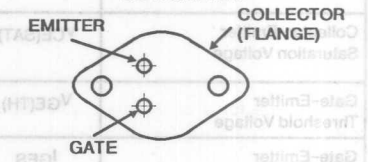
The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

IGBTs are ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

This type is supplied in the JEDEC TO-204AA package.

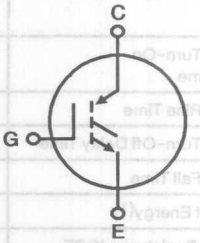
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		HGTM12N60D1	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	600	V
Collector Current Continuous			
@ T_C = +25°	I_{C25}	21	A
@ V_{GE} = 15V @ T_C = +90°	I_{C90}	12	A
Collector Current Pulsed (1)	I_{CM}	48	A
Gate-Emitter Voltage Continuous	V_{GES}	±25	V
Switching Safe Operating Area at T_J = +150°C	SSOA	30A @ 0.8BV_{CES}	-
Power Dissipation Total @ T_C = +25°C	P_D	75	W
Power Dissipation Derating T_C > +25°C		0.6	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C

(1) Repetitive Rating: Pulse width limited by maximum junction temperature.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2829.1

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A, V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	1.0	μA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +125^oC$	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C90}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	1.9	2.5	V
			$T_C = +125^oC$	-	2.1	2.7	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = +25^oC$	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C90}, V_{CE} = 0.5\ BV_{CES}$		-	7.2	-	V
On-State Gate Charge	$Q_{G(on)}$	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	45	60	nC
			$V_{GE} = 20V$	-	70	90	nC
Current Turn-On Delay Time	$t_{d(on)i}$	$L = 500\mu H, I_C = I_{C90}, R_g = 25\Omega$, $V_{GE} = 15V, T_J = 150^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{ri}			-	150	-	ns
Current Turn-Off Delay Time	$t_{d(off)i}$			-	430	600	ns
Current Fall Time	t_{fi}			-	430	600	ns
Turn-Off Energy(1)	W_{off}			-	1.8	-	mJ
Thermal Resistance IGBT	$R_{\theta JC}$			-	-	1.67	$^oC/W$

(1) Turn-off Energy Loss (W_{off}) is defined as the integral of the instantaneous power loss starting at the trailing idge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A) The HGTM12N60D1 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

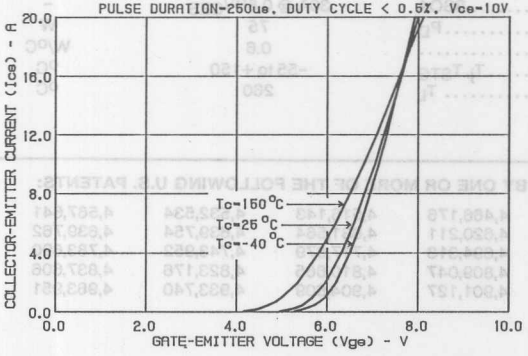


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

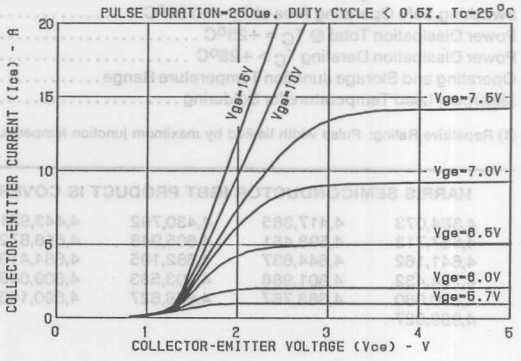


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

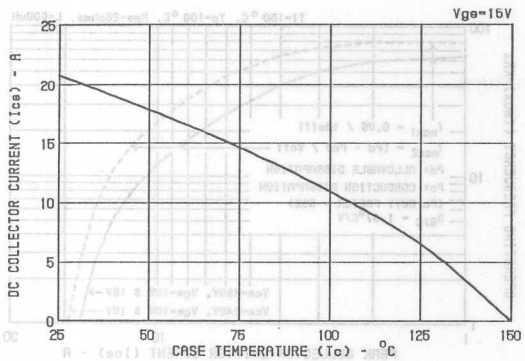


FIGURE 3. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

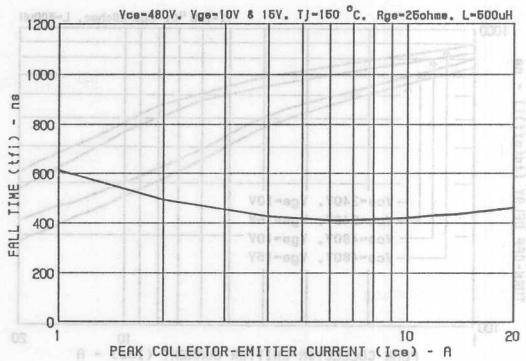


FIGURE 4. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

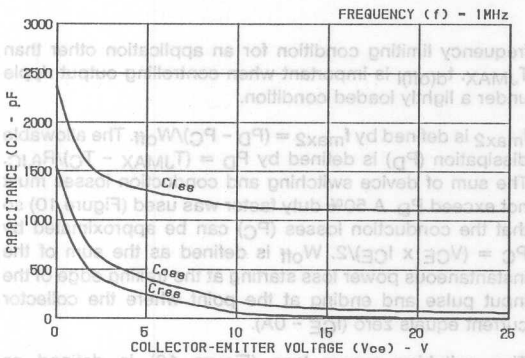


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

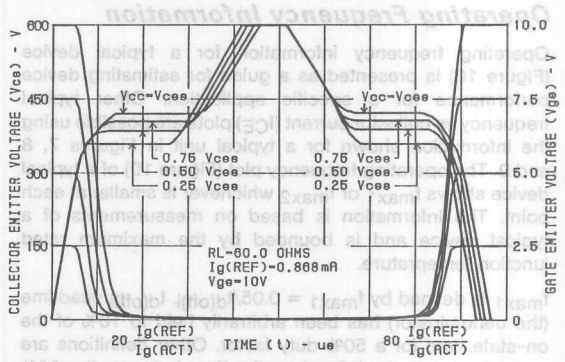


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260.)

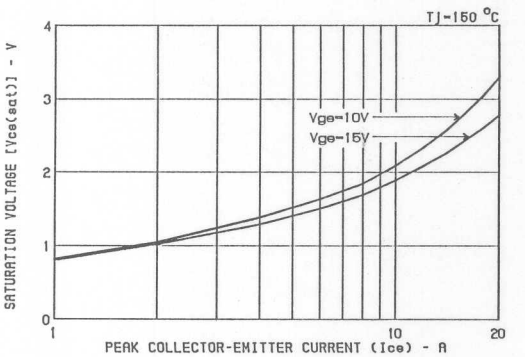


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

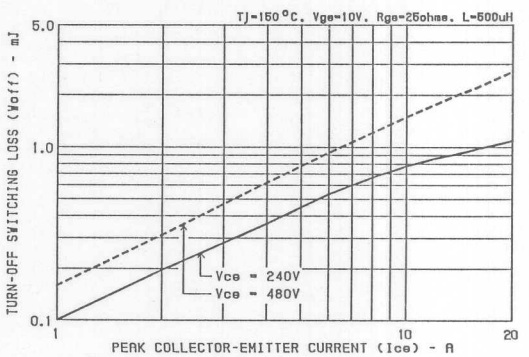


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

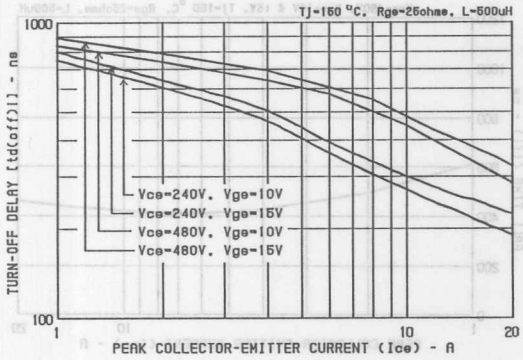


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMMITER CURRENT

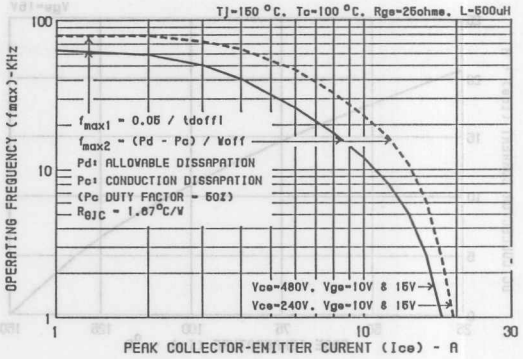


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{max1} or f_{max2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temeprature.

f_{max1} is defined by $f_{max1} = 0.05/t_{d(off)i}$. $t_{d(off)i}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(off)i}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(off)i}$ is important when controlling output ripple under a lightly loaded condition.

f_{max2} is defined by $f_{max2} = (P_D - P_C)/W_{off}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} \times I_{CE})/2$. W_{off} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} - 0A).

The switching power loss (Figure 10) is defined as $f_{max1} \times W_{off}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS HGTP12N60D1

May 1992

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)

Features

- 12 Amp, 600 Volt
- Latch Free Operation
- Typical Fall Time <500ns
- High Input Impedance
- Low Conduction Loss

Description

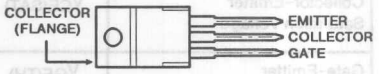
The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

IGBTs are ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

This type is supplied in the JEDEC TO-220AB package.

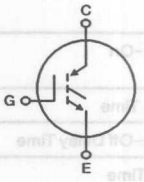
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		HGTP12N60D1	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	600	V
Collector Current Continuous			
@ T_C = +25°	I_{C25}	21	A
@ V_{GE} = 15V @ T_C = +90°	I_{C90}	12	A
Collector Current Pulsed (1)	I_{CM}	48	A
Gate-Emitter Voltage Continuous	V_{GES}	±25	V
Switching Safe Operating Area at T_J = +150°C	SSOA	30A @ 0.8BV_{CES}	-
Power Dissipation Total @ T_C = +25°C	P_D	75	W
Power Dissipation Derating T_C > +25°C		0.6	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C

(1) Repetitive Rating: Pulse width limited by maximum junction temperature.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2830.1

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250μA, V_{GE} = 0V		600	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	V_{CE} = BV_{CES}	T_C = +25°C	-	-	1.0	μA
		V_{CE} = 0.8 BV_{CES}	T_C = +125°C	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C90}, V_{GE} = 15V	T_C = +25°C	-	1.9	2.5	V
			T_C = +125°C	-	2.1	2.7	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}	T_C = +25°C	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}		-	7.2	-	V
On-State Gate Charge	$Q_{G(on)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	-	45	60	nC
			V_{GE} = 20V	-	70	90	nC
Current Turn-On Delay Time	$t_{d(on)i}$	L = 500μH, I_C = I_{C90}, R_g = 25Ω, V_{GE} = 15V, T_J = 150°C, V_{CE} = 0.8 BV_{CES}		-	100	-	ns
Current Rise Time	t_{ri}			-	150	-	ns
Current Turn-Off Delay Time	$t_{d(off)i}$			-	430	600	ns
Current Fall Time	t_{fi}			-	430	600	ns
Turn-Off Energy(1)	W_{off}			-	1.8	-	mJ
Thermal Resistance IGBT	$R_{\theta JC}$			-	-	1.67	°C/W

(1) Turn-off Energy Loss (W_{off}) is defined as the integral of the instantaneous power loss starting at the trailing idge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A) The HGTP12N60D1 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

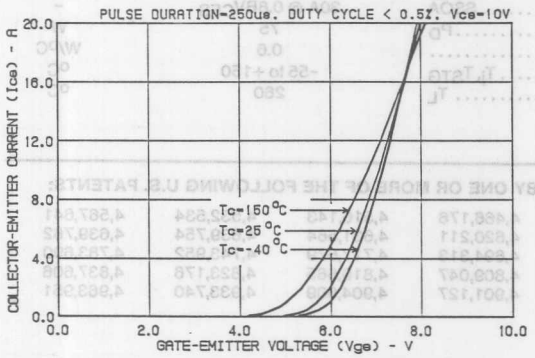


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

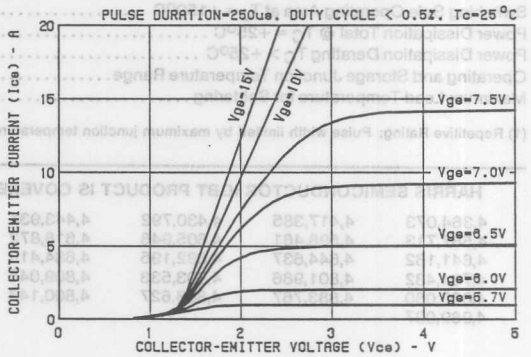


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

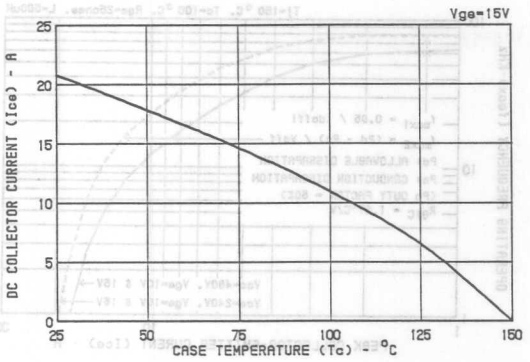


FIGURE 3. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

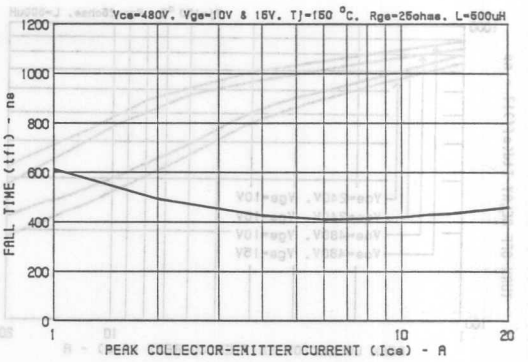


FIGURE 4. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

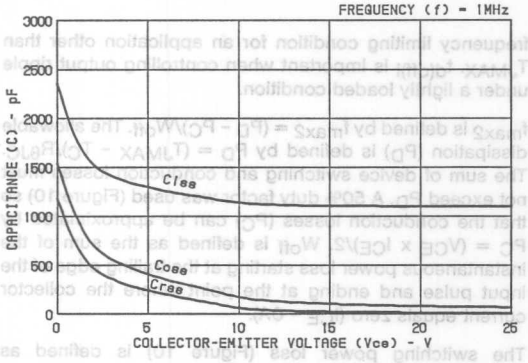


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

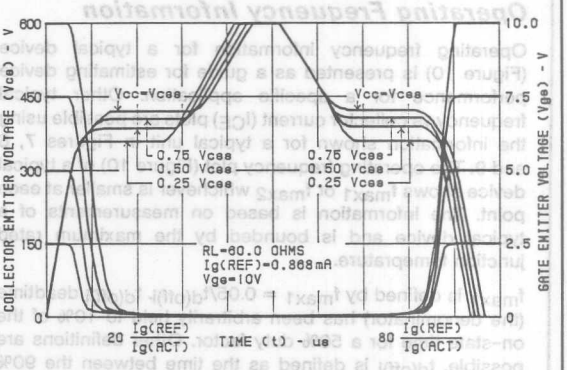


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260.)

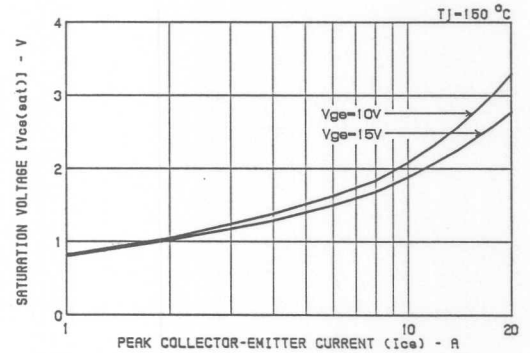


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

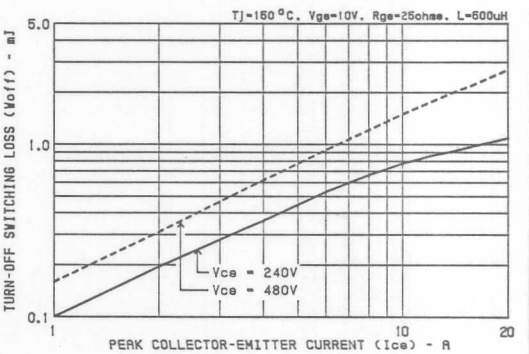


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

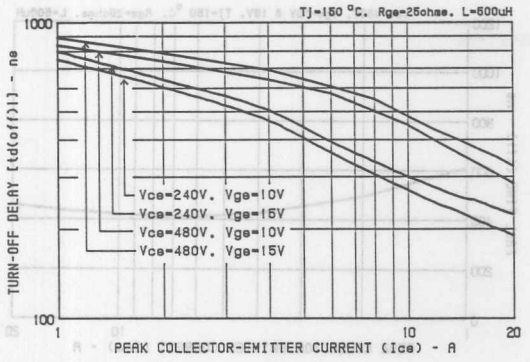


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMMITER CURRENT

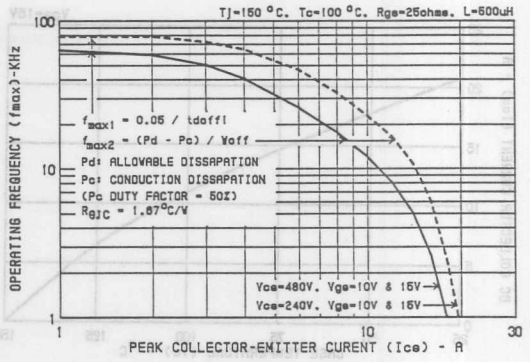


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{max1} or f_{max2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temeprature.

f_{max1} is defined by $f_{max1} = 0.05/t_{d(off)i}$. $t_{d(off)i}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(off)i}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(off)i}$ is important when controlling output ripple under a lightly loaded condition.

f_{max2} is defined by $f_{max2} = (P_D - P_C)/W_{off}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} \times I_{CE})/2$. W_{off} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} - 0A).

The switching power loss (Figure 10) is defined as $f_{max1} \times W_{off}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HGTH20N40C1/40E1/50C1/50E1
HGTM20N40C1/40E1/50C1/50E1
HGTP15N40C1/40E1/50C1/50E1

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs)

August 1991

Features

- 15A and 20A, 400V and 500V
- $V_{CE(ON)}$: 2.5V
- T_{Fi}: 1μs, 0.5μs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance
- No Anti-Parallel Diode

Applications

- Power Supplies
- Motor Drives
- Protection Circuits

Description

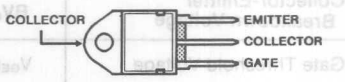
The HGTH20N40C1, HGTH20N40E1, HGTH20N50C1, HGTH20N50E1, HGTM20N40C1, HGTM20N40E1, HGTM20N50C1, HGTM20N50E1, HGTP15N40C1, HGTP15N40E1, HGTP15N50C1 and HGTP15N50E1 are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high-voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low-power integrated circuits.

The HGTH-types are supplied in the JEDEC TO-218AC plastic package and the HGTP-types in the JEDEC TO-220AB plastic package.

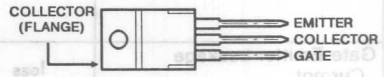
The HGTM-types are supplied in the JEDEC TO-204AA steel package.

Packages

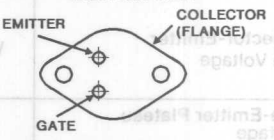
HGTH-TYPES JEDEC TO-218AC
TOP VIEW



HGTP-TYPES JEDEC TO-220AB
TOP VIEW

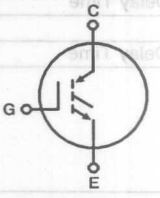


HGTM-TYPES JEDEC TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

	HGTH20N40C1 HGTM20N40C1 HGTH20N40E1 HGTM20N40E1	HGTH20N50C1 HGTM20N50C1 HGTH20N50E1 HGTM20N50E1	HGTP15N40C1 HGTP15N40E1	HGTP15N50C1 HGTP15N50E1	UNITS
Collector-Emitter Voltage ..... V_{CES}	400	500	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ ..... V_{CGR}	400	500	400	500	V
Reverse Collector-Emitter Voltage ..... $V_{CES(rev.)}$	-5	-5	-5	-5	V
Gate-Emitter Voltage ..... V_{GE}	±20	±20	±20	±20	V
Collector Current Continuous ..... I_C	20	20	15	15	A
Collector Current Pulsed ..... I_{CM}	35	35	35	35	A
Power Dissipation @ T_C = 25°C ..... P_D	100	100	75	75	W
Power Dissipation Derate Above T_C = 25°C	0.8	0.8	0.6	0.6	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2174.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C = 25° C) unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			HGTH20N40C1 HGTH20N40E1 HGTM20N40C1 HGTM20N40E1 HGTP15N40C1 HGTP15N40E1		HGTH20N50C1 HGTH20N50E1 HGTM20N50C1 HGTM20N50E1 HGTP15N50C1 HGTP15N50E1		
			Min.	Max.	Min.	Max.	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1 mA V_{GE} = 0	400	—	500	—	V
Gate Threshold Voltage	$V_{GE}(th)$	V_{GE} = V_{CE} I_C = 1 mA	2	4.5	2	4.5	V
Zero-Gate Voltage Collector Current	I_{CES}	V_{CE} = 400 V V_{CE} = 500 V	— —	250 —	— —	— 250	μA
		T_C = 125° C V_{CE} = 400 V V_{CE} = 500 V	— — —	— 1000 —	— — —	— — 1000	
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V V_{CE} = 0	—	100	—	100	nA
Reverse Collector-Emitter Leakage Current	I_{CE}	R_{GE} = 0 Ω V_{EC} = 5 V	—	-5	—	-5	mA
Collector-Emitter On Voltage	$V_{CE}(on)$	I_C = 20 A V_{GE} = 10 V	—	2.5	—	2.5	V
		I_C = 35 A V_{GE} = 20 V	—	3.2	—	3.2	
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 10 A V_{CE} = 10 V	—	6 (typ.)	—	6 (typ.)	V
On-State Gate Charge	$Q_g(on)$	I_C = 10 A V_{CE} = 10 V	—	33 (typ.)	—	33 (typ.)	nC
Turn-On Delay Time	$t_d(on)$	I_C = 20 A $V_{CE(CLP)}$ = 300 V L = 25 μH T_J = 100° C V_{GE} = 10 V R_g = 25 Ω	—	50	—	50	ns
Rise Time	t_r		—	50	—	50	
Turn-Off Delay Time	$t_d(off)$		—	400	—	400	
Fall Time	t_{fi} 40E1 50E1		Typ. 680	1000	Typ. 680	1000	
	40C1 50C1		400	500	400	500	
Turn-Off Energy Loss per Cycle (off switching dissipation = E_{off} x frequency)	E_{off} 40E1 50E1	I_C =10 A $V_{CE(CLP)}$ = 300 V L = 25 μH T_J = 100° C V_{GE} = 10 V R_g = 25 Ω	1810 (typ.)				μJ
	40C1 50C1		1070 (typ.)				
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	HGTH/HGTM	—	1.25	—	1.25	°C/W
		HGTP	—	1.67	—	1.67	

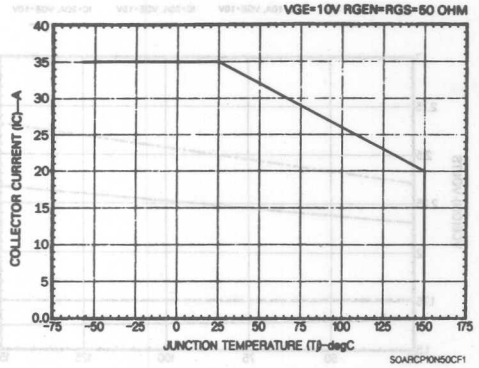


Fig. 1 - Maximum switching current level for all types. R_g = 25 Ω, V_{GE} = 0 V are the minimum allowable values.

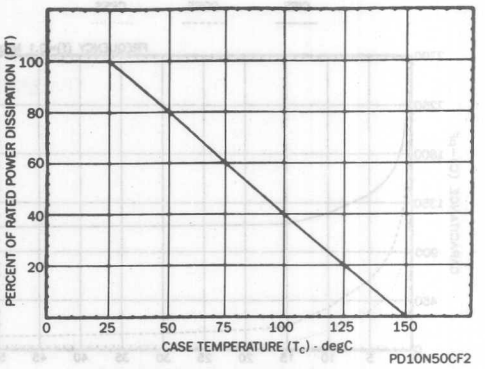


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

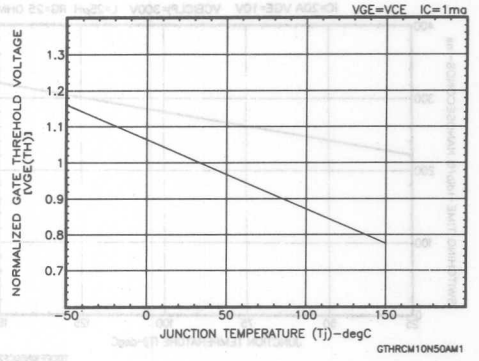


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

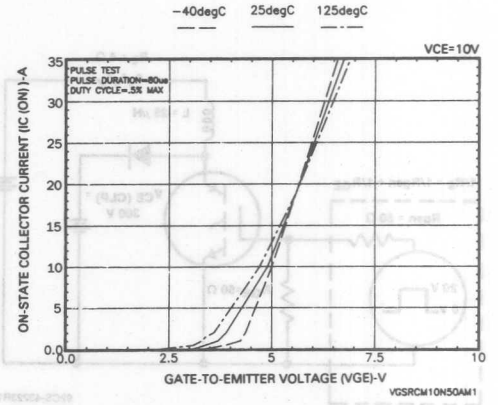


Fig. 4 - Typical transfer characteristics for all types.

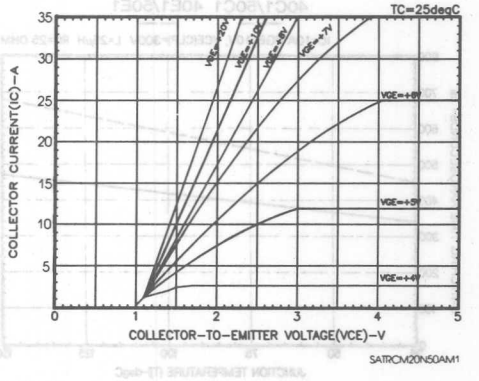


Fig. 5 - Typical saturation characteristics for all types.

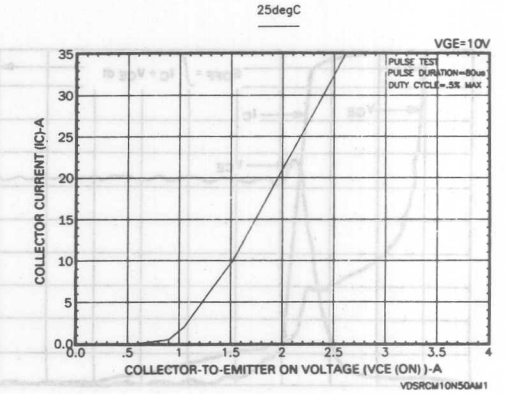


Fig. 6 - Typical collector-to-emitter on-voltage as a function of collector current for all types.

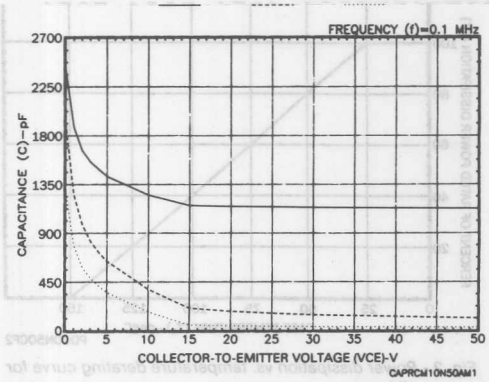


Fig. 7 - Capacitance as a function of collector-to-emitter voltage for all types.

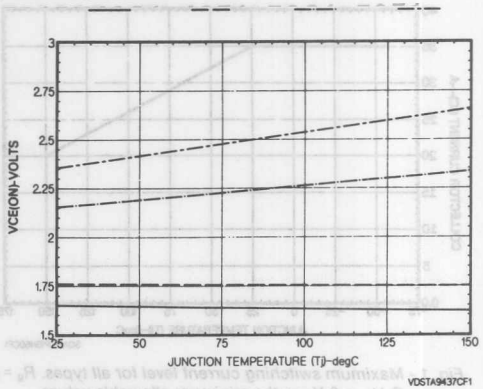


Fig. 8 - Typical V_{CE} (on) vs. temperature for all types.

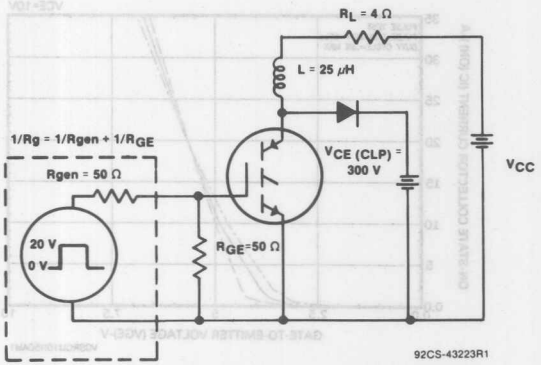


Fig. 9 - Inductive switching test circuit.

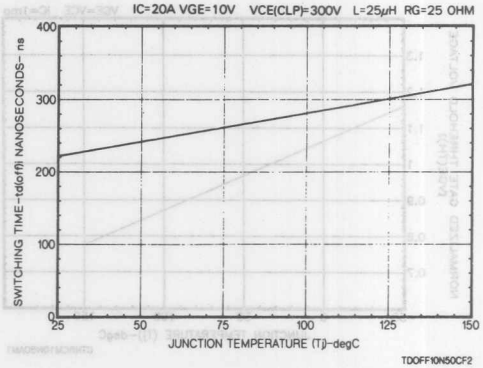


Fig. 10 - Typical turn-off delay time for all types.

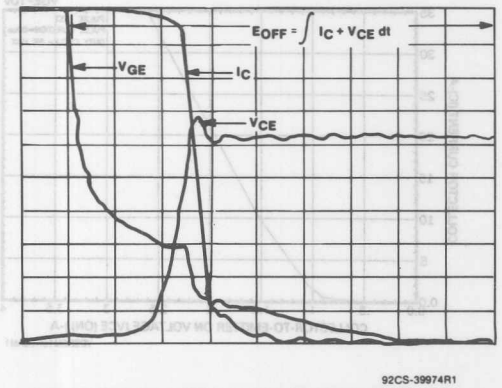


Fig. 11 - Typical inductive switching waveforms.

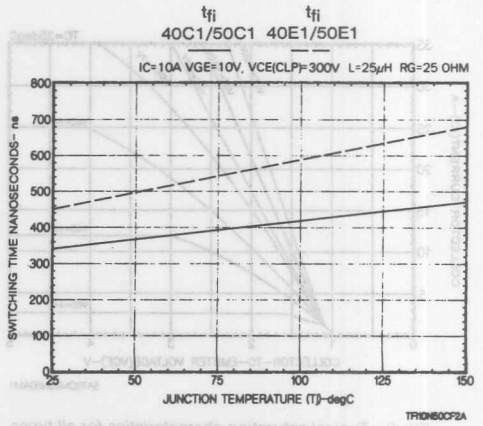


Fig. 12 - Typical fall time for all types.

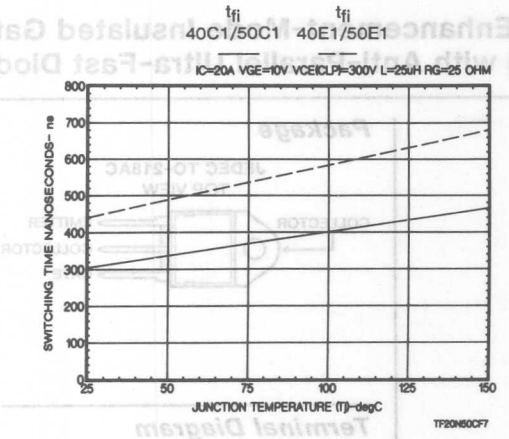


Fig. 13 - Typical fall time for all types (I_C = 20 A).

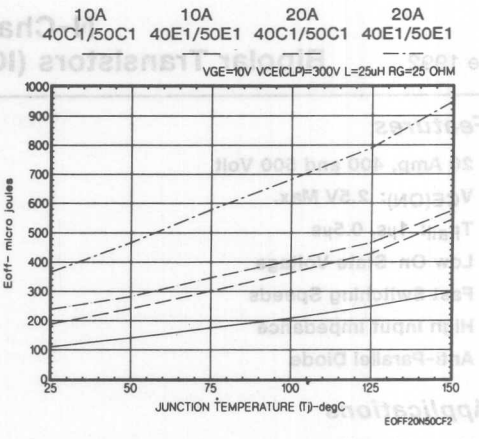
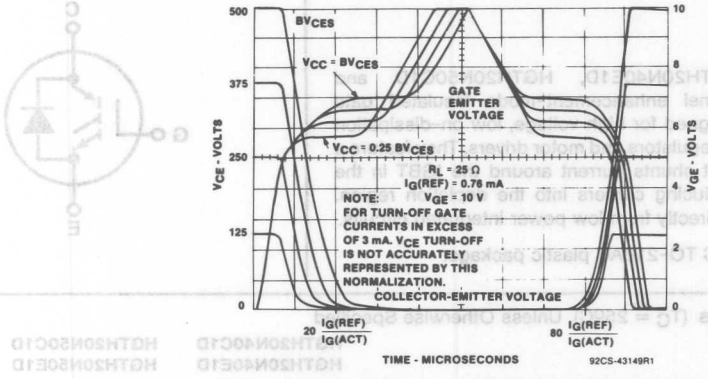


Fig. 14 - Typical clamped inductive turn-off switching loss/cycle.



Refer to Harris application notes AN-7254 and AN-7260 on the use of normalized switcing waveforms.

Fig. 15 - Normalized switching waveforms at constant gate current.

HARRIS

HGTH20N40C1D, E1D
HGTH20N50C1D, E1D

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistors (IGBTs) with Anti-Parallel Ultra-Fast Diode

June 1992

Features

- 20 Amp, 400 and 500 Volt
- $V_{CE(ON)}$: 2.5V Max.
- T_{Fall}: 1μs, 0.5μs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance
- Anti-Parallel Diode

Applications

- Power Supplies
- Motor Drives
- Protective Circuits

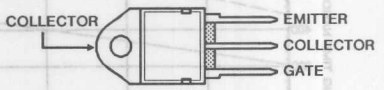
Description

The HGTH20N40C1D, HGTH20N40E1D, HGTH20N50C1D and HGTH20N50E1D are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. They feature a discrete anti-parallel diode that shunts current around the IGBT in the reverse direction without introducing carriers into the depletion region. These types can be operated directly from low power integrated circuits.

They are supplied in the JEDEC TO-218AC plastic package.

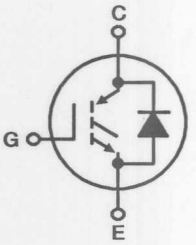
Package

JEDEC TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		HGTH20N40C1D HGTH20N40E1D	HGTH20N50C1D HGTH20N50E1D	UNITS
Collector-Emitter Voltage	V_{CES}	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	V_{CGR}	400	500	V
Gate-Emitter Voltage	V_{GE}	±20	±20	V
Collector Current Continuous	I_C	20	20	A
Collector Current Pulsed	I_{CM}	35	35	A
Diode Forward Current Continuous				
@ T_C = +25°C	I_{f25}	35	35	A
@ T_J = +90°C	I_{f90}	20	20	A
Power Dissipation Total @ T_C = +25°C	P_D	100	100	W
Power Dissipation Derating T_C = +25°C		0.8	0.8	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2271.2**

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS HGTH20N40C1D HGTH20N40E1D MIN.	LIMITS HGTH20N40C1D HGTH20N40E1D MAX.	LIMITS HGTH20N50C1D HGTH20N50E1D MIN.	LIMITS HGTH20N50C1D HGTH20N50E1D MAX.	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1 mA V_{GE} = 0	400	—	500	—	V
Gate Threshold Voltage	$V_{GE}(th)$	V_{GE} = V_{CE} I_C = 1 mA	2	4.5	2	4.5	V
Zero-Gate Voltage Collector Current	I_{CES}	V_{CE} = 400 V	—	250	—	—	μA
		V_{CE} = 500 V	—	—	—	250	μA
		T_C = 125° C V_{CE} = 400 V	—	1000	—	—	μA
		V_{CE} = 500 V	—	—	—	1000	μA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V V_{CE} = 0	—	100	—	100	nA
Collector-Emitter On-Voltage	$V_{CE}(on)$	I_C = 20 A V_{GE} = 10 V	—	2.5	—	2.5	V
		I_C = 35 A V_{GE} = 20 V	—	3.2	—	3.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 10 A V_{CE} = 10 V	—	6 (typ)	—	6 (typ)	V
On-State Gate Charge	$Q_G(on)$	I_C = 10 A V_{CE} = 10 V	—	33(typ)	—	33(typ)	nC
Turn-On Delay Time	$t_d(on)$	I_C = 20 A $V_{CE}(clp)$ = 300 V L = 25 μH T_J = 100° C V_{GE} = 10 V R_g = 25 Ω	—	50	—	50	ns
Rise Time	t_r		—	50	—	50	ns
Turn-Off Delay Time	$t_d(off)$		—	400	—	400	ns
Fall Time	t_{fi}						ns
	40E1D 50E1D		TYP 680	1000	TYP 680	1000	ns
	40C1D 50C1D		TYP 400	500	TYP 400	500	ns
Turn-Off Energy Loss per Cycle (off switching dissipation = E_{off} x frequency)	E_{off}	I_C = 20 A $V_{CE}(clp)$ = 300 V L = 25 μH T_J = 100° C V_{GE} = 10 V R_g = 25 Ω					μJ
	40E1D 50E1D		1810 (typ)				μJ
	40C1D 50C1D		1070 (typ)				μJ
Thermal Resistance Junction-to-Case	$R\theta_{JC}$		—	1.25	—	1.25	°C/W
Diode Forward Voltage	V_{EC}	I_{EC} = 20 A	—	2	—	2	V
Diode Reverse Recovery Time	T_{rr}	I_{EC} = 20 A di/dt = 100 A/μs	—	100	—	100	ns

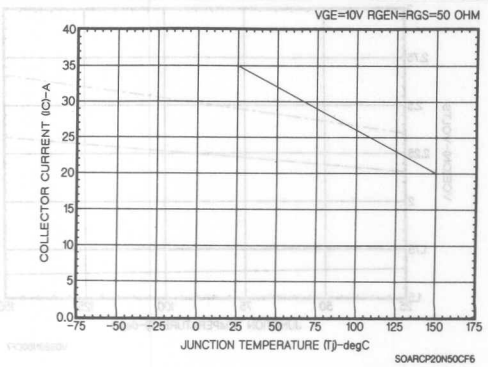


Fig. 1 - Maximum switching current level for all types. Minimum allowable values are R_g = 50 Ω, V_{GE} = 0 V.

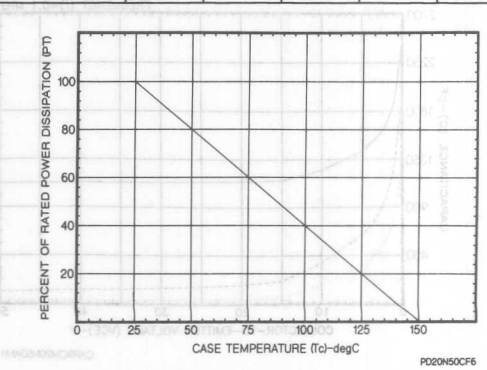


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

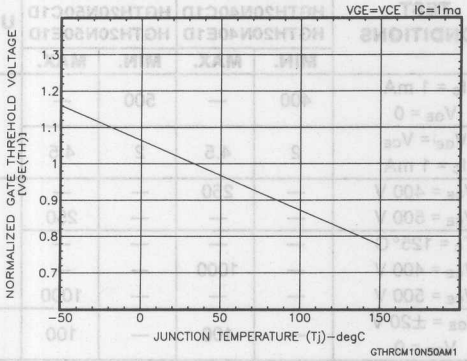


Fig. 3 - Typical normalized gate-threshold voltage as a function of junction temperature for all types.

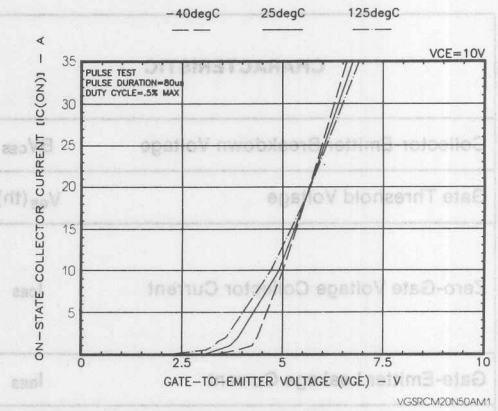


Fig. 4 - Typical transfer characteristics for all types.

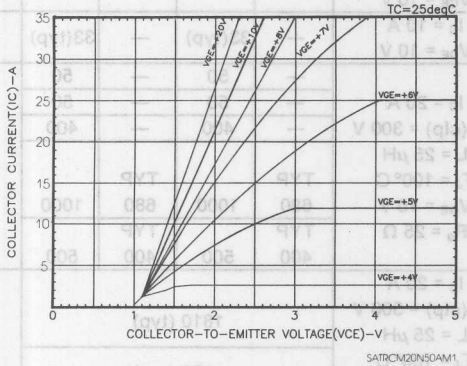


Fig. 5 - Typical saturation characteristics for all types.

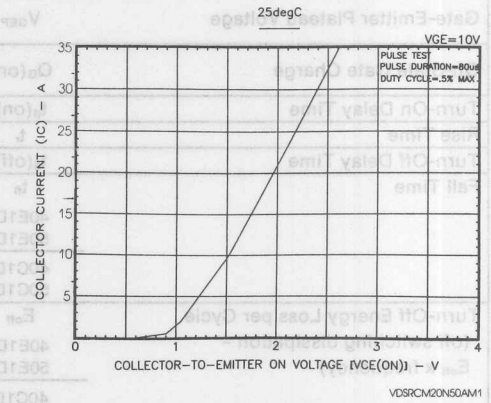


Fig. 6 - Typical collector-to-emitter on-voltage as a function of collector current for all types.

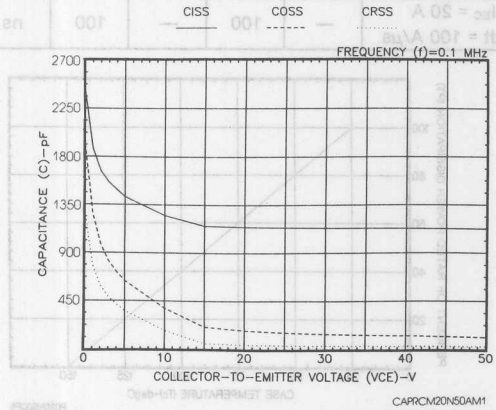


Fig. 7 - Capacitance as a function of collector-to-emitter voltage for all types.

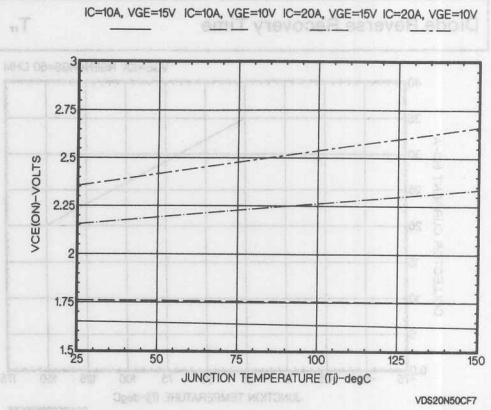


Fig. 8 - Typical $V_{CE}(on)$ vs. temperature for all types.

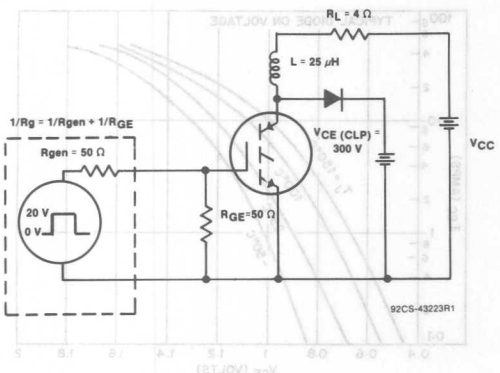


Fig. 9 - Inductive switching test circuit.

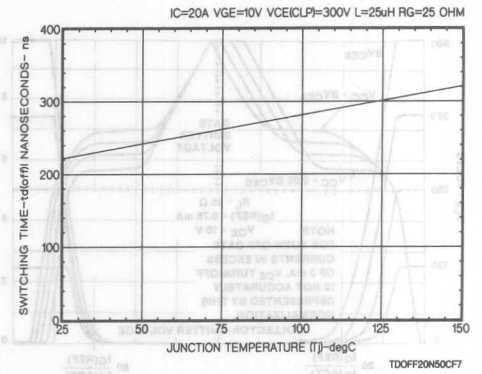


Fig. 10 - Typical turn-off delay time for all types.

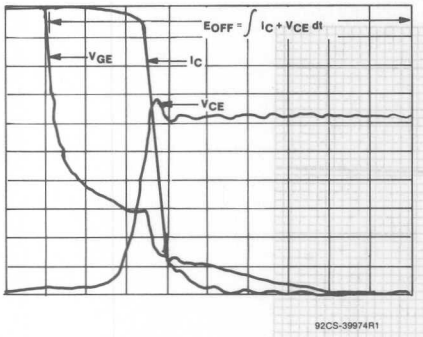


Fig. 11 - Typical inductive switching waveforms.

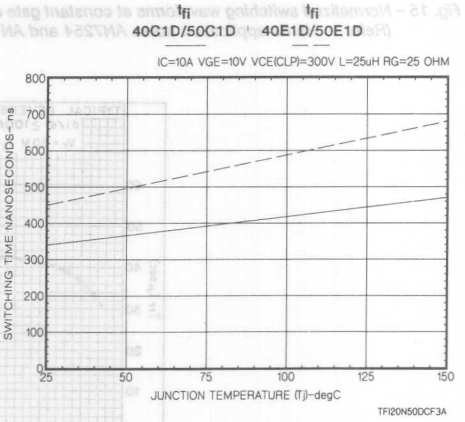


Fig. 12 - Typical fall time for all types (I_C = 10 A).

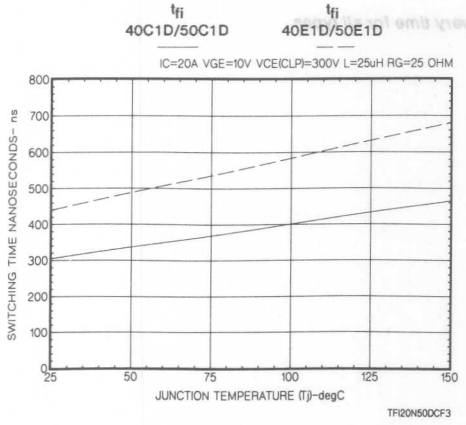


Fig. 13 - Typical fall time for all types (I_C = 20 A).

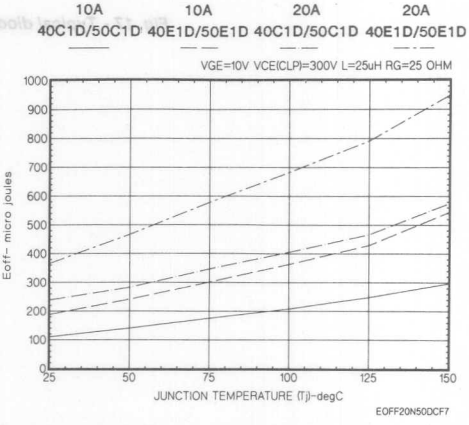


Fig. 14 - Typical clamped inductive turn-off switching loss/cycle.

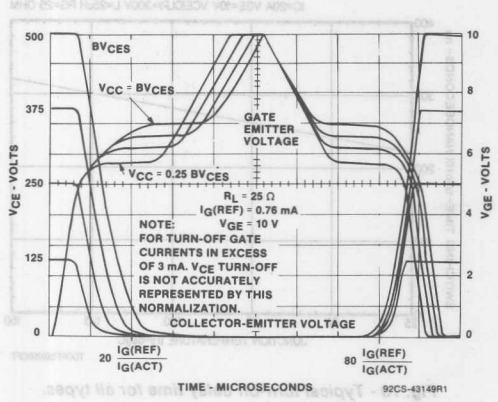


Fig. 15 – Normalized switching waveforms at constant gate current. (Refer to Harris application notes AN7254 and AN7260.)

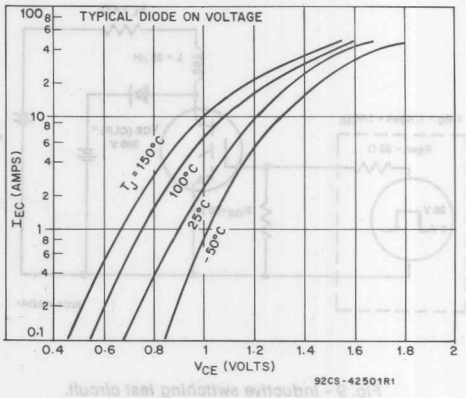


Fig. 16 - Typical diode collector-to-emitter voltage vs. current for all types.

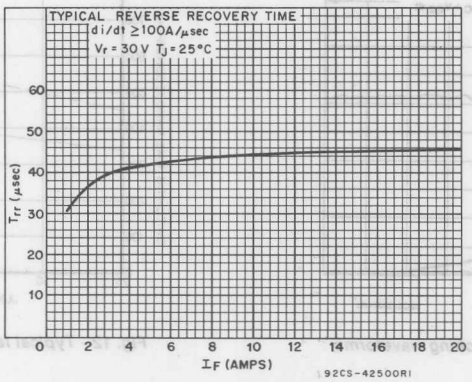


Fig. 17 - Typical diode reverse-recovery time for all types.

HARRIS HGTG20N50C1D

May 1992

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT) with Anti-Parallel Ultra-Fast Diode

Features

- 20 Amp, 500 Volt
- Latch Free Operation
- Typical Fall Time < 500ns
- High Input Impedance
- Low Conduction Loss
- With Anti-Parallel Diode
- t_{rr} < 60ns

Description

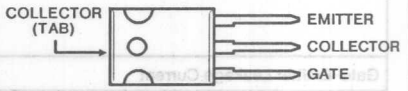
The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C. The diode used in parallel with the IGBT is an ultrafast (t_{rr} < 60ns) with soft recovery characteristic.

IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

This type is supplied in the JEDEC TO-247 package.

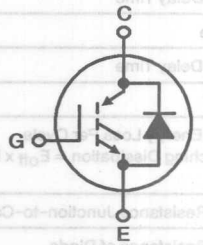
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		HGTG20N50C1D	UNITS
Collector-Emitter Voltage	BV_{CES}	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	500	V
Collector Current Continuous			
@T_C = 25°C	I_{C25}	26	A
@T_C = 90°C	I_{C90}	20	A
Collector Current Pulsed (1)	I_{CM}	35	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Diode Forward Current			
@T_C = 25°C	I_{f25}	26	A
@T_C = 90°C	I_{f90}	20	A
Power Dissipation Total @T_C = 25°C	P_D	75	W
Power Dissipation Derating T_C > 25°C		0.8	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C

(1) (T_J = 150°C, Min. R_{GE} = 25Ω w/o latch)

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2796.1**

Electrical Characteristics At Case Temperature (T_C = 25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS HGTG20N50C1D MIN	LIMITS HGTG20N50C1D MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1mA, V_{GE} = 0	500	-	V
Gate Threshold Voltage	$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 1mA	2	4.5	V
Zero-Gate Voltage Collector Current	I_{CES}	V_{CE} = 500V	-	250	μA
		T_C = 125°C V_{CE} = 500V	- -	- 1000	μA μA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V, V_{CE} = 0	-	100	nA
Collector-Emitter On-Voltage	$V_{CE(SAT)}$	I_C = 20A, V_{GE} = 10V	-	2.5	V
		I_C = 35A, V_{GE} = 20V	-	3.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 10A, V_{CE} = 10V	-	6 (typ)	V
On-State Gate Charge	Q_G(on)	I_C = 10A, V_{CE} = 10V	-	33 (typ)	nC
Turn-On Delay Time	$t_{d(on)i}$	I_C = 20A, V_{CE}(clp) = 300V L = 25μH, T_J = 100°C V_{GE} = 10V, R_g = 25Ω	-	50	ns
Rise Time	t_{ri}		-	50	ns
Turn-Off Delay Time	$t_{d(off)i}$		-	400	ns
Fall Time	t_{fi}		400 (typ)	500	ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = E_{off} x Frequency)	E_{off}	I_C = 20A, V_{CE}(clp) = 300V L = 25μH, T_J = 100°C V_{GE} = 10V, R_g = 25Ω	1070 (typ)		μJ
Thermal Resistance Junction-to-Case (IGBT)	$R\theta_{JC}$		-	1.25	°C/W
Thermal Resistance of Diode	$R\theta_{JC}$		-	1.5	°C/W
Diode Forward Voltage	V_{EC}	I_{EC} = 20A	-	1.8	V
Diode Reverse Recovery Time	t_{rr}	I_{EC} = 20A, di/dt = 100A/μs	-	60	ns

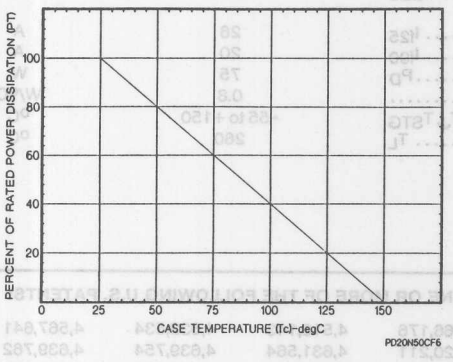


FIGURE 1. POWER DISSIPATION VS. TEMPERATURE DERATING CURVE FOR ALL TYPES.

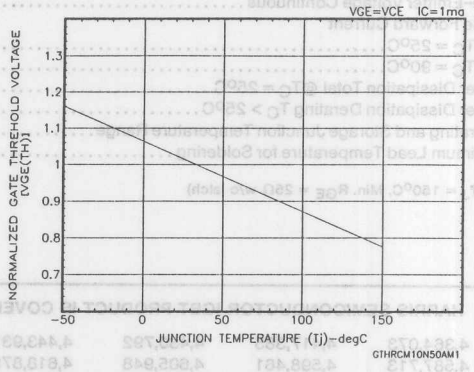


FIGURE 2. TYPICAL NORMALIZED GATE-THRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE FOR ALL TYPES.

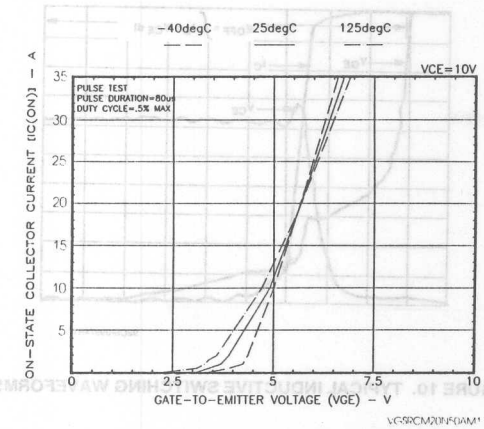


FIGURE 3. TYPICAL TRANSFER CHARACTERISTICS FOR ALL TYPES.

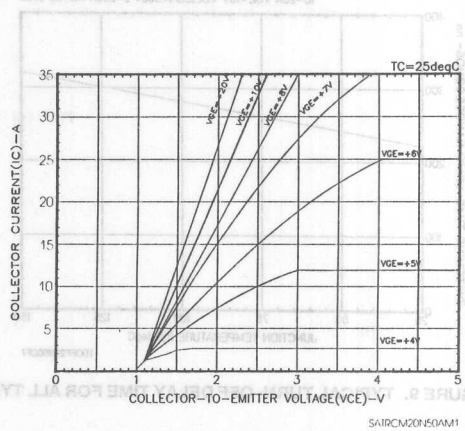


FIGURE 4. TYPICAL SATURATION CHARACTERISTICS FOR ALL TYPES.

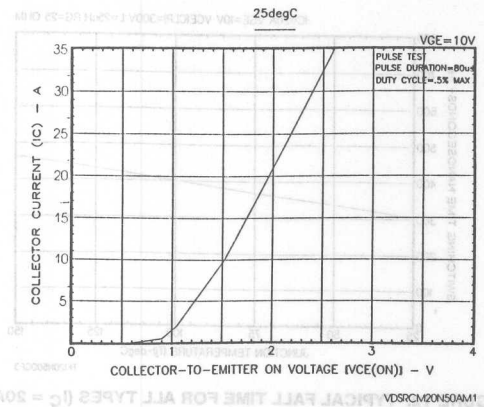


FIGURE 5. TYPICAL COLLECTOR-TO-EMITTER ON-VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT FOR ALL TYPES.

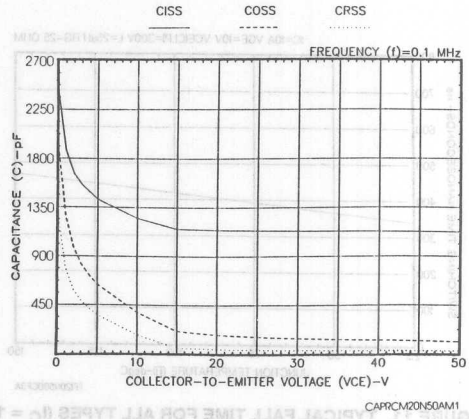


FIGURE 6. CAPACITANCE AS A FUNCTION OF COLLECTOR-TO-EMITTER VOLTAGE FOR ALL TYPES.

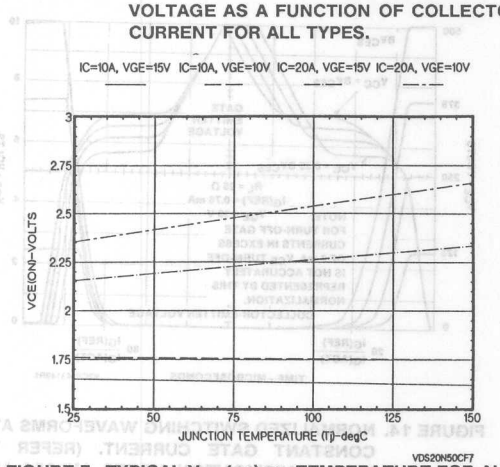


FIGURE 7. TYPICAL $V_{CE}(on)$ vs. TEMPERATURE FOR ALL TYPES.

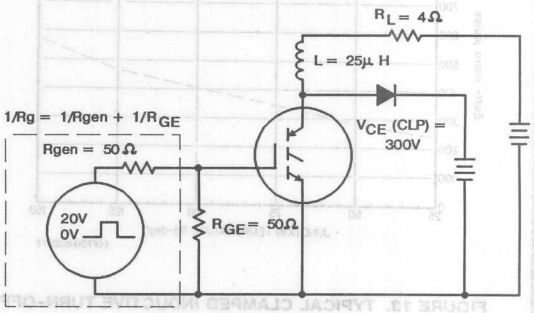


FIGURE 8. INDUCTIVE SWITCHING TEST CIRCUIT.

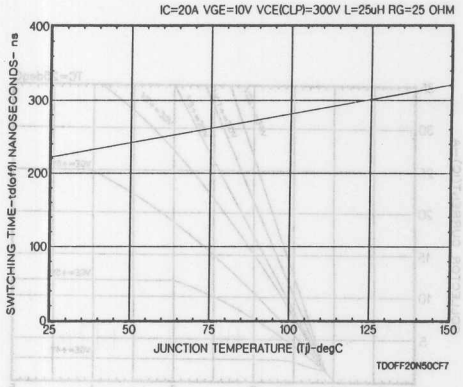


FIGURE 9. TYPICAL TURN-OFF DELAY TIME FOR ALL TYPES

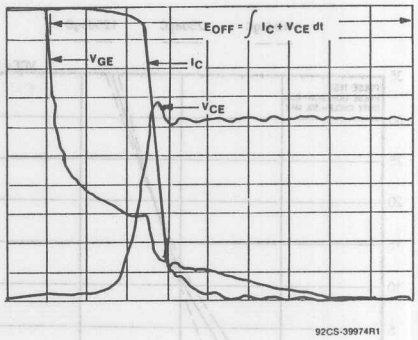


FIGURE 10. TYPICAL INDUCTIVE SWITCHING WAVEFORMS.

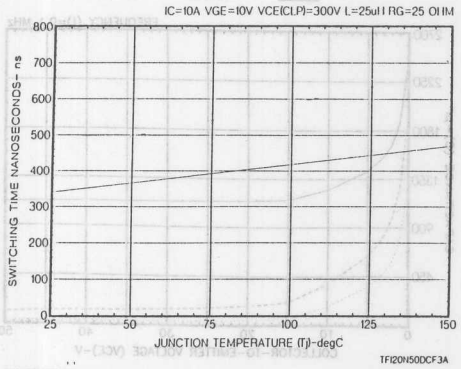


FIGURE 11. TYPICAL FALL TIME FOR ALL TYPES (I_C = 10A).

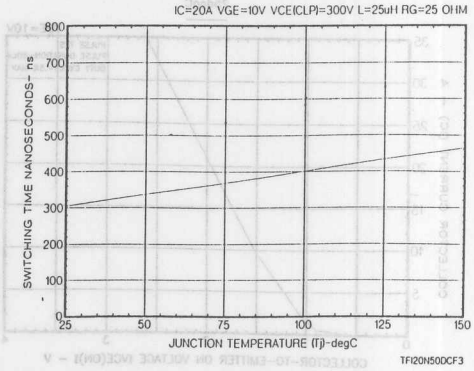


FIGURE 12. TYPICAL FALL TIME FOR ALL TYPES (I_C = 20A).

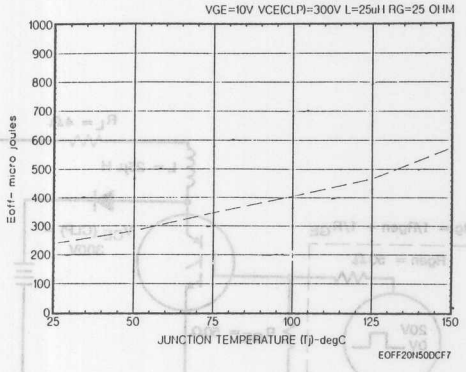


FIGURE 13. TYPICAL CLAMPED INDUCTIVE TURN-OFF SWITCHING LOSS/CYCLE

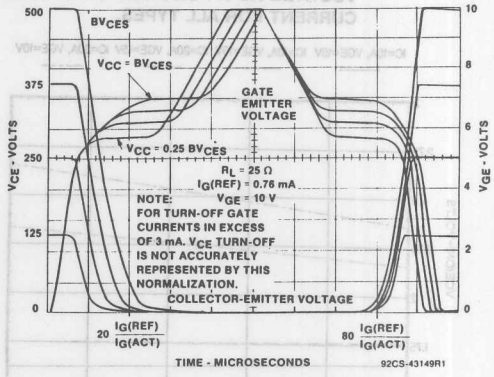


FIGURE 14. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260.)

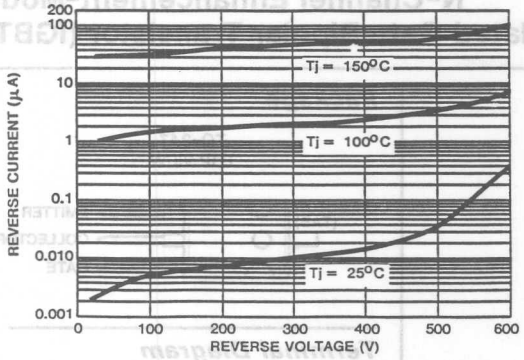


FIGURE 15. TYPICAL DIODE REVERSE VOLTAGE vs. REVERSE CURRENT.

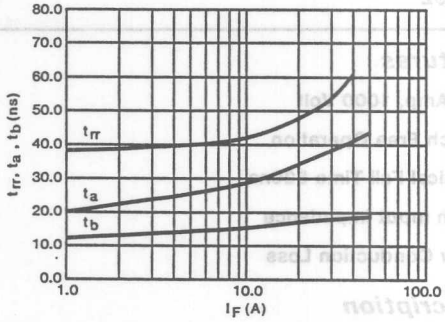


FIGURE 16. TYPICAL t_{rr}, t_a, t_b vs. FORWARD CURRENT.

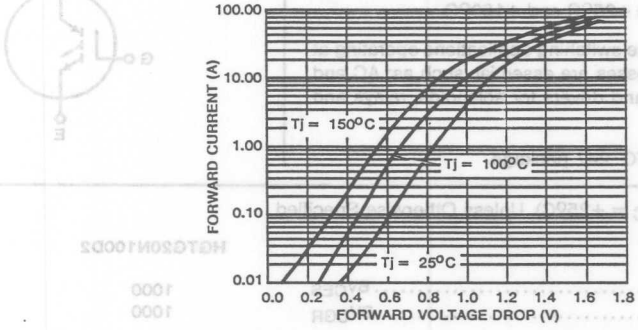


FIGURE 17. FORWARD VOLTAGE vs. FORWARD CURRENT CHARACTERISTIC.

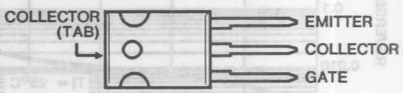
Insulated Gate Bipolar Transistor (IGBT)

Features

- 34 Amp, 1000 Volt
- Latch Free Operation
- Typical Fall Time 520ns
- High Input Impedance
- Low Conduction Loss

Package

TO-247
TOP VIEW



Description

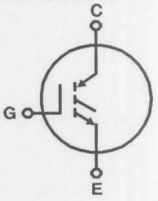
The HGTG20N100D2 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

IGBTs are ideal for many high voltaage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

This type is supplied in the JEDEC TO-247 package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		HGTG20N100D2	UNITS
Collector-Emitter Voltage	BV_{CES}	1000	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	1000	V
Collector Current Continuous			
@ T_C = +25°	I_{C25}	34	A
@ T_C = +90°	I_{C90}	20	A
Collector Current Pulsed (1)	I_{CM}	100	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at T_J = +150°C	SSOA	100A @ 0.8BV_{CES}	-
Power Dissipation Total @ T_C = +25°C	P_D	150	W
Power Dissipation Derating T_C > +25°C		1.20	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.125" from case for 5 seconds)	T_L	260	°C
Short Circuit Withstand Time(2)	t_{SC}		
@V_{GE} = 15V		3	µs
@V_{GE} = 10V		15	µs

(1) Repetitive Rating: Pulse width limited by maximum junction temperature.

(2) $V_{CE(pk)}$ = 600V, T_C = 125°C, R_{GE} = 25Ω

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2826.1**

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250μA, V_{GE} = 0V		1000	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	V_{CE} = BV_{CES}	T_C = +25°C	-	-	250	μA
		V_{CE} = 0.8 BV_{CES}	T_C = +125°C	-	-	1.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C90}, V_{GE} = 15V	T_C = +25°C	-	3.1	3.8	V
			T_C = +125°C	-	2.9	3.6	V
		I_C = I_{C90}, V_{GE} = 10V	T_C = +25°C	-	3.3	4.1	V
			T_C = +125°C	-	3.2	4.0	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 500μA, V_{CE} = V_{GE}	T_C = +25°C	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±250	nA
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}		-	7.1	-	V
On-State Gate Charge	$Q_{G(on)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	-	120	160	nC
			V_{GE} = 20V	-	163	212	nC
Current Turn-On Delay Time	$t_{d(on)i}$	L = 50μH, I_C = I_{C90}, R_g = 25Ω, V_{GE} = 15V, T_J = 125°C, V_{CE} = 0.8 BV_{CES}		-	100	-	ns
Current Rise Time	t_{ri}			-	150	-	ns
Current Turn-Off Delay Time	$t_{d(off)i}$			-	500	650	ns
Current Fall Time	t_{fi}			-	520	680	ns
Turn-Off Energy(1)	W_{off}			-	3.7	-	mJ
Current Turn-On Delay Time	$t_{d(on)i}$	L = 50μH, I_C = I_{C90}, R_g = 25Ω, V_{GE} = 10V, T_J = 125°C, V_{CE} = 0.8 BV_{CES}		-	100	-	ns
Current Rise Time	t_{ri}			-	150	-	ns
Current Turn-Off	$t_{d(off)i}$			-	410	530	ns
Current Fall Time	t_{fi}			-	520	680	ns
Turn-Off Energy(1)	W_{off}			-	3.7	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	.7	.83	°C/W

(1) Turn-off Energy Loss (W_{off}) is defined as the integral of the instantaneous power loss starting at the trailing idge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A) The HGTG20N100D2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

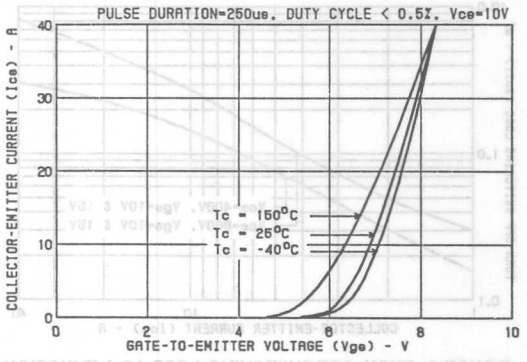


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

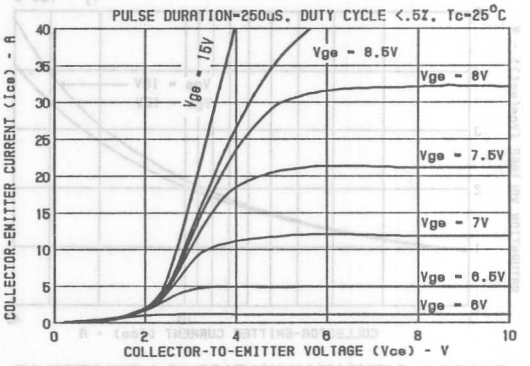


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

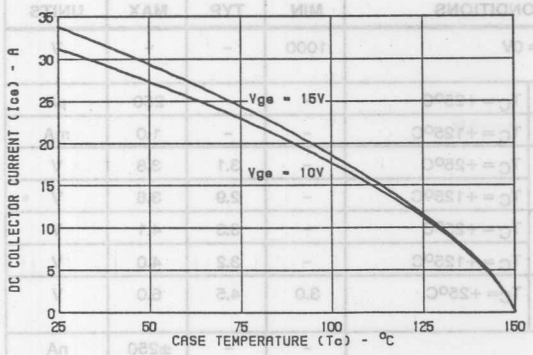


FIGURE 3. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

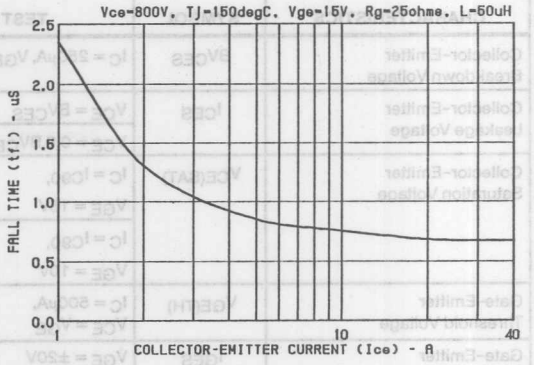


FIGURE 4. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

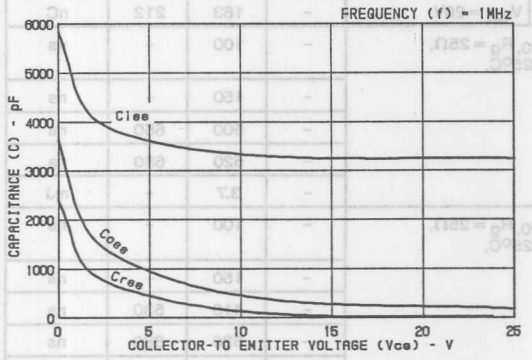


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

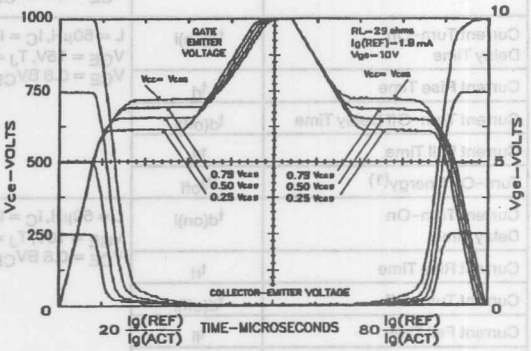


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260.)

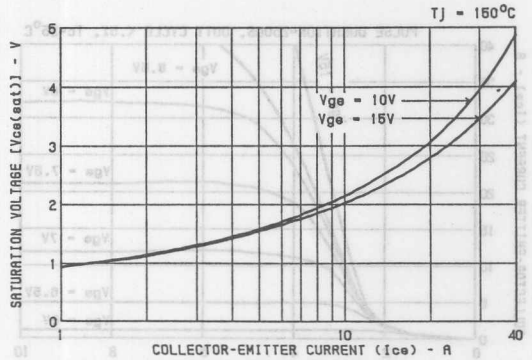


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

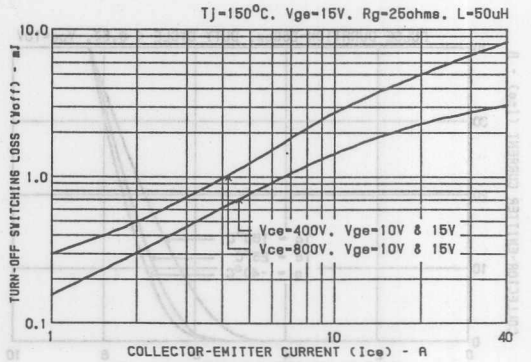


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

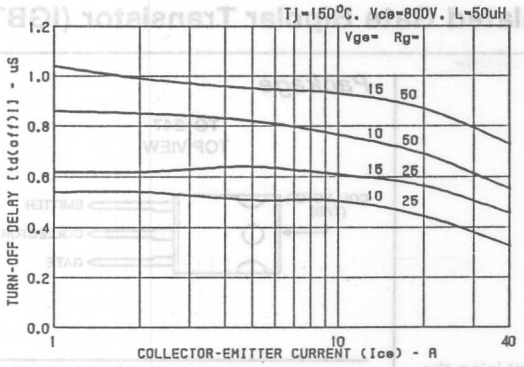


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMMITER CURRENT.

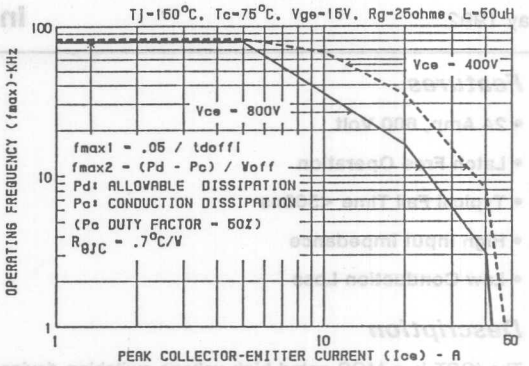


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE.

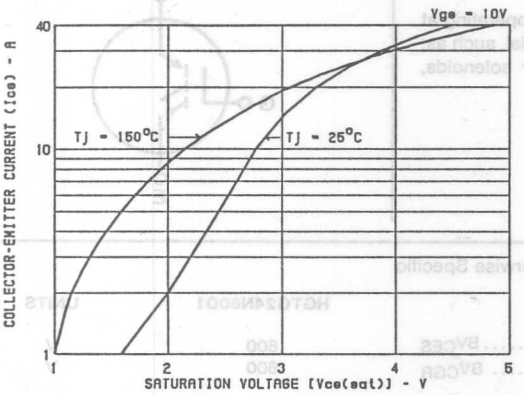


FIGURE 11. COLLECTOR-EMITTER SATURATION VOLT.

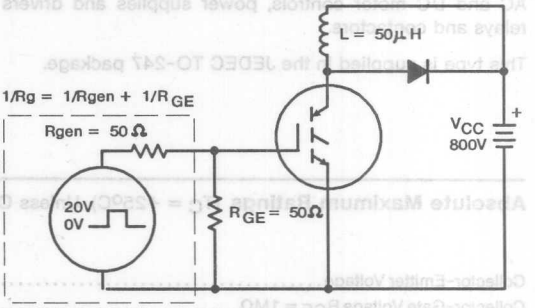


FIGURE 12. INDUCTION SWITCHING TEST CIRCUIT.

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{max1} or f_{max2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temeprature.

f_{max1} is defined by $f_{max1} = 0.05/t_{d(off)i}$. $t_{d(off)i}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(off)i}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(off)i}$ is important when controlling output ripple under a lightly loaded condition.

f_{max2} is defined by $f_{max2} = (P_D - P_C)/W_{off}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} \times I_{CE})/2$. W_{off} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} - 0A).

The switching power loss (Figure 10) is defined as $f_{max1} \times W_{off}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS

HGTG24N60D1

May 1992

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)

Features

- 24 Amp, 600 Volt
- Latch Free Operation
- Typical Fall Time <500ns
- High Input Impedance
- Low Conduction Loss

Description

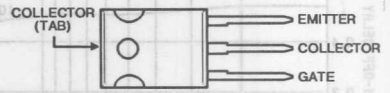
The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

IGBTs are ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

This type is supplied in the JEDEC TO-247 package.

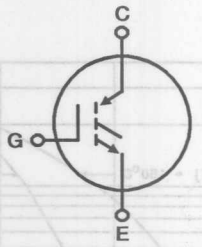
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specific

		HGTG24N60D1	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	600	V
Collector Current Continuous			
@ T_C = +25°	I_{C25}	40	A
@ V_{GE} = 15V @ T_C = +90°	I_{C90}	24	A
Collector Current Pulsed(1)	I_{CM}	96	A
Gate-Emitter Voltage Continuous	V_{GES}	±25	V
Switching Safe Operating Area at T_J = +150°C	SSOA	60A @ 0.8BV_{CES}	-
Power Dissipation Total @ T_C = +25°C	P_D	125	W
Power Dissipation Derating T_C > +25°C		1.0	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.125" from case for 5 seconds)	T_L	260	°C

(1) Repetitive Rating: Pulse width limited by maximum junction temperature.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2831.1**

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250μA, V_{GE} = 0V		600	–	–	V
Collector-Emitter Leakage Voltage	I_{CES}	V_{CE} = BV_{CES}	T_C = +25°C	–	–	1.0	mA
		V_{CE} = 0.8 BV_{CES}	T_C = +125°C	–	–	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C90}, V_{GE} = 15V	T_C = +25°C	–	1.7	2.3	V
			T_C = +125°C	–	1.9	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}	T_C = +25°C	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		–	–	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}		–	6.3	–	V
On-State Gate Charge	$Q_{G(on)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	–	120	155	nC
			V_{GE} = 20V	–	155	200	nC
Current Turn-On Delay Time	$t_{d(on)i}$	L = 500μH, I_C = I_{C90}, R_g = 25Ω, V_{GE} = 15V, T_J = 150°C, V_{CE} = 0.8 BV_{CES}		–	100	–	ns
Current Rise Time	t_{ri}			–	150	–	ns
Current Turn-Off Delay Time	$t_{d(off)i}$			–	700	900	ns
Current Fall Time	t_{fi}			–	450	600	ns
Turn-Off Energy(1)	W_{off}			–	4.3	–	mJ
Thermal Resistance	$R_{\theta JC}$			–	–	1.00	°C/W

(1) Turn-off Energy Loss (W_{off}) is defined as the integral of the instantaneous power loss starting at the trailing idge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A) The HGTG24N60D1 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

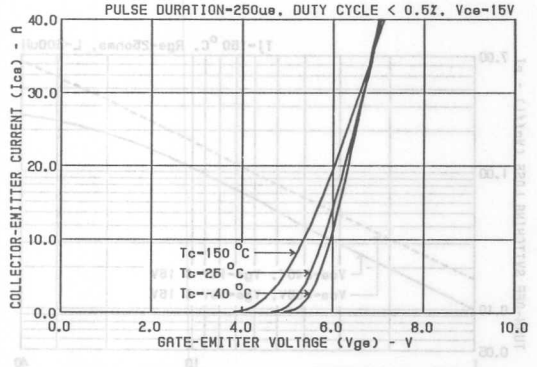


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

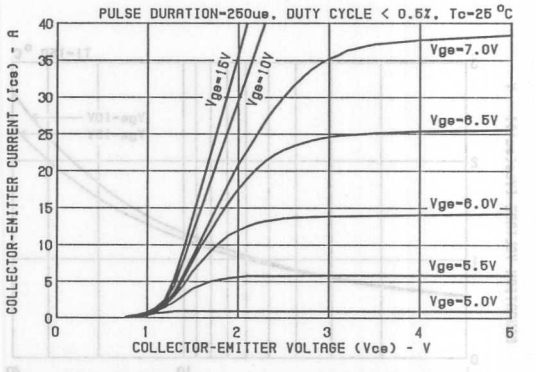


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

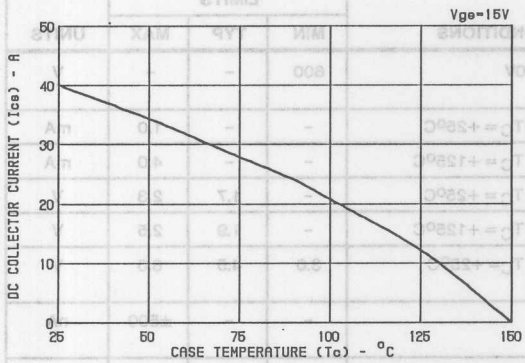


FIGURE 3. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

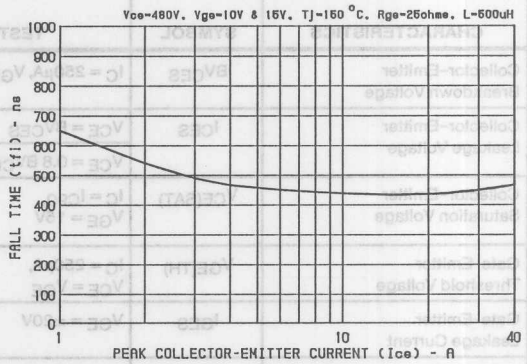


FIGURE 4. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

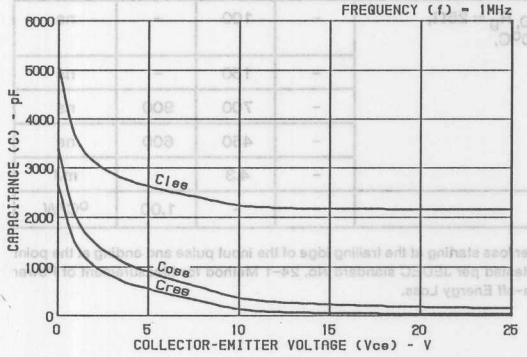


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

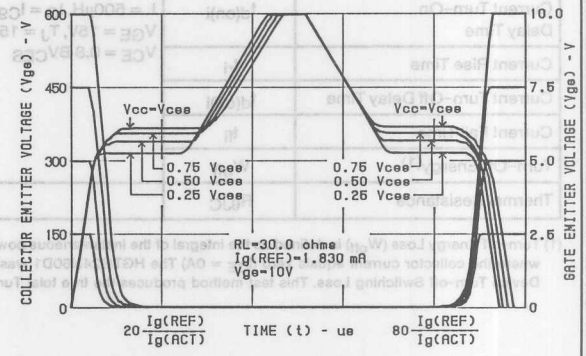


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260.)

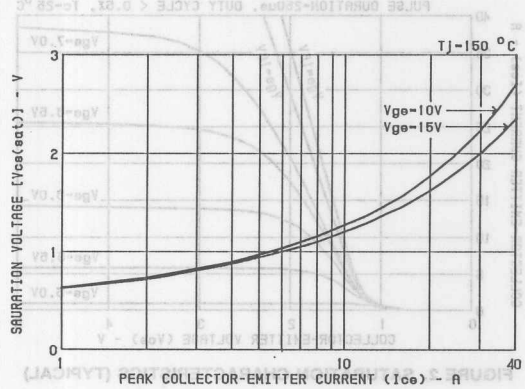


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

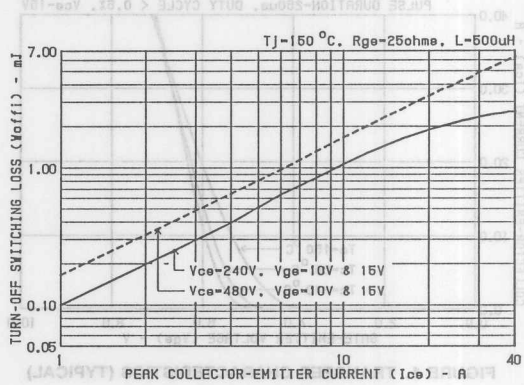


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

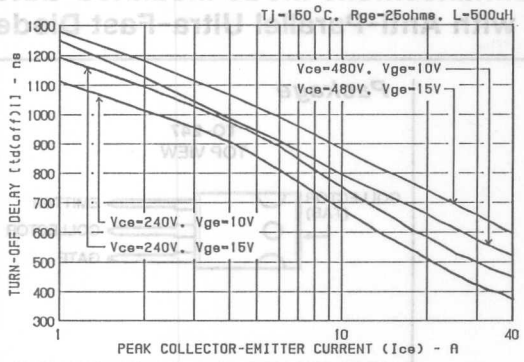


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMMITER CURRENT

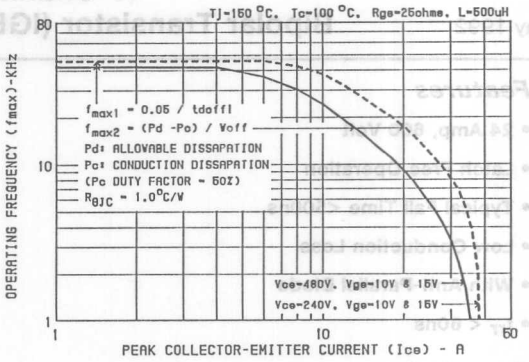


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{max1} or f_{max2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temeprature.

f_{max1} is defined by $f_{max1} = 0.05/t_{d(off)i}$. $t_{d(off)i}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(off)i}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(off)i}$ is important when controlling output ripple under a lightly loaded condition.

f_{max2} is defined by $f_{max2} = (P_D - P_C)/W_{off}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} \times I_{CE})/2$. W_{off} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A).

The switching power loss (Figure 10) is defined as $f_{max1} \times W_{off}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS HGTG24N60D1D

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT) with Anti-Parallel Ultra-Fast Diode

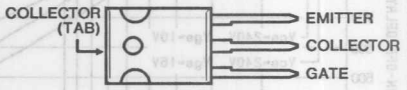
May 1992

Features

- 24 Amp, 600 Volt
- Latch Free Operation
- Typical Fall Time <500ns
- Low Conduction Loss
- With Anti-Parallel Diode
- t_{rr} < 60ns

Package

TO-247
TOP VIEW



Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C. The diode used in parallel with the IGBT is an ultrafast (t_{rr} < 60ns) with soft recovery characteristic.

The IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

This type is supplied in the JEDEC TO-247 package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specific

		HGTG24N60D1D	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	600	V
Collector Current Continuous			
@ T_C = +25°	I_{C25}	40	A
@ T_C = +90°	I_{C90}	24	A
Collector Current Pulsed(1)	I_{CM}	96	A
Gate-Emitter Voltage Continuous	V_{GES}	±25	V
Switching Safe Operating Area at T_J = +150°C	SSOA	60A @ 0.8BV_{CES}	-
Diode Forward Current			
@ T_C = +25°	I_{f25}	40	A
@ T_C = +90°	I_{f90}	24	A
Power Dissipation Total @ T_C = +25°C	P_D	125	W
Power Dissipation Derating T_C > +25°C		1.0	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.125" from case for 5 seconds)	T_L	260	°C

(1) Repetitive Rating: Pulse width limited by maximum junction temperature.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2797.1**

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 280μA, V_{GE} = 0V		600	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	V_{CE} = BV_{CES}	T_C = +25°C	-	-	280	μA
		V_{CE} = 0.8 BV_{CES}	T_C = +125°C	-	-	5.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C90}, V_{GE} = 15V	T_C = +25°C	-	1.7	2.3	V
			T_C = +125°C	-	1.9	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}	T_C= +25°C	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}		-	6.3	-	V
On-State Gate Charge	$Q_{G(on)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	-	120	155	nC
			V_{GE} = 20V	-	155	200	nC
Current Turn-On Delay Time	$t_{d(on)i}$	L = 500μH, I_C = I_{C90}, R_g = 25Ω, V_{GE} = 15V, T_J = 150°C, V_{CE} = 0.8 BV_{CES}		-	100	-	ns
Current Rise Time	t_{ri}			-	150	-	ns
Current Turn-Off	$t_{d(off)i}$			-	700	900	ns
Current Fall Time	t_{fi}			-	450	600	ns
Turn-Off Energy(1)	W_{off}			-	4.3	-	mJ
Thermal Resistance (FG BT)	$R_{\theta JC}$			-	-	1.00	°C/W
Thermal Resistance Diode	$R_{\theta JC}$			-	-	1.5	°C/W
Diode Forward Voltage	V_{EC}	I_{EC} = 24A		-	-	1.50	V
Diode Reverse Recovery Time	t_{rr}	I_{EC} = 24A, di/dt = 100A/μs		-	-	60	ns

(1) Turn-off Energy Loss (W_{off}) is defined as the integral of the instantaneous power loss starting at the trailing idge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A) The HGTG24N60D1D was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

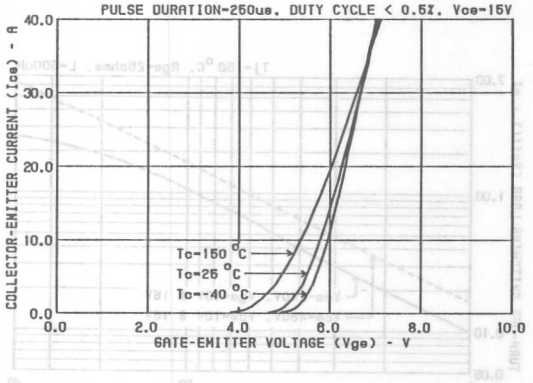


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

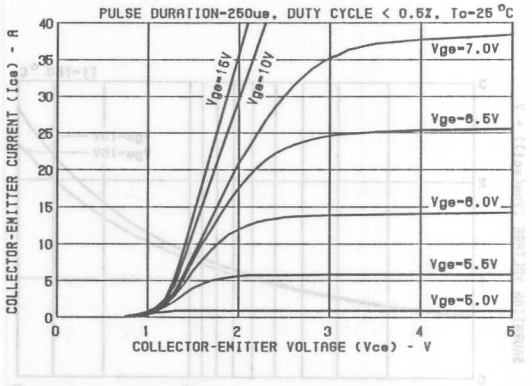


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

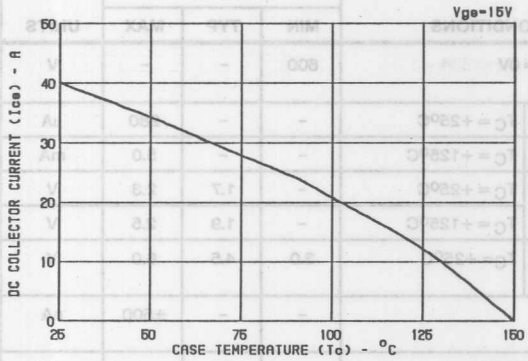


FIGURE 3. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

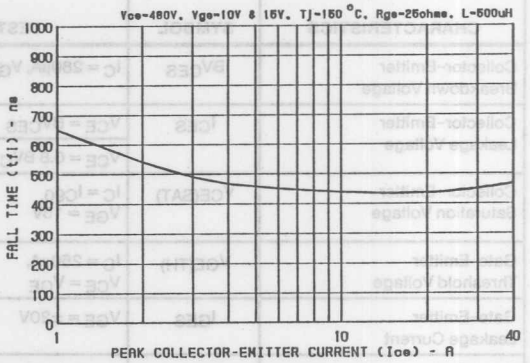


FIGURE 4. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

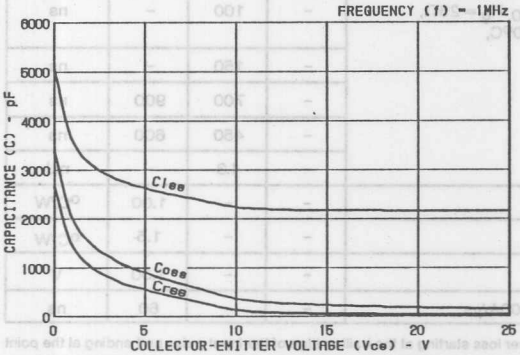


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

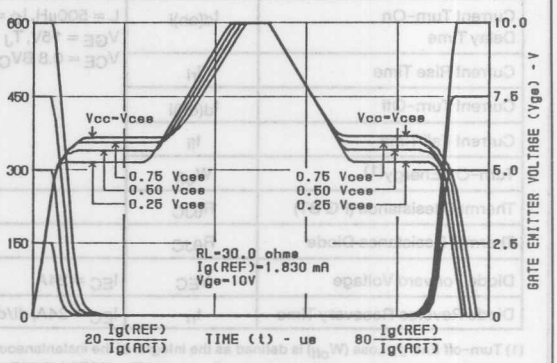


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260.)

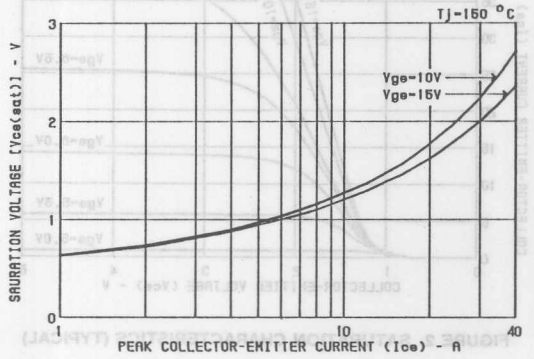


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

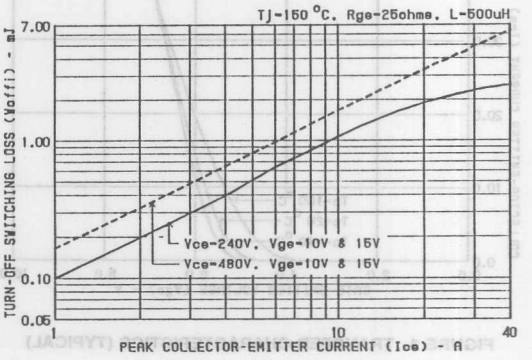


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

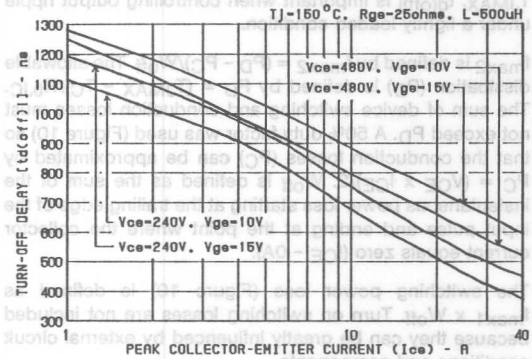


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMMITER CURRENT.

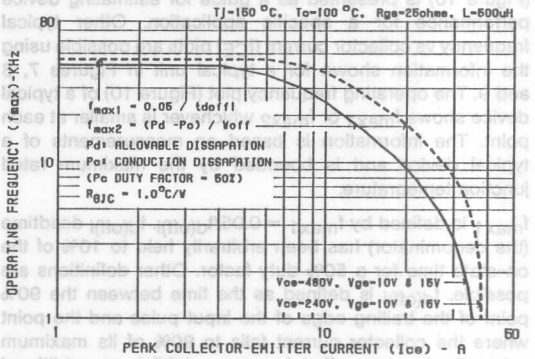


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE.

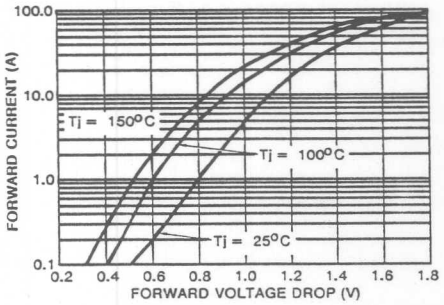


FIGURE 11. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC.

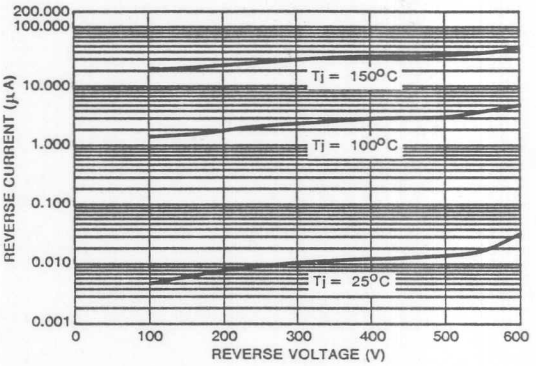


FIGURE 12. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC.

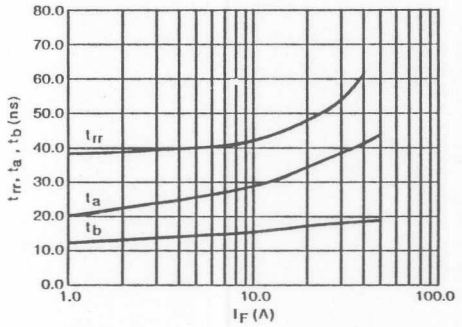


FIGURE 13. TYPICAL t_{rr}, t_a, t_b vs FORWARD CURRENT

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{max1} or f_{max2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temeprature.

f_{max1} is defined by $f_{max1} = 0.05/t_{d(off)i}$. $t_{d(off)i}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(off)i}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(off)i}$ is important when controlling output ripple under a lightly loaded condition.

f_{max2} is defined by $f_{max2} = (P_D - P_C)/W_{off}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} \times I_{CE})/2$. W_{off} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} - 0A).

The switching power loss (Figure 10) is defined as $f_{max1} \times W_{off}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS HGTM24N60D1

May 1992

N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)

Features

- 24 Amp, 600 Volt
- Latch Free Operation
- Typical Fall Time <500ns
- High Input Impedance
- Low Conduction Loss

Description

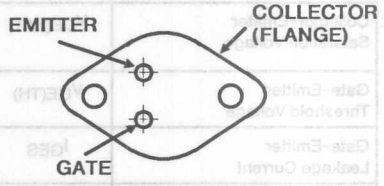
The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

IGBTs are ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

This type is supplied in the JEDEC TO-204AA package.

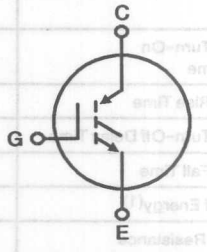
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specific

	HGTG24N60D1	UNITS
Collector-Emitter Voltage ..... BV_{CES}	600	V
Collector-Gate Voltage R_{GE} = 1MΩ ..... BV_{CGR}	600	V
Collector Current Continuous		
@ T_C = +25° ..... I_{C25}	40	A
@ V_{GE} = 15V @ T_C = +90° ..... I_{C90}	24	A
Collector Current Pulsed(1) ..... I_{CM}	96	A
Gate-Emitter Voltage Continuous ..... V_{GES}	±25	V
Switching Safe Operating Area at T_J = +150°C ..... SSOA	60A @ 0.8BV_{CES}	-
Power Dissipation Total @ T_C = +25°C ..... P_D	125	W
Power Dissipation Derating T_C > +25°C	1.0	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L	260	°C
(0.125" from case for 5 seconds)		

(1) Repetitive Rating: Pulse width limited by maximum junction temperature.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2832.1**

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250μA, V_{GE} = 0V		600	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	V_{CE} = BV_{CES}	T_C = +25°C	-	-	1.0	mA
		V_{CE} = 0.8 BV_{CES}	T_C = +125°C	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C90}, V_{GE} = 15V	T_C = +25°C	-	1.7	2.3	V
			T_C = +125°C	-	1.9	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}	T_C = +25°C	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}		-	6.3	-	V
On-State Gate Charge	$Q_{G(on)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	-	120	155	nC
			V_{GE} = 20V	-	155	200	nC
Current Turn-On Delay Time	$t_{d(on)i}$	L = 500μH, I_C = I_{C90}, R_g = 25Ω, V_{GE} = 15V, T_J = 150°C, V_{CE} = 0.8 BV_{CES}		-	100	-	ns
Current Rise Time	t_{ri}			-	150	-	ns
Current Turn-Off Delay Time	$t_{d(off)i}$			-	700	900	ns
Current Fall Time	t_{fi}			-	450	600	ns
Turn-Off Energy(1)	W_{off}			-	4.3	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	-	1.00	°C/W

(1) Turn-off Energy Loss (W_{off}) is defined as the integral of the instantaneous power loss starting at the trailing idge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A) The HGTM24N60D1 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

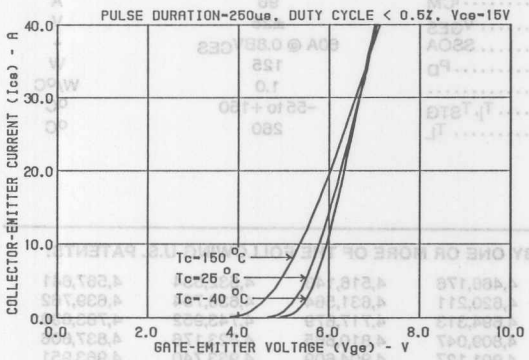


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

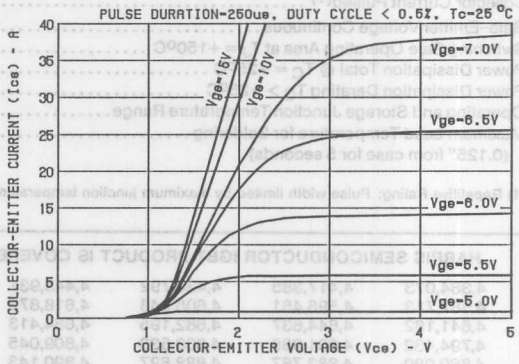


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

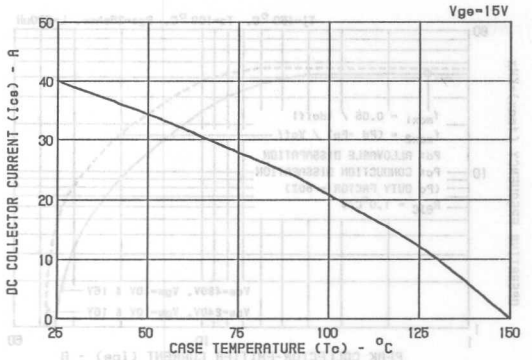


FIGURE 3. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

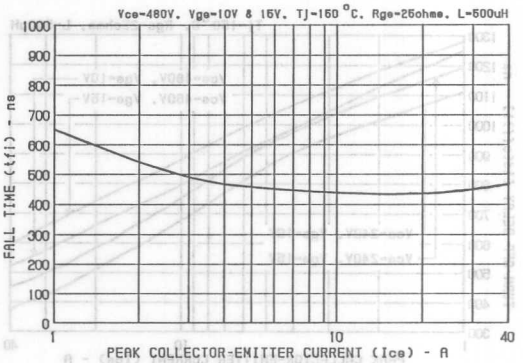


FIGURE 4. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

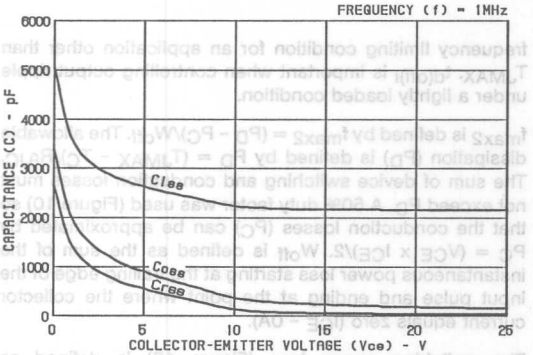


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

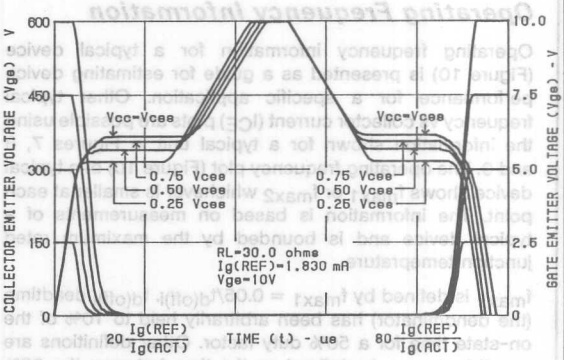


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260.)

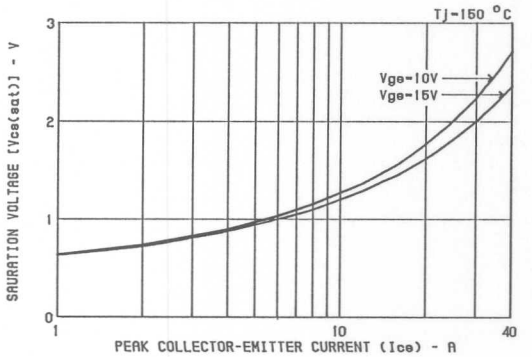


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

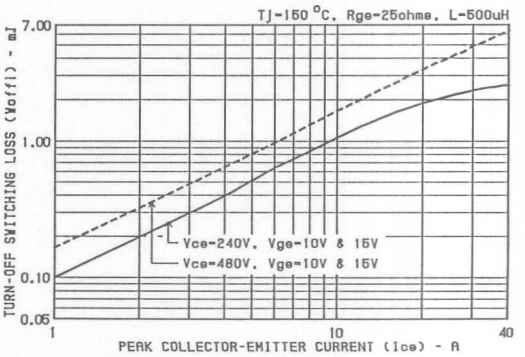


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

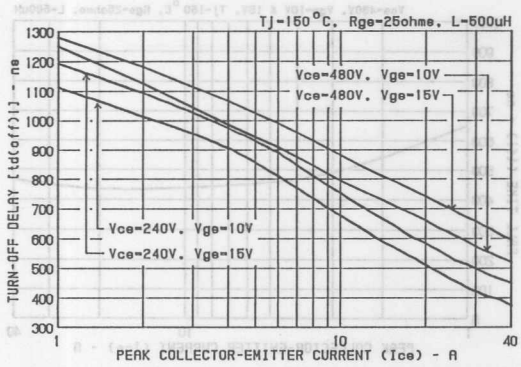


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMMITER CURRENT

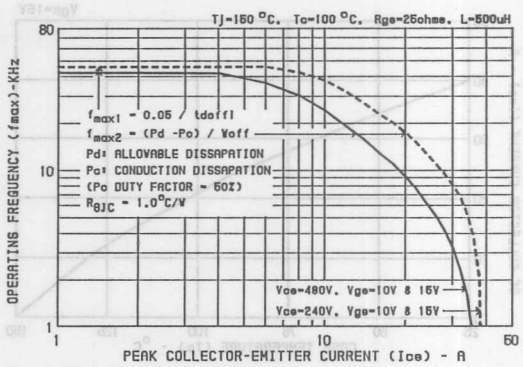


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{max1} or f_{max2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temeprature.

f_{max1} is defined by $f_{max1} = 0.05/t_{d(off)i}$. $t_{d(off)i}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(off)i}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(off)i}$ is important when controlling output ripple under a lightly loaded condition.

f_{max2} is defined by $f_{max2} = (P_D - P_C)/W_{off}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} \times I_{CE})/2$. W_{off} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} - 0A).

The switching power loss (Figure 10) is defined as $f_{max1} \times W_{off}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS HGTA32N60E2

May 1992

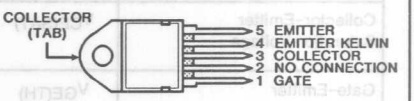
N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)

Features

- 50 Amp, 600 Volt
- Latch Free Operation
- Typical Fall Time - 620ns
- High Input Impedance
- Low Conduction Loss

Package

MO-093 (5 LEAD)
TOP VIEW



Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C.

IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

This type is supplied in the JEDEC TO-218 (5-lead) package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		HGTA32N60E2	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage R_{GE} = 1MΩ	V_{CGR}	600	V
Collector Current Continuous			
@T_C = 25°C	I_{C25}	50	A
@V_{ge} = 15V, @T_C = 90°C	I_{C90}	32	A
Collector Current Pulsed (1)	I_{CM}	200	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area T_J = +150°C	SSOA	200A @ 0.8 BV_{CES}	-
Power Dissipation Total @T_C = 25°C	P_D	208	W
Power Dissipation Derating T_C > 25°C		1.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (2)			
@V_{ge} = 15V	t_{sc}	3	µS
@V_{ge} = 10V	t_{sc}	15	µS

(1) Repetitive Rating: Pulse width limited by maximum junction temperature.

(2) V_{CE} (pk) = 360V, T_C = 125°C, R_{ge} = 25Ω

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2833.1

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	250	μA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +125^oC$	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C90}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	2.4	2.9	V
			$T_C = +125^oC$	-	2.4	3.0	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 1mA$, $V_{CE} = V_{GE}$	$T_C = +25^oC$	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±500	nA
Gate-Emitter Plateau Voltage	$V_{GE(pl)}$	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$		-	6.5	-	V
On-State Gate Charge	$Q_{G(on)}$	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	200	260	nC
			$V_{GE} = 20V$	-	265	345	nC
Current Turn-On Delay Time	$t_{d(on)i}$	$L = 500\mu H$, $I_C = I_{C90}$, $R_g = 25\Omega$, $V_{GE} = 15V$, $T_J = 125^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{ri}			-	150	-	ns
Current Turn-Off Delay Time	$t_{d(off)i}$			-	630	820	ns
Current Fall Time	t_{fi}			-	620	800	ns
Turn-Off Energy(1)	W_{off}			-	3.5	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.5	0.6	$^oC/W$

(1) Turn-off Energy Loss (W_{off}) is defined as the integral of the instantaneous power loss starting at the trailing idge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A) The HGTA32N60E2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

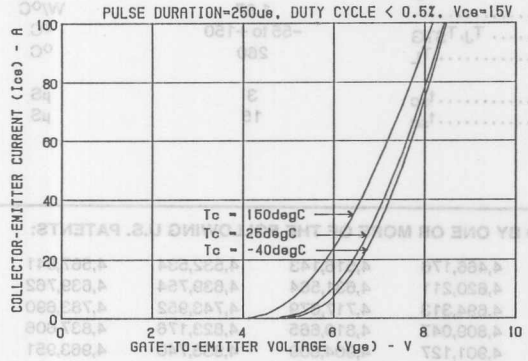


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

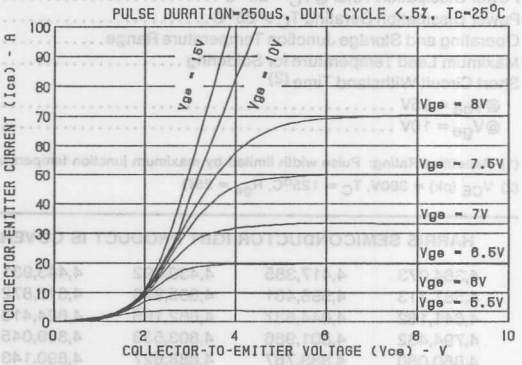


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

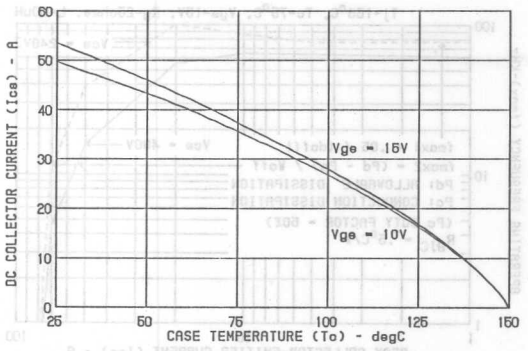


FIGURE 3. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

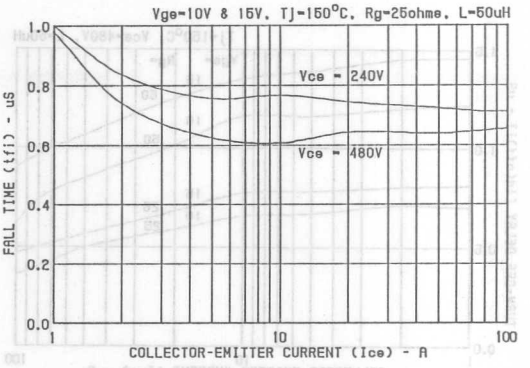


FIGURE 4. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

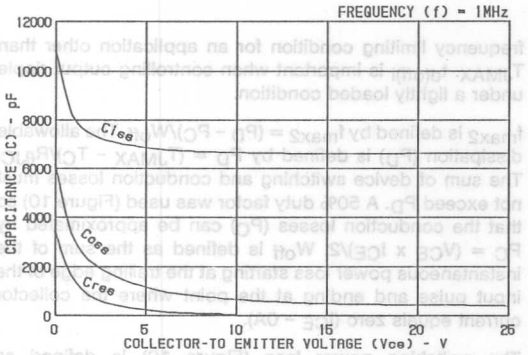


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

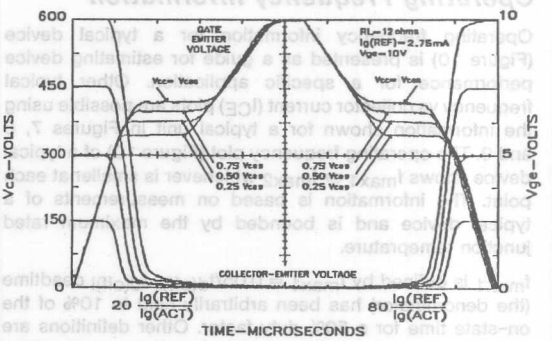


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260).

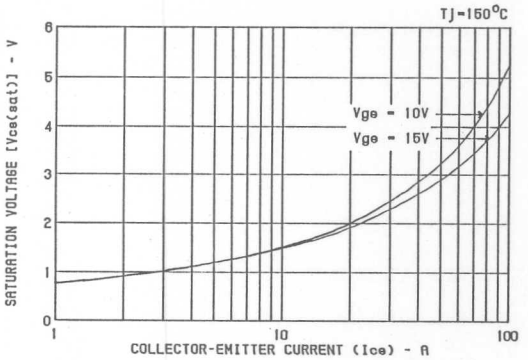


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

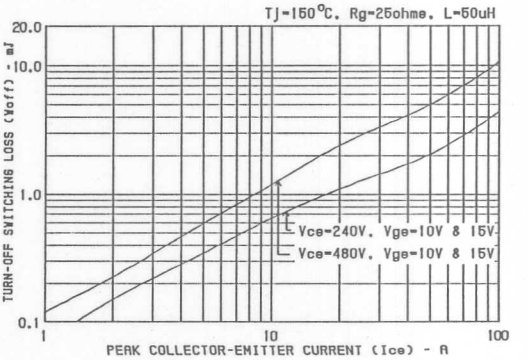


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

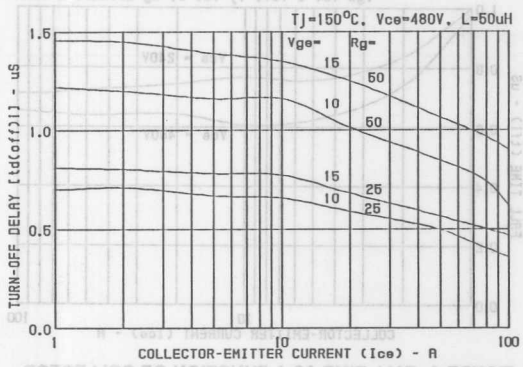


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMMITER CURRENT

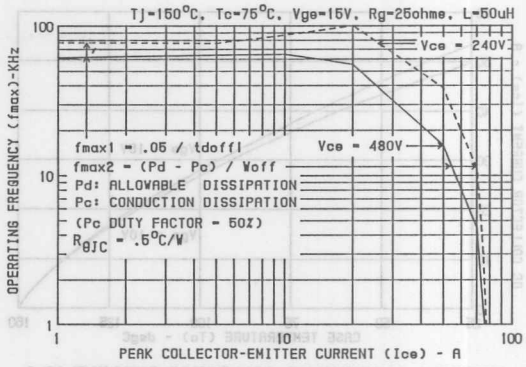


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{max1} or f_{max2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temeprature.

f_{max1} is defined by $f_{max1} = 0.05/t_{d(off)i}$. $t_{d(off)i}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(off)i}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(off)i}$ is important when controlling output ripple under a lightly loaded condition.

f_{max2} is defined by $f_{max2} = (P_D - P_C)/W_{off}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} \times I_{CE})/2$. W_{off} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A).

The switching power loss (Figure 10) is defined as $f_{max1} \times W_{off}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS HGTG32N60E2

May 1992

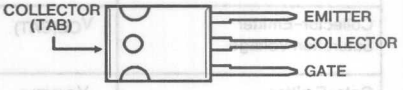
N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)

Features

- 50 Amp, 600 Volt
- Latch Free Operation
- Typical Fall Time - 600ns
- High Input Impedance
- Low Conduction Loss

Package

TO-247
TOP VIEW



Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C.

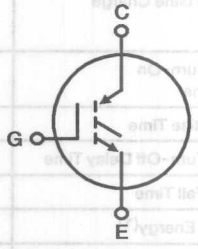
IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

This device incorporates generation two design techniques which yield improved peak current capability and larger short circuit withstand capability than previous designs.

This type is supplied in the JEDEC TO-247 package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		HGTG32N60E2	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage R_{GE} = 1MΩ	V_{CGR}	600	V
Collector Current Continuous			
@T_C = 25°C	I_{C25}	50	A
@V_{ge} = 15V, @T_C = 90°C	I_{C90}	32	A
Collector Current Pulsed (1)	I_{CM}	200	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at T_J = +150°C	SSOA	200A @ 0.8 BV_{CES}	-
Power Dissipation Total @T_C = 25°C	P_D	208	W
Power Dissipation Derating T_C > 25°C		1.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (2)			
@V_{ge} = 15V	t_{sc}	3	µS
@V_{ge} = 10V	t_{sc}	15	µS

(1) Repetitive Rating: Pulse width limited by maximum junction temperature.
(2) V_{CE} (pk) = 360V, T_C = 125°C, R_{ge} = 25Ω

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073 4,417,385 4,430,792 4,443,931 4,466,176 4,516,143 4,532,534 4,567,641
4,587,713 4,598,461 4,605,948 4,618,872 4,620,211 4,631,564 4,639,754 4,639,762
4,641,162 4,644,637 4,682,195 4,684,413 4,694,313 4,717,679 4,743,952 4,783,690
4,794,432 4,801,986 4,803,533 4,809,045 4,809,047 4,810,665 4,823,176 4,837,606
4,860,080 4,883,767 4,888,627 4,890,143 4,901,127 4,904,609 4,933,740 4,963,951
4,969,027

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2828.1

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250μA, V_{GE} = 0V		600	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	V_{CE} = BV_{CES}	T_C = +25°C	-	-	250	μA
		V_{CE} = 0.8 BV_{CES}	T_C = +125°C	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C90}, V_{GE} = 15V	T_C = +25°C	-	2.4	2.9	V
			T_C = +125°C	-	2.4	3.0	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 1mA, V_{CE} = V_{GE}	T_C = +25°C	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±500	nA
Gate-Emitter Plateau Voltage	$V_{GE(pl)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}		-	6.5	-	V
On-State Gate Charge	$Q_{G(on)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	-	200	260	nC
			V_{GE} = 20V	-	265	345	nC
Current Turn-On Delay Time	$t_{d(on)i}$	L = 500μH, I_C = I_{C90}, R_g = 25Ω, V_{GE} = 15V, T_J = 125°C, V_{CE} = 0.8 BV_{CES}		-	100	-	ns
Current Rise Time	t_{ri}			-	150	-	ns
Current Turn-Off Delay Time	$t_{d(off)i}$			-	630	820	ns
Current Fall Time	t_{fi}			-	620	800	ns
Turn-Off Energy(1)	W_{off}			-	3.5	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.5	0.6	°C/W

(1) Turn-off Energy Loss (W_{off}) is defined as the integral of the instantaneous power loss starting at the trailing idge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A) The HGTG32N60E2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

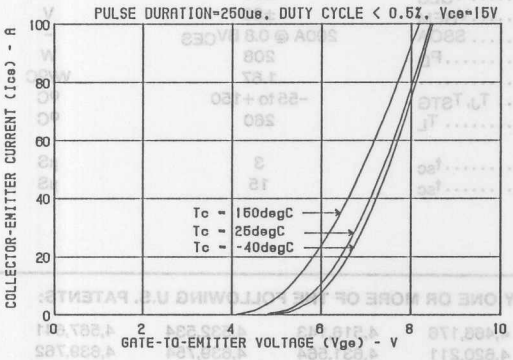


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

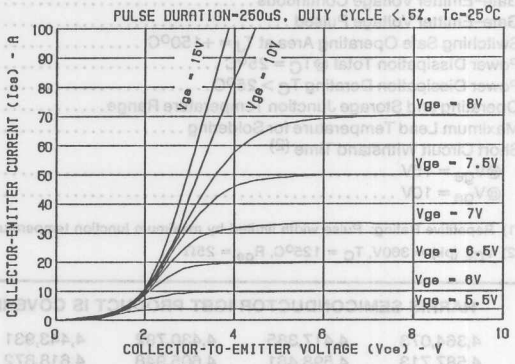


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

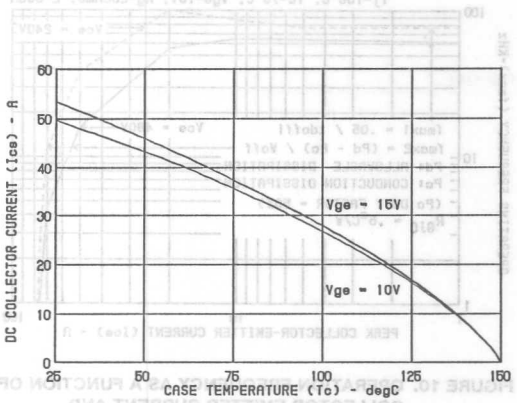


FIGURE 3. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE.

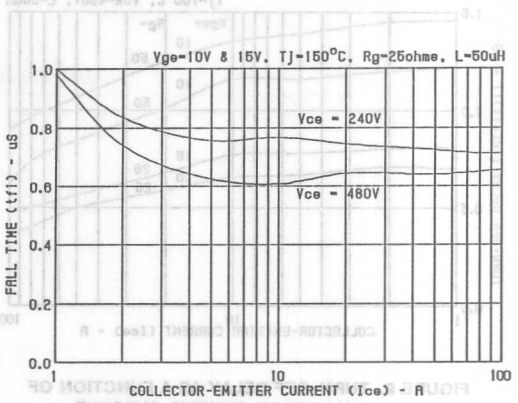


FIGURE 4. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

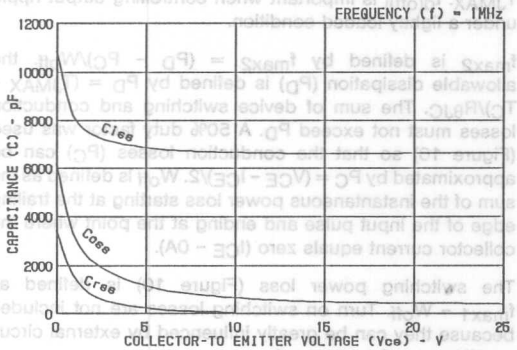


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE.

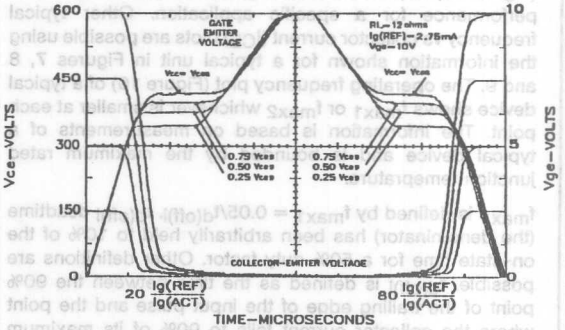


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260).

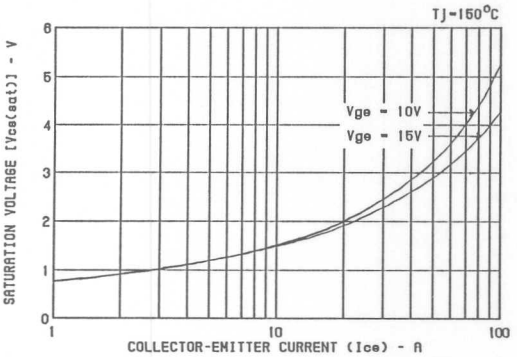


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

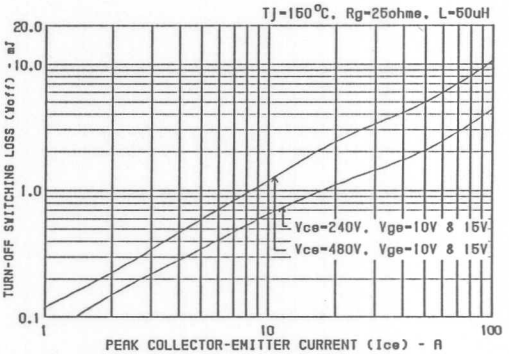


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

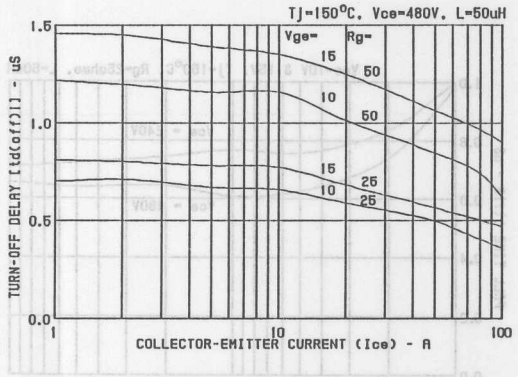


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

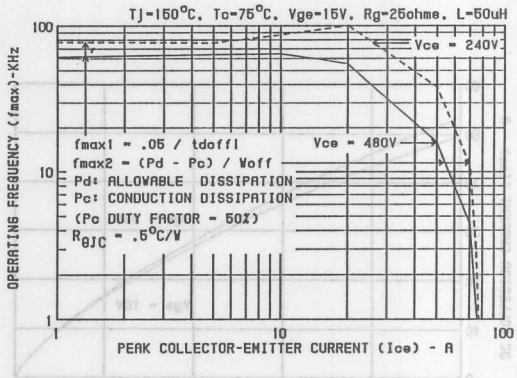


FIGURE 10. OPERATION FREQUENCY AS A FUNCTION OF COLLECTOR EMITTER CURRENT AND VOLTAGE

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{max1} or f_{max2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temeprature.

f_{max1} is defined by $f_{max1} = 0.05/t_{d(off)i}$. $t_{d(off)i}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(off)i}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(off)i}$ is important when controlling output ripple under a lightly loaded condition.

f_{max2} is defined by $f_{max2} = (P_D - P_C)/W_{off}$. the allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} - I_{CE})/2$. W_{off} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} - 0A).

The switching power loss (Figure 10) is defined as $f_{max1} - W_{off}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS HGTG34N100E2

August 1991

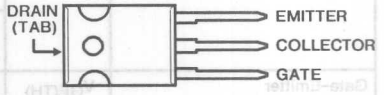
N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)

Features

- 55 Amp 1000 Volt
- Latch Free Operation
- Typical Fall Time - 710ns
- High Input Impedance
- Low Conduction Loss

Package

TO-247
TOP VIEW



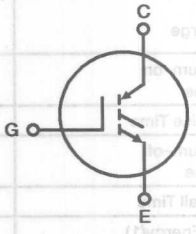
Description

The HGTG34N100E2* is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

The IGBTs are ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

*Formerly Developmental Type #TA9895

Terminal Diagram



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

			UNITS
Collector-Emitter Voltage	BV_{CES}	1000	V
Collector-Gate Voltage, R_{GE} =1MΩ	V_{CGR}	1000	V
Collector Current Continuous			
@T_C = +25°C	I_{C25}	55	A
@V_{ge} =15V, @T_C = +90°C	I_{C90}	34	A
Collector Current Pulsed(1)	I_{CM}	200	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area			
@T_J = +150°C	SSOA	200A @ .8 BV_{CES}	-
Power Dissipation Total	P_D		
@T_C = +25°C		208	W
Derating T_C > +25°C		1.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time(2)	t_{sc}		
@V_{ge} =15V		3	µS
@V_{ge}=10V		10	µS

(1) Repetitive Rating: Pulse width limited by maximum junction temperature.

(2) $V_{CE(pk)}$ = 600V, T_C = 125°C, R_{GE} = 25Ω

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2827**

Electrical Characteristics $T_C = +25^oC$, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A, V_{GE} = 0V$		1000	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	1.0	mA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +125^oC$	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C90}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	2.8	3.2	V
			$T_C = +125^oC$	-	2.8	3.1	V
		$I_C = I_{C90}$, $V_{GE} = 10V$	$T_C = +25^oC$	-	2.9	3.3	V
			$T_C = +125^oC$	-	3.0	3.4	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 1mA$, $V_{CE} = V_{GE}$	$T_C = +25^oC$	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±500	nA
Gate-Emitter Plateau Voltage	$V_{GE(pl)}$	$I_C = I_{C90}, V_{CE} = 0.5\ BV_{CES}$		-	7.3	-	V
On-State Gate Charge	$Q_{G(on)}$	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	185	240	nC
			$V_{GE} = 20V$	-	240	315	nC
Current Turn-on Delay Time	$t_{d(on)i}$	$L = 50\mu H, I_C = I_{C90}, R_g = 25\Omega$, $V_{GE} = 15V, T_J = +125^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{ri}			-	150		ns
Current Turn-off Delay Time	$t_{d(off)i}$			-	610	795	ns
Current Fall Time	t_{fi}			-	710	925	ns
Turn-off Energy(1)	W_{off}			-	7.1	-	mJ
Current Turn-on Delay Time	$t_{d(on)i}$	$L = 50\mu H, I_C = I_{C90}, R_g = 25\Omega$, $V_{GE} = 10V, T_J = +125^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{ri}			-	150	-	ns
Current Turn-off Delay Time	$t_{d(off)i}$			-	460	600	ns
Current Fall Time	t_{fi}			-	670	870	ns
Turn-off Energy(1)	W_{off}			-	6.5	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.5	0.6	$^oC/W$

(1) Turn-off Energy Loss (W_{off}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A). The HGTG34N100E2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

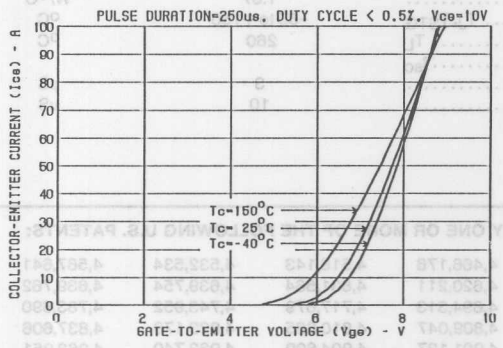


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

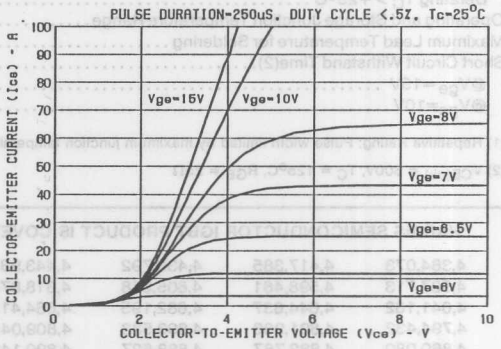


FIGURE 2. SATURATION CHARACTERISTIC (TYPICAL)

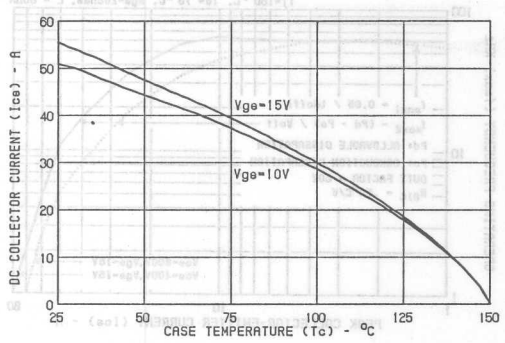


FIGURE 3. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

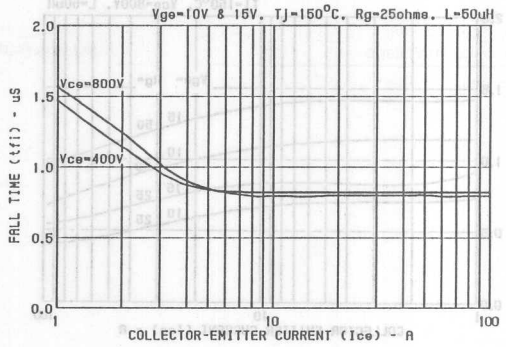


FIGURE 4. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

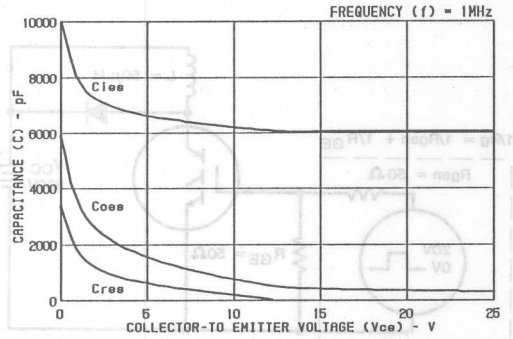


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

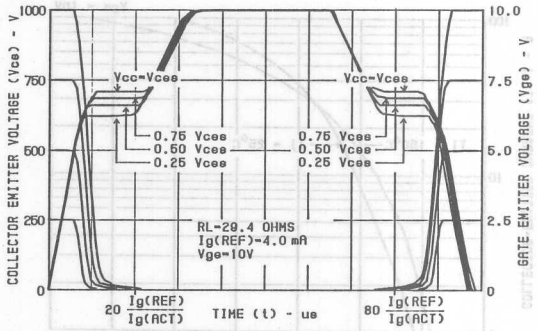


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260.)

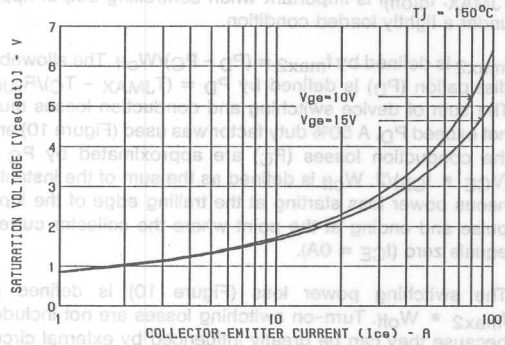


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

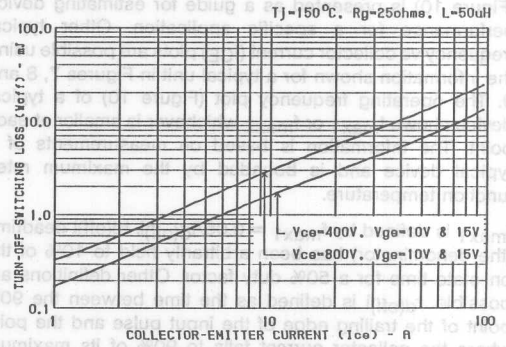


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

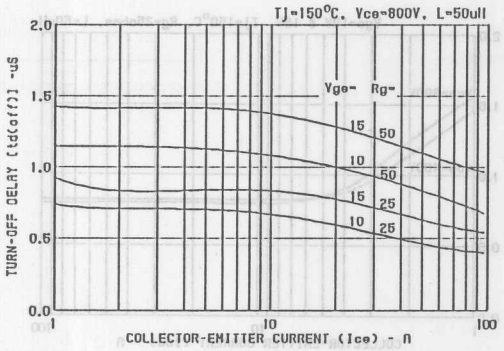


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

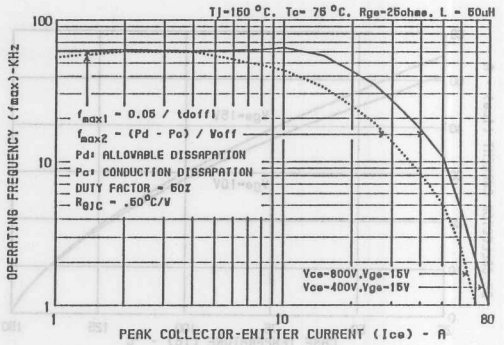


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE.

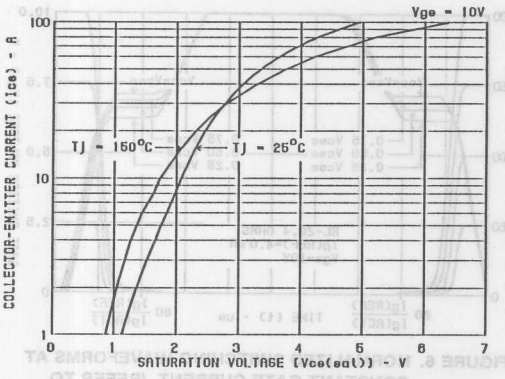


FIGURE 11. COLLECTOR-EMITTER SATURATION VOLAGE.

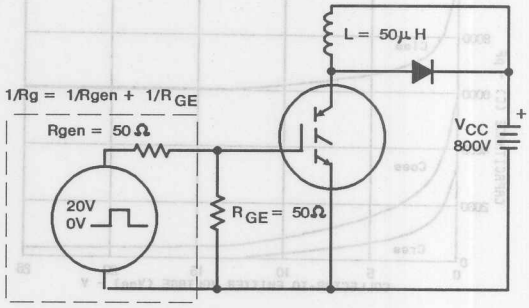


FIGURE 12. INDUCTIVE SWITCHING TEST CIRCUIT.

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{max1} or f_{max2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{max1} is defined by $f_{max1} = 0.05/t_{d(off)i}$. $t_{d(off)i}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(off)i}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(off)i}$ is important when controlling output ripple under a lightly loaded condition.

f_{max2} is defined by $f_{max2} = (P_D - P_C)/W_{off}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \bullet I_{CE})/2$. W_{off} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A).

The switching power loss (Figure 10) is defined as $f_{max2} \bullet W_{off}$. Turn-on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

POWER MOSFETs 8

INTELLIGENT DISCRETES

DATASHEETS		PAGE
HGTB12N60D1C	Current Sensing N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)	8-3
RLP1N06CLE	Voltage-Clamping Current-Limiting ESD-Protected N-Channel Enhancement-Mode Power Field-Effect Transistor	8-25
RLP1N08LE	Current Limited ESD Protected N-Channel Enhancement-Mode Power Field-Effect Transistor	8-7
RFB18N10CS/ RFB18N10CSVM/ RFB18N10CSHM	Current Sensing N-Channel Enhancement-Mode Power Field-Effect Transistor	8-14
RLP5N08LE	Current Limited ESD Protected N-Channel Enhancement-Mode Power Field-Effect Transistor	8-19

8 POWER MOSFETs

INTELLIGENT DISCRETES

DATASHEETS		PAGE
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HARRIS HGTB12N60D1C

Current Sensing N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)

August 1991

Features

- 12A, 600V
- $r_{DS(ON)}$ 0.27Ω
- Low $V_{CE(SAT)}$ at 25A ..... 2.5V Typ
- Ultra-fast Turn-On ..... 100ns Typ
- Polysilicon MOS Gate - Voltage Controlled Turn On/Off
- High Current Handling at +100°C 10A
- Current Sensing Pilot

Description

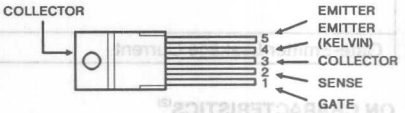
The HGTB12N60D1C Insulated-Gate Bipolar Transistor is a MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs and bipolar transistors, and current sensing pilots. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGBT are also similar to power MOSFETs. An important difference is the equivalent $r_{DS(ON)}$ drain resistance which is modulated to a low value (ten times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between +25°C and +150°C, offering extended power handling capability.

The IGBT is ideal for many high-voltage switching applications operating at low frequencies and where low conduction losses are essential, such as AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

The HGTB12N60D1C is supplied in a 5 lead JEDEC TS-001 package.

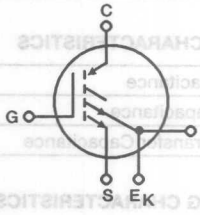
Package

TS-001 (5 LEAD)
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		HGTB12N60D1C	UNITS
Collector-Emitter Voltage (V_{GE} = 0V)	V_{CES}	600	V
Collector-Gate Voltage (R_{GE} = 1MΩ)	V_{CGR}	600	V
Collector Current Continuous	I_C		
@ T_C = +100°C		12	A
@ T_C = +25°C		18	A
Collector Current Pulsed (1)	I_{CM}	40	A
Gate-Emitter Voltage	V_{GE}	±25	V
Power Dissipation Total @ T_C = +25°C	P_D	75	W
Power Dissipation Derating T_C > +25°C		0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering (1/8 inch from case for 5 seconds)	T_L	260	°C

(1) Repetitive Rating: Pulse width limited by maximum junction temperature. Gate control turn-off not allowed above 50A.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2326.1

ELECTRICAL CHARACTERISTICS T_C = 25°C Unless Otherwise Specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage	BV_{CES}	V_{GE} = 0 V, I_C = 25 μA	600	—	—	V
Collector Cut-off Current	I_{CES}	V_{CE} = Max. Rating V_{GE} = 0 V, T_C = 25° C	—	—	250	μA
		V_{CE} = Max. Rating x 0.8 V_{GE} = 0 V, T_C = 150° C[1]	—	—	4	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V	—	—	±500	nA
ON CHARACTERISTICS[2]						
Gate Threshold Voltage	$V_{GE(th)}$	V_{CE} = V_{GE}, I_C = 250 μA T_C = 25°C T_C = 150°C	2 —	4 2.5	5 —	V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	V_{GE} = 15 V, I_C = 10 A, T_C = 25°C V_{GE} = 15 V, I_C = 10 A, T_C = 150°C V_{GE} = 10 V, I_C = 10 A, T_C = 25°C	— — —	2.5 2.8 2.9	2.7 — —	V
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ies}	V_{GE} = 0 V	—	1050	—	pF
Output Capacitance	C_{oes}	V_{CE} = 25 V	—	340	—	pF
Reverse Transfer Capacitance	C_{res}	f = 1 MHz	—	10	—	pF
SWITCHING CHARACTERISTICS[2] (See Figs. 8 & 9)						
Turn-On Delay Time	$t_{d(on)}$	Resistive Load, T_J = 125°C	—	100	—	ns
Rise Time	t_r	I_C = 10 A, V_{CE} = 500 V	—	100	—	ns
Turn-Off Delay Time	$t_{d(off)}$	V_{GE} = 15 V	—	0.4	—	μs
Fall Time	t_f	$R_{G(on)}$ = 50 Ω, $R_{G(off)}$ = 100 Ω	—	2.5	—	μs
Turn-Off Delay Time	$t_{d(off)}$	Inductive Load, T_J = 125°C	—	0.8	1.2	μs
Fall Time	t_f	L = 45 μH, I_C = 10 A	—	0.8	1.0	μs
Equivalent Fall Time	$t_{f(eq)}$	V_{CE}(clamp) = 500 V, V_{GE} = 15 V $R_{G(on)}$ = 50 Ω, $R_{G(off)}$ = 100 Ω	—	0.6	0.8	μs
Turn-Off Switching Losses	E_f		—	1.6	2.0	mJ
PILOT CHARACTERISTICS[2] [3] [4]						
Pilot - Emitter Kelvin Voltage I_C = 5 A I_C = 10 A I_C = 20 A	V_{PEK}	V_{GE} = 15 Vdc, R_P = 2 KΩ	 — 1.4 —	 1.25 1.67 2.06	 — 1.8 —	 V

[1] Applies for 3.3°C per watt maximum thermal resistance, case-to-ambient.
[2] Pulse test: Pulse widths ≤ 300 μs, duty cycle ≤ 2%.
[3] Refer to Fig. 10.
[4] When Not in Use Connect E_P to Emitter.

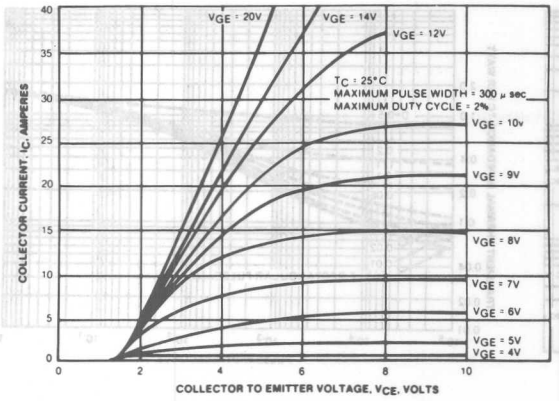


Fig. 1 - Typical output characteristics.

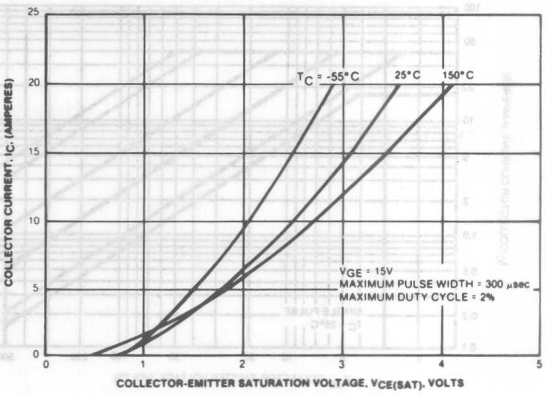


Fig. 2 - Typical collector-emitter saturation voltage.

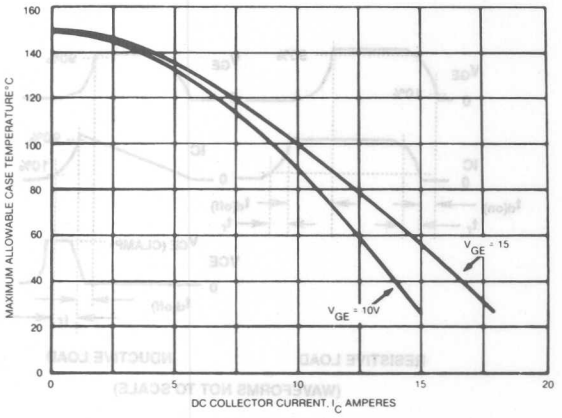


Fig. 3 - Maximum allowable case temperature vs. DC collector current.

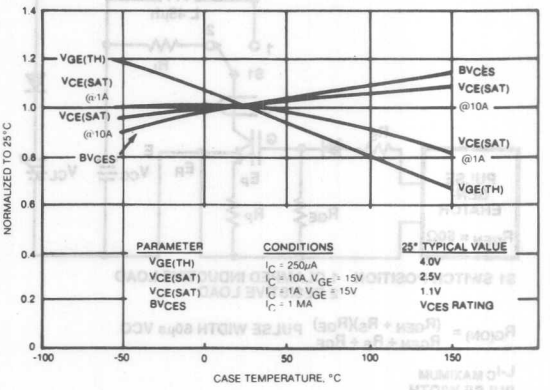


Fig. 4 - Typical temperature dependence of parameters.

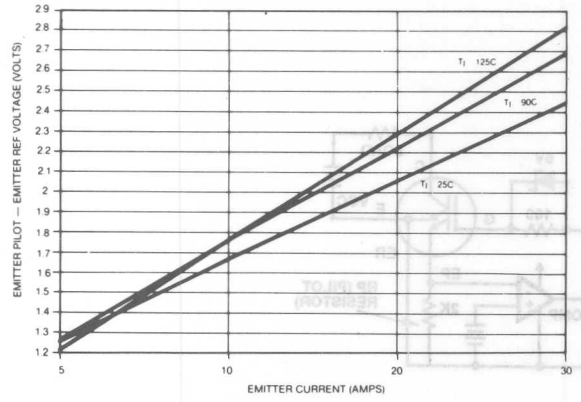


Fig. 5A - Typical emitter pilot characteristics 2 Kohm pilot resistor.

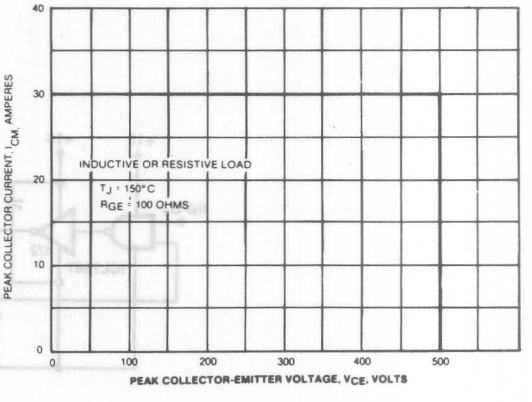


Fig. 5B - Turn-off safe operating area.

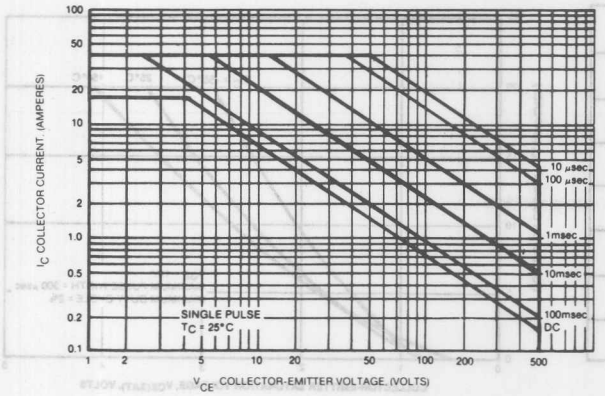


Fig. 6 - Turn-on safe operating area.

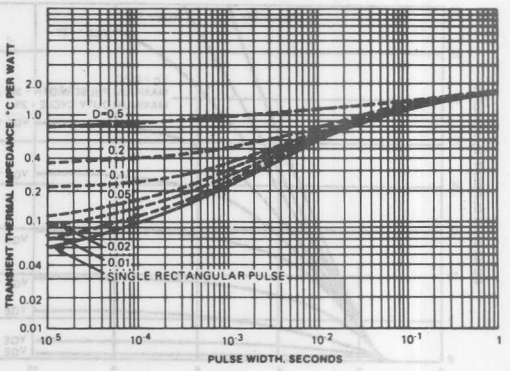


Fig. 7 - Maximum transient thermal impedance.

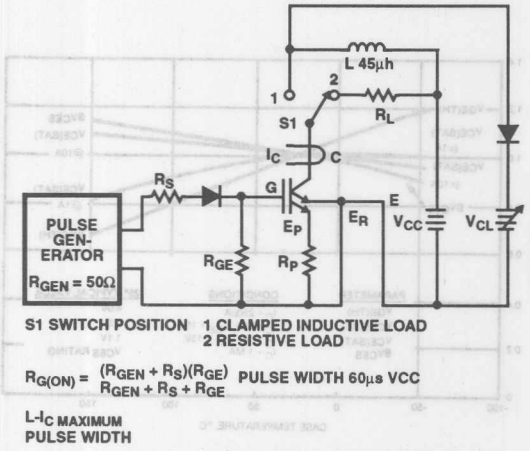


Fig. 8 - Basic switching test circuit.

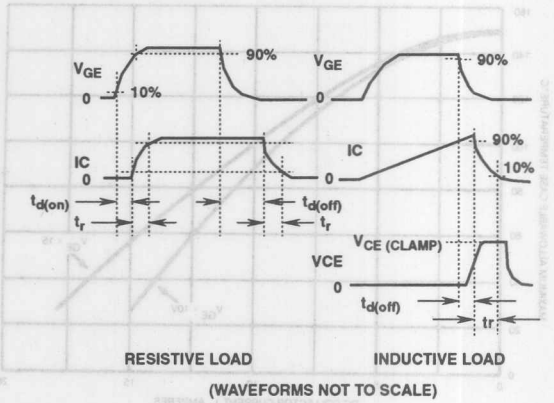


Fig. 9 - Switching waveforms.

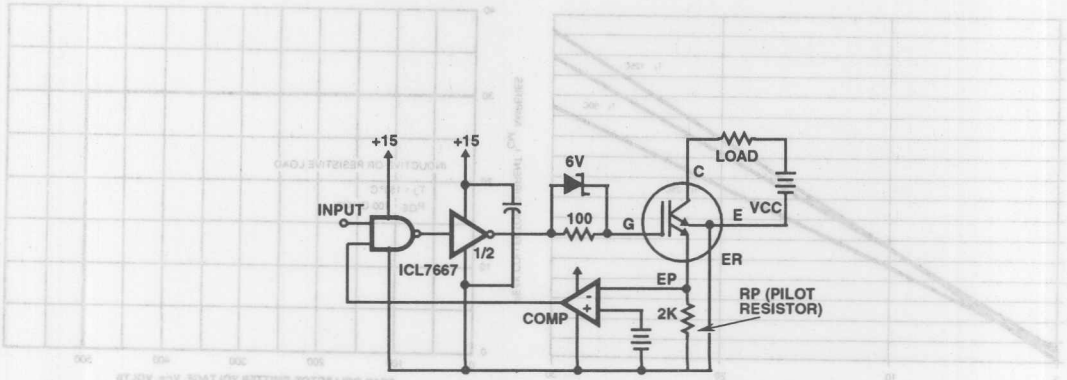


Fig. 10 - Typical circuit utilizing the emitter pilot for

HARRIS

RLP1N08LE

May 1992

Current Limited ESD Protected N-Channel Enhancement-Mode Power Field-Effect Transistor

Features

- 1A, 80V
- $r_{DS(ON)} = 0.75\Omega$
- I_{LIMIT} at +150°C ..... 1.5A Max
- Built-In Current Limiting
- ESD Protected
- Controlled Switching Limits EMI and RFI
- Specified for +150°C Operation
- Temperature Compensated Spice Model Provided

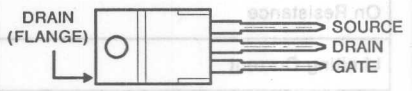
Description

The RLP1N08LE is a semi-smart monolithic power circuit which incorporates a lateral bipolar transistor, two resistors, a zener diode, and a PowerMOS transistor. Good control of the current-limiting levels allows use of these devices where a shorted load condition may be encountered. "Logic level" gates allow this device to be fully biased on with only 5 volts from gate to source. The zener diode provides ESD protection up to 2kV. These devices can be produced on the standard PowerMOS production line.

The RLP-series types are supplied in the JEDEC TO-220AB plastic packages.

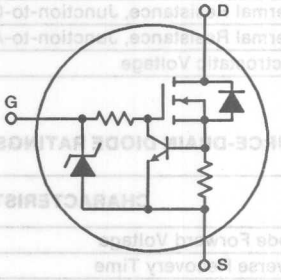
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RLP1N08LE	UNITS
Drain-Source Voltage	V_{DSS}	80	V
Drain-Gate Voltage	V_{DGR}	80	V
Gate-Source Voltage (1)	V_{GS}	5.5	V
Reverse Voltage Gate Bias Not Allowed			
Electrostatic Voltage at 100pF, 1500Ω	ESD	2	kV
Drain Current, Continuous	I_D	Self Limited	
Power Dissipation Total @ T_C = +25°C	P_D	75	W
Power Dissipation Derating T_C > +25°C		0.24	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +150	°C

(1) May be exceeded if current is limited to 10mA.

8 INTELLIGENT DISCRETES

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2252.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified.*

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V	80	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	1	2	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65 V, V_{GS} = 0 V	—	1	μA
		T_C = 150°C	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 5 V, T_C = 150°C	—	50	
On Resistance	$r_{DS}(on)$	I_D = 1 A, V_{GS} = 5 V	—	0.75	Ω
		T_C = 150°C	—	1.5	
Limiting Current	$I_{DS}(Lim)$	V_{DS} = 15 V, V_{GS} = 5 V	1.8	3	A
		T_C = 150°C	1.1	1.5	
Turn-On Time	t(on)	V_{DD} = 30 V, I_D = 1 A, V_{GS} = 5 V, R_{GS} = 25 Ω, R1 = 30 Ω	—	6.5	μs
Turn-On Delay Time	$t_d(on)$		—	1.5	
Rise Time	t_r		1	5	
Turn-Off Delay Time	$t_d(off)$		—	7.5	
Fall Time	t_f		1	5	
Turn-Off Time	t(off)		—	12.5	
Plateau Voltage	V(plateau)	I_D = 1 A, V_{DS} = 15 V	—	5	V
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		—	4.17	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		—	80	
Electrostatic Voltage	ESD	Human Model (100 pF, 1.5 kΩ)	2000	—	V

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD} = 1 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 1 A	—	1	ms

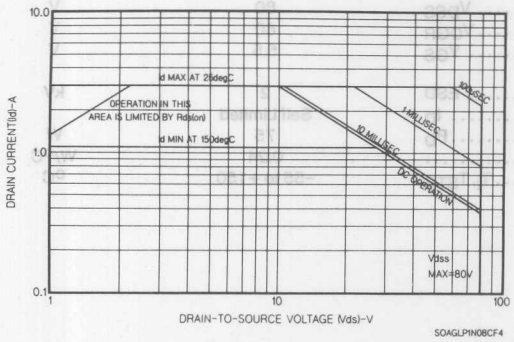


Fig. 1 - Safe-operating-area curve.

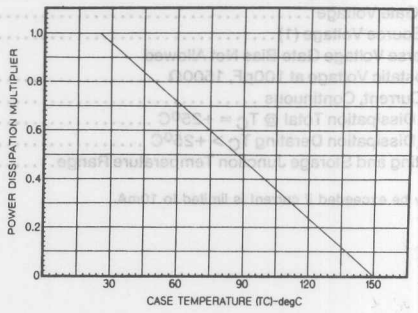


Fig. 2 - Normalized power dissipation vs. temperature derating curve.

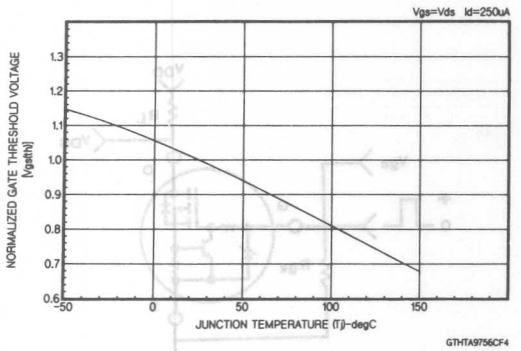


Fig. 3 - Typical normalized gate-threshold voltage.

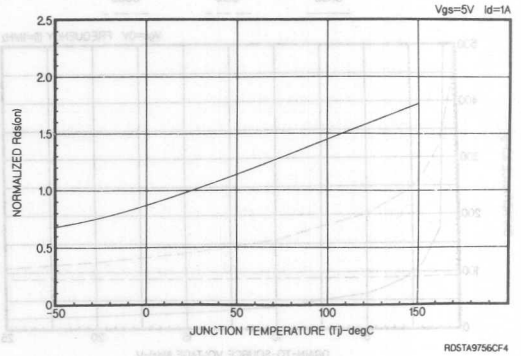


Fig. 4 - Normalized $r_{DS}(on)$ vs. junction temperature.

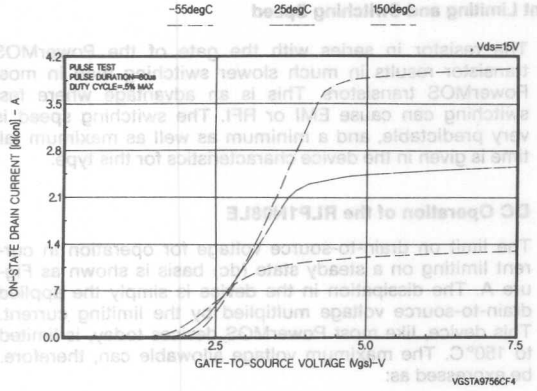


Fig. 5 - Typical transfer characteristics.

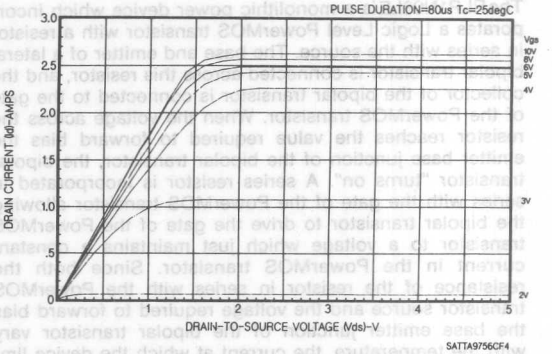


Fig. 6 - Typical saturation characteristics.

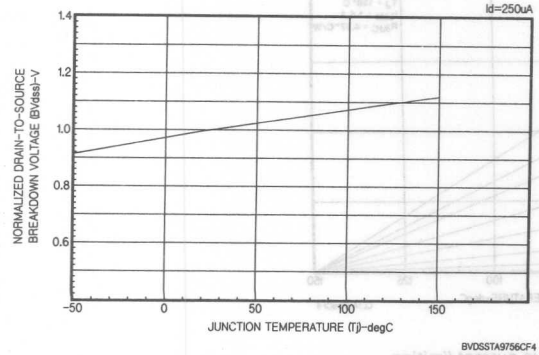


Fig. 7 - Drain-source breakdown voltage vs. temperature.

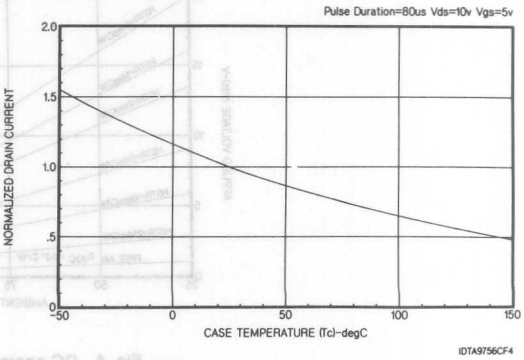


Fig. 8 - Normalized current limit vs. temperature.

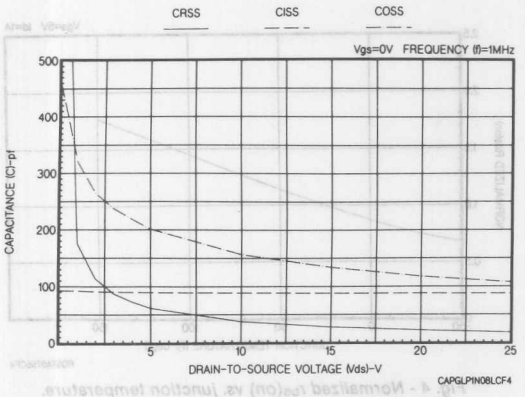


Fig. 9 - Typical capacitance vs. voltage.

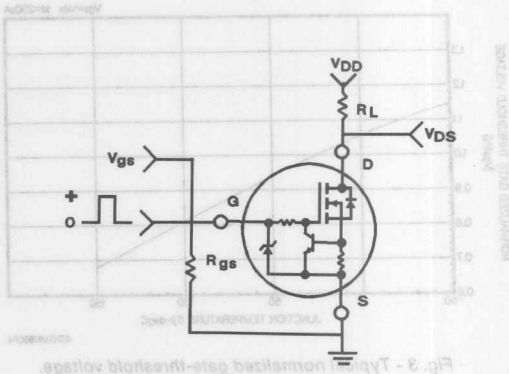


Fig. 10 - Switching test circuit.

Temperature Dependence of Current Limiting and Switching Speed

The RLP1N08LE is a monolithic power device which incorporates a Logic Level PowerMOS transistor with a resistor in series with the source. The base and emitter of a lateral bipolar transistor is connected across this resistor, and the collector of the bipolar transistor is connected to the gate of the PowerMOS transistor. When the voltage across the resistor reaches the value required to forward bias the emitter base junction of the bipolar transistor, the bipolar transistor "turns on". A series resistor is incorporated in series with the gate of the PowerMOS transistor allowing the bipolar transistor to drive the gate of the PowerMOS transistor to a voltage which just maintains a constant current in the PowerMOS transistor. Since both the resistance of the resistor in series with the PowerMOS transistor source and the voltage required to forward bias the base emitter junction of the bipolar transistor vary with the temperature, the current at which the device limits is a function of temperature. This dependence is shown in Figure 8.

The resistor in series with the gate of the PowerMOS transistor results in much slower switching than in most PowerMOS transistors. This is an advantage where fast switching can cause EMI or RFI. The switching speed is very predictable, and a minimum as well as maximum fall time is given in the device characteristics for this type.

DC Operation of the RLP1N08LE

The limit on drain-to-source voltage for operation in current limiting on a steady state (dc) basis is shown as Figure A. The dissipation in the device is simply the applied drain-to-source voltage multiplied by the limiting current. This device, like most PowerMOS devices today, is limited to 150°C. The maximum voltage allowable can, therefore. be expressed as:

$$V_s = \frac{(150 - T_{ambient})}{I_{lim}\,(R_{\theta JC} + R_{\theta})}$$

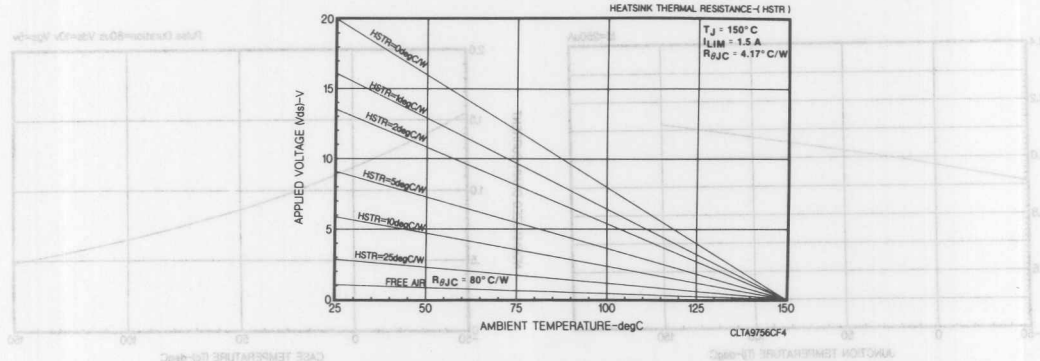


Fig. A - DC operation in current limiting.

Duty Cycle Operation of the RLP1N08LE

In many applications either the drain-to-source voltage or the gate drive is not available 100% of the time. The copper header on which the RLP1N08LE is mounted has a very large thermal storage capability, so for pulse widths of less than 100 milliseconds, the temperature of the header can be considered a constant case temperature calculated simply as:

$$T_c = (V_{SD} * I_D * D * R_{\theta CA}) + \text{Tambient}$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to 150°C and using the T_C calculated above, the expression for maximum V_{SD} under duty cycle operation is:

$$V_{SD} = \frac{150 - T_c}{I_{lim} * D * R_{\theta JC}}$$

These values are plotted as Figures B1 - B5 for various heat sink thermal resistances.

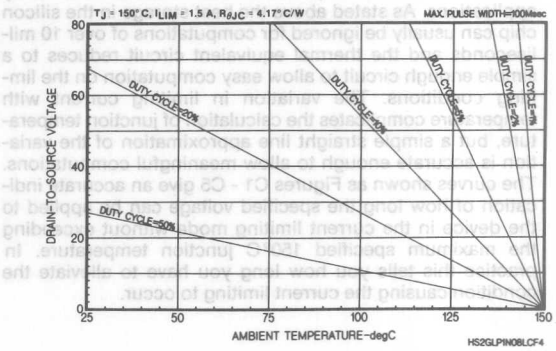


Fig. B1 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 2°C/W)

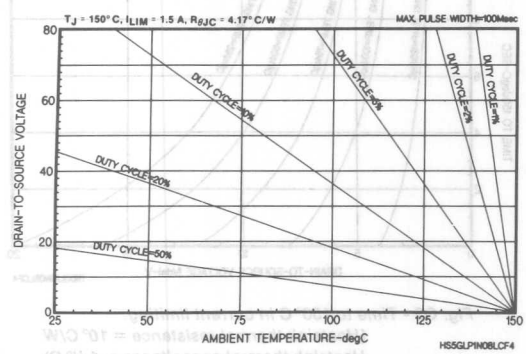


Fig. B2 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 5°C/W)

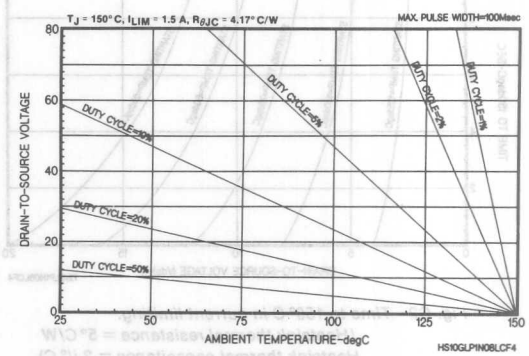


Fig. B3 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 10°C/W)

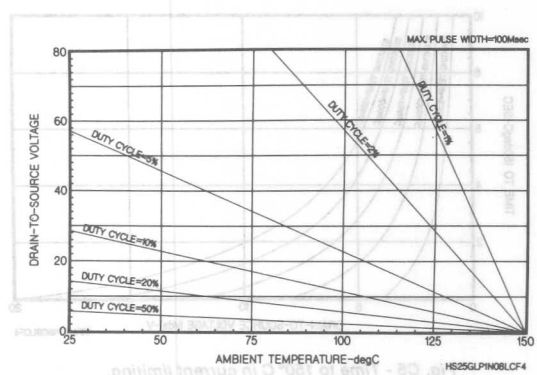


Fig. B4 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 25°C/W)

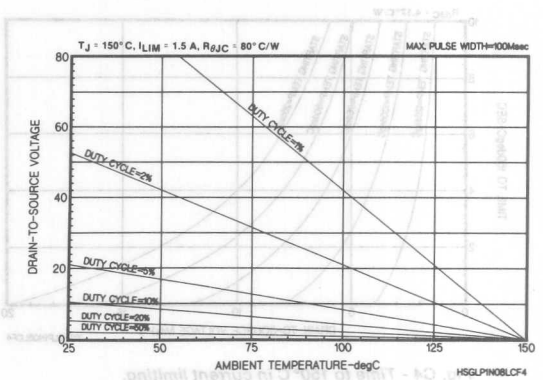


Fig. B5 - Maximum V_{DS} vs. ambient temperature in current limiting. (No external heatsink)

Limited Time Operations of the RLP1N08LE

Protection for a limited period of time is sufficient for many applications. As stated above the heat storage in the silicon chip can usually be ignored for computations of over 10 milliseconds and the thermal equivalent circuit reduces to a simple enough circuit to allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as Figures C1 - C5 give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified 150°C junction temperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

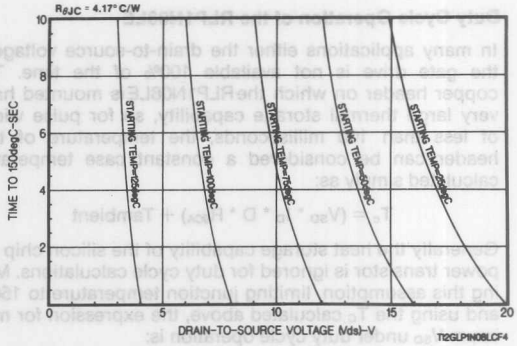


Fig. C1 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 2° C/W
Heatsink thermal capacitance = 4 j/° C)

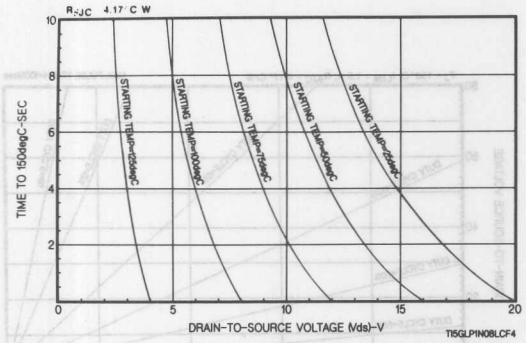


Fig. C2 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 5° C/W
Heatsink thermal capacitance = 2 j/° C)

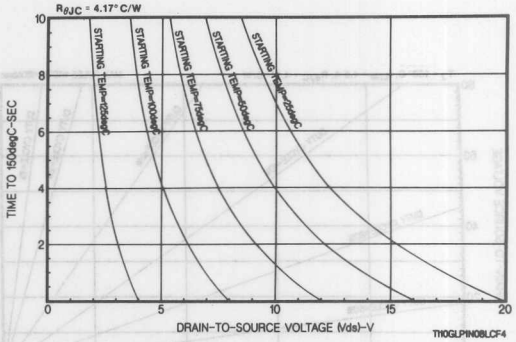


Fig. C3 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 10° C/W
Heatsink thermal capacitance = 1 j/° C)

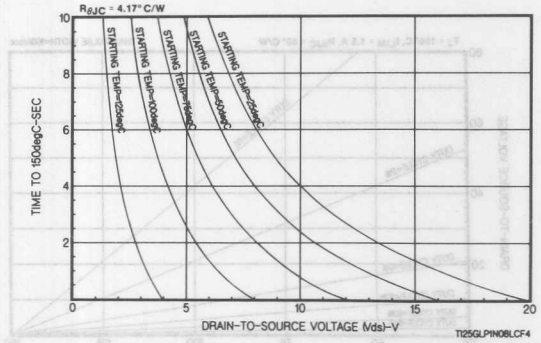


Fig. C4 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 25° C/W
Heatsink thermal capacitance = 5 j/° C)

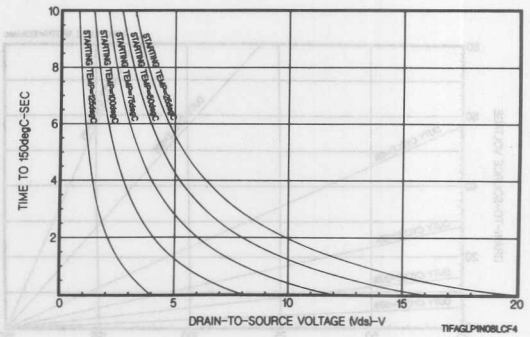


Fig. C5 - Time to 150° C in current limiting.
(No external heatsink)

Spice Model (RLP1N08LE)

```
.SUBCKT RLP1N08LE  2  1  3;  rev 09/16/91
*Nominal Temperature = 25°C
.MODEL MOSMOD NMOS (VTO=1.7  KP=2.1  IS=1e-30  N=10  TOS=1  L=1u  W=1u)
Vto  21  6  0.33
Rsource  8  7  RDSMOD  0.28
Rdrain  5  16  RDSMOD  0.2
.MODEL RDSMOD RES (TC1=7.54E-3  TC2=2.23E-5)
.MODEL RVTOMOD RES (TC1=-2.23E3  TC2=-5.29E-7)
.MODEL RVTOMOD2 RES (TC1=0  TC2=0)
Ebreak 11  7  17  18  107.3
.MODEL RBKMOD RES (TC1=1.11E-3  TC2=-6.83E-7)
.MODEL DBKMOD D (RS=2.78  TRS1=-8.88E-3  TRS2=2.55E-5)
.MODEL DBDMOD D (IS=9.91E-15  RS=3.01E-1  TRS1=3.79E-3  TRS2=1.11E-6  +CJO=4.32E-10  TT=2E-7
Cin  6  8  3.75E-10
Ca  12  8  6.5E-10
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-3  VOFF=-1)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-1  VOFF=-3)
.MODEL DPLCAPMOD D (CJO=2E-10  IS=1e-30  N=10)
Cb  12  14  6.5E-10
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-1.65  VOFF=3.35)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=3.35  VOFF=-1.65)
Rgate  9  20  4.48E3
Lgate  1  9  9.5E-10
Ldrain  2  5  2.5E-9
Lsource  3  7  2.5E-9
Dbody  7  5  DBDMOD
Dbreak  5  11  DBKMOD
Dplcap  10  5  DPLCAPMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Evto  20  6  18  8  1
It  8  17  1
MOS1  16  6  8  8  MOSMOD  M=0.99
MOS2  16  21  8  8  MOSMOD  M=0.01
Rbreak  17  18  RBKMOD  1
Rin  6  8  1e9
Rvto  18  19  RVTOMOD  1
S1a  6  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
*Current Limiting Control Section
.MODEL RSMOD RES (TC1=3.2E-3)
Q Control 20  8  7  QMOD  10
.MODEL QMOD NPN (BF=5  VJE=0.5)
*ESD Protection
DESD  7  9  DESMOD
.MODEL DESMOD D(BV=7.185  TBV1=3.5E-4  TBV2=2.2E-6)
.ENDS
```

HARRIS

RFB18N10CS/ CSVM/CSHM

Current Sensing N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 18A, 100V
- $r_{DS(ON)}$ 0.1Ω
- Built-In Current Sensing Ratio ..... 1560 ± 2.5%
- UIS SOA Rating Curve (Single Pulse)
- -55°C to +175°C Operating and Storage Temperature

Description

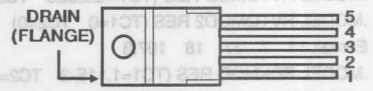
The RFB18N10CS, RFB18N10CSVM, RFB18N10CSHM are n-channel enhancement-mode silicon-gate power field-effect transistors which have a built-in current sensing function. The current sense lead provides an accurate fraction of the drain current that can be used as a feedback signal for control and/or protection. These devices can be repeatedly and economically produced on the standard PowerMOS production line.

The RFB-series are supplied in various lead configurations of the TS-001 (5 lead) case style plastic package.

Because of space limitations, branding (marking) on types RFB18N10CS, RFB18N10CSVM and RFB18N10CSHM is F18N10CS.

Package

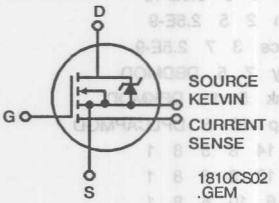
TS-001 (5 LEAD)
TOP VIEW



TERMINAL CONNECTIONS
1 - Gate
2 - Current Sense
3 - Drain
4 - Source Kelvin
5 - Source

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFB18N10CS RFB18N10CSVM RFB18N10CSHM	UNITS
Drain-Source Voltage	V_{DSS}	100	V
Drain-Gate Voltage	V_{DGR}	100	V
Gate-Source Voltage	V_{GS}	±20V	V
Drain Current, Continuous	I_D	18	A
Drain Current, Pulsed	I_{DM}	56	A
Single Pulse Avalanche Rating, Refer to UIS SOA Curve (Figure 10)			
Power Dissipation Total @ T_C = +25°C	P_D	79	W
Power Dissipation Derating T_C > +25°C		0.53	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2430.2

ELECTRICAL CHARACTERISTICS At Case Temperature (T_C) = +25°C, Unless Otherwise Specified.

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	ID = 0.25 mA, VGS = 0V	100	–	V
Gate Threshold Voltage	VGS(th)	VGS = VDS, ID = 0.25 mA	2	4	V
Zero Gate Voltge Drain Current	IDSS	VGS = 0V VDS = 100V, Tc = 25°C VDS = 80V, Tc = 175°C	– –	250 1000	µA
Gate-Source Leakage Current	IGSS	VGS = ±20V, VDS = 0V	–	±500	nA
Static Drain-Source On Resistance	rDS(on)	ID = 9A, VGS = 10V	–	0.10	Ω
Forward Transconductance	gfs	ID = 9A, VDS = 15V	4.7	–	S (℧)
Current Sensing Ratio	r	ID= 14A, VGS = 10V	1480	1640	
Turn-On Delay Time	td(on)	VDS =50V	–	14	ns
Rise Time	tr	ID = 14A	–	63	ns
Turn-Off Delay Time	td(off)	VGS = 10V	–	33	ns
Fall Time	tr	Rgs = 12Ω	–	38	ns
Total Gate Charge	Qg (total)	ID = 14A, VDS = 80V VGS = 10V	–	20	nC
Thermal Resistance, Junction-to-Case	RθJC		–	1.9	°C/W
Thermal Resistance, Junction-to-Ambient	RθJA		–	75	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	VSD	ISD = 14A	–	1.5	V
Reverse Recovery Time	trr	ISD = 14A, dISD/dt = 100A/µs	–	310	ns

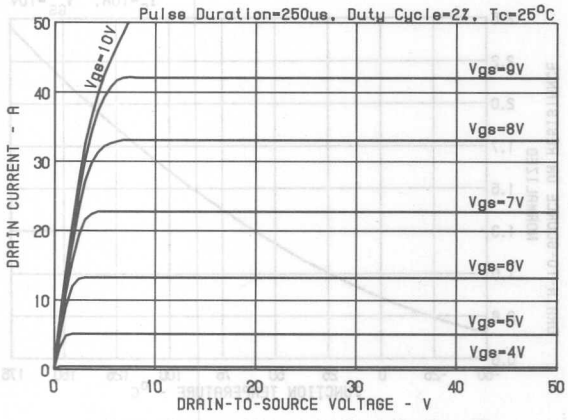


Figure 1 – Typical output characteristics.

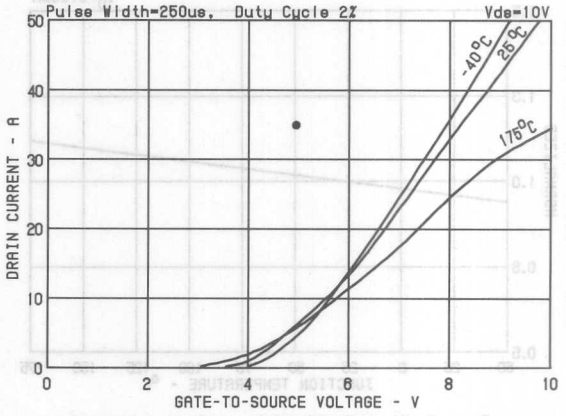


Figure 2 – Typical transfer characteristics.

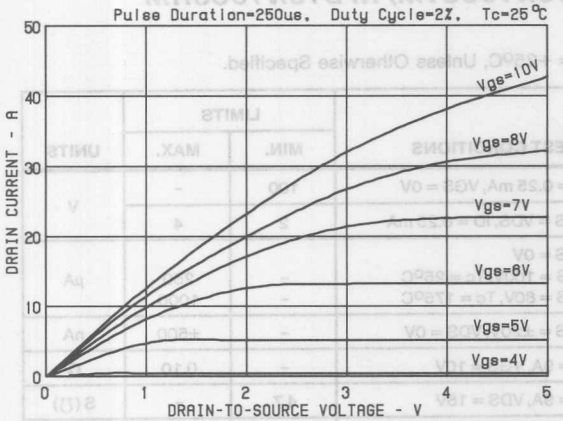


Figure 3 – Typical saturation characteristics.

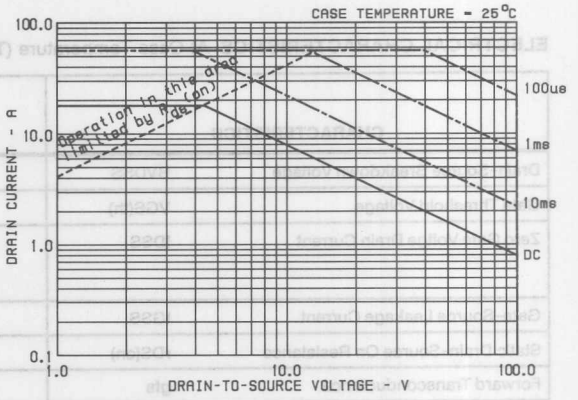


Figure 4 – Maximum safe operating area.
(Curves must be derated linearly with increase in case temperature.)

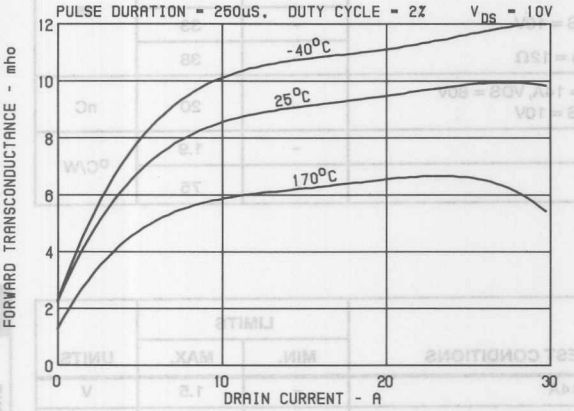


Figure 5 – Typical transconductance vs drain current.

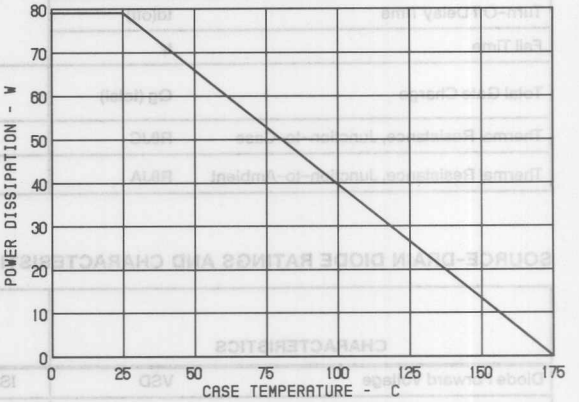


Figure 6 – Power dissipation vs case temperature derating curve.

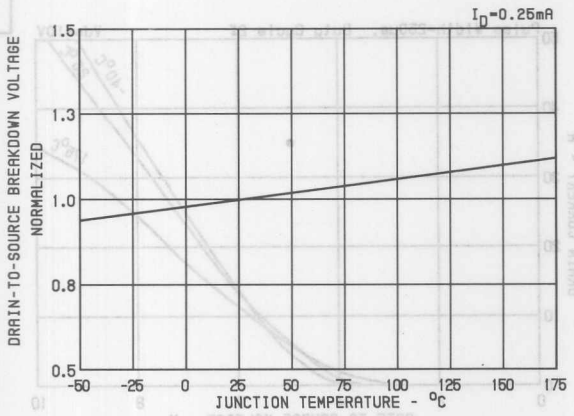


Figure 7 – Normalized breakdown voltage vs temperature.

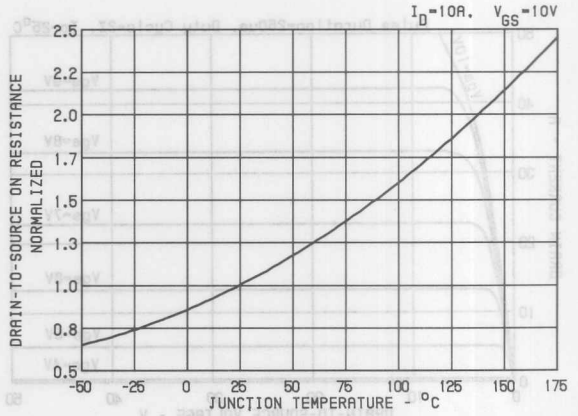


Figure 8 – Normalized on-resistance vs temperature.

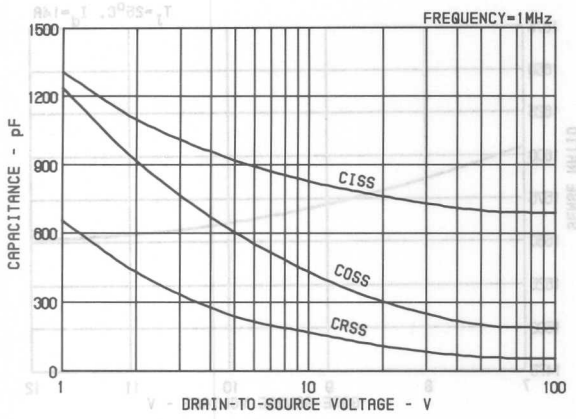


Figure 9 – Typical capacitance vs drain-to-source voltage.

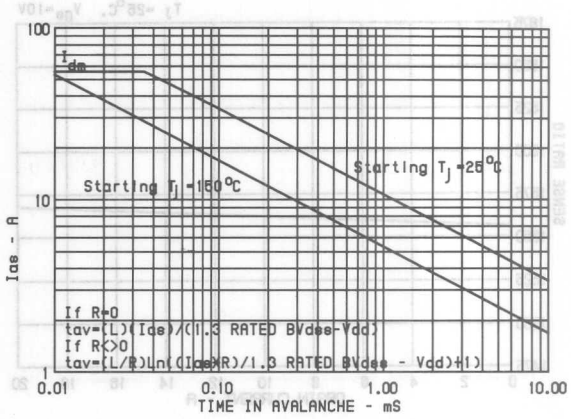


Figure 10 – Unclamped-Inductive switching safe operating area.

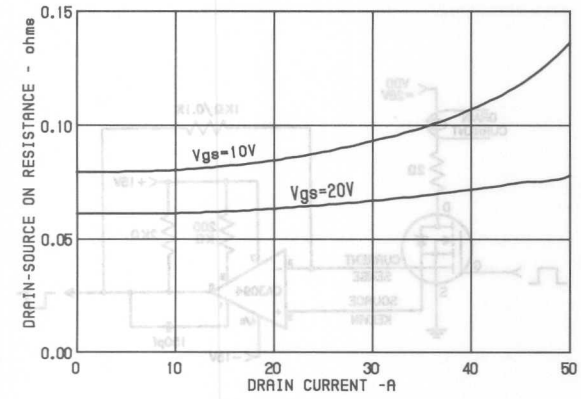


Figure 11 – Typical on-resistance vs drain current.

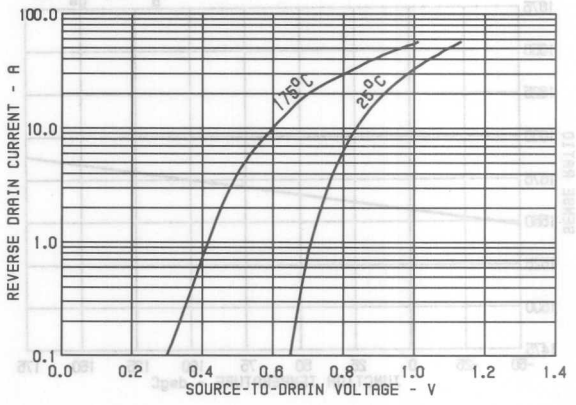


Figure 12 – Typical source-drain-diode forward voltage.

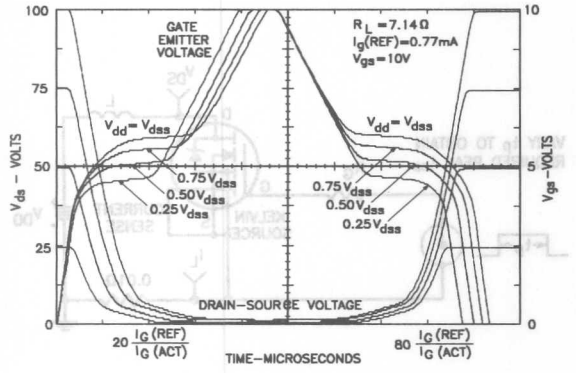


Figure 13 – Normalized switching waveforms for constant gate-current. (Refer to Harris application notes AN7254 and AN7260.)

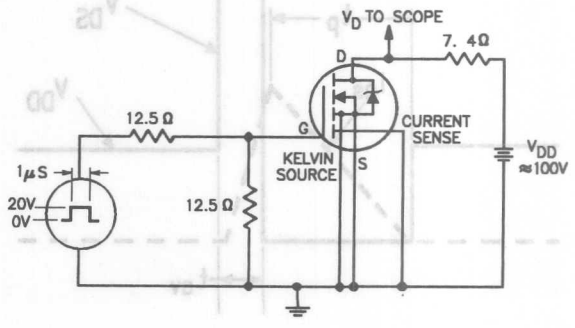


Figure 14 – Switching timetest circuit.

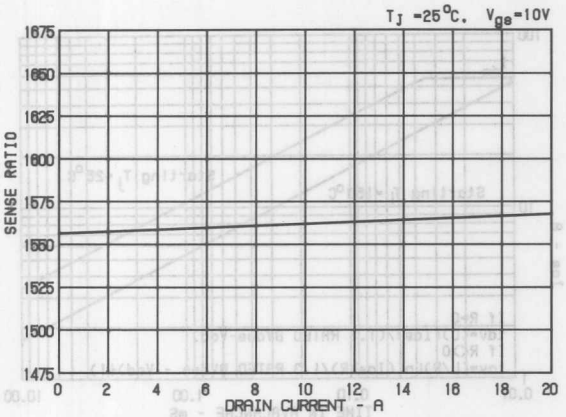


Figure 15 – Current sense ratio vs drain current.

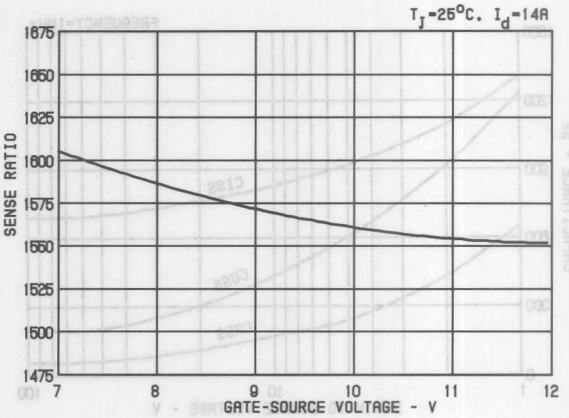


Figure 16 – Current sense ratio vs gate voltage.

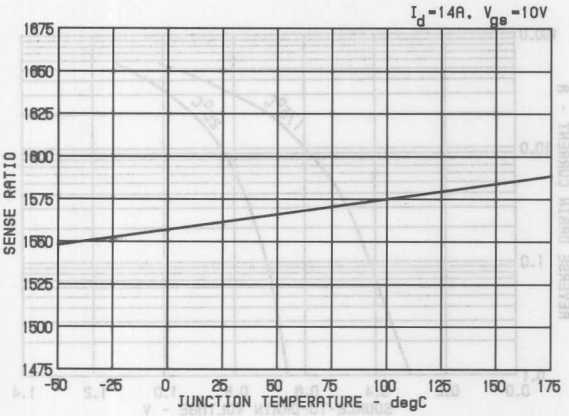


Figure 17 – Current sense ratio vs junction temperature.

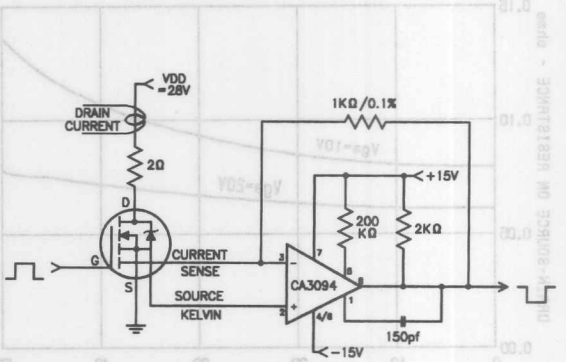


Figure 18 – Current sense ratio test circuit.

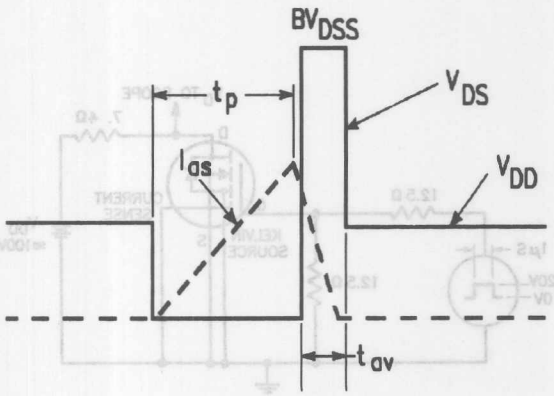


Figure 19 – UIS waveforms.

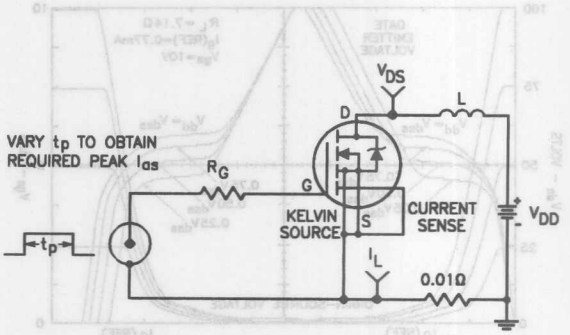


Figure 20 – UIS test circuit.

HARRIS

RLP5N08LE

May 1992

Current Limited ESD Protected N-Channel Enhancement-Mode Power Field-Effect Transistor

Features

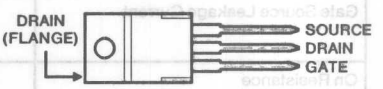
- 5.5A, 80V
- $R_{DS(ON)}$ 0.12Ω
- I_{Limit} ..... 5.5A to 8.5A at +150°C
- Built In Current Limiting
- E_{SD} Protected ..... 2KV Min
- Controlled Switching Limits EMI and RFI
- Specified For +150°C Operation
- +175°C Rated Junction Temperature
- Logic Level Gate

Description

The RLP5N08LE is an "Intelligent Discrete" monolithic power circuit which incorporates a small signal bipolar transistor, two resistors, a zener diode, and a PowerMOS transistor. Low $R_{DS(ON)}$ is achieved by the use of separate current sensing cells. Good control of the current limiting levels allows these devices to be used where it is anticipated that a shorted load condition may be encountered. "Logic Level" gates allow this device to be fully biased on with only 5.0V from gate to source. The zener diode provides E_{SD} protection of 2KV minimum.

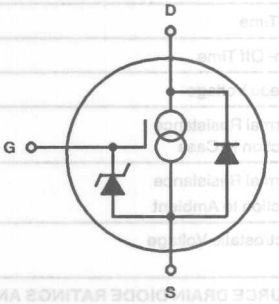
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RLP5N08LE	UNITS
Drain-Source Voltage	V_{DSS}	80	V
Drain-Gate Voltage	V_{DGR}	80	V
Gate-Source Voltage	V_{GS}	5.5	V
Reverse Voltage Gate Bias Not Allowed			
Electrostatic Voltage at 100pF, 1500Ω	ESD	2	kV
Drain Current, Continuous	I_D	Self Limited	
Power Dissipation Total @ T_C = +25°C	P_D	72	W
Power Dissipation Derating T_C > +25°C		0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	°C

8

INTELLIGENT DISCRETES

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2493.1**

Electrical Characteristics At Case Temperature (T_C = +25°C), Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA V_{GS} = 0V	80	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS} I_D = 0.25mA	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V V_{GS} = 0V	-	1	µA
		at T_C = +150°C	-	50	µA
Gate Source Leakage Current	I_{GSS}	V_{GS} = 5V	-	1	µA
		at T_C = +150°C	-	50	µA
On Resistance	$R_{DS(ON)}$	I_D = 5.5A V_{GS} = 5.0V	-	0.12	Ω
		at T_C = +150°C	-	0.24	Ω
Limiting Current	$I_{DS(Limit)}$	V_{DS} = 15.0V V_{GS} = 5.0V	9.0	14	A
		@ T_C = 150°C	5.5	8.5	A
Turn-On Time	$t_{(ON)}$	V_{DD} = 30.0V	-	6.5	µs
Turn-On Delay Time	$t_{D(ON)}$	I_D = 5.5A	-	1.5	µs
Rise Time	t_R	V_{GS} = 5.0V	1.0	5.0	µs
Turn-Off Delay Time	$t_{D(OFF)}$	R_{GS} = 25Ω	-	10.0	µs
Fall Time	t_F	R_L = 5.45Ω	1.0	5.0	µs
Turn-Off Time	$t_{(OFF)}$		-	15.0	µs
Plateau Voltage	$V_{(PLATEAU)}$	I_D = 7.5A V_{DS} = 15.0V	-	5.0	V
Thermal Resistance Junction to Case	$R\theta_{JC}$		-	2.083	°C/W
Thermal Resistance Junction to Ambient	$R\theta_{JC}$		-	75	°C/W
Electrostatic Voltage	E_{SD}	Human Model (100pF, 1.5kΩ) Mil-Std-883S (Category B2)	2000	-	V
SOURCE DRAIN DIODE RATINGS AND CHARACTERISTICS					
Forward Voltage	V_{SD}	I_{SD} = 5.5A	-	1.5	V
Reverse Recovery Time	T_{RR}	I_F = 5.5A	-	1.0	ms

Performance Curves

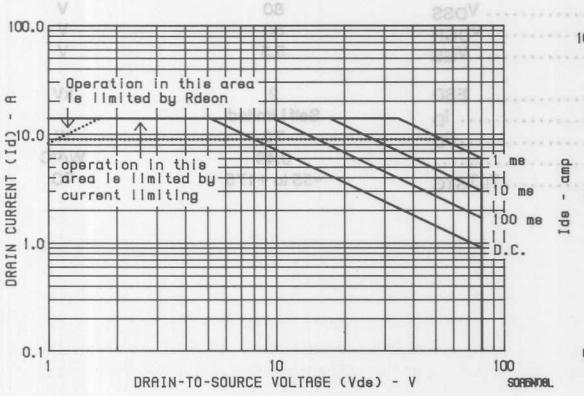


FIGURE 1. SAFE OPERATING AREA CURVE

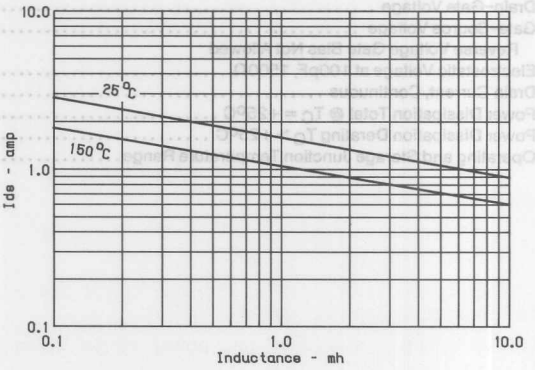


FIGURE 2. UNCLAMPED INDUCTIVE SWITCHING SOA (SINGLE PULSE UIS SOA)

Performance Curves (Continued)

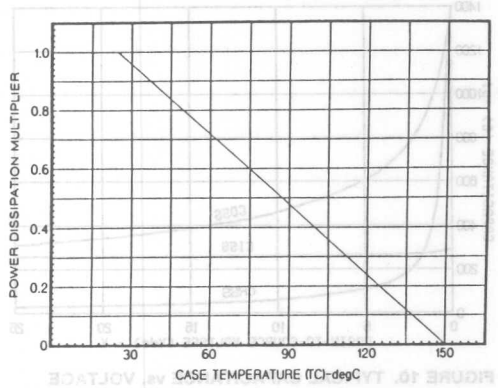


FIGURE 3. NORMALIZED POWER DISSIPATION vs. TEMPERATURE DERATING CURVE

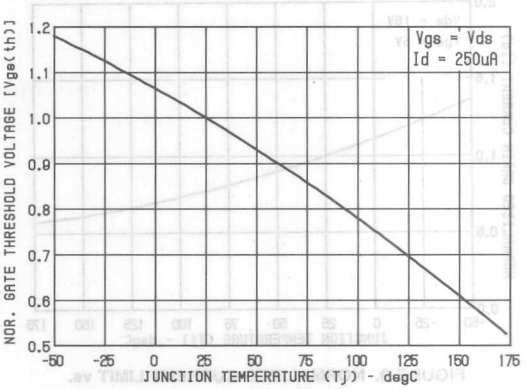


FIGURE 4. TYPICAL NORMALIZED GATE THRESHOLD VOLTAGE

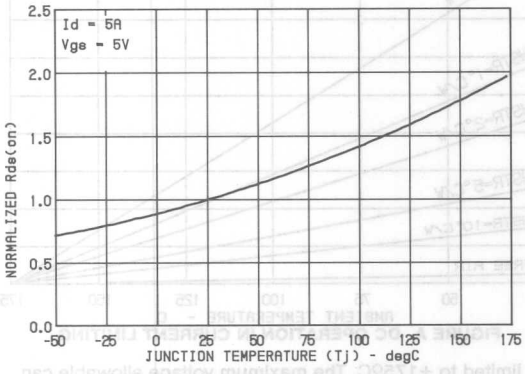


FIGURE 5. NORMALIZED $R_{DS(ON)}$ vs. JUNCTION TEMPERATURE

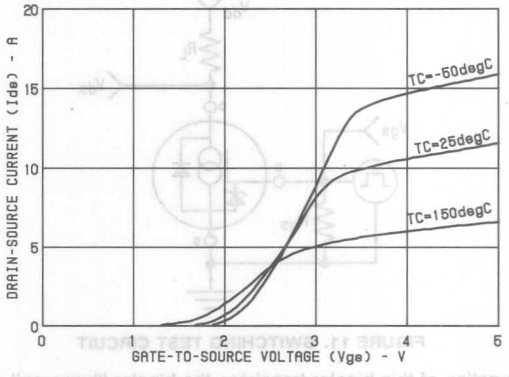


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

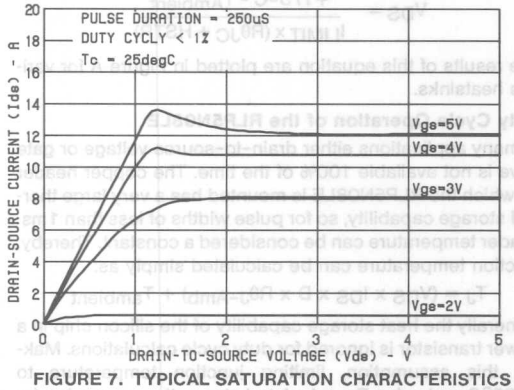


FIGURE 7. TYPICAL SATURATION CHARACTERISTICS

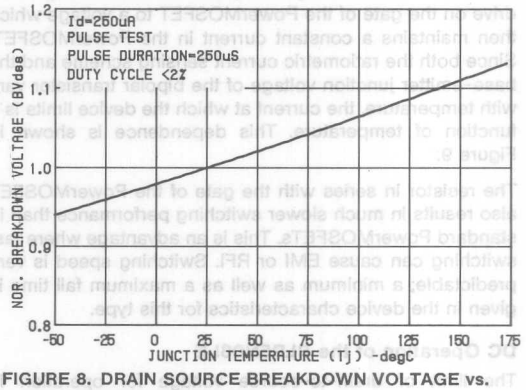


FIGURE 8. DRAIN SOURCE BREAKDOWN VOLTAGE vs. TEMPERATURE

Temperature Dependence of Current Limiting and Switching Speed Performance

The RLP5N08LE is a monolithic power device which incorporates a Logic Level PowerMOS transistor with a current sensing scheme and control circuitry to enable the device to self limit drain-source current flow. The current sensing scheme supplies current to a resistor that is connected across the base to emitter of a bipolar transistor in the control section. The collector of this bipolar transistor is connected to the gate of the PowerMOSFET. When the ratiometric current from the current sensing reaches the value required to forward bias the base-emitter

Performance Curves (Continued)

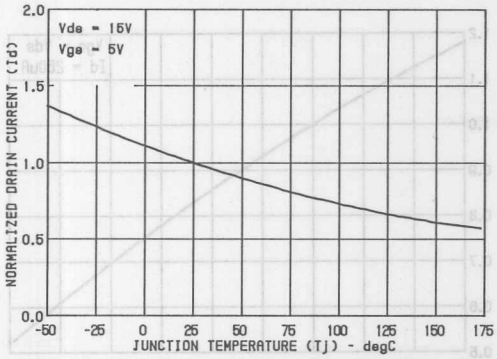


FIGURE 9. NORMALIZED CURRENT LIMIT vs. TEMPERATURE

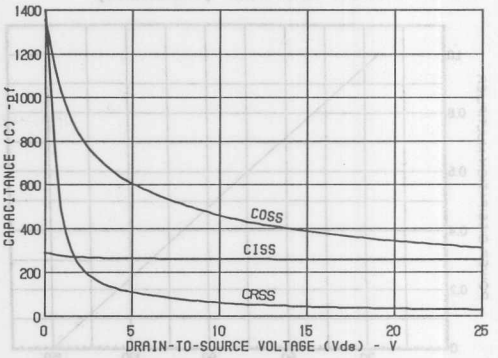


FIGURE 10. TYPICAL CAPACITANCE vs. VOLTAGE

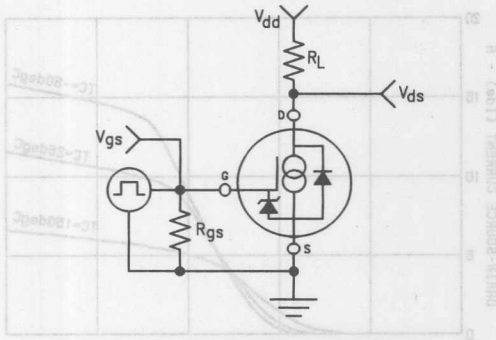


FIGURE 11. SWITCHING TEST CIRCUIT

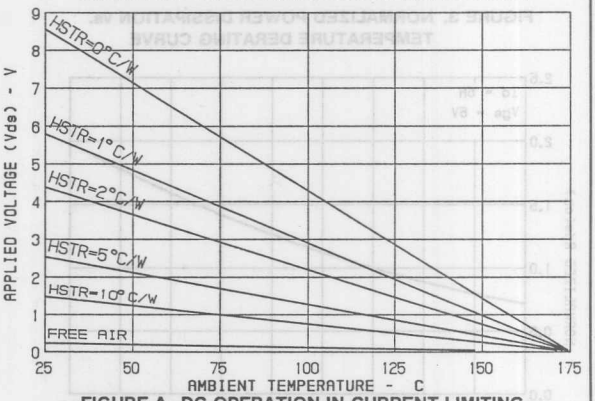


FIGURE A. DC OPERATION IN CURRENT LIMITING

junction of this bipolar transistor, the bipolar "turns-on". A resistor is incorporated in series with the gate of the PowerMOSFET allowing the bipolar transistor to adjust the drive on the gate of the PowerMOSFET to a voltage which then maintains a constant current in the PowerMOSFET. Since both the ratiometric current sensing scheme and the base-emitter junction voltage of the bipolar transistor vary with temperature, the current at which the device limits is a function of temperature. This dependence is shown in Figure 9.

The resistor in series with the gate of the PowerMOSFET also results in much slower switching performance than in standard PowerMOSFETs. This is an advantage where fast switching can cause EMI or RFI. Switching speed is very predictable; a minimum as well as a maximum fall time is given in the device characteristics for this type.

DC Operation of the RLP5N08LE

The limit of drain-to-source voltage for operation in current limiting on a steady state (DC) basis is shown in equation below. The dissipation in the device is simply the applied drain-to-source voltage multiplied by the limiting current. This device, like most PowerMOSFET devices, is limited to +175°C. The maximum voltage allowable can, therefore, be expressed as:

$$V_{DS} = \frac{+175^{o}C - T_{Ambient}}{I_{LIMIT} \times (R\theta_{JC} + HSTR)}$$

The results of this equation are plotted in Figure A for various heatsinks.

Duty Cycle Operation of the RLP5N08LE

In many applications either drain-to-source voltage or gate drive is not available 100% of the time. The copper header on which the RLP5N08LE is mounted has a very large thermal storage capability, so for pulse widths of less than 1ms header temperature can be considered a constant. Thereby, junction temperature can be calculated simply as:

$$T_J = (V_{DS} \times I_{DS} \times D \times R\theta_{J\text{-}Amb}) + T_{ambient}$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to +175°C and using T_C calculated above, the expression for maximum V_{DS} under duty cycle operation is:

$$V_{DS} = \frac{+175^{o}C - T_{ambient}}{I_{LIMIT} \times D \times R\theta_{J\text{-}ambient}}$$

These values are plotted as Figures B1 - B6 for various heatsink thermal resistances.

Performance Curves (Continued)

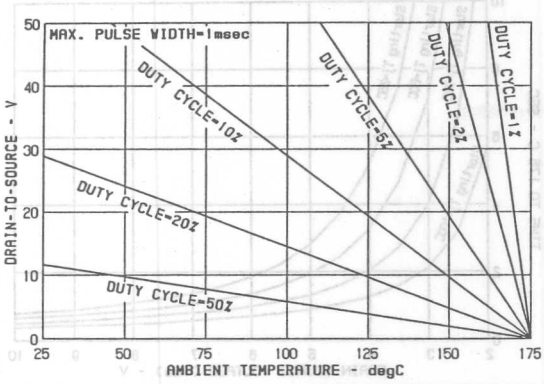


FIGURE B1. MAXIMUM V_{DS} vs. TEMPERATURE IN CURRENT LIMITING.
(HEATSINK THERMAL RESISTANCE = 1°C/W)
(T_J = +175°C, I_{LIMIT} = 5.5A, R_{JC} = 2.083°C/W)

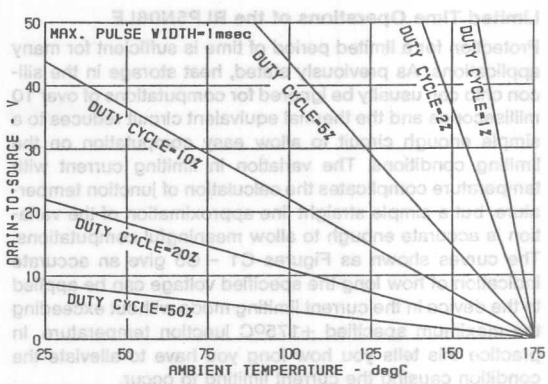


FIGURE B2. MAXIMUM V_{DS} vs. TEMPERATURE IN CURRENT LIMITING
(HEATSINK THERMAL RESISTANCE = 2°C/W)
(T_J = +175°C, I_{LIMIT} = 5.5A, R_{JC} = 2.083°C/W)

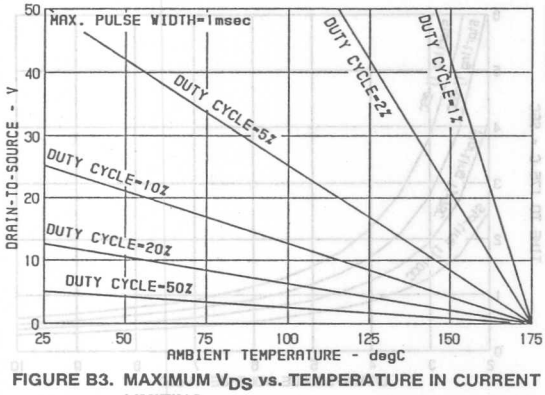


FIGURE B3. MAXIMUM V_{DS} vs. TEMPERATURE IN CURRENT LIMITING.
(HEATSINK THERMAL RESISTANCE = 5°C/W)
(T_J = +175°C, I_{LIMIT} = 5.5A, R_{JC} = 2.083°C/W)

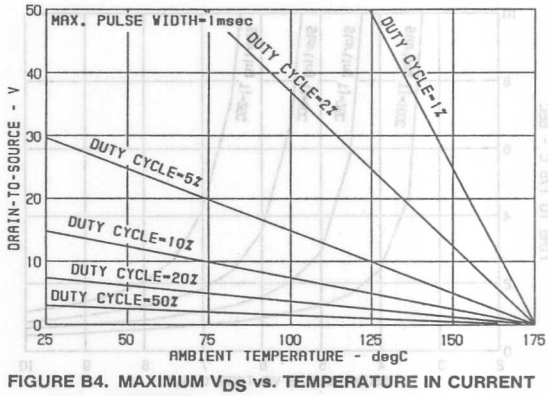


FIGURE B4. MAXIMUM V_{DS} vs. TEMPERATURE IN CURRENT LIMITING.
(HEATSINK THERMAL RESISTANCE = 10°C/W)
(T_J = +175°C, I_{LIMIT} = 5.5A, R_{JC} = 2.083°C/W)

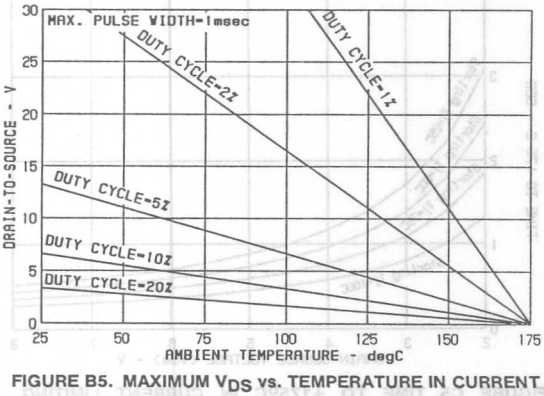


FIGURE B5. MAXIMUM V_{DS} vs. TEMPERATURE IN CURRENT LIMITING.
(HEATSINK THERMAL RESISTANCE = 25°C/W)
(T_J = +175°C, I_{LIMIT} = 5.5A, R_{JC} = 2.083°C/W)

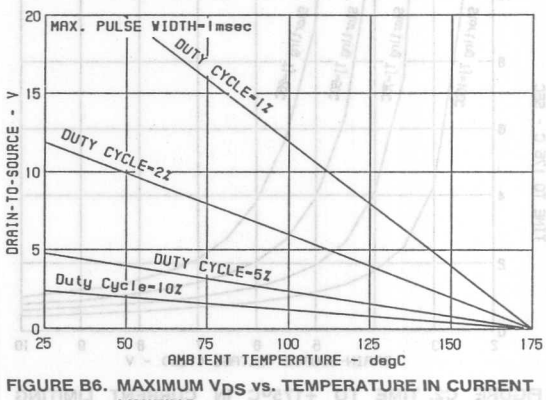


FIGURE B6. MAXIMUM V_{DS} vs. TEMPERATURE IN CURRENT LIMITING.
(NO EXTERNAL HEATSINK)
(T_J = +175°C, I_{LIMIT} = 5.5A, R_{JC} = 2.083°C/W)

Performance Curves (Continued)

Limited Time Operations of the RLP5N08LE

Protection for a limited period of time is sufficient for many applications. As previously stated, heat storage in the silicon chip can usually be ignored for computations of over 10 milliseconds and the thermal equivalent circuit reduces to a simple enough circuit to allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as Figures C1 - C5 give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified +175°C junction temperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

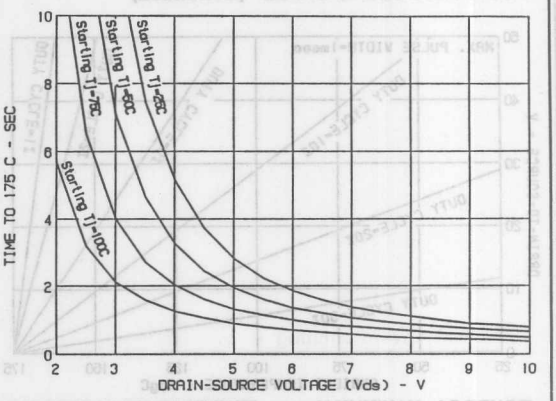


FIGURE C3. TIME TO +175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 5°C/W, HEATSINK THERMAL CAPACITANCE = 2J/°C)

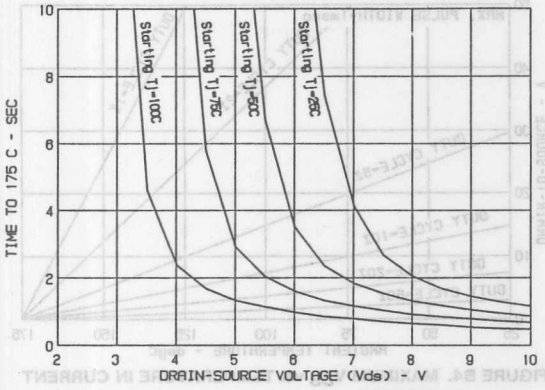


FIGURE C1. TIME TO +175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 1°C/W, HEATSINK THERMAL CAPACITANCE = 8J/°C)

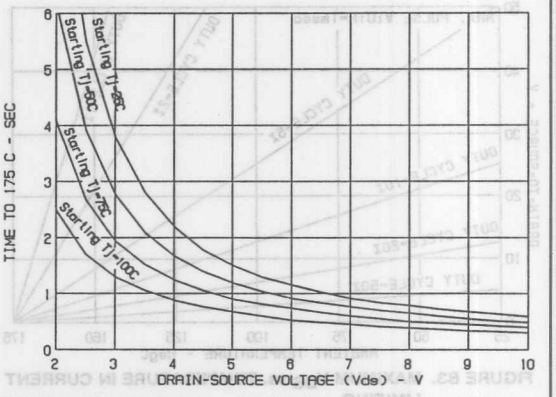


FIGURE C4. TIME TO +175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 10°C/W, HEATSINK THERMAL CAPACITANCE = 1J/°C)

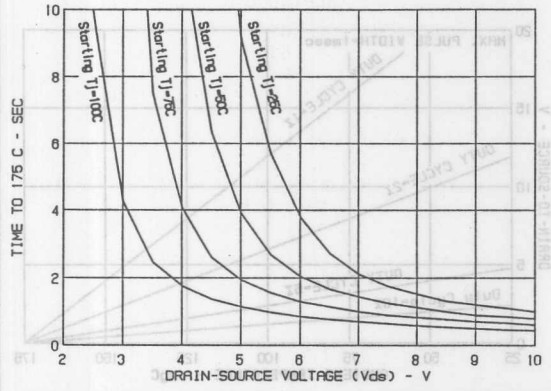


FIGURE C2. TIME TO +175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 2°C/W, HEATLINK THERMAL CAPACITANCE = 4J/°C)

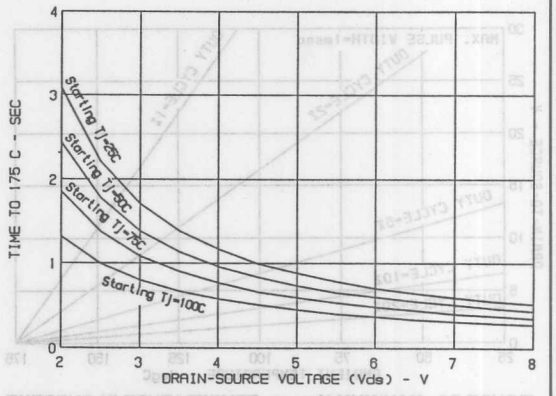


FIGURE C5. TIME TO +175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 25°C/W, HEATSINK THERMAL CAPACITANCE = 0.5J/°C)

HARRIS RLP1N06CLE

Voltage-Clamping Current-Limited ESD-Protected N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

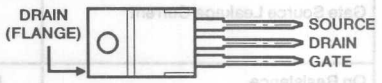
- 1A, 55V
- $R_{DS(ON)}$ 0.75Ω
- I_{Limit} ..... 1.1A to 1.5A Max @ +150°C
- Built In Voltage Clamp
- Built In Current Limiting
- E_{SD} Protected ..... 2KV Min
- Controlled Switching Limits EMI and RFI
- +175°C Rated Junction Temperature
- Logic Level Gate

Description

The RLP1N06CLE is an intelligent monolithic power circuit which incorporates a lateral bipolar transistor, resistors, zener diodes, and a PowerMOS transistor. The current limiting of this device allows it to be used safely in circuits where it is anticipated that a shorted load condition may be encountered. The drain-source voltage clamping offers precision control of the circuit voltage when switching inductive loads. "Logic Level" gates allow this device to be fully biased on with only 5.0V from gate to source. Input protection is provided for ESD up to 2KV.

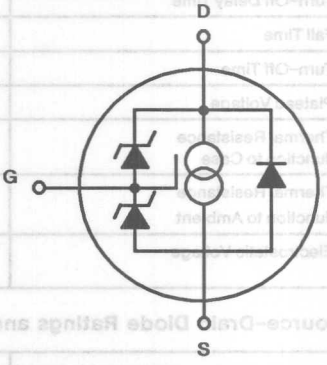
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RLP1N06CLE	UNITS
Drain-Source Voltage	V_{DSS}	55	V
Drain-Gate Voltage	V_{DGR}	55	V
Gate-Source Voltage*	V_{GS}	5.5	V
Reverse Voltage Gate Bias Not Allowed			
Electrostatic Voltage at T_C = +25°C	ESD	2	kV
Drain Current, Continuous	I_D	Self Limited	
Power Dissipation Total @ T_C = +25°C	P_D	36	W
Power Dissipation Derating T_C > +25°C		0.24	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +175	°C

* May be exceeded if current is limited to 10mA.

8 INTELLIGENT DISCRETES

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2839

Electrical Characteristics At Case Temperature (T_C = +25°C), Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain Source Breakdown Voltage	BV_{DSS}	I_D = 20mA V_{GS} = 0V	55	70	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS} I_D = 0.25mA	1	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 45V V_{GS} = 0V	-	5	µA
		at T_C = +150°C	-	20	µA
Gate Source Leakage Current	I_{GSS}	V_{GS} = 5V	-	5	µA
		at T_C = +150°C	-	20	µA
On Resistance	$R_{DS(ON)}$	I_D = 1A V_{GS} = 5.0V	-	0.75	Ω
		at T_C = +150°C	-	1.5	Ω
Limiting Current	$I_{DS(Limit)}$	V_{DS} = 15.0V V_{GS} = 5.0V	1.8	3	A
		@ T_C = 150°C	0.9	1.5	A
Turn-On Time	$t_{(ON)}$	V_{DD} = 30.0V	-	6.5	µs
Turn-On Delay Time	$t_{D(ON)}$	I_D = 1A	-	1.5	µs
Rise Time	t_R	V_{GS} = 5.0V	1.0	5.0	µs
Turn-Off Delay Time	$t_{D(OFF)}$	R_{GS} = 25Ω	-	7.5	µs
Fall Time	t_F	R_L = 30Ω	1.0	5.0	ms
Turn-Off Time	$t_{(OFF)}$		-	12.5	µs
Plateau Voltage	$V_{(PLATEAU)}$	I_D = 1A V_{DS} = 15.0V	-	5.0	V
Thermal Resistance Junction to Case	$R\theta_{JC}$		-	4.17	°C/W
Thermal Resistance Junction to Ambient	$R\theta_{JC}$		-	80	°C/W
Electrostatic Voltage	E_{SD}	Human Model (100pF, 1.5kΩ) Mil-Std-883B (Category B2)	2000	-	V

Source-Drain Diode Ratings and Characteristics

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 5.5A	-	1.5	V
Reverse Recovery Time	T_{RR}	I_F = 5.5A	-	1.0	ms

Performance Curves

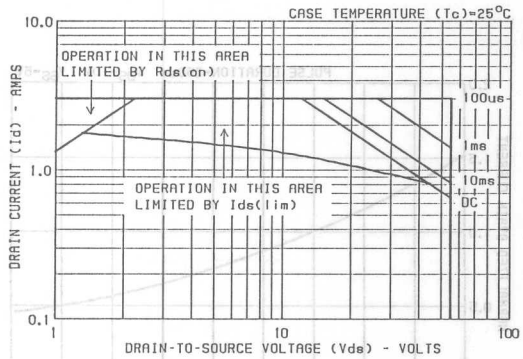


FIGURE 1. SAFE-OPERATING-AREA CURVE

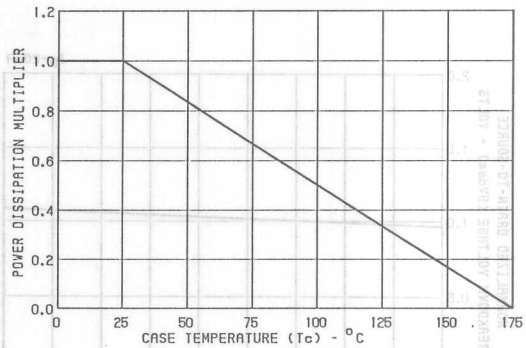


FIGURE 2. NORMALIZED POWER DISSIPATION vs. TEMPERATURE DERATING CURVE

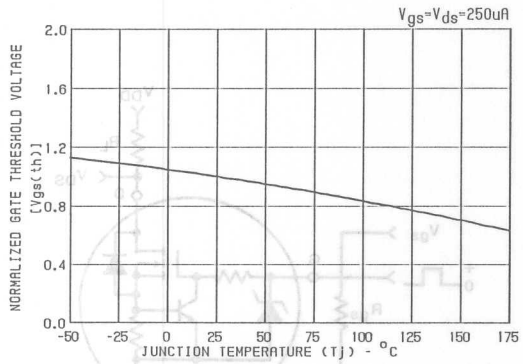


FIGURE 3. TYPICAL NORMALIZED GATE-THRESHOLD VOLTAGE

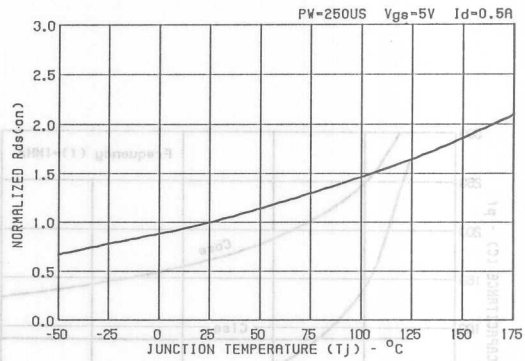


FIGURE 4. NORMALIZED $r_{DS(ON)}$ vs. JUNCTION TEMPERATURE

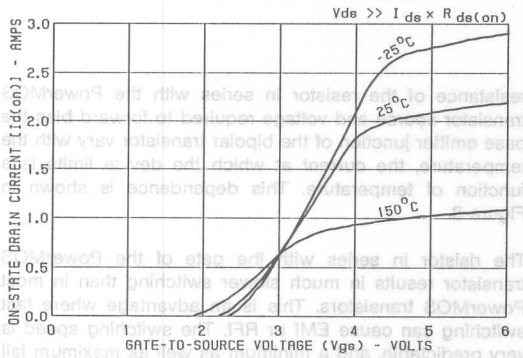


FIGURE 5. TYPICAL TRANSFER CHARACTERISTICS

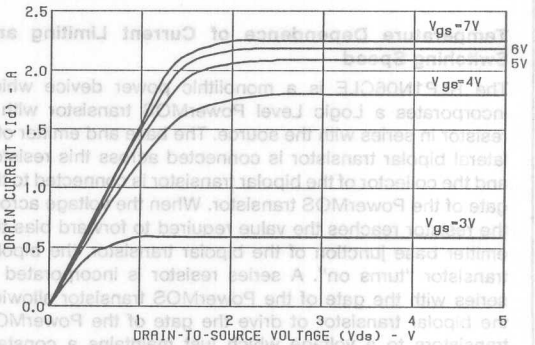


FIGURE 6. TYPICAL SATURATION CHARACTERISTICS

8

INTELLIGENT DISCRETES

Performance Curves (Continued)

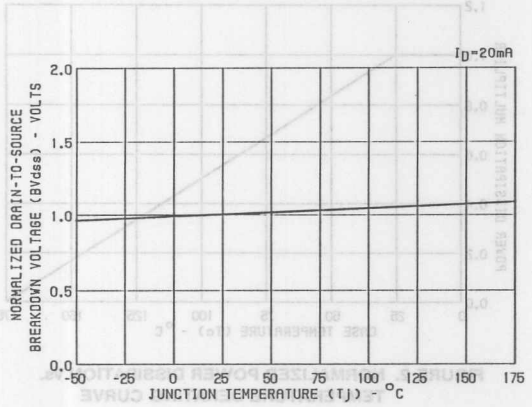


FIGURE 7. DRAIN-SOURCE BREAKDOWN VOLTAGE vs. TEMPERATURE

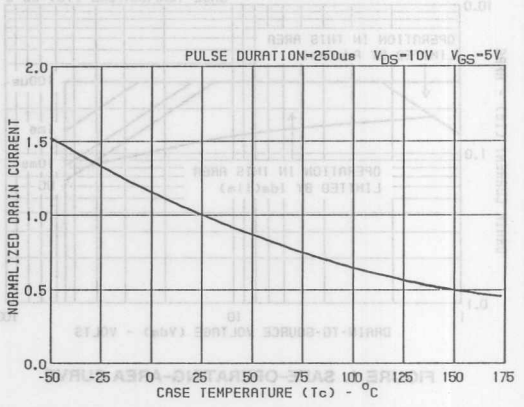


FIGURE 8. NORMALIZED CURRENT LIMIT vs. TEMPERATURE

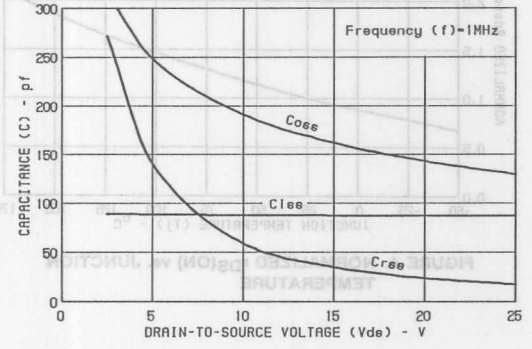


FIGURE 9. TYPICAL CAPACITANCE vs. VOLTAGE

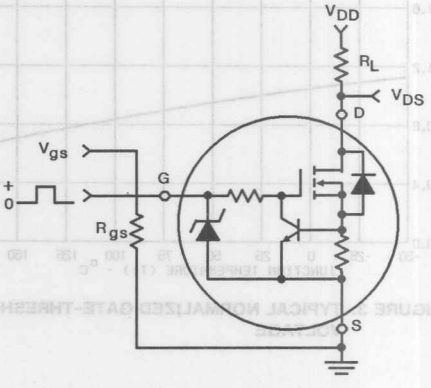


FIGURE 10. SWITCHING TEST CIRCUIT

Temperature Dependence of Current Limiting and Switching Speed

The RLP1N06CLE is a monolithic power device which incorporates a Logic Level PowerMOS transistor with a resistor in series with the source. The base and emitter of a lateral bipolar transistor is connected across this resistor, and the collector of the bipolar transistor is connected to the gate of the PowerMOS transistor. When the voltage across the resistor reaches the value required to forward bias the emitter base junction of the bipolar transistor, the bipolar transistor "turns on". A series resistor is incorporated in series with the gate of the PowerMOS transistor allowing the bipolar transistor ot drive the gate of the PowerMOS transistors to a voltage which just maintains a constant current in the PowerMOS transistor. Since both the resistance of the resistor in series with the PowerMOS transistor source and voltage required to forward bias the base emitter junction of the bipolar transistor vary with the temperature, the current at which the device limits is a function of temperature. This dependence is shown in Figure 8.

The risistor in series with the gate of the PowerMOS transistor results in much slower switching than in most PowerMOS transistors. This is an advantage where fast switching can cause EMI or RFI. The switching speed is very predictable, and a minimum as well as maximum fall time is given in the device characteristics for this type.

Performance Curves (Continued)

DC Operation of the RLP1N06CLE

The limit of the drain-to-source voltage for operation in current limiting on a steady state (DC) basis is shown as Figure A. The dissipation in the device is simply the applied drain-to-source voltage multiplied by the limiting current. This device, like most PowerMOSFET devices today, is limited to +150°C. The maximum voltage allowable can, therefore, be expressed as:

$$V_S = \frac{+150^oC - T_{Ambient}}{I_{LIMIT} \times (R\theta_{JC} + R\theta)}$$

Duty Cycle Operation of the RLP1N06CLE

In many applications either the drain-to-source voltage or the gate drive is not available 100% of the time. The copper header on which the RLP1N06CLE is mounted has a very large thermal storage capability, so for pulse widths of less than 100 milliseconds, the temperature of the header can be considered a constant case temperature calculated simply as:

$$T_C = (V_{SD} \times I_D \times D \times R\theta_{CA}) + T_{ambient}$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to +150°C and using the T_C calculated above, the expression for maximum V_{SD} under duty cycle operation is:

$$V_{SD} = \frac{+175^oC - T_C}{I_{LIMIT} \times D \times R\theta_{JC}}$$

These values are plotted as Figures B1 - B5 for various heatsink thermal resistances.

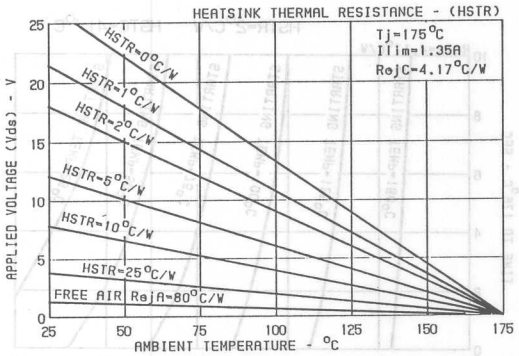


FIGURE A. DC OPERATION IN CURRENT LIMITING

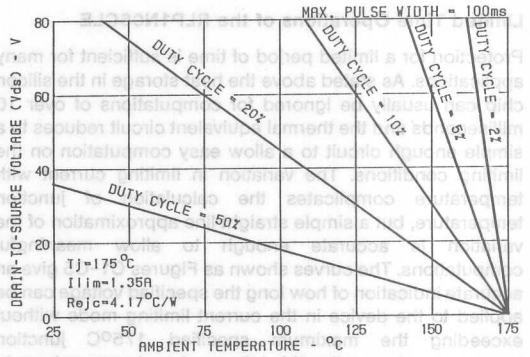


FIGURE B1. MAXIMUM V_{DS} vs. AMBIENT TEMPERATURE IN CURRENT LIMITING. (HEATSINK THERMAL RESISTANCE = 2°C/W)

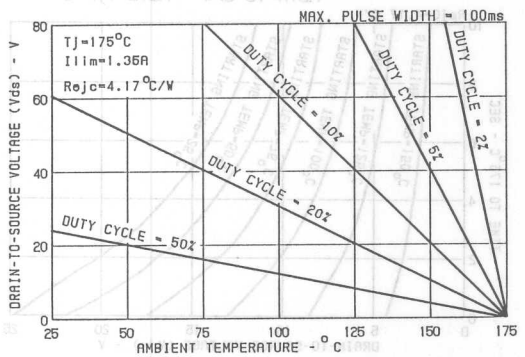


FIGURE B2. MAXIMUM V_{DS} vs. AMBIENT TEMPERATURE IN CURRENT LIMITING. (HEATSINK THERMAL RESISTANCE = 5°C/W)

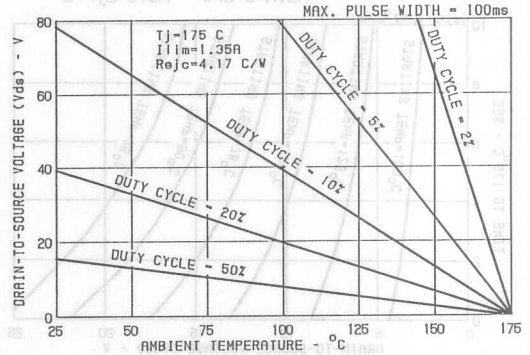


FIGURE B3. MAXIMUM V_{DS} vs. AMBIENT TEMPERATURE IN CURRENT LIMITING. (HEATSINK THERMAL RESISTANCE = 10°C/W)

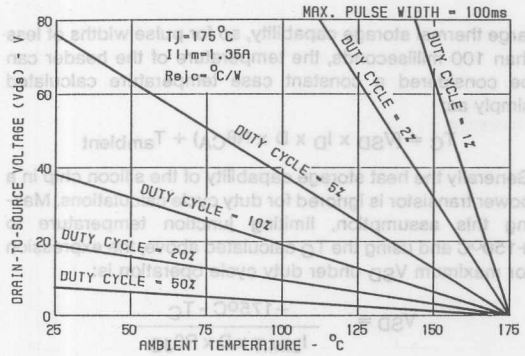


FIGURE B4. MAXIMUM V_{DS} vs. AMBIENT TEMPERATURE IN CURRENT LIMITING. (HEATSINK THERMAL RESISTANCE = 25°C/W)

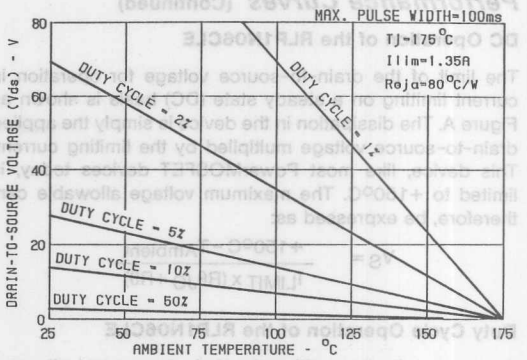


FIGURE B5. MAXIMUM V_{DS} vs. AMBIENT TEMPERATURE IN CURRENT LIMITING. (NO EXTERNAL HEATSINK)

Limited Time Operations of the RLP1N06CLE

Protection for a limited period of time is sufficient for many applications. As stated above the heat storage in the silicon chip can usually be ignored for computations of over 10 milliseconds and the thermal equivalent circuit reduces to a simple enough circuit to a allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as Figures C1-C5 give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified 175°C junction temperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

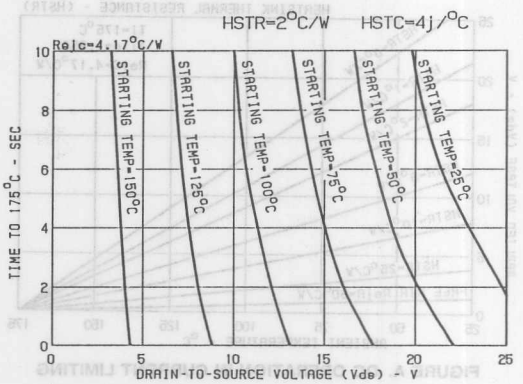


FIGURE C1. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 2°C/W HEATSINK THERMAL CAPACITANCE = 4j/°C)

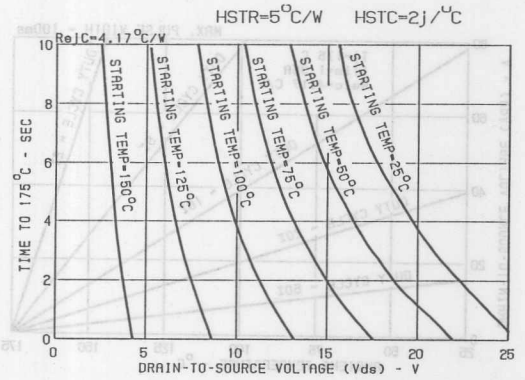


FIGURE C2. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 5°C/W HEATSINK THERMAL CAPACITANCE = 2j/°C)

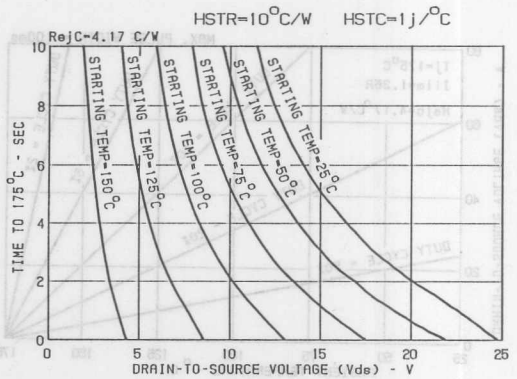


FIGURE C3. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 10°C/W HEATSINK THERMAL CAPACITANCE = 1j/°C)

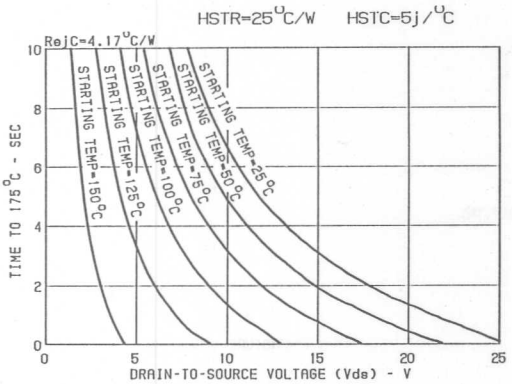


FIGURE C4. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 25°C/W HEATSINK THERMAL CAPACITANCE = 5j/°C)

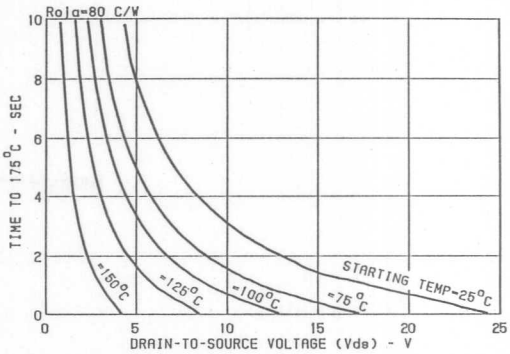


FIGURE C5. TIME TO 175°C IN CURRENT LIMITING (NO EXTERNAL HEATSINK)

FIGURE C4. TIME TO 175°C IN CURRENT LIMITING
(HEATSINK THERMAL RESISTANCE = 25°C/W
HEATSINK THERMAL CAPACITANCE = 5J/°C)

FIGURE C5. TIME TO 175°C IN CURRENT LIMITING
(NO EXTERNAL HEATSINK)

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Military Power Products

Military and aerospace requirements for high-reliability solid-state devices are extremely large and diverse, not only in terms of performance, operating conditions, and reliability, but also in terms of logistics and procurement. As a result of these requirements, the military services have jointly developed specifications and standards under which most military end-use solid-state devices are procured. To simplify procurement, logistics, and the development of reliability data, MIL specs are not issued for the full spectrum of devices manufactured: rather, they are restricted to those devices for which significant need is demonstrated and are specified so that the device can have as wide applicability as possible. Although the limits for operating conditions may exceed these required for some applications, they simplify procurement and assure a supply of devices for the majority of military equipment. These standards also cover a wide range of requirements for the manufacturer on such things as:

(a) The procedure and requirements for a manufacturer to become certified to manufacture MIL-spec parts.

(b) The requirements for qualifying parts.

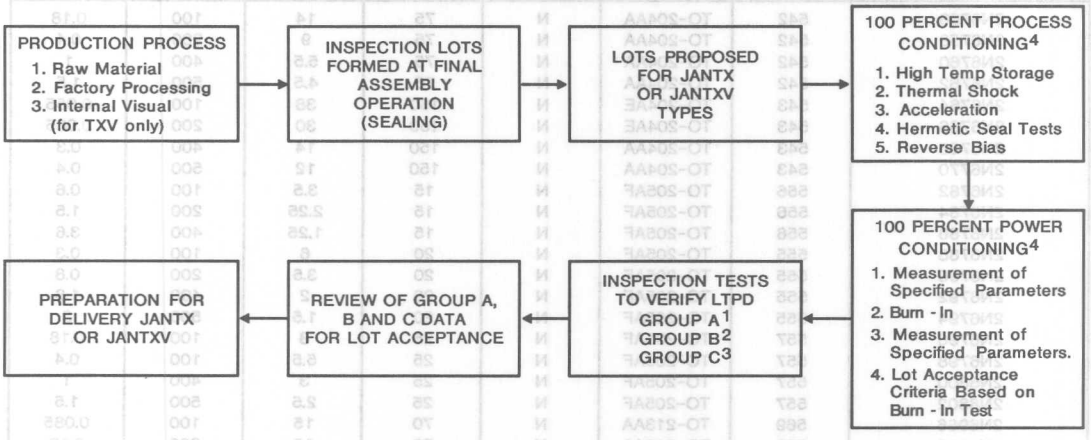
(c) Product-assurance provisions, in such areas as quality control, inspection procedures, personnel training, cleanliness, failure analysis, and documentation.

(d) Test methods and procedures.

(e) Marking and identification of product.

(f) Preservation and packing.

JANTX and JANTXV Products Flow Chart



NOTES:

1. Group A electrical performance tests performed on a lot sample basis.
2. Group B environmental, mechanical and life tests (storage and operating) performed on a lot sample basis.
3. Group C environmental and life tests performed on a time period basis.
4. Tests shall be performed in the order as shown.

JANTX and JANTXV Solid-State Power Devices

The major military specification used for the procurement of discrete solid-state devices by the military is MIL-S-19500.

MIL-S-19500 is the specification for the familiar "JAN" type solid state devices. Detailed electrical specifications are prepared as needed by the three military services and coordinated by the Defense Electronic Supply Center (DESC).

Levels of reliability are defined by MIL-S-19500. JANTX types receive 100 percent process conditioning, and power conditioning, and are subjected to lot acceptance based on delta parameter criteria in addition to Group A, Group B, and Group C lot sampling. JANTXV types are subjected to 100 percent (JTXV) internal visual inspection in addition to all of the JANTX tests in accordance with MIL-STD-750 test methods and MIL-S-19500.

DESC publishes "QPL-19500", a Qualified Products List of all types and suppliers approved to produce and brand devices in accordance with MIL-S-19500.

The following tables list approved "QPL" types that Harris can supply.

Most of Harris Power MOSFETs can also be supplied with similar process and power conditioning tests and delta criteria.

QPL APPROVED TYPES JANTX POWER MOSFETs

N-CHANNEL TYPES	MIL-S-19500/	PACKAGE	CHANNEL	P_T (W)	I_D (A)	BV_{DSS} (V)	$r_{DS(ON)}$ Ω
2N6756	542	TO-204AA	N	75	14	100	0.18
2N6758	542	TO-204AA	N	75	9	200	0.4
2N6760	542	TO-204AA	N	75	5.5	400	1
2N6762	542	TO-204AA	N	75	4.5	500	1.5
2N6764	543	TO-204AE	N	150	38	100	0.055
2N6766	543	TO-204AE	N	150	30	200	0.085
2N6768	543	TO-204AA	N	150	14	400	0.3
2N6770	543	TO-204AA	N	150	12	500	0.4
2N6782	556	TO-205AF	N	15	3.5	100	0.6
2N6784	556	TO-205AF	N	15	2.25	200	1.5
2N6786	556	TO-205AF	N	15	1.25	400	3.6
2N6788	555	TO-205AF	N	20	6	100	0.3
2N6790	555	TO-205AF	N	20	3.5	200	0.8
2N6792	555	TO-205AF	N	20	2	400	1.8
2N6794	555	TO-205AF	N	20	1.5	500	3
2N6796	557	TO-205AF	N	25	8	100	0.18
2N6798	557	TO-205AF	N	25	5.5	100	0.4
2N6800	557	TO-205AF	N	25	3	400	1
2N6802	557	TO-205AF	N	25	2.5	500	1.5
2N6966	569	TO-213AA	N	70	15	100	0.085
2N6967	569	TO-213AA	N	70	13	200	0.18
2N6968	569	TO-213AA	N	70	7.5	400	0.55
2N6969	569	TO-213AA	N	70	6.0	500	0.85
P-CHANNEL TYPES	**MIL-S-19500/**	**PACKAGE**	**CHANNEL**	**P_T (W)**	**I_D (A)**	**BV_{DSS} (V)**	**$r_{DS(ON)}$ Ω**
2N6895	565	TO-205AF	P	8.33	-1.5	-100	3.65
2N6896	565	TO-204AA	P	60	-6	-100	0.6
2N6897	565	TO-204AA	P	100	-12	-100	0.3
2N6898	565	TO-204AE	P	150	-25	-100	0.2
2N6849	564	TO-205AF	P	25	-6.5	-100	0.3
2N6851	564	TO-205AF	P	25	-4.0	-200	0.8
N-CHANNEL LOGIC-LEVEL TYPES	**MIL-S-19500/**	**PACKAGE**	**CHANNEL**	**P_T (W)**	**I_D (A)**	**BV_{DSS} (V)**	**$r_{DS(ON)}$ Ω**
2N6901	570	TO-205AF	N	8.33	1.69	100	1.4
2N6902	566	TO-204AA	N	75	12	100	0.2
2N6903	570	TO-205AF	N	8.33	0.98	200	3.65
2N6904	566	TO-204AA	N	75	8	200	0.65

Military Screening For Non QPL Types

New discrete devices not yet covered by military specifications, offer technological advances or have special performance characteristics which have advantages to the designer of Military and Aerospace equipment. Harris cooperates with the users in establishment of specifications patterned after MIL standards.

Harris Military Power Products are processed in accordance with provisions of MIL STD. The desired screening test sequence can be chosen from the models shown in the screening table.

Group B and Group C tests will be performed when requested in accordance with MIL-S-19500.

MILITARY SCREENING FOR NON QPL TYPES

SCREEN	MIL-S-19500 MIL-STD-750 METHOD	CONDITION	JANS REQUIREMENTS	JANTXV REQUIREMENTS	JANTX REQUIREMENTS
1. Internal Visual	2069	Bipolar Trans. MOSFETs	100%	100%	-
2. High Temp Life (LTPD) (Stabilization Bake)	1032	24 hrs. min at max rated storage temperature	Optional	Optional	Optional
3. Thermal Shock (Temp. Cycling)	1051	No dwell is required at 25°C. Test condition C. 20 cycles, t (extremes) > 10 min.	100%	100%	100%
4. Constant Acceleration (Note 1)	2006	Y_1 direction at 20,000 G min except at 10,000 G min for devices with power rating of > 10 watts at T_C = 25°C. The 1 min hold time requirement shall not apply.	100%	Optional	Optional
5. Particle Impact Noise Detection	2052	Condition A	100%	-	-
6. Hermetic Seal Fine (Note 1)	1071	Test condition G or H, max leak rate = $5x10^{-8}$ atm cc/s except $5x10^{-7}$ atm cc/s for devices with internal cavity > 0.3cc.	Optional if done in screen 14.	100% (Note 4)	100% (Note 4)
Gross		Test condition C or D.	Optional	100% (Note 4)	100% (Note 4)
7. Serialization		See 3.7.9	100%		
8. Interim Electrical Parameters		As specified.	100% (read and record)		
9. High Temp Reverse Bias (HTRB)		48 hrs min at T_A = 150°C (min) and minimum applied voltage as follows:			
Burn-In for Bipolar Transistors	1039	Condition A Bipolar transistors (min) of rated V_{CB}	100%	100%	100%
Burn-In for MOSFETs	1042	Condition B MOSFETs 80% (min) of rated V_{GS}			

SCREEN	MIL-STD-750 METHOD	CONDITION	JANS REQUIREMENTS	JANTXV REQUIREMENTS	JANTX REQUIREMENTS
10. Interim Electrical and Delta Parameters		As specified but including all delta parameters as a minimum. Leakage current shall be measured on each device before any other test is made.	100% (Measure all specified parameters within 16 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 12)	100% (Measure all specified parameters within 24 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 12)	100% (Measure all specified parameters within 24 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 12)
11. Power Burn-In		As specified	100%	100%	100%
Burn-In (Transistors)	1039	Transistors. Test condition B.	240 hrs (min)	160 hrs (min)	160 hrs (min)
Burn-In MOSFETs	1042	MOSFETs A	240 hrs (min)	160 hrs (min)	160 hrs (min)
12. Final Electrical Test		As specified.	100%	100%	100%
Interim Electrical		All interim and delta parameter measurements must be completed within 96 hrs after removal from burn-in conditions	Interim electrical and delta parameters as a minimum. (Read and record.)	Interim electrical and delta parameters as a minimum. (Read and record.)	Interim electrical and delta parameters as a minimum. (Read and record.)
Other Electrical Parameters			Group A, sub-groups 2 and 3.	Group A, sub-groups 2 and 3.	Group A, sub-groups 2 and 3.
13. Hermetic Seal	1071	(Same as 5 on previous page) (Note 2)	100%	Optional (Note 4)	Optional (Note 4)
Fine (Note 1)					
Gross					
13. Radiography	2076	(Note 2)	100%	-	-
14. External Visual Examination	2071	To be performed after complete marking.	100%	-	-

NOTE:

1. Omit fine leak seal test and constant acceleration test for double plug, non-internal cavity diode construction.
2. The radiographic and seal screens for JANS may be performed in any order following final electrical test. Glass diodes shall not be painted until after seal tests. When hermetic seal testing is performed in screen 5 it does not have to be performed again in screen 12 for double plug, non-internal cavity diode construction.
3. Reverse-blocking test shall replace power burn-in for power rectifiers at $\geq$ 10 amp rating at $T_C \geq 100^{o}C$ and all thyristors.
4. Fine and gross seal leak test for JANTX and JANTXV shall be performed in either block 6 or block 13.

DESC Standard Military Drawing Types

New TO-204 and TO-254 packaged rugged n-channel MOSFETs are available to DESC standard military drawings. These types are tested to JANTX and JANTXV reliability levels.

DESC SMD #	TYPE	JAN	JTX	TXV	PACKAGE	P_D (W)	I_D (A)	BV_{DSS} (V)	r_{DS} (ON) Ω
89009	2N7119	–	X	X	TO-204AA	75	14	100	0.18
89009	2N7120	–	X	X	TO-204AA	75	9	200	0.40
89009	2N7121	–	X	X	TO-204AA	75	5.5	400	1.0
89009	2N7122	–	X	X	TO-204AA	75	4.5	500	1.5
89007	2N7123	–	X	X	TO-204AE	150	38	100	0.055
89007	2N7124	–	X	X	TO-204AE	150	30	200	0.085
89007	2N7125	–	X	X	TO-204AA	150	14	400	0.30
89007	2N7126	–	X	X	TO-204AA	150	12	500	0.40
89026	2N7224	–	X	X	TO-254AA	150	30	100	0.07
89026	2N7225	–	X	X	TO-254AA	150	27	200	0.10
89026	2N7227	–	X	X	TO-254AA	150	14	400	0.315
89026	2N7228	–	X	X	TO-254AA	150	12	500	0.415
89025	2N7241	–	X	X	TO-254AA	75	14	100	0.195
89025	2N7242	–	X	X	TO-254AA	75	9	200	0.415
89025	2N7243	–	X	X	TO-254AA	75	5.5	400	1.0
89025	2N7244	–	X	X	TO-254AA	75	4.5	500	1.5

Introduction To Rad Hard MOSFETs

Tactical Applications

- Radiation Hardness Assurance Program
- Rated at 10K Rads (Si)

The Harris Semiconductor Sector has formed a Radiation Hardness Assurance Program (RHAP) directed toward certain TACTICAL rad hard users which assures a minimum level of hardness for "off the shelf" needs where the volume of application mandates economy. Power MOSFET's from the FR series are a part of the RHAP effort. The FR parts are not selected from standard commercial product but are semiconductor die specially designed, processed, and treated for SECOND GENERATION hardened power MOSFET'S. Pre radiation specifications are met after exposure to 10 KRAD (Si) total dose.

Strategic Applications

- Rated at 100K and 1000K Rad(Si)

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFET's of both N and P channel enhancement types with ratings from 100 to 500 volts, 1 to 60 amperes, and on resistance as low as 40 milliohms. Total dose hardness is offered at 100K and 1000K RAD(Si) with neutron hardness ranging from 1E13 n/cm2 for 500 volt product to 1E14 n/cm2 for 100 volt product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 rads/sec without current limiting and 2E12 rads/sec with current limiting. Heavy ion survival from single event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

Harris Rad Hard MOS Nomenclature

FR	I	XXXX	X	X

RELIABILITY SCREENING LEVEL

1. Commercial (Non TX)
2. TX Equivalent of MIL-S-19500
3. TXV Equivalent of MIL-S-19500
4. Space Equivalent of MIL-S-19500

RADIATION LEVEL ASSURANCE

D - 10K rads (Si)

R - 100K rads (Si)

H - 1 Megarad (Si)

DIE DESIGNATION

3 or 4 Characters

PACKAGE DESIGNATION

M - TO-204AA

K - TO-204AE

L - TO-205AF

S - TO 257AA

F - TO-254AA

HARRIS RADIATION HARDENED MOSFETs

Radiation Hardness Assurance Program

N-CHANNEL RAD HARD POWER MOSFETS

PART NO.	DIE SIZE (MILS)	DIE SIZE	INITIAL RATINGS				POST RAD: 10K RADS		
			MAX RATED BV_{DSS}	MAX RATED I_{DS}	MAX RATED r_{DS} (ON)	V_{GS} (TH) (V)	BV_{DSS} (V)	r_{DS} (ON) (Ω)	V_{GS} (TH) (V)
FRM130D	126 X 182	3	100	14	0.18	2 - 4	100	0.18	2 - 4
FRM230D	126 X 182	3	200	8	0.50	2 - 4	200	0.50	2 - 4
FRM234D	126 X 182	3	250	7	0.70	2 - 4	250	0.70	2 - 4
FRM430D	126 X 182	3	500	3	2.50	2 - 4	500	2.50	2 - 4
FRL130D	126 X 182	3	100	8	0.18	2 - 4	100	0.18	2 - 4
FRL230D	126 X 182	3	200	5	0.50	2 - 4	200	0.50	2 - 4
FRL234D	126 X 182	3	250	4	0.70	2 - 4	250	0.70	2 - 4
FRL430D	126 X 182	3	500	2	2.50	2 - 4	500	2.50	2 - 4
FRS130D	126 X 182	3	100	12	0.195	2 - 4	100	0.195	2 - 4
FRS230D	126 X 182	3	200	7	0.515	2 - 4	200	0.515	2 - 4
FRS234D	126 X 182	3	250	4	0.715	2 - 4	250	0.715	2 - 4
FRS430D	126 X 182	3	500	3	2.52	2 - 4	500	2.52	2 - 4
FRM140D	170 X 200	4	100	23	0.13	2 - 4	100	0.13	2 - 4
FRM240D	170 X 200	4	200	16	0.24	2 - 4	200	0.24	2 - 4
FRM244D	170 X 200	4	250	12	0.40	2 - 4	250	0.40	2 - 4
FRM440D	170 X 200	4	500	6	1.40	2 - 4	500	1.40	2 - 4
FRS140D	170 X 200	4	100	23	0.145	2 - 4	100	0.145	2 - 4
FRS240D	170 X 200	4	200	12	0.255	2 - 4	200	0.255	2 - 4
FRS244D	170 X 200	4	250	9	0.415	2 - 4	250	0.415	2 - 4
FRS440D	170 X 200	4	500	5	1.42	2 - 4	500	1.42	2 - 4
FRK150D	259 X 265	5	100	40	0.055	2 - 4	100	0.055	2 - 4
FRK250D	259 X 265	5	200	27	0.10	2 - 4	200	0.10	2 - 4
FRK254D	259 X 265	5	250	20	0.17	2 - 4	250	0.17	2 - 4
FRM450D	259 X 265	5	500	10	0.60	2 - 4	500	0.60	2 - 4
FRF150D	259 X 265	5	100	25	0.07	2 - 4	100	0.07	2 - 4
FRF250D	259 X 265	5	200	23	0.115	2 - 4	200	0.115	2 - 4
FRF254D	259 X 265	5	250	17	0.185	2 - 4	250	0.185	2 - 4
FRF450D	259 X 265	5	500	9	0.615	2 - 4	500	0.615	2 - 4
FRK160D	266 X 366	6	100	66	0.04	2 - 4	100	0.04	2 - 4
FRK260D	266 X 366	6	200	46	0.07	2 - 4	200	0.07	2 - 4
FRK264D	266 X 366	6	250	34	0.12	2 - 4	250	0.12	2 - 4
FRK460D	266 X 366	6	500	17	0.40	2 - 4	500	0.40	2 - 4

Megarad Parts

N-CHANNEL RAD HARD POWER MOSFETS

REGISTRATION PENDING TYPE	PRESENT PART NO.	DIE SIZE (MILS)	DIE SIZE	POST RAD: 100K RADS			POST RAD: 1 MRAD		
				BV_{DSS} (V)	$r_{DS(ON)}$ (Ω)	$V_{GS(TH)}$ (V)	BV_{DSS} (V)	$r_{DS(ON)}$ (Ω)	$V_{GS(TH)}$ (V)
2N7271	FRM130R, H	126 X 182	3	100	0.18	2 - 4	95	0.26	1.5 - 4.5
2N7274	FRM230R, H	126 X 182	3	200	0.50	2 - 4	190	0.70	1.5 - 4.5
2N7277	FRM234R, H	126 X 182	3	250	0.70	2 - 4	235	0.88	1.5 - 4.5
2N7280	FRM430R, H	126 X 182	3	500	2.50	2 - 4	TBD	2.75	1.5 - 4.5
2N7272	FRL130R, H	126 X 182	3	100	0.18	2 - 4	95	0.26	1.5 - 4.5
2N7275	FRL230R, H	126 X 182	3	200	0.50	2 - 4	190	0.70	1.5 - 4.5
2N7278	FRL234R, H	126 X 182	3	250	0.70	2 - 4	235	0.88	1.5 - 4.5
2N7281	FRL430R, H	126 X 182	3	500	2.50	2 - 4	TBD	2.75	1.5 - 4.5
2N7273	FRS130R, H	126 X 182	3	100	0.195	2 - 4	95	0.28	1.5 - 4.5
2N7276	FRS230R, H	126 X 182	3	200	0.515	2 - 4	190	0.72	1.5 - 4.5
2N7279	FRS234R, H	126 X 182	3	250	0.715	2 - 4	235	0.90	1.5 - 4.5
2N7282	FRS430R, H	126 X 182	3	500	2.52	2 - 4	TBD	2.77	1.5 - 4.5
2N7283	FRM140R, H	170 X 200	4	100	0.13	2 - 4	95	0.19	1.5 - 4.5
2N7285	FRM240R, H	170 X 200	4	200	0.24	2 - 4	190	0.34	1.5 - 4.5
2N7287	FRM244R, H	170 X 200	4	250	0.40	2 - 4	235	0.50	1.5 - 4.5
2N7289	FRM440R, H	170 X 200	4	500	1.40	2 - 4	TBD	1.55	1.5 - 4.5
2N7284	FRS140R, H	170 X 200	4	100	0.145	2 - 4	95	0.21	1.5 - 4.5
2N7286	FRS240R, H	170 X 200	4	200	0.255	2 - 4	190	0.36	1.5 - 4.5
2N7288	FRS244R, H	170 X 200	4	250	0.415	2 - 4	235	0.52	1.5 - 4.5
2N7290	FRS440R, H	170 X 200	4	500	1.42	2 - 4	TBD	1.57	1.5 - 4.5
2N7291	FRK150R, H	259 X 265	5	100	0.055	2 - 4	100	0.08	1.5 - 4.5
2N7293	FRK250R, H	259 X 265	5	200	0.10	2 - 4	200	0.14	1.5 - 4.5
2N7295	FRK254R, H	259 X 265	5	250	0.17	2 - 4	250	0.21	1.5 - 4.5
2N7297	FRK450R, H	259 X 265	5	500	0.60	2 - 4	500	0.66	1.5 - 4.5
2N7292	FRF150R, H	259 X 265	5	100	0.07	2 - 4	100	0.10	1.5 - 4.5
2N7294	FRF250R, H	259 X 265	5	200	0.115	2 - 4	200	0.16	1.5 - 4.5
2N7296	FRF254R, H	259 X 265	5	250	0.185	2 - 4	250	0.23	1.5 - 4.5
2N7298	FRF450R, H	259 X 265	5	500	0.615	2 - 4	500	0.68	1.5 - 4.5
2N7299	FRK160R, H	266 X 366	6	100	0.04	2 - 4	100	0.06	1.5 - 4.5
2N7301	FRK260R, H	266 X 366	6	200	0.07	2 - 4	200	0.10	1.5 - 4.5
2N7303	FRK264R, H	266 X 366	6	250	0.12	2 - 4	250	0.15	1.5 - 4.5
2N7305	FRK460R, H	266 X 366	6	500	0.40	2 - 4	500	0.44	1.5 - 4.5

Radiation Hardness Assurance Program

P-CHANNEL RAD HARD POWER MOSFETS

PART NO.	DIE SIZE (MILS)	DIE SIZE	INITIAL RATINGS				POST RAD: 10K RADS		
			MAX RATED BV_{DSS}	MAX RATED I_{DS}	MAX RATED r_{DS} (ON)	V_{GS} (TH) (V)	BV_{DSS} (V)	r_{DS} (ON) (Ω)	V_{GS} (TH) (V)
FRM9130D	126 X 182	3	100	6	0.55	2 - 4	100	0.55	2 - 4
FRM9230D	126 X 182	3	200	4	1.30	2 - 4	200	1.30	2 - 4
FRL9130D	126 X 182	3	100	5	0.55	2 - 4	100	0.55	2 - 4
FRL9230D	126 X 182	3	200	3	1.30	2 - 4	200	1.30	2 - 4
FRS9130D	126 X 182	3	100	6	0.565	2 - 4	100	0.565	2 - 4
FRS9230D	126 X 182	3	200	4	1.32	2 - 4	200	1.32	2 - 4
FRM9140D	170 X 200	4	100	11	0.30	2 - 4	100	0.30	2 - 4
FRM9240D	170 X 200	4	200	7	0.72	2 - 4	200	0.72	2 - 4
FRS9140D	170 X 200	4	100	11	O.315	2 - 4	100	0.315	2 - 4
FRS9240D	170 X 200	4	200	7	0.735	2 - 4	200	0.735	2 - 4
FRK9150D	258 X 264	5	100	26	0.125	2 - 4	100	0.125	2 - 4
FRM9250D	258 X 264	5	200	17	0.30	2 - 4	200	0.30	2 - 4
FRF9150D	258 X 264	5	100	23	0.14	2 - 4	100	0.14	2 - 4
FRF9250D	258 X 264	5	200	14	0.315	2 - 4	200	0.315	2 - 4
FRK9160D	266 X 366	6	100	40	0.085	2 - 4	100	0.085	2 - 4
FRK9260D	266 X 366	6	200	26	0.20	2 - 4	200	0.20	2 - 4

Megarad Parts

P-CHANNEL RAD HARD POWER MOSFETS

REGISTRATION PENDING TYPE NO.	PRESENT PART NO.	DIE SIZE (MILS)	DIE SIZE	POST RAD: 100K RADS			POST RAD: 1 MRAD		
				BV_{DSS} (V)	r_{DS} (ON) (Ω)	V_{GS} (TH) (V)	BV_{DSS} (V)	r_{DS} (ON) (Ω)	V_{GS} (TH) (V)
2N7307	FRM9130R, H	126 X 182	3	100	0.55	2 - 4	95	0.80	2 - 6
2N7310	FRM9230R, H	126 X 182	3	200	1.30	2 - 4	190	1.80	2 - 6
2N7308	FRL9130R, H	126 X 182	3	100	0.55	2 - 4	95	0.80	2 - 6
2N7311	FRL9230R, H	126 X 182	3	200	1.30	2 - 4	190	1.80	2 - 6
2N7309	FRS9130R, H	126 X 182	3	100	0.565	2 - 4	95	0.82	2 - 6
2N7312	FRS9230R, H	126 X 182	3	200	1.32	2 - 4	190	1.83	2 - 6
2N7316	FRM9140R, H	170 X 200	4	100	0.30	2 - 4	95	0.44	2 - 6
2N7318	FRM9240R, H	170 X 200	4	200	0.72	2 - 4	190	1.00	2 - 6
2N7317	FRS9140R, H	170 X 200	4	100	0.315	2 - 4	95	0.46	2 - 6
2N7319	FRS9240R, H	170 X 200	4	200	0.735	2 - 4	190	1.02	2 - 6
2N7322	FRK9150R, H	258 X 264	5	100	0.125	2 - 4	95	0.18	2 - 6
2N7324	FRM9250R, H	258 X 264	5	200	0.30	2 - 4	190	0.42	2 - 6
2N7323	FRF9150R, H	258 X 264	5	100	0.14	2 - 4	95	0.20	2 - 6
2N7325	FRF9250R, H	258 X 264	5	200	0.315	2 - 4	190	0.44	2 - 6
2N7328	FRK9160R, H	266 X 366	6	100	0.085	2 - 4	95	0.12	2 - 6
2N7330	FRK9260R, H	266 X 366	6	200	0.20	2 - 4	190	0.28	2 - 6

Radiation Hardness Assurance Program

P-CHANNEL RAD HARD POWER MOSFETS

PART NO.	DIE SIZE (MILS)	DIE SIZE	INITIAL RATINGS				POST RAD: 10K RADS		
			MAX RATED BV_{DSS}	MAX RATED I_{DS}	MAX RATED r_{DS} (ON)	V_{GS} (TH) (V)	BV_{DSS} (V)	r_{DS} (ON) (Ω)	V_{GS} (TH) (V)
FRM9130D	128 X 182	3	100	6	0.85	2 – 4	100	0.85	2 – 4
FRM9230D	128 X 182	3	200	4	1.30	2 – 4	200	1.30	2 – 4
FRL9130D	128 X 182	3	100	6	0.85	2 – 4	100	0.85	2 – 4
FRL9230D	128 X 182	3	200	3	1.30	2 – 4	200	1.30	2 – 4
FRM9130D	128 X 182	3	100	6	0.585	2 – 4	100	0.585	2 – 4
FRM9230D	128 X 182	3	200	4	1.32	2 – 4	200	1.32	2 – 4
FRM9140D	170 X 200	4	100	11	0.30	2 – 4	100	0.30	2 – 4
FRM9240D	170 X 200	4	200	7	0.72	2 – 4	200	0.72	2 – 4
FRM9140D	170 X 200	4	100	11	0.315	2 – 4	100	0.315	2 – 4
FRM9240D	170 X 200	4	200	7	0.735	2 – 4	200	0.735	2 – 4
FRK9130D	258 X 264	5	100	26	0.125	2 – 4	100	0.125	2 – 4
FRM9250D	258 X 264	5	200	17	0.30	2 – 4	200	0.30	2 – 4
FRF9150D	258 X 264	5	100	23	0.14	2 – 4	100	0.14	2 – 4
FRF9250D	258 X 264	5	200	14	0.315	2 – 4	200	0.315	2 – 4
FRK9160D	268 X 368	6	100	40	0.085	2 – 4	100	0.085	2 – 4
FRK9260D	268 X 368	6	200	26	0.20	2 – 4	200	0.20	2 – 4

Mspared Parts

P-CHANNEL RAD HARD POWER MOSFETS

REGISTRATION PENDING TYPE NO.	PRESENT PART NO.	DIE SIZE (MILS)	DIE SIZE	POST RAD: 100K RADS			POST RAD: 1 MRAD		
				BV_{DSS} (V)	r_{DS} (ON) (Ω)	V_{GS} (TH) (V)	BV_{DSS} (V)	r_{DS} (ON) (Ω)	V_{GS} (TH) (V)
2N7307	FRM9130R,H	128 X 182	3	100	0.85	2 – 4	95	0.80	2 – 6
2N7310	FRM9230R,H	128 X 182	3	200	1.30	2 – 4	190	1.80	2 – 6
2N7308	FRL9130R,H	128 X 182	3	100	0.85	2 – 4	95	0.80	2 – 6
2N7311	FRL9230R,H	128 X 182	3	200	1.30	2 – 4	190	1.80	2 – 6
2N7309	FRM9130R,H	128 X 182	3	100	0.585	2 – 4	95	0.82	2 – 6
2N7312	FRM9230R,H	128 X 182	3	200	1.32	2 – 4	190	1.83	2 – 6
2N7316	FRM9140R,H	170 X 200	4	100	0.30	2 – 4	95	0.44	2 – 6
2N7319	FRM9240R,H	170 X 200	4	200	0.72	2 – 4	190	1.00	2 – 6
2N7317	FRM9140R,H	170 X 200	4	100	0.315	2 – 4	95	0.46	2 – 6
2N7319	FRM9240R,H	170 X 200	4	200	0.735	2 – 4	190	1.02	2 – 6
2N7322	FRK9150R,H	258 X 264	5	100	0.125	2 – 4	95	0.18	2 – 6
2N7324	FRM9250R,H	258 X 264	5	200	0.30	2 – 4	190	0.42	2 – 6
2N7323	FRF9150R,H	258 X 264	5	100	0.14	2 – 4	95	0.20	2 – 6
2N7325	FRF9250R,H	258 X 264	5	200	0.315	2 – 4	190	0.44	2 – 6
2N7328	FRK9160R,H	268 X 368	6	100	0.085	2 – 4	95	0.12	2 – 6
2N7330	FRK9260R,H	268 X 368	6	200	0.20	2 – 4	190	0.28	2 – 6

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PREVIEW PRODUCTS

DATA SHEETS		PAGE
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RFA14N50BE	N-Channel Enhancement-Mode Power Field-Effect Transistor	10-23
RFD3N08L RFD3N08LSM	N-Channel Logic Level Power Field Effect Transistors	10-26
RFD4N06L RFD4N06LSM	N-Channel Logic Level Power Field Effect Transistors	10-28
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RFG70N06, RFP70N06	N-Channel Enhancement-Mode Power Field-Effect Transistors	10-32

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PREVIEW PRODUCTS

DATA SHEETS		PAGE
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IRFR110, IRFU110	N-Channel Power MOSFETs Avalanche Energy Rated	10-7
IRFR214, IRFU214	N-Channel Power MOSFETs Avalanche Energy Rated	10-13
IRF614	N-Channel Power MOSFETs Avalanche Energy Rated	10-18
RFA14N05E	N-Channel Enhancement-Mode Power Field-Effect Transistor	10-23
RFD3N06L, RFD3N06LSM	N-Channel Logic Level Power Field Effect Transistors	10-28
RFD4N06L, RFD4N06LSM	N-Channel Logic Level Power Field Effect Transistors	10-28
RFP15N06L	N-Channel Logic Level Power Field-Effect Transistor	10-30
RFP70N06, RFP70N06	N-Channel Enhancement-Mode Power Field-Effect Transistors	10-32

HARRIS HGTG30N120E2

August 1991

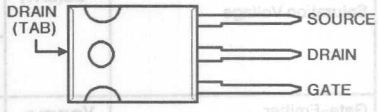
N-Channel Enhancement-Mode Insulated Gate Bipolar Transistor (IGBT)

Features

- 50 Amp 1200 Volt
- Latch Free Operation
- Typical Fall Time - 580ns
- High Input Impedance
- Low Conduction Loss

Package

TO-247
TOP VIEW



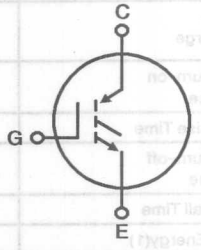
Description

The HGTG30N120E2* is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

The IGBTs are ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

*Formerly Developmental Type #49010

Terminal Diagram



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		HGTG30N120E2	UNITS
Collector-Emitter Voltage	BV_{CES}	1200	V
Collector-Gate Voltage, R_{GE} = 1MΩ	V_{CGR}	1200	V
Collector Current Continuous			
@T_C = +25°C	I_{C25}	50	A
@V_{ge} = 15V @T_C = +90°C	I_{C90}	30	A
Collector Current Pulsed(1)	I_{CM}	200	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area			
@T_J = +150°C	SSOA	200A @ 0.8 BV_{CES}	-
Power Dissipation Total	P_D		
@T_C = +25°C		208	W
Derating T_C > +25°C		1.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time(2)	t_{sc}		
@V_{ge} = 15V		6	µS
@V_{ge} = 10V		15	µS

(1) Repetitive Rating: Pulse width limited by maximum junction temperature.

(2) $V_{CE(pk)}$ = 720V, T_C = 125°C, R_{GE} = 25Ω

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2834

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250μA, V_{GE} = 0V		1200	-	-	V
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = BV_{CES}	T_C = +25°C	-	-	1.0	mA
		V_{CE} = 0.8 BV_{CES}	T_C = +125°C	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C90}, V_{GE} = 15V	T_C = +25°C	-	3.0	3.5	V
			T_C = +125°C	-	3.2	3.5	V
		I_C = I_{C90}, V_{GE} = 10V	T_C = +25°C	-	3.2	3.8	V
			T_C = +125°C	-	3.4	3.8	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 1mA, V_{CE} = V_{GE}	T_C = +25°C	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±500	nA
Gate-Emitter Plateau Voltage	$V_{GE(pl)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}		-	7.3	-	V
On-State Gate Charge	$Q_{G(on)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	-	185	240	nC
			V_{GE} = 20V	-	240	315	nC
Current Turn-on Delay Time	$t_{d(on)i}$	L = 50μH, I_C = I_{C90}, R_g = 25Ω, V_{GE} = 15V, T_J = +125°C, V_{CE} = 0.8 BV_{CES}		-	100	-	ns
Current Rise Time	t_{ri}			-	150		ns
Current Turn-off Delay Time	$t_{d(off)i}$			-	760	990	ns
Current Fall Time	t_{fi}			-	580	750	ns
Turn-off Energy(1)	W_{off}			-	8.4	-	mJ
Current Turn-on Delay Time	$t_{d(on)i}$	L = 50μH, I_C = I_{C90}, R_g = 25Ω, V_{GE} = 10V, T_J = +125°C, V_{CE} = 0.8 BV_{CES}		-	100	-	ns
Current Rise Time	t_{ri}			-	150	-	ns
Current Turn-off Delay Time	$t_{d(off)i}$			-	610	790	ns
Current Fall Time	t_{fi}			-	580	750	ns
Turn-off Energy(1)	W_{off}			-	8.4	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.5	0.6	°C/W

(1) Turn-off Energy Loss (W_{off}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A). The HGTG30N120E2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

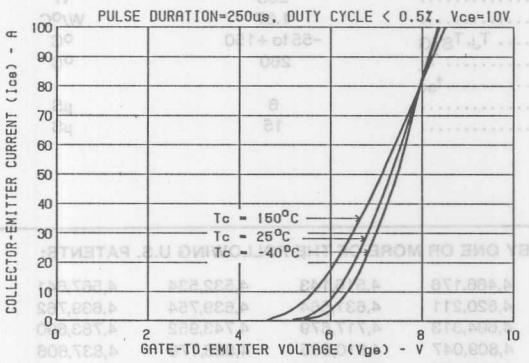


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

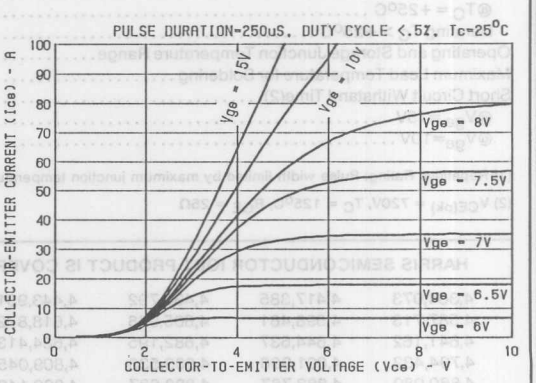


FIGURE 2. SATURATION CHARACTERISTIC (TYPICAL)

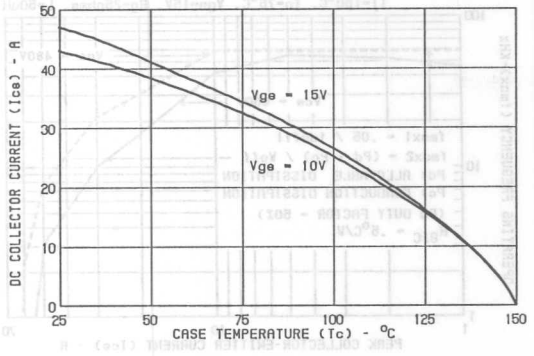


FIGURE 3. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

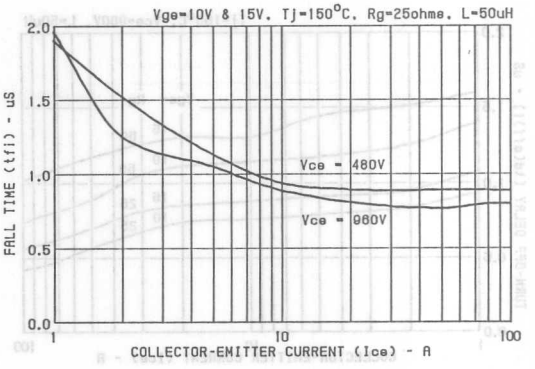


FIGURE 4. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

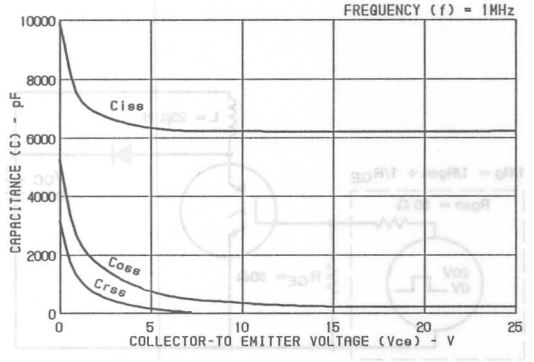


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

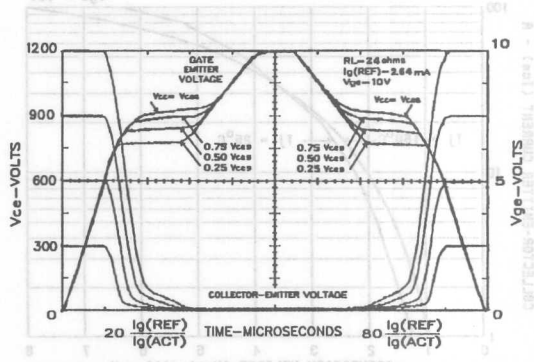


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260.)

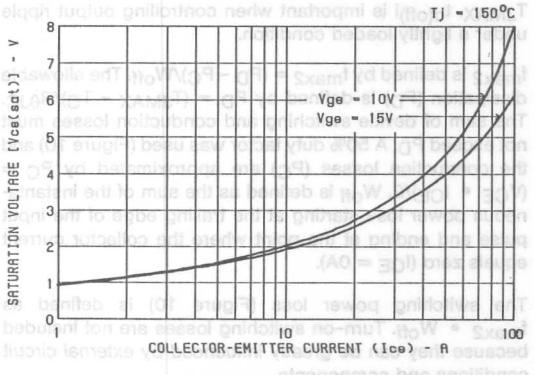


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

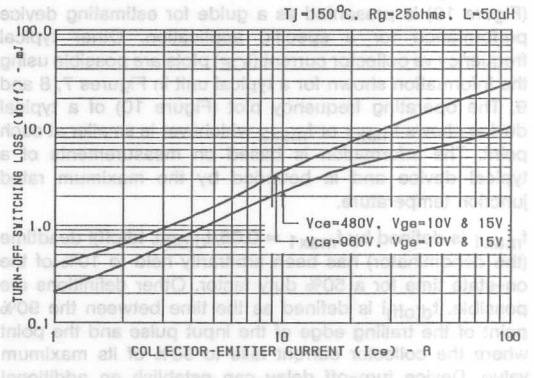


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

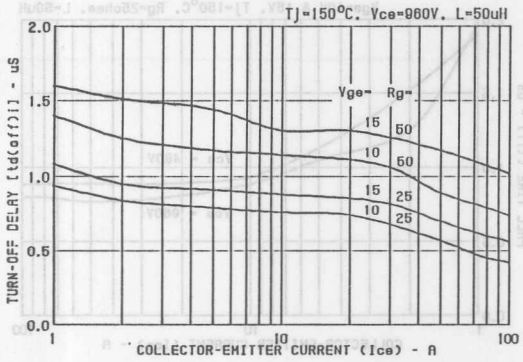


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT.

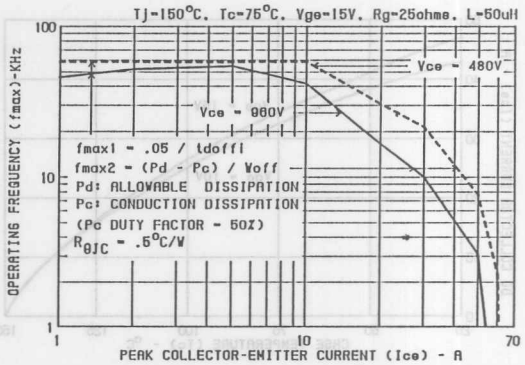


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE.

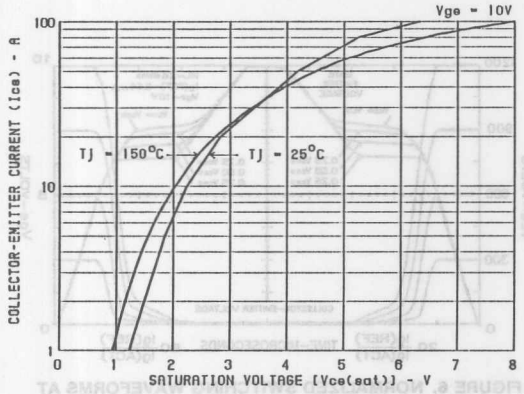


FIGURE 11. COLLECTOR-EMITTER SATURATION VOLAGE.

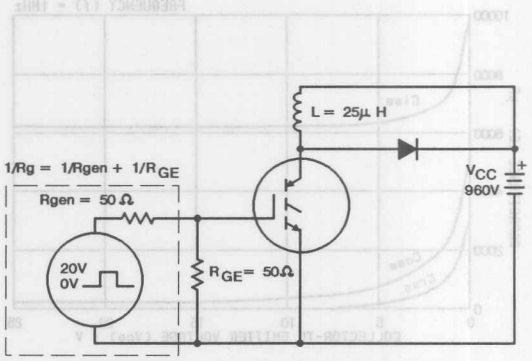


FIGURE 12. INDUCTIVE SWITCHING TEST CIRCUIT.

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{max1} or f_{max2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{max1} is defined by $f_{max1} = 0.05/t_{d(off)i}$. $t_{d(off)i}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(off)i}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(off)i}$ is important when controlling output ripple under a lightly loaded condition.

f_{max2} is defined by $f_{max2} = (P_D - P_C)/W_{off}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \bullet I_{CE})/2$. W_{off} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A).

The switching power loss (Figure 10) is defined as $f_{max2} \bullet W_{off}$. Turn-on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS SEMICONDUCTOR

IRFR110
IRFU110

N-Channel Power MOSFETs Avalanche Energy Rated

May 1992

Features

- 4.7A, 100V
- $r_{DS(ON)} = 0.54\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature

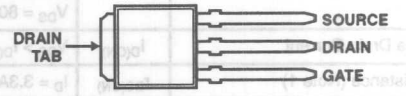
Description

The IRFR110 and IRFU110 are n-channel enhancement-mode silicon-gate power field-effect transistors designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These advanced power MOSFETs are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

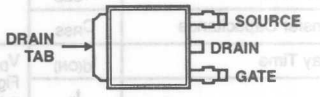
The IRFR110 is supplied in the JEDEC TO-251AA plastic package and the IRFU110 in the JEDEC TO-252AA plastic package.

Packages

TO-251AA
TOP VIEW

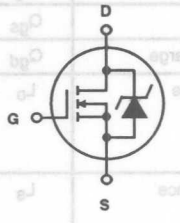


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFR110, IRFU110	UNITS
Drain-Source Voltage (1)	V_{DS}	100	V
Drain-Gate Voltage	V_{DGR}	100	V
Continuous Drain Current			
T_C = +25°C	I_D	4.7	A
T_C = +100°C	I_D	3.3	A
Pulsed Drain Current (2)	I_{DM}	17	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	30	W
Linear Derating Factor		0.2	W/°C
Single Pulse Avalanche Rating (3) (See Fig. 14)	E_{AS}	19	mj
Operating and Storage Temperature	T_J, T_{STG}	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve. (Figure 5)
3. V_{DD} = 25V, Starting T_J = +25°C, L = 1.3mH, R_G = 25Ω, Peak I_L = 4.7A.

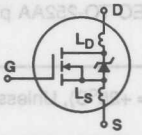
10 PREVIEW PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

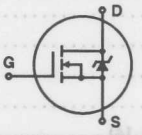
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File Number 3275

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA	2	-	4	V
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V	-	-	250	μA
		V_{DS} = 80V, V_{GS} = 0V, T_J = +150°C	-	-	1000	μA
On-State Drain Current	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)Max}$, V_{GS} = 10V	4.7	-	-	A
On Resistance (Note 1)	$r_{DS(ON)}$	I_D = 3.3A, V_{GS} = 10V	-	0.41	0.54	Ω
Forward Transconductance (Note 1)	g_{fs}	V_{DS} = ≥ 50V, I_{DS} = 3.3A	1.3	2.0	-	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	180	-	pF
Output Capacitance	C_{OSS}		-	82	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	15	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D = 5.6A, R_G = 24Ω, R_D = 9.1Ω, See Figure 15 (MOSFET switching times are essentially independent of operating temperature)	-	7.6	11	ns
Rise Time	t_r		-	24	36	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	14	21	ns
Fall Time	t_f		-	14	21	ns
Total Gate Charge	Q_g	V_{GS} = 10V, I_D = 5.6A, V_{DS} = 0.8 x Max Rating. See Figure 16 (Gate charge is essentially independent of operating temperature)	-	5.2	7.7	nC
Gate-Source Charge	Q_{gs}		-	1.5	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	2.2	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad. 	-	7.5	-	nH
Junction to Case	$R_{\theta JC}$		-	-	5.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.7	-	°C/W
Junction to Ambient	$R_{\theta JA}$	Free air operation	-	-	110	°C/W

Source-Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 	-	-	4.7	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}		-	-	17	A
Diode Forward Voltage (Note 1)	V_{SD}	T_J = +25°C, I_S = 4.7A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_S = 5.6A, dI_F/dt = 100A/μs	46	96	200	ns
Reverse Recovery Charge	Q_{RR}	T_J = +25°C, I_S = 5.6A, dI_F/dt = 100A/μs	0.17	0.38	0.83	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

NOTES: 1. Pulse Test: Pulse width ≤ 300μs. Duty Cycle ≤ 2%

2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

Performance Curves

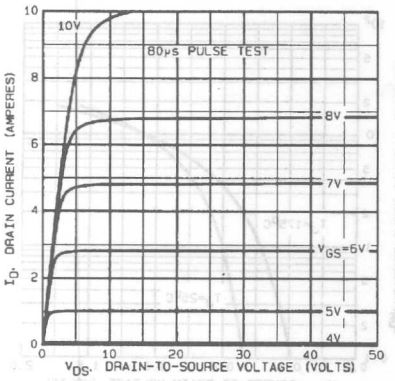


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

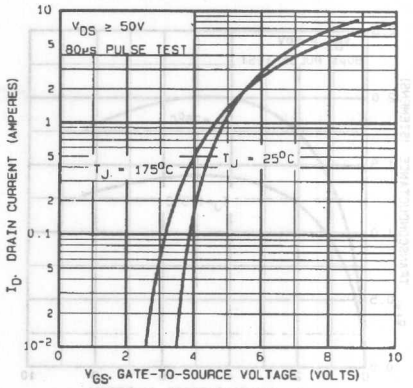


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

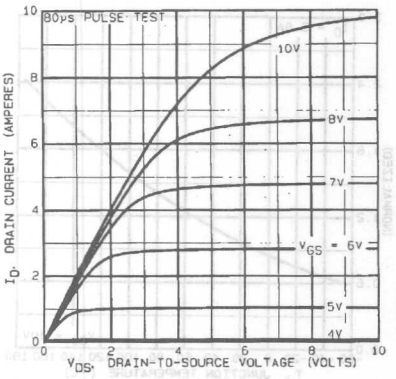


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

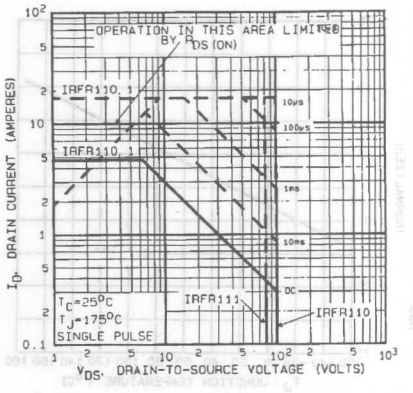


FIGURE 4. MAXIMUM SAFE OPERATING AREA

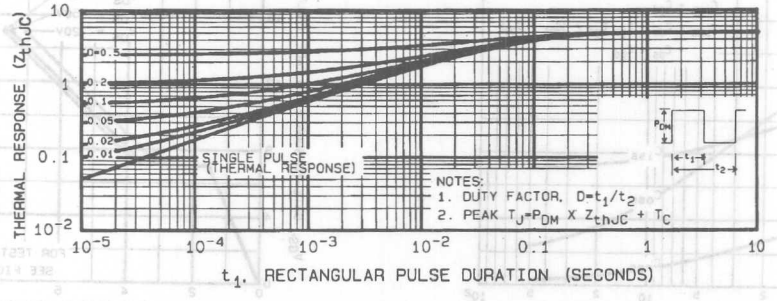


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

10 PREVIEW PRODUCTS

Performance Curves (Continued)

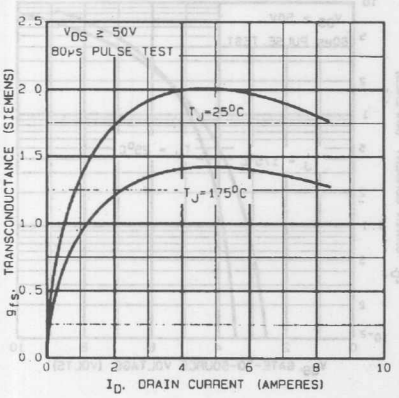


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

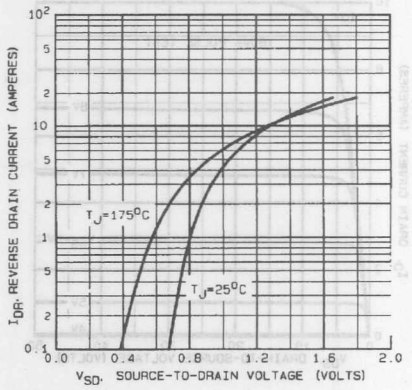


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

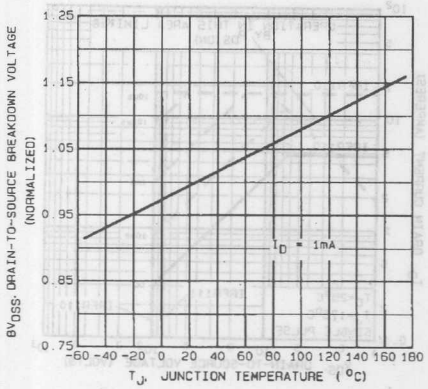


FIGURE 8 BREAKDOWN vs TEMPERATURE

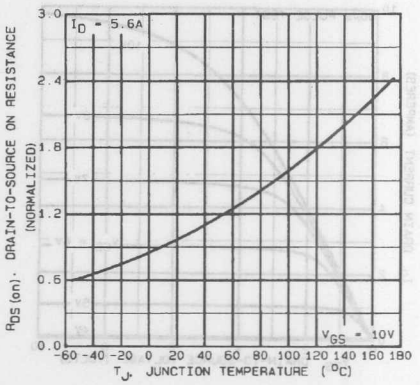


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

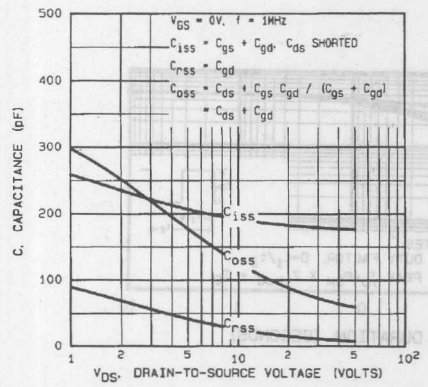


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

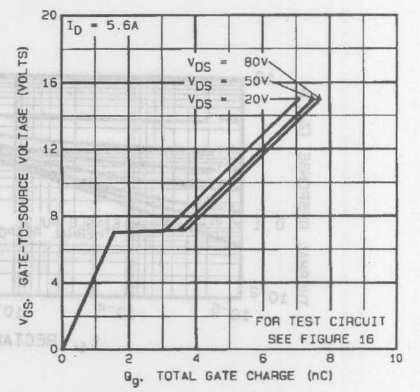


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

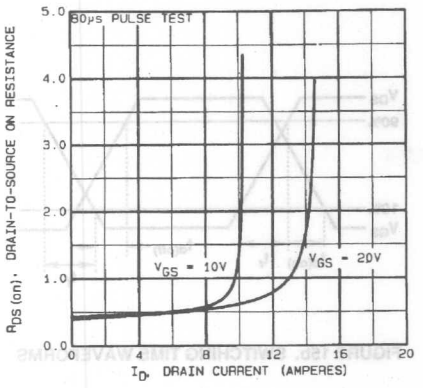


FIGURE 12. TYPICAL ON-RESISTANCE vs DRAIN CURRENT

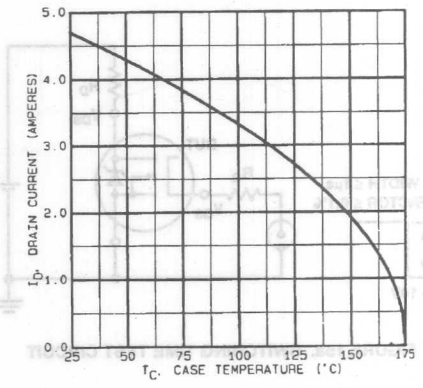


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

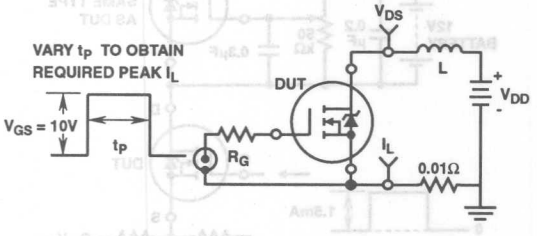


FIGURE 14a. UNCLAMPED INDUCTIVE TEST CIRCUIT

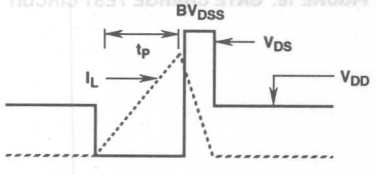


FIGURE 14b. UNCLAMPED INDUCTIVE WAVEFORMS

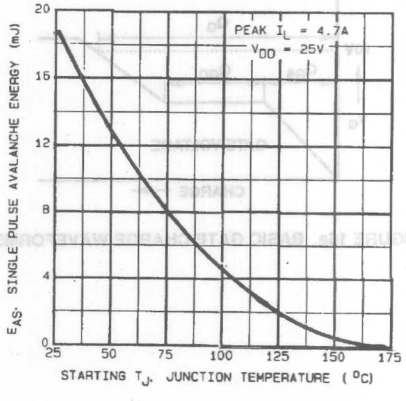


FIGURE 14c. MAXIMUM AVALANCHE vs STARTING JUNCTION TEMPERATURE

10 PREVIEW PRODUCTS

Performance Curves (Continued)

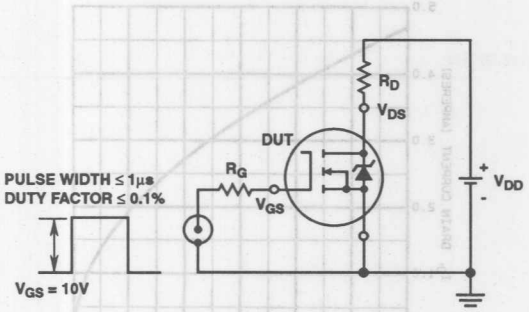


FIGURE 15a. SWITCHING TIME TEST CIRCUIT

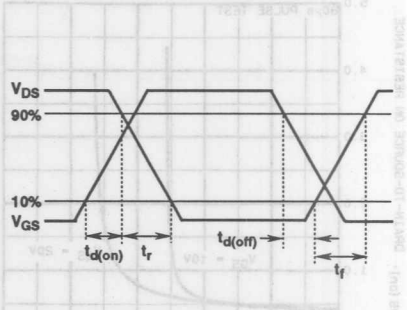


FIGURE 15b. SWITCHING TIME WAVEFORMS

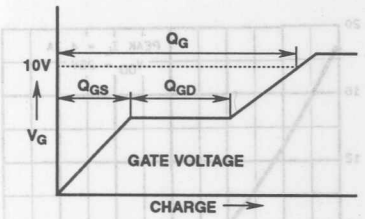


FIGURE 16a. BASIC GATE CHARGE WAVEFORMS

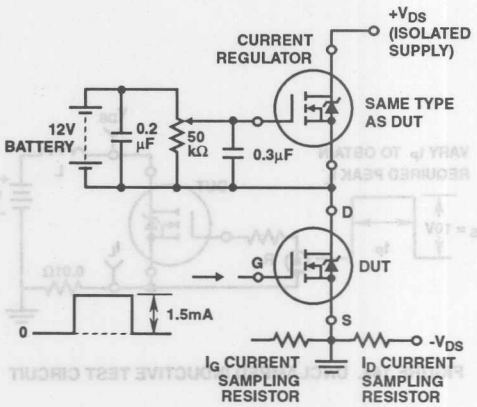


FIGURE 16. GATE CHARGE TEST CIRCUIT

HARRIS SEMICONDUCTOR

IRFR214
IRFU214

N-Channel Power MOSFETs
Avalanche Energy Rated

May 1992

Features

- 2.2A, 250V
- $r_{DS(on)} = 2.0\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- High Input Impedance
- +150°C Operating Temperature

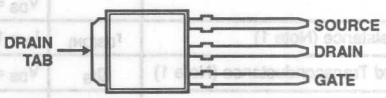
Description

The IRFR214 and IRFU214 (TA17443) are n-channel enhancement-mode silicon-gate power field-effect transistors designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These advanced power MOSFETs are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

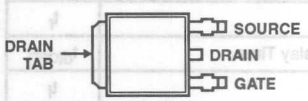
The IRFR214 is supplied in the JEDEC TO-251AA plastic package and the IRFU214 in the JEDEC TO-252AA plastic package.

Package

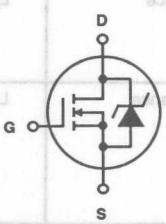
TO-251AA
TOP VIEW



TO-252AA
TOP VIEW



Terminal Diagram



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFR214, IRFU214	UNITS
Drain-Source Voltage (1)	V_{DS}	250	V
Drain Gate Voltage	V_{DGR}	250	V
Continuous Drain Current			
T_C = +25°C	I_D	2.2	A
T_C = +100°C	I_D	1.4	A
Pulsed Drain Current (2)	I_{DM}	8.8	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	25	W
Linear Derating Factor		0.20	W/°C
Single Pulse Avalanche Rating (3) (See Fig. 12)	E_{AS}	61	mj
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	°C

NOTES:

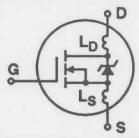
1. T_J = +25°C to +150°C.
2. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve.
3. V_{DD} = 50V, Starting T_J = +25°C, L = 21mH, R_G = 25Ω, Peak I_L = 2.2A

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

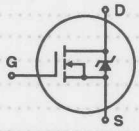
Copyright © Harris Corporation 1992

File Number 3274

Electrical Characteristics $T_C = +25°C$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$	250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2	-	4	V
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 250V$, $V_{GS} = 0V$	-	-	250	μA
		$V_{DS} = 200V$, $V_{GS} = 0V$, $T_J = +125°C$	-	-	1000	μA
On Resistance (Note 1)	$r_{DS(ON)}$	$I_D = 1.3A$, $V_{GS} = 10V$	-	1.6	2.0	Ω
Forward Transconductance (Note 1)	g_{fs}	$V_{DS} = 50V$, $I_{DS} = 1.3A$	1.1	-	-	S
Input Capacitance	C_{ISS}	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0MHz See Figure 10	-	140	-	pF
Output Capacitance	C_{OSS}		-	42	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	9.6	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 125V$, $I_D = 2.7A$, $R_G = 24\Omega$, $R_D = 45\Omega$, See Figure 15 (MOSFET switching times are essentially independent of operating temperature)	-	7.0	-	ns
Rise Time	t_r		-	7.6	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	16	-	ns
Fall Time	t_f		-	7.0	-	ns
Total Gate Charge	Q_{g10}	$V_{GS} = 10V$, $I_D = 2.7A$ $V_{DS} = 0.8$ x Max Rating. See Figure 16 for test circuit (Gate charge is essentially independent of operating temperature)	-	-	10	nC
Gate-Source Charge	Q_{gs}		-	-	1.8	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	-	5.5	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad. 	-	7.5	-	nH
Junction to Case	$R_{\theta JC}$		-	-	5.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.7	-	°C/W
Junction to Ambient	$R_{\theta JA}$	Free air operation	-	-	110	°C/W

Source-Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 	-	-	2.2	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}		-	-	8.8	A
Diode Forward Voltage (Note 1)	V_{SD}	$T_J = +25°C$, $I_{SD} = 2.2A$, $V_{GS} = 0V$	-	-	2.0	V
Reverse Recovery Time	t_{rr}	$T_J = +25°C$, $I_{SD} = 2.7A$, $dI_{SD}/dt = 100A/\mu s$	97	-	390	ns
Reverse Recovery Charge	Q_{RR}	$T_J = +25°C$, $I_{SD} = 2.7A$, $dI_{SD}/dt = 100A/\mu s$	0.32	-	1.3	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

NOTES: 1. Pulse Test: Pulse width ≤ 300μs. Duty Cycle ≤ 2%

2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 11).

Performance Curves

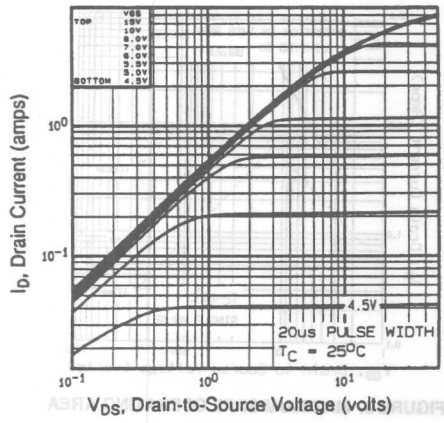


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS (T_C = +25°C)

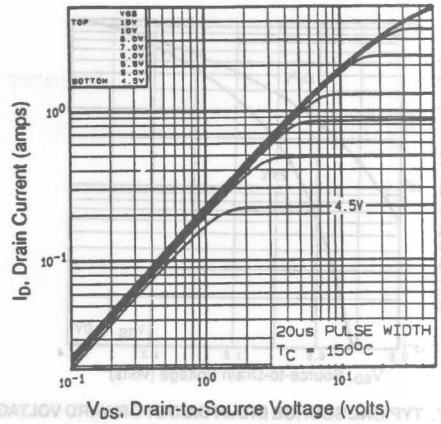


FIGURE 2. TYPICAL OUTPUT CHARACTERISTICS (T_C = +150°C)

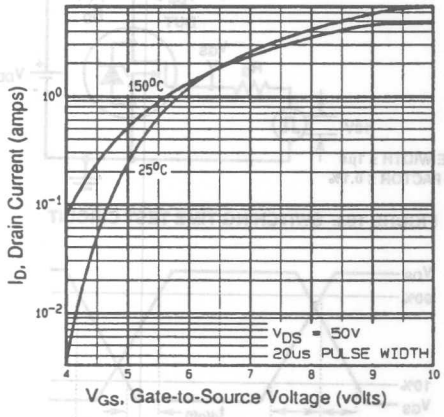


FIGURE 3. TYPICAL TRANSFER CHARACTERISTICS

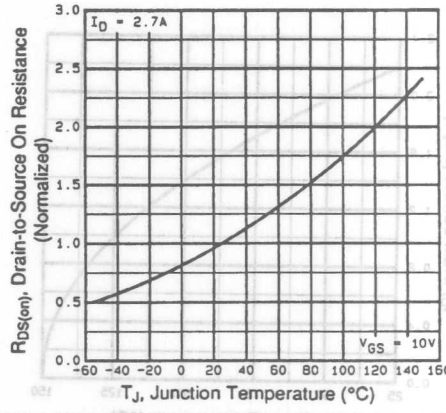


FIGURE 4. NORMALIZED ON-RESISTANCE vs TEMPERATURE

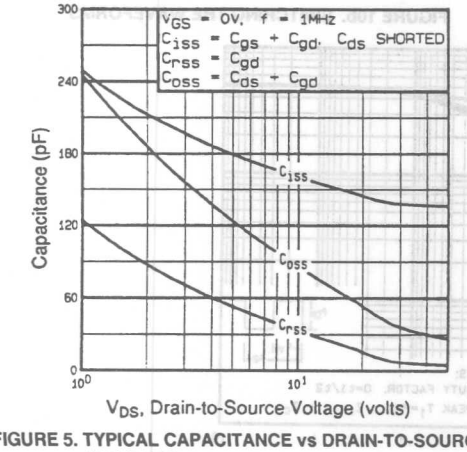


FIGURE 5. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

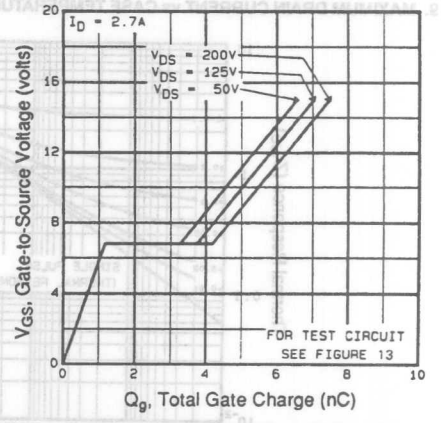


FIGURE 6. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

10

PREVIEW PRODUCTS

Performance Curves (Continued)

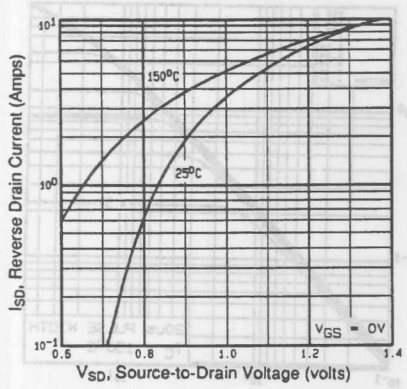


FIGURE 7. TYPICAL SOURCE DRAIN DIODE FORWARD VOLTAGE

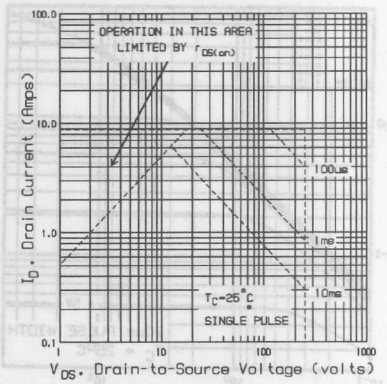


FIGURE 8. MAXIMUM SAFE OPERATING AREA

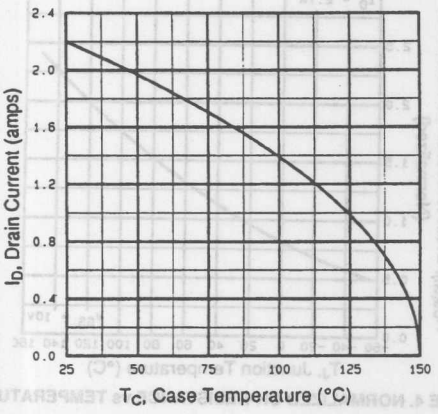


FIGURE 9. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

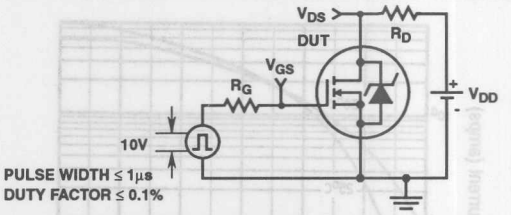


FIGURE 10a. SWITCHING TIME TEST CIRCUIT

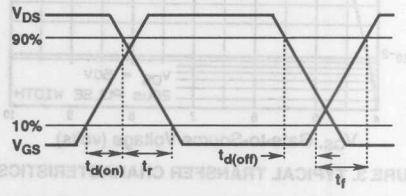


FIGURE 10b. SWITCHING THE WAVEFORMS

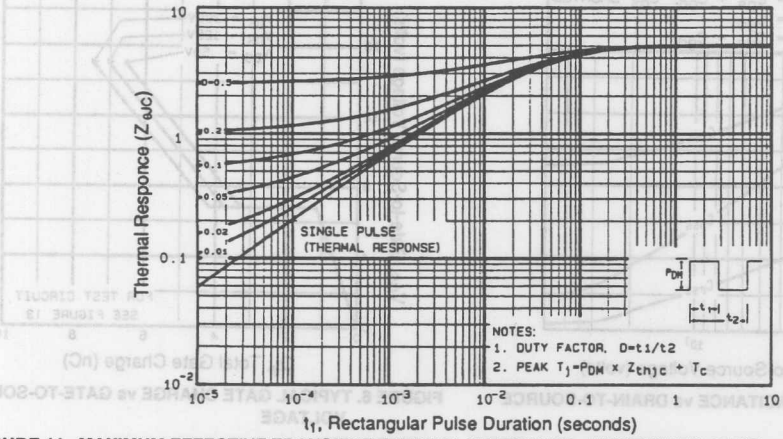


FIGURE 11. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

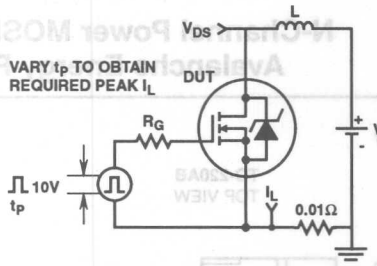


FIGURE 12a. UNCLAMPED INDUCTIVE TEST CIRCUIT

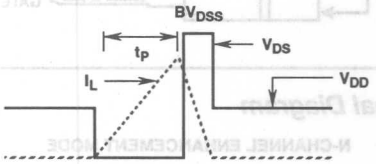


FIGURE 12b. UNCLAMPED INDUCTIVE WAVEFORMS

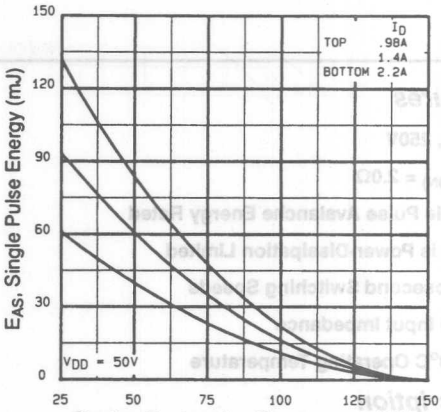


FIGURE 12c. MAX. AVALANCHE ENERGY vs DRAIN CURRENT

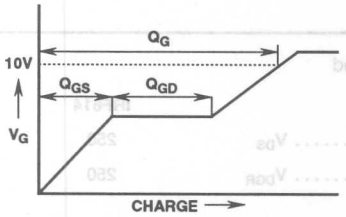


FIGURE 13a. BASIC GATE CHARGE WAVEFORM

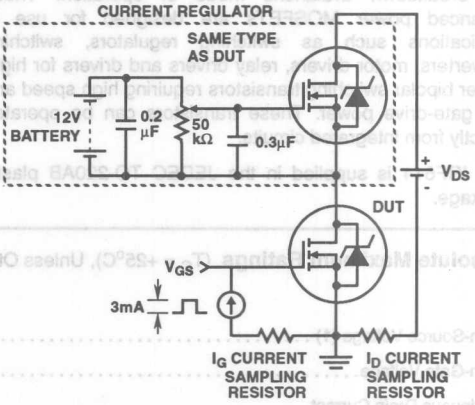


FIGURE 13b. GATE CHARGE TEST CIRCUIT

HARRIS SEMICONDUCTOR

IRF614

N-Channel Power MOSFETs Avalanche Energy Rated

May 1992

Features

- 2.0A, 250V
- $r_{DS(ON)} = 2.0\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- High Input Impedance
- +150°C Operating Temperature

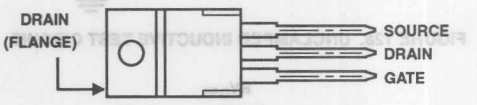
Description

The IRF614 (TA17443) is an n-channel enhancement-mode silicon-gate power field-effect transistor designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These advanced power MOSFETs are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

The IRF614 is supplied in the JEDEC TO-220AB plastic package.

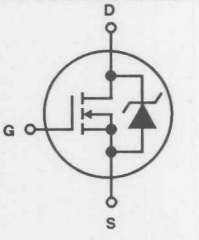
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF614	UNITS
Drain-Source Voltage (1)	V_{DS}	250	V
Drain-Gate Voltage	V_{DGR}	250	V
Continuous Drain Current			
T_C = +25°C	I_D	2.0	A
T_C = +100°C	I_D	1.3	A
Pulsed Drain Current (2)	I_{DM}	8.0	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	20	W
Linear Derating Factor		0.16	W/°C
Single Pulse Avalanche Rating (3) (See Fig. 14)	E_{as}	61	mj
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	°C

NOTES:

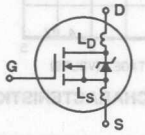
1. T_J = +25°C to +150°C.
2. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve. (Figure 5)
3. V_{DD} = 50V, Starting T_J = +25°C, L = 21mH, R_G = 25Ω, Peak I_L = 2.2A.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

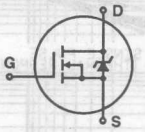
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File Number 3273

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V	250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA	2	-	4	V
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 250V, V_{GS} = 0V	-	-	250	µA
		V_{DS} = 200V, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)Max}$, V_{GS} = 10V	2.0	-	-	A
On Resistance (Note 1)	$r_{DS(ON)}$	I_D = 1.0A, V_{GS} = 10V	-	1.6	2.0	Ω
Forward Transconductance (Note 1)	g_{fs}	V_{DS} = 2 x V_{GS}, I_{DS} = 1.0A	0.8	1.2	-	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	180	-	pF
Output Capacitance	C_{OSS}		-	53	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	14	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 2.0A, R_G = 24Ω, R_D = 61Ω, See Figure 16 (MOSFET switching times are essentially independent of operating temperature)	-	8.9	13	ns
Rise Time	t_r		-	12	18	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	18	27	ns
Fall Time	t_f		-	8.9	15	ns
Total Gate Charge	Q_{g10}	V_{GS} = 10V, I_D = 2.0A V_{DS} = 0.8 x Max Rating. See Figure 17 for test circuit (Gate charge is essentially independent of operating temperature)	-	9.6	14.4	nC
Gate-Source Charge	Q_{gs}		-	2.4	3.6	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	4.5	6.7	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad. 	-	7.5	-	nH
Junction to Case	$R_{\theta JC}$		-	-	6.4	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.50	-	°C/W
Junction to Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W

Source-Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 	-	-	2.0	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}		-	-	8.0	A
Diode Forward Voltage (Note 1)	V_{SD}	T_J = +25°C, I_{SD} = 2.0A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_{SD} = 2.0A, dI_{SD}/dt = 100A/µs	67	-	340	ns
Reverse Recovery Charge	Q_{RR}	T_J = +25°C, I_{SD} = 2.0A, dI_{SD}/dt = 100A/µs	0.24	0.54	1.2	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

NOTES: 1. Pulse Test: Pulse width ≤ 300µs. Duty Cycle ≤ 2%

2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

Performance Curves

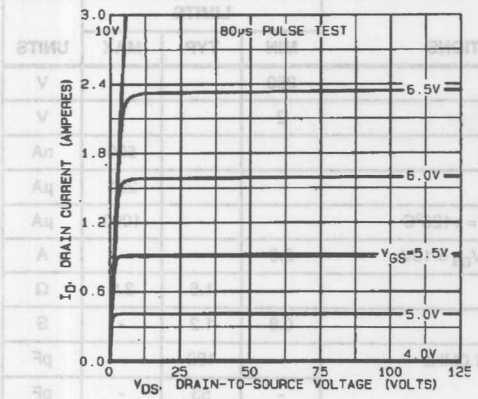


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

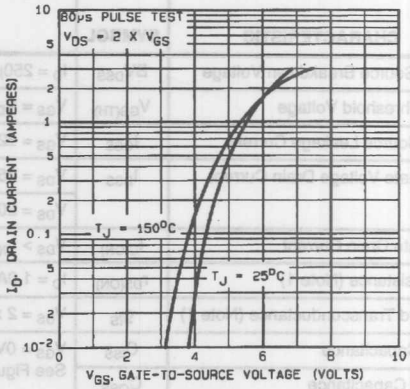


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

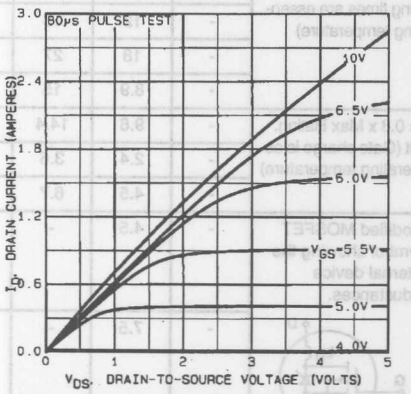


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

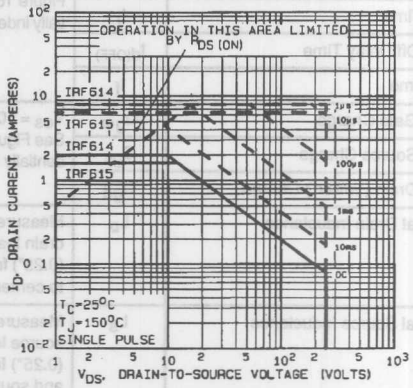


FIGURE 4. MAXIMUM SAFE OPERATING AREA

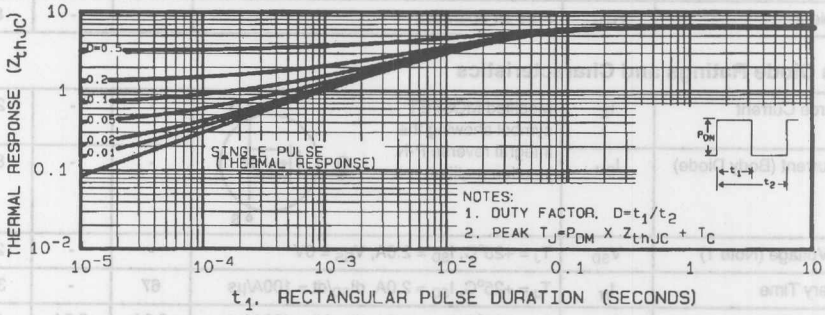


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

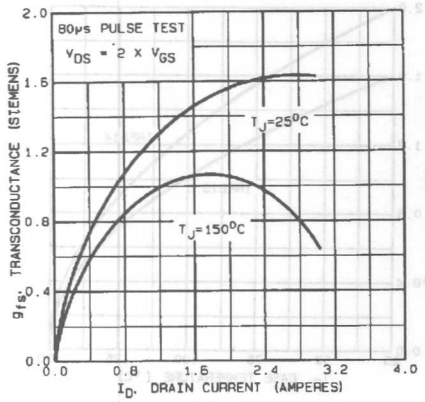


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

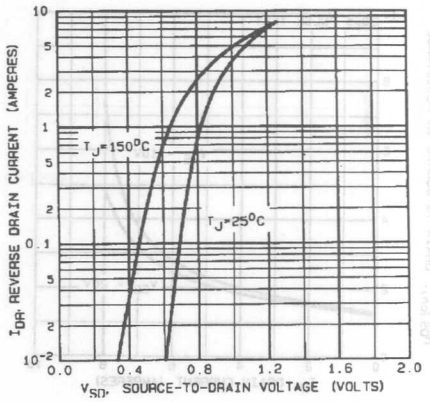


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

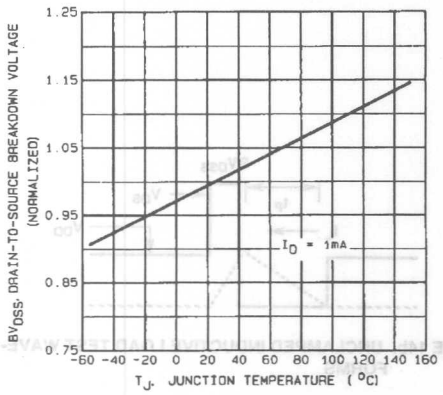


FIGURE 8 BREAKDOWN vs TEMPERATURE

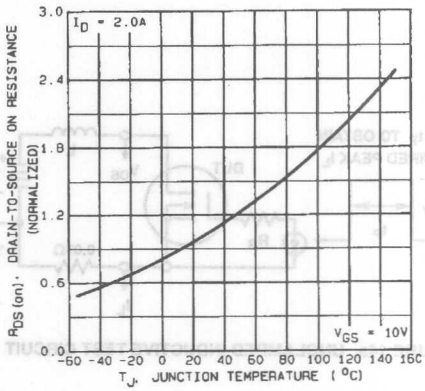


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

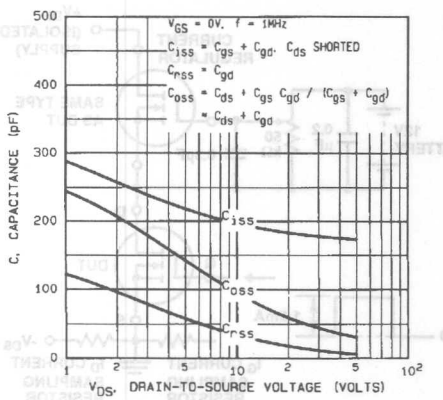


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

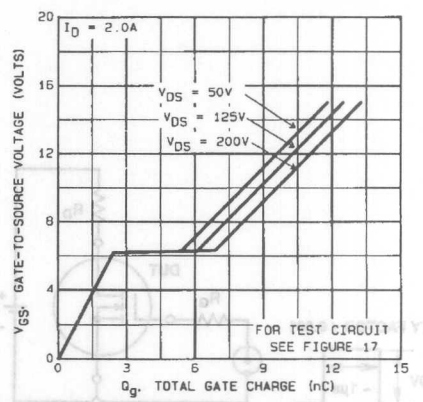


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

10 PREVIEW PRODUCTS

Performance Curves (Continued)

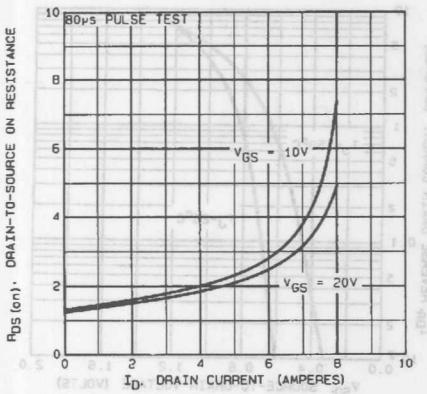


FIGURE 12. TYPICAL ON-RESISTANCE vs DRAIN CURRENT

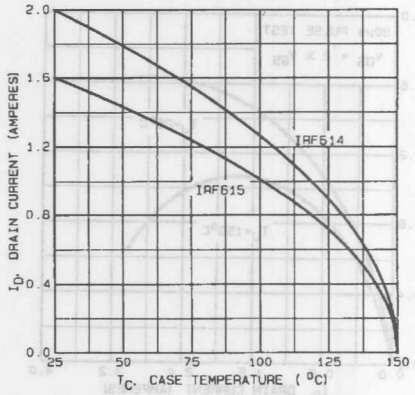


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

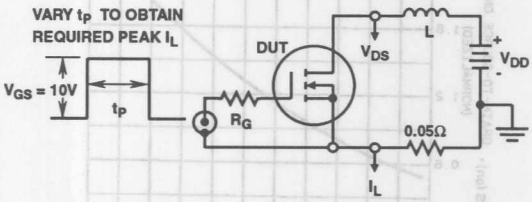


FIGURE 14a. UNCLAMPED INDUCTIVE TEST CIRCUIT

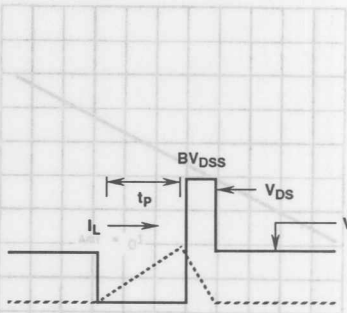


FIGURE 14b. UNCLAMPED INDUCTIVE LOAD TEST WAVEFORMS

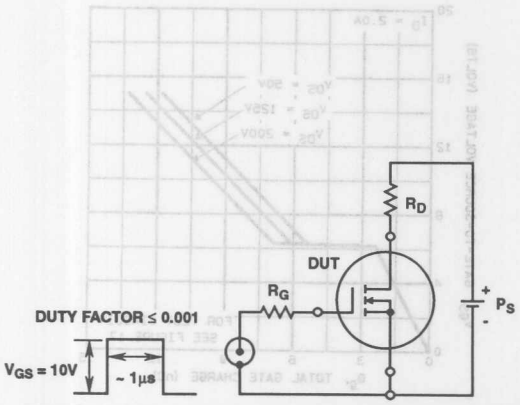


FIGURE 15. SWITCHING TIME TEST CIRCUIT

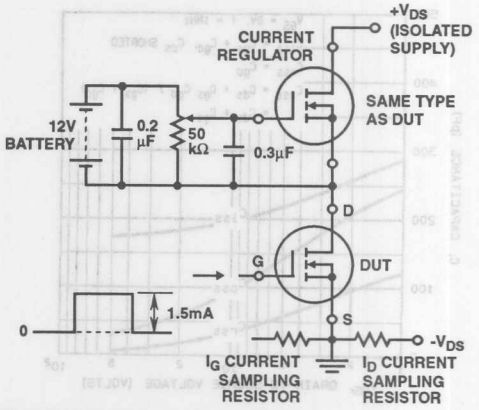


FIGURE 16. GATE CHARGE TEST CIRCUIT

HARRIS

RFA14N50BE

DEVELOPMENTAL

August 1991

N-Channel Enhancement-Mode Power Field-Effect Transistor

Features

- 14A, 500V
- $R_{DS(ON)}$: 0.4Ω
- Fall Time = 5ns
- Very Fast Turn-Off Characteristics
- Nanosecond Switching Speeds
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Electrostatic Discharge Protected

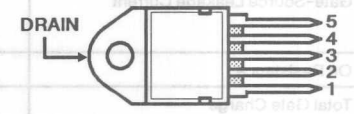
Description

The RFA14N50BE is an n-channel fast switching MOSFET transistor that is designed for switching regulators, inverters and motor drivers. The RFA14N50BE is a monolithic structure incorporating a high voltage, high current MOSFET, a control MOSFET and Esd protection diodes. As indicated in the symbol to the right, the turn on of the main MOSFET is controlled by Gate 1 (G1). The control MOSFET, controlled by Gate 2 (G2), is distributed throughout the structure and provides a very low impedance and low inductive path to discharge the gate of the main MOSFET rapidly when very fast turn-off is desired. A separate return connection, Source Kelvin (Sk), is provided for the gate drive circuits to avoid voltage induced transients from the output circuits during switching. The RFA14N50BE MOSFET transistor can be operated directly from integrated circuits.

The RFA14N50BE is supplied in the JEDEC MO-093 (5-lead) plastic package.

Package

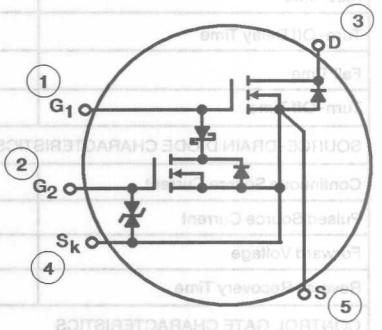
MO-093
TOP VIEW



1 - Gate 1
2 - Gate 2
3 - Drain
4 - Source Kelvin
5 - Source

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFA14N50BE	UNITS
Drain-Source Voltage	V_{DSS}	500	V
Drain Current, Continuous	I_D	14	A
Pulsed	I_{DM}	56	A
Gate-Source Voltage	V_{GS}	+14, -0.3	V
Control FET Gate-Source Voltage	V_{GS}	+14, -0.3	V
Electrostatic Discharge Rating, Mil-Std-883, Category B(2)	E_{SD}	2	KV
Avalanche Current	I_{AR}	14	A
Single Pulse Avalanche Rating	E_{AS}	760	mJ
Control FET Avalanche Current	I_{AR}	1.5	A
Control FET Single Pulse Avalanche Rating	E_{AS}	50	mJ
Power Dissipation, at T_C = +25°C	P_D	180	W
Derating T_C > +25°C		1.4	W/°C
Control FET Power Dissipation, at T_C = 25°C	P_D	21	W
Derated T_C > +25°C		0.17	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +175	°C

10 PREVIEW PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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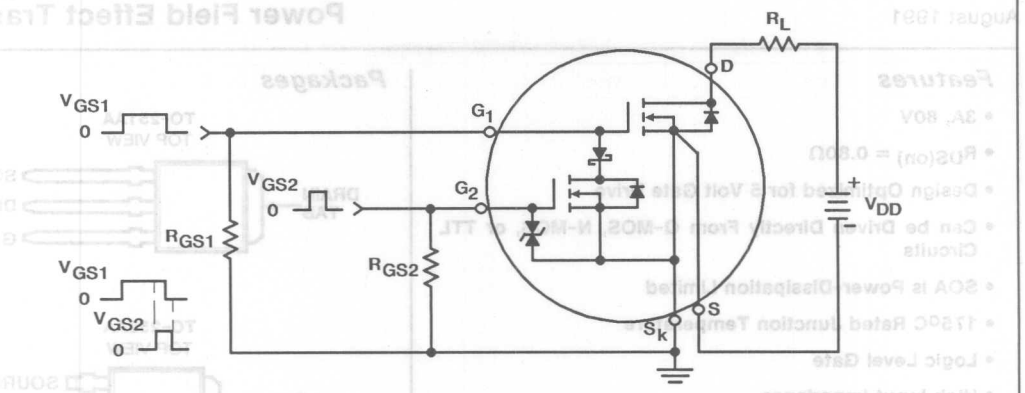
File Number 2835

Electrical Characteristics At Case Temperature (T_C = +25°C), Unless Otherwise Specified

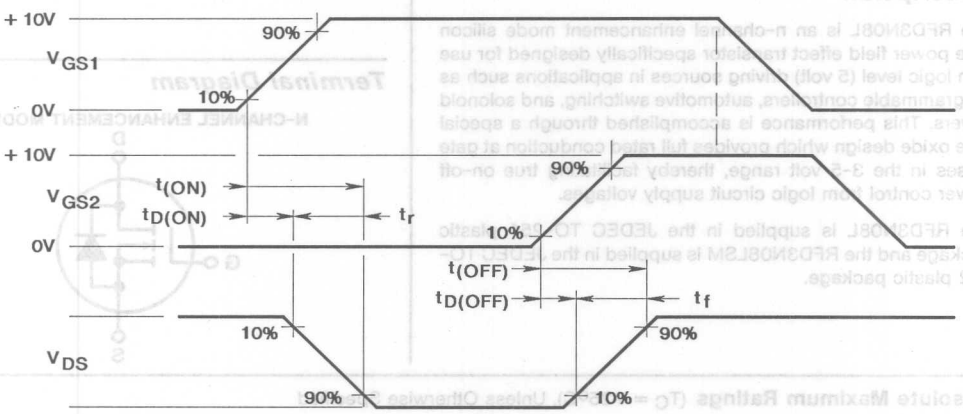
PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	500	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA	2	–	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500V, V_{GS} = 0V	–	–	250	μA
		at T_C = +125°C	–	–	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±12V	–	–	1	μA
		V_{GS} = -0.3V	–	–	-1	μA
On Resistance	$R_{DS(ON)}$	I_D = 14.0A, V_{GS} = 10V	–	–	0.4	Ω
Total Gate Charge	Q_G	V_{DS} = 400V, I_D = 14A	–	–	135	nC
Gate Charge at 5V	$Q_{G(5)}$	RL = 28.6Ω, V_{GS} = 0-10V	–	–	75	nC
Threshold Gate Charge	$Q_{G(TH)}$			–	5.0	nC
SWITCHING CHARACTERISTICS						
Turn-On Time	$t_{(ON)}$	V_{DD} = 250V, I_D = 14A	–	–	75	ns
Turn-On Delay Time	$t_{D(ON)}$	R_L = 17.9Ω	–	14	–	ns
Rise Time	t_r	R_{GS1} = 6.25Ω, R_{GS2} = 20Ω	–	30	–	ns
Turn-Off Delay Time	$t_{D(OFF)}$	V_{GS1} = V_{GS2} = +10V	–	15	–	ns
Fall Time	t_f		–	5	–	ns
Turn-Off Time	$t_{(OFF)}$		–	–	50	ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
Continuous Source Current	I_S		–	–	14	A
Pulsed Source Current	I_{SM}		–	–	56	A
Forward Voltage	V_{SD}	I_S = 14A, V_{GS} = 0V	–	–	1.4	V
Reverse Recovery Time	T_{RR}	I_F = 4A, V_{GS} = 0V	–	–	750	ns
CONTROL GATE CHARACTERISTICS						
Static Drain-to-Source	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 1.0A	–	2.2	–	Ω
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1.0mA, V_{GS} = 0V	14	15	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	3	–	5	V
Total Gate Charge	Q_G	V_{GS} = 10V, I_D = 1.0A	–	–	5	nC
THERMAL RESISTANCE						
Junction-to-Case	$R\theta_{JC}$	–	–	–	0.70	°C/W
Junction to Ambient	$R\theta_{JA}$	–	–	–	40	°C/W

Resistive Switching

SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS



HARRIS

RFD3N08L
RFD3N08LSM

N-Channel Logic Level Power Field Effect Transistors

August 1991

Features

- 3A, 80V
- $R_{DS(on)} = 0.80\Omega$
- Design Optimized for 5 Volt Gate Drive
- Can be Driven Directly From Q-MOS, N-MOS, or TTL Circuits
- SOA is Power-Dissipation Limited
- 175°C Rated Junction Temperature
- Logic Level Gate
- High Input Impedance

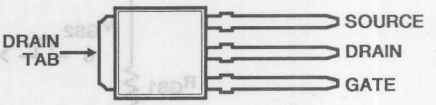
Description

The RFD3N08L is an n-channel enhancement mode silicon gate power field effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solonoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control from logic circuit supply voltages.

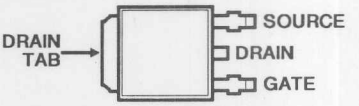
The RFD3N08L is supplied in the JEDEC TO-251 plastic package and the RFD3N08LSM is supplied in the JEDEC TO-252 plastic package.

Packages

TO-251AA
TOP VIEW

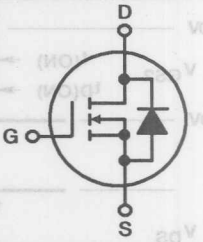


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS} 80V
Drain-Gate Voltage, ($R_{GS} = 1m\Omega$), V_{DGR} 80V
Gate-Source Voltage, V_{GS} ..... ±10V
Drain Current:
  RMS Continuous, I_D 3A
  Pulsed, I_{DM} 7A
Power Dissipation, P_D:
  $T_C = +25^oC$ 30W
  Derate Above $T_C = +25^oC$ ..... 0.20W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG} ..... -55 to +175°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

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File Number 2836

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0V		80	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250µA		1	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 70V		–	1	µA
		V_{DS} = 70V @ T_C = 125°C		–	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 10V, V_{DS} = 0V		–	100	nA
Drain-Source on Voltage	$V_{DS(on)}$	I_D = 1.5A, V_{GS} = 5V		–	1.2	Ω
		I_D = 3A, V_{GS} = 5V		–	2.5	V
On Resistance	$R_{DS(on)}$	I_D = 1.5A, V_{GS} = 5V		–	0.8	Ω
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to 10V	V_{DD} = 48V	–	8	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0 to 5V	I_D = 2A	–	5	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to 1V	R_L = 24Ω	–	1	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 3A, V_{DS} = 15V		–	4.5	V
Turn-On Delay Time	$t_{D(on)}$	V_{DD} = 40V, I_D = 1A		–	20	ns
Rise Time	t_R	R_G = 6.25V, V_{GS} = 5V		–	130	ns
Turn-Off Delay Time	$t_{D(off)}$			–	40	ns
Fall Time	t_F			–	160	ns
Thermal Resistance, Junction to Case	$R_{\theta JC}$			–	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Forward Voltage	V_{SD}	I_{SD} = 1A	–	1.4	V
Reverse Recovery Time	t_{rr}	I_f = 2A, di_f/dt = 100A/µs	–	150(typ.)	ns

HARRIS

RFD4N06L
RFD4N06LSM

N-Channel Logic Level Power Field Effect Transistors

August 1991

Features

- 4A, 60V
- $R_{DS(on)} = 0.60\Omega$
- Design Optimized for 5 Volt Gate Drive
- Can be Driven Directly From Q-MOS, N-MOS, or TTL Circuits
- SOA is Power-Dissipation Limited
- 175°C Rated Junction Temperature
- Logic Level Gate
- High Input Impedance

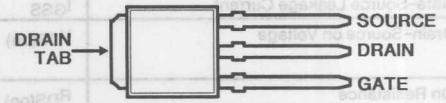
Description

The RFD4N06L is an n-channel enhancement mode silicon gate power field effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solonoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control from logic circuit supply voltages.

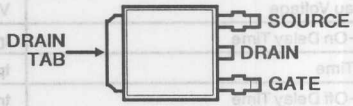
The RFD4N06L is supplied in the JEDEC TO-251 plastic package and the RFD4N06LSM is supplied in the JEDEC TO-252 plastic package.

Packages

TO-251AA
TOP VIEW

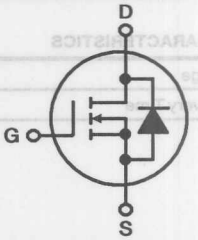


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS} 60V
Drain-Gate Voltage, V_{DSS} 60V
Gate-Source Voltage, V_{GS} ..... ±10V
Drain Current:
  RMS Continuous, I_D 4A
  Pulsed, I_{DM} 10A
Power Dissipation, P_D:
  T_C = +25°C 30W
  Derate Above T_C = +25°C ..... 0.20W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG} ..... -55 to +175°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

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File Number **2837**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain–Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0V		60	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA		1	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50V		–	1	μA
		V_{DS} = 50V @ T_C = 125°C		–	50	μA
Gate–Source Leakage Current	I_{GSS}	V_{GS} = ± 10V, V_{DS} = 0V		–	100	nA
Drain–Source on Voltage	$V_{DS(on)}$	I_D = 1A, V_{GS} = 5V		–	0.8	V
		I_D = 2A, V_{GS} = 5V		–	2.0	V
		I_D = 4A, V_{GS} = 7.5V		–	4.0	V
On Resistance	$R_{DS(on)}$	I_D = 1A, V_{GS} = 5V		–	0.6	Ω
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to 10V	V_{DD} = 48V	–	8	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0 to 5V	I_D = 2A	–	5	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to 1V	R_L = 24Ω	–	1	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 4A, V_{DS} = 15V		–	4.5	V
Turn–On Delay Time	$t_{D(on)}$	V_{DD} = 30V, I_D = 1A		–	20	ns
Rise Time	t_R	R_G = 6.25V, V_{GS} = 5V		–	130	ns
Turn–Off Delay Time	$t_{D(off)}$			–	40	ns
Fall Time	t_F			–	160	ns
Thermal Resistance, Junction to Case	$R_{\theta JC}$			–	5	°C/W

Source–Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Forward Voltage	V_{SD}	I_{SD} = 1A	–	1.4	V
Reverse Recovery Time	t_{rr}	I_f = 2A, di_f/dt = 100A/μs	–	150(typ.)	ns

HARRIS

RFP15N08L

August 1991

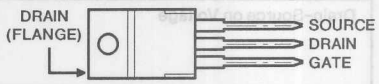
N-Channel Logic Level Power Field-Effect Transistor

Features

- 15A, 80V
- $r_{DS(ON)}$: 0.14Ω
- Design Optimized for 5 Volt Gate Drive
- Can be Driven Directly from Q-MOS, N-MOS, TTL Circuits
- SOA is Power-Dissipation Limited
- +175°C Rated Junction Temperature
- Logic Level Gate
- High Input Impedance

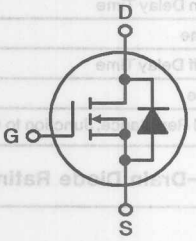
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Description

The RFP15N08L is an n-channel enhancement mode silicon gate power field effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solonoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control from logic circuit supply voltages.

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP15N08L	UNITS
Drain-Source Voltage	V_{DSS}	80	V
Drain-Gate Voltage	V_{DGR}	80	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current, RMS Continuous	I_D	15	A
Pulsed	I_{DM}	40	A
Power Dissipation Total @ T_C = +25°C	P_D	72	W
Power Dissipation Derating T_C = +25°C		0.48	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2840

Electrical Characteristics At Case Temperature (T_C = +25°C), Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA	V_{GS} = 0V	80	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}	I_D = 1mA	1	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V		–	1	µA
		V_{DS} = 65V	at T_C = +125°C	–	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V	V_{DS} = 0V	–	100	nA
Drain-Source On Voltage	$V_{DS(ON)}$	I_D = 7.5A	V_{GS} = 5V	–	1.05	V
		I_D = 15A	V_{GS} = 5V	–	3.0	V
On Resistance	$R_{DS(ON)}$	I_D = 7.5A	V_{GS} = 5V	–	0.14	Ω
Total Gate Charge	$Q_{G(TOTAL)}$	V_{GS} = 0-10V	V_{DD} = 64V	–	80	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0-5V	I_D = 15A	–	45	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0-1V	R_L = 4.27Ω	–	3	nC
Plateau Voltage	$V_{(PLATEAU)}$	I_D =15A	V_{DS} =15V	–	4.5	V
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 40V	I_D = 7.5A	–	40	ns
Rise Time	t_r	R_G = 6.25Ω	V_{GS} = 5V	–	325	ns
Turn-Off Delay Time	$t_{D(OFF)}$			–	325	ns
Fall Time	t_f			–	325	ns
Thermal Resistance Junction to Case	$R\theta_{JC}$	–		–	2.083	°C/W

Source-Drain Diode Ratings and Characteristics

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 7.5A	–	1.4	V
Reverse Recovery Time	T_{RR}	I_F = 4A, di_f/dt = 100a/µs	–	225(typ)	ns

HARRIS SEMICONDUCTOR

RFG70N06
RFP70N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

June 1992

Features

- 70A, 60V
- $r_{DS(on)} = 0.014\Omega$
- UIS Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature
- Temperature Compensated SPICE Model Provided

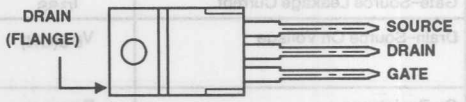
Description

The RFG70N06 and RFP70N06 N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

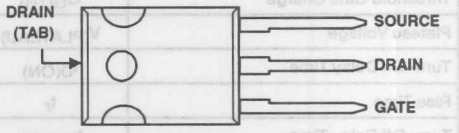
the RFG70N06 is supplied in the JEDEC TO-247 plastic package and the RFP70N06 is supplied in the JEDEC TO-220AB plastic package.

Packages

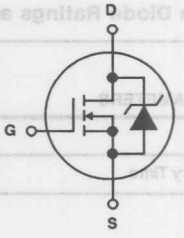
TO-220AB
TOP VIEW



TO-247
TOP VIEW



Terminal Diagram



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFG70N06, RFP70N06	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	70	A
Pulsed Drain Current	I_{DM}	180	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
T_C = +25°C	P_D	150	W
Derate above +25°C	P_T	1.0	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3206

Electrical Characteristics

At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V,	T_C = +25°C	-	-	1	µA
		V_{GS} = 0V	T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(on)}$	I_D = 70A, V_{GS} = 10V		-	-	14	mΩ
Turn-On Time	$t_{(on)}$	V_{DD} = 30V, I_D = 70A, R_L = 0.43Ω, V_{GS} = +10V, R_{GS} = 2.5Ω		-	-	125	ns
Turn-On Delay Time	$t_{d(on)}$			-	12	-	ns
Rise Time	t_r			-	50	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	40	-	ns
Fall Time	t_f			-	15	-	ns
Turn-Off Time	$t_{(off)}$			-	-	125	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0V to 20V	V_{DD} = 48V, I_D = 70A, R_L = 0.68Ω	-	185	215	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	100	115	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0V to 2V		-	5.5	6.5	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 70A, V_{DS} = 15V		-	-	7.5	V
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	3000	-	pF
Output Capacitance	C_{oss}			-	900	-	pF
Reverse Transfer Capacitance	C_{rss}			-	300	-	pF
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 30V, I_D = 70A, L = 0.21µH, R_L = 0.43Ω, V_{GS} = 10V, R_{GS} = 2.5Ω		-	-	1.0	mJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.0	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 70A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 70A, dI_{SD}/dt = 100A/µs	-	-	125	ns

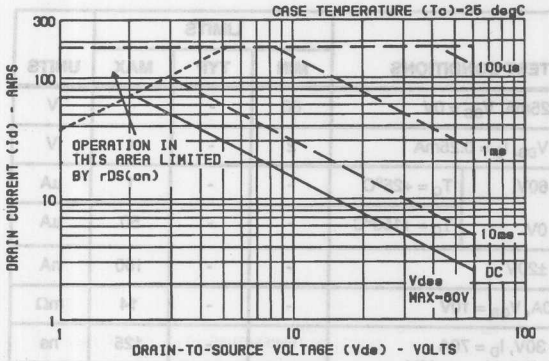


FIGURE 1. SAFE OPERATING AREA CURVE

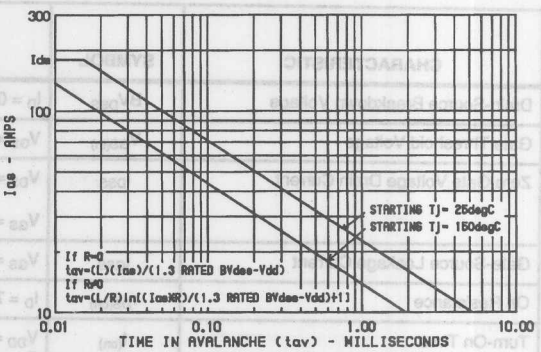


FIGURE 2. UNCLAMPED INDUCTIVE SWITCHING

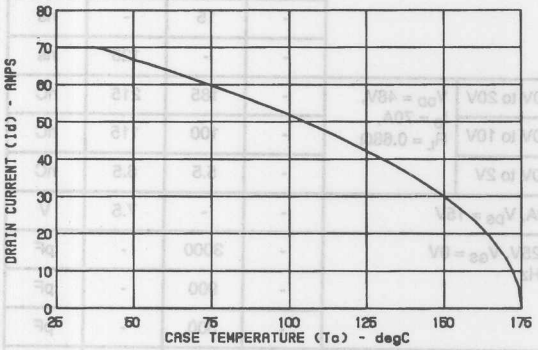


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs. TEMPERATURE

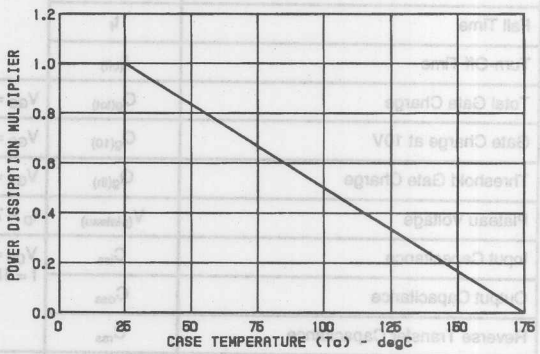


FIGURE 4. NORMALIZED POWER DISSIPATION vs. TEMPERATURE DERATING CURVE

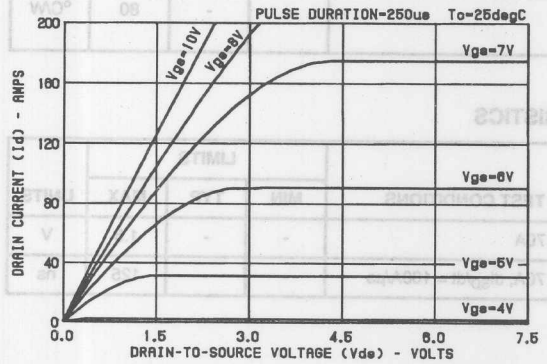


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

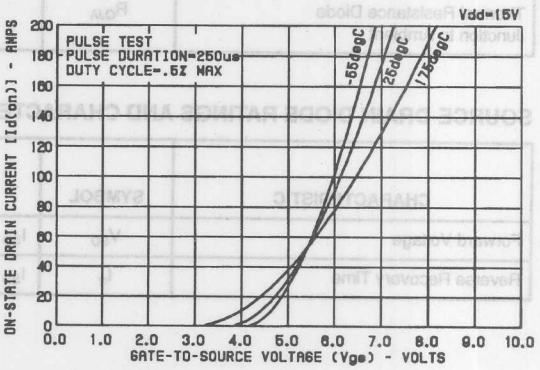


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

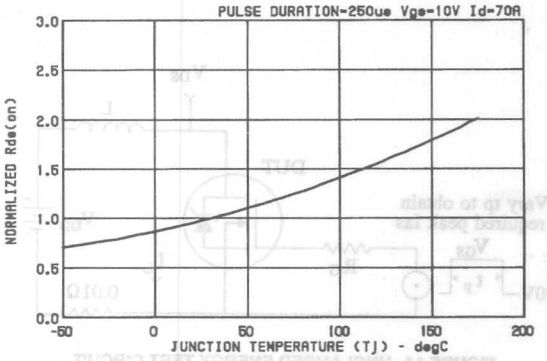


FIGURE 7. NORMALIZED $r_{DS(on)}$ vs. JUNCTION TEMPERATURE

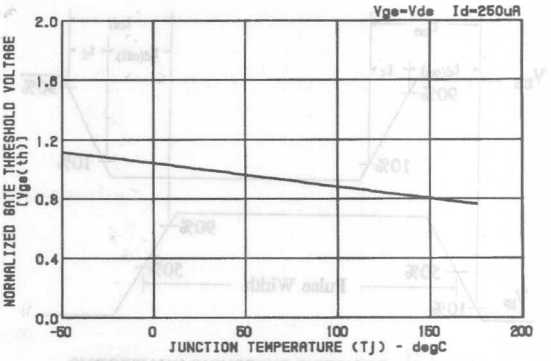


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs. TEMPERATURE

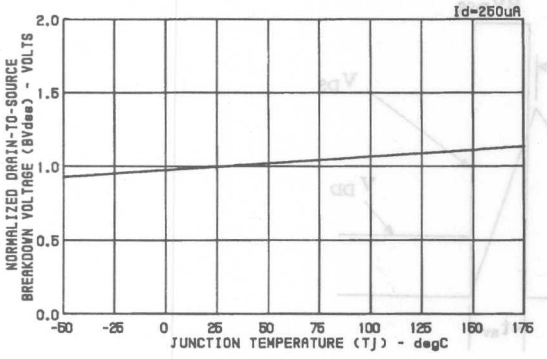


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs. TEMPERATURE

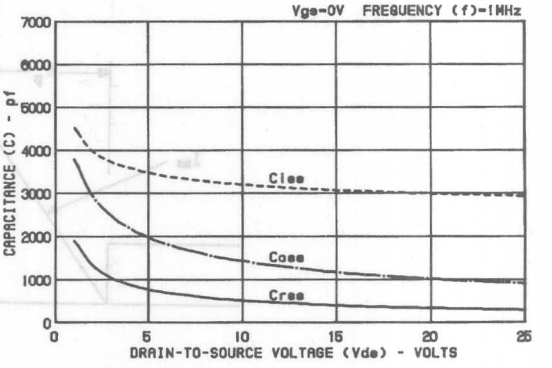


FIGURE 10. TYPICAL CAPACITANCE vs. VOLTAGE

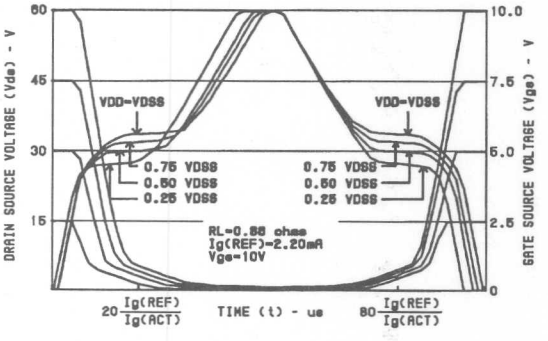


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

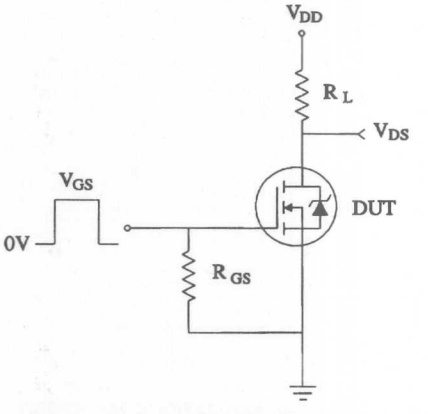


FIGURE 12. RESISTIVE SWITCHING TEST CIRCUIT

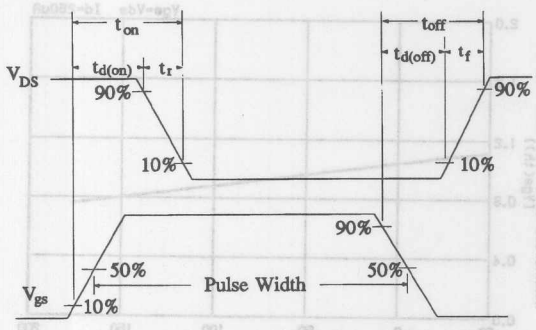


FIGURE 13. RESISTIVE SWITCHING WAVEFORMS

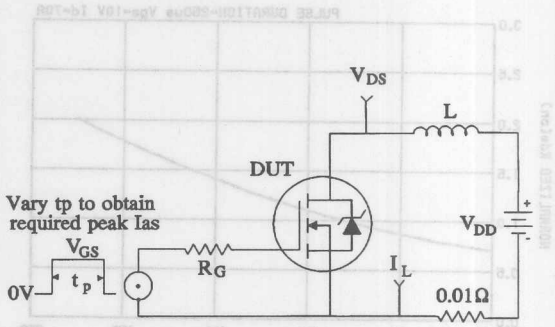


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

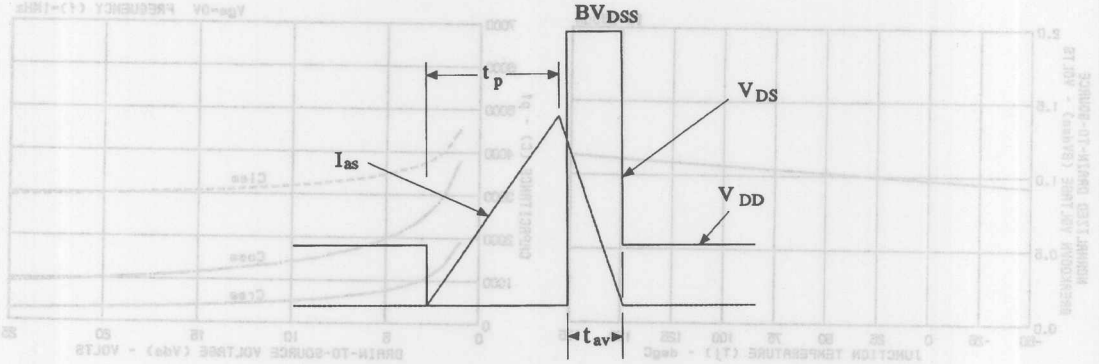
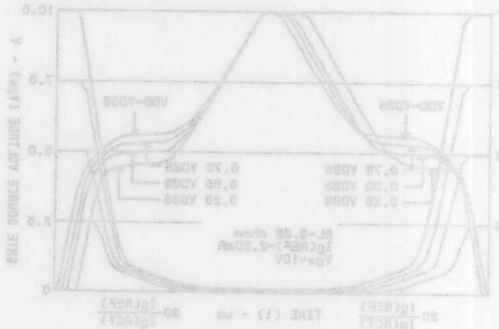


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS



PSPICE Model For the RFG70N06, RFP70N06

```
SUBCKT TA49007 2 1 3 ;        rev 3/20/92
*Nom Temp=25 deg C

Ca 12 8 5.56e-9
Cb 15 14 5.303e-9
Cin 6 8 2.63e-9

Dbody 7 5 DBDMOD
Dplcap 10 5 DPLCAPMOD
Dbreak 5 11 DBKMOD

Ebreak 11 7 17 18 65.1
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evto 20 6 18 8 1

It 8 17 1

Lgate 1 9 3.10e-9
Ldrain 2 5 1e-9
Lsource 3 7 1.82e-9

Mos1 16 6 8 8 MOSMOD M=0.99
Mos2 16 21 8 8 MOSMOD M=0.01

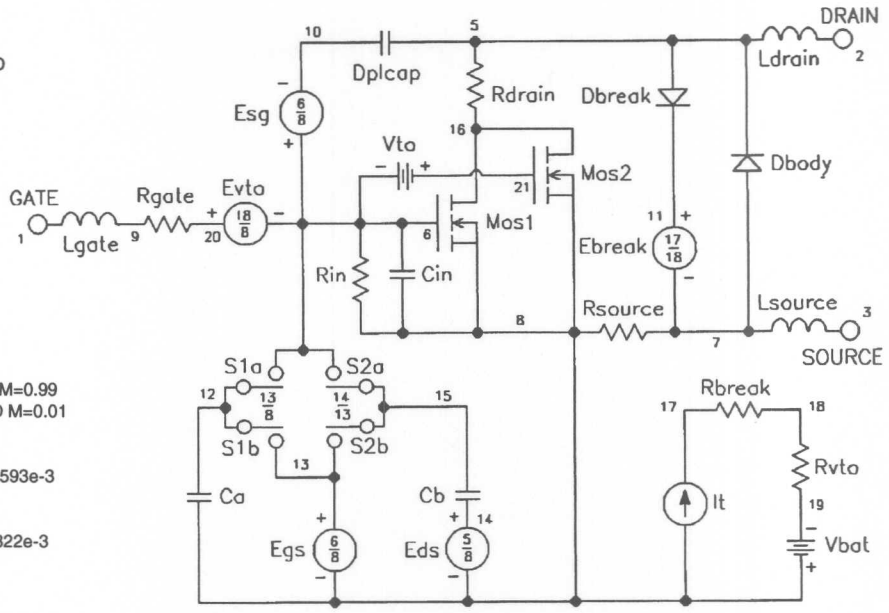
Rbreak 17 18 RBKMOD 1
Rdrain 5 16 RDSMOD 4.6593e-3
Rgate 9 20 1.21
Rin 6 8 1e9
Rsource 8 7 RDSMOD 1.822e-3
Rvto 18 19 RVTOMOD 1

S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 8 19 DC 1
Vto 21 6 0.6977

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.90 VOFF=-2.90)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.90 VOFF=-4.90)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.20 VOFF=4.80)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.80 VOFF=-3.20)
.MODEL DBDMOD D (IS=1.11e-12 RS=2.91e-3 TRS1=3.26e-3 TRS2=-5.07e-6 CJO=3.12e-9 TT=6.18e-8)
.MODEL DBKMOD D (RS=9.46e-2 TRS1=8.47e-4 TRS2=-1.31e-6)
.MODEL DPLCAPMOD D (CJO=1.92e-9 IS=1e-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.674 KP=38.507 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.55e-4 TC2=5.99e-8)
.MODEL RDSMOD RES (TC1=5.01e-3 TC2=2.37e-5)
.MODEL RVTOMOD RES (TC1=-3.71e-3 TC2=-6.01e-7)

.ENDS
```



Note: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

PSPICE Model For the RFG70N06, RFP70N06

```
SUBCKT TA49007 2 1 3 ;        rev 3/20/92
*Nom Temp=25 deg C

Ca 12 8 5.58e-9
Cb 15 14 5.303e-9
Cin 6 8 2.62e-9

Dbody 7 5 DBDMOD
Dplcap 10 5 DPLCAPMOD
Dbreak 5 11 DBKMOD

Ebreak 11 7 17 18 65.1
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evto 20 6 18 8 1

I 8 17 1

Lgate 1 9 3.10e-9
Ldrain 2 5 1e-9
Lsource 3 7 1.82e-9

Mos1 16 6 8 8 MOSMOD M=0.99
Mos2 16 21 8 8 MOSMOD M=0.01

Rbreak 17 18 RBKMOD 1
Rdrain 5 16 RDSMOD 4.8592e-3
Rgate 9 20 1.2Ω
Rin 6 8 1e9
Rsource 8 7 RDSMOD 1.822e-3
Rvto 18 19 RVTOMOD 1

S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 8 19 DC 1
Vto 21 6 0.697

.MODEL S1AMOD VSWITCH (RON=1e-6 ROFF=0.1 VON=-4.50 VOFF=-2.50)
.MODEL S1BMOD VSWITCH (RON=1e-6 ROFF=0.1 VON=-2.50 VOFF=-4.50)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.20 VOFF=-4.80)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.80 VOFF=-3.20)
.MODEL DBDMOD D (IS=1.11e-12 RS=2.81e-3 TRS1=3.26e-3 TRS2=-8.07e-6 CJO=3.12e-9 TT=8.18e-8)
.MODEL DBKMOD D (RS=0.468e-2 TRS1=8.47e-4 TRS2=-1.31e-6)
.MODEL DPLCAPMOD D (CJO=1.82e-9 IS=1e-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.874 KP=38.507 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.35e-4 TC2=5.99e-6)
.MODEL RDSMOD RES (TC1=5.01e-3 TC2=2.37e-5)
.MODEL RVTOMOD RES (TC1=-3.71e-3 TC2=-8.01e-7)

.ENDS
```

Note: For further discussion of the PSPICE model consult A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options; authored by William J. Hepp and C. Frank Wheatley.

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POWER DRIVERS AND SWITCHES

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HARRIS SEMICONDUCTOR

CA3169

Solenoid and Motor Driver (1/2 H Driver)

May 1992

Features

- Chip Encapsulated in a 5-Lead Plastic TO-220 Style Package (VERSA-VI)
- Output Short Circuit Protection
- Thermal Overload Protection
- Solenoid Inductive "Kick" Protection with Internal-Clamp Diodes
- Output Sink and Source Capacity of 600mA Minimum Overtemperature
- Horizontal and Vertical Mounting Packages Available
- Separate Sink Circuit and Source Circuit, Each Individually Controlled

Applications

- Latching Solenoid Driver (Single and Multiple)
- Non-Latching Solenoid Driver
- Relay Driver
- Lamp Controller
- Lamp Driver
- Motor Controller (Forward and Reverse)
- Stepper Motor Controller
- On-Off Logic Controllers (TTL Logic)
- Intermediate Power Driver
- Triac, SCR, and Transistor Drivers

Description

The CA3169 ia a monolithic integrated circuit capable of driving lamps and other devices that can be changed between two states (on or off). Transistors, SCR's, and triacs are some of the solid state devices that can be controlled by the CA3169. This device can also control relays, solenoids (latching or nonlatching), motors (DC - forward and reverse) and DC stepping motors.

The CA3169 contains a separate source driver circuit with internal current limiting protection and a separate sink driver circuit. The sink driver contains an energy absorbing diode to protect the device against any inductive "kick" during state changes. The CA3169 is protected against overvoltage conditions on the output drivers and overtemperature conditions (thermal-shutdown protection).

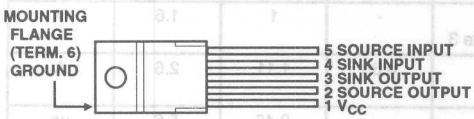
The input operating levels are TTL compatible. The source and sink outputs are in their off condition (non-conducting) when their respective inputs are in a HI state, or open-circuited. The outputs are in their on state (conducting) when their respective inputs are LO. The VERSA-VI package is available with two lead configurations. The CA3169 has a vertical-mount lead form, and the CA3169M has a horizontal-mount lead form.

Ordering Information

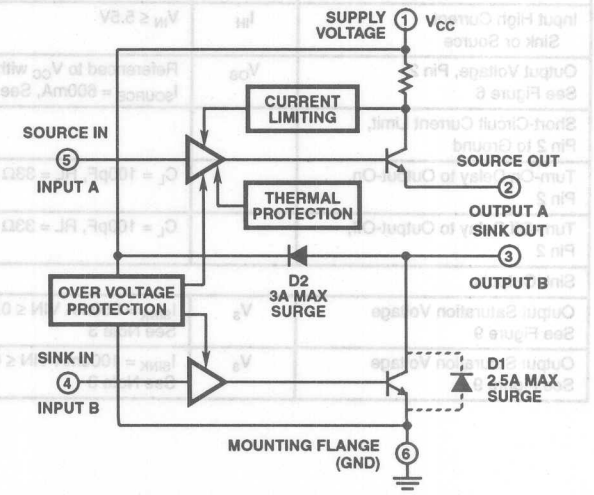
PART NUMBER	TEMPERATURE	PACKAGE
CA33169	-40°C to +85°C	5 Lead Plastic SIP Staggered Vertical
CA33169M	-40°C to +85°C	5 Lead Plastic SIP Surface Mount

Pinout

5 PIN PLASTIC TO-220 SIP
TOP VIEW



Functional Block Diagram



11 POWER DRIVERS AND SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 1277.2

Absolute Maximum Ratings

Supply Voltage (Pin 1 to GND)
- Positive . . . . . 41V DC
- Negative . . . . . 1.4V DC
- Sink Current 1.9A
- Source Current . . . . . Controlled by Internal Current Limiting

Input Voltage:
- Sink Input (Pin 4 to GND) 17V
- Source Input (Pin 5 to GND) 17V

Maximum Forward Current - Diode D1 . . . . . 2.5A
Maximum Forward Current - Diode D2 . . . . . 3A
Power Dissipation, P_D at T_A = 90°C 15W
Thermal Resistance, Junction to Case: . . . . . 4°C/W
- Junction Temperature . . . . . +150°C
- Operating Temperature . . . . . -40°C to +85°C
- Storage Temperature . . . . . -55°C to +150°C

Lead Temperature (During Soldering):
At Distance 1/16 ± 1/32 in. (1.59 ± 0.79mm)
- from case for 10s max. . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications at T_A = +25°C, V_{CC} = 10.5V to 18V Unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Leakage Current, Pin 2 See Figure5		Inputs Open V_{CC} = 4V to 18V Source and Sink Loads = 20Ω	-110	±0.5	110	µA
Output Leakage Current, Pin 3 See Figure 5		Inputs Open V_{CC} = 4V to 18V Source and Sink Loads = 20Ω	-110	±0.5	110	
Thermal Resistance	θ_{JC}		-	3	4	°C/W
Quiescent Current, Pin 1 See Figure 4		Device "ON" Input Terminals Shorted, V_{CC} = 14V	-	70	100	mA
Quiescent Current, Pin 1 See Figure 3		Device "OFF" Input Terminals Open, V_{CC} = 14V	-	17	40	
Thermal Shutdown Temperature		R_L = Short Circuit	128	140	162	°C
Overvoltage Shutdown -Circuit Upper Trip Point, Pin 1 Voltage See Figure7		R_L = 20Ω	20	25	27	V
Overvoltage Shutdown - Circuit Lower Trip Point, Pin 1 Voltage See Figure 7		R_L = 20Ω	18	21.4	23	
Input Logic Levels; Source Input - Pin 5, Sink Input - Pin 4						
Input Low Threshold Sink or Source	V_{IL}	V_{CC} = 14V (See Note 1)	-	0.4	0.8	V
Input High Threshold Sink or Source	V_{IH}	V_{CC} = 14V (See Note 2)	1.9	2.4	-	
Input Low Current Sink or Source	I_{LL}	$V_{IN} \leq 0.4V$	-0.9	-0.3	-	mA
Input High Current Sink or Source	I_{IH}	$V_{IN} \leq 5.5V$	-110	-23	110	µA
Output Voltage, Pin 2 See Figure 6	V_{OS}	Referenced to V_{CC} with I_{SOURCE} = 600mA, See Note 3	-	1	1.6	V
Short-Circuit Current Limit, Pin 2 to Ground			0.65	1.11	2.6	A
Turn-On Delay to Output-On, Pin 2		C_L = 100pF, RL = 33Ω	-	0.45	5.6	µs
Turn-Off Delay to Output-Off, Pin 2		C_L = 100pF, RL = 33Ω	-	5	55	µs
Sink Outputs						
Output Saturation Voltage See Figure 9	V_3	I_{SINK} = 600mA VIN ≤ 0.4V See Note 3	-	0.3	0.85	V
Output Saturation Voltage See Figure 9	V_3	I_{SINK} = 1000mA VIN ≤ 0.4V See Note 3	-	0.8	1.65	

Electrical Specifications at T_A = +25°C, V_{CC} = 10.5V to 18V Unless otherwise specified. **(Continued)**

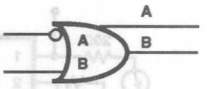
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Turn-On Delay to Output-On Pin 3	T_{ON}	CL = 100pF, RL = 33Ω to V_{CC}	-	0.45	5.6	µs
Turn-Off Delay to Output-Off Pin 3	T_{OFF}	CL = 100pF, RL = 33Ω to V_{CC}	-	0.95	25	

NOTES:

1. I_{SOURCE} or $I_{SINK} \leq 600mA$, $V_{OS} \leq 1.5V$, $V_{SINK} \leq 0.75V$.
2. I_{SOURCE} or $I_{SINK} \leq 100\mu A$, V_{SOURCE} = GND, for V_{SINK} 20Ω to V_{CC}.
3. Measured over temperature range of -40°C to +85°C.

TRUTH TABLE FOR SOLENOID DRIVER
TTL Logic Conditions: 0 ≤ VL ≤ 0.8, 1.9 ≤ VH ≤ 5.5

INPUT A SOURCE IN	INPUT B SINK IN	OUTPUT A SOURCE OUT	OUTPUT B SINK OUT
V_L	V_L	HIGH (ON)	LOW (ON)
V_L	V_H	HIGH (ON)	(OFF)
V_H	V_L	(OFF)	LOW (ON)
V_H	V_H	(OFF)	(OFF)



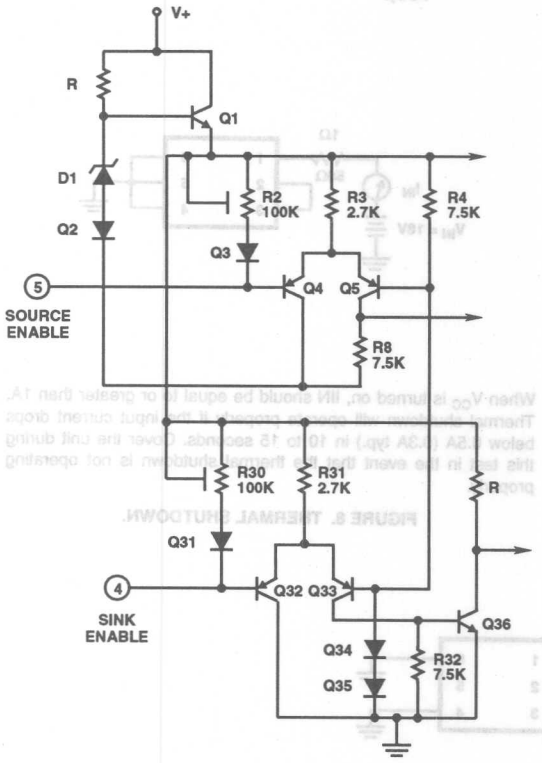


FIGURE 1. DETAILED SCHEMATIC OF THE INPUT CIRCUIT FOR CA3169.

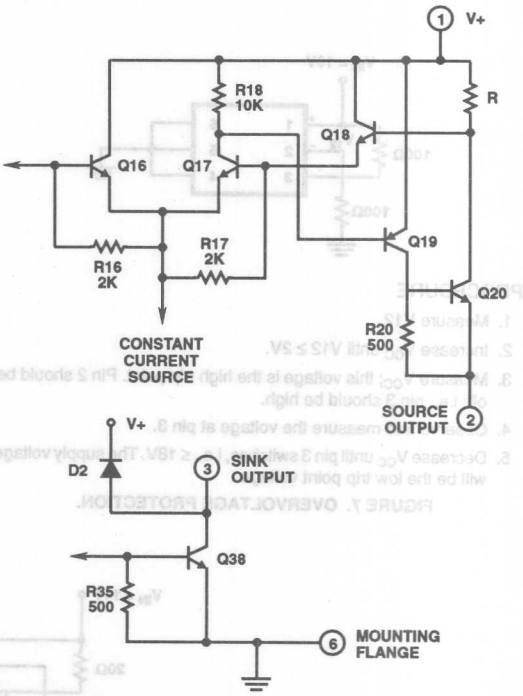


FIGURE 2. DETAILED SCHEMATIC OF THE OUTPUT CIRCUIT FOR CA3169.

Test Circuits

(VCC = VIN = PIN 1 VOLTAGE)

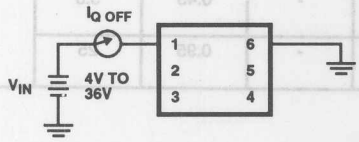


FIGURE 3. QUIESCENT CURRENT DEVICE "OFF".

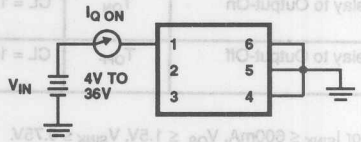


FIGURE 4. QUIESCENT CURRENT DEVICE "ON".

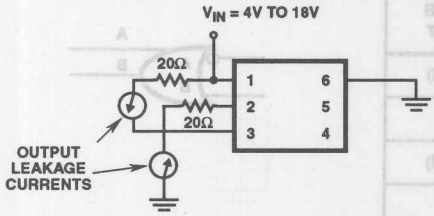


FIGURE 5. OUTPUT LEAKAGE CURRENTS.

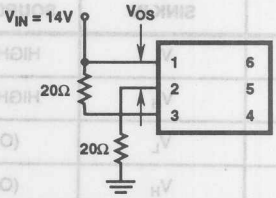
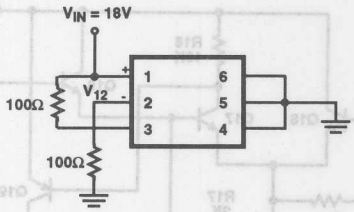


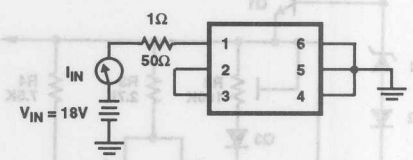
FIGURE 6. OUTPUT SOURCE VOLTAGE (REFERENCED TO VCC).



PROCEDURE

1. Measure V12.
2. Increase V_{CC} until V12 ≥ 2V.
3. Measure V_{CC}; this voltage is the high trip point. Pin 2 should be off; i.e., pin 3 should be high.
4. Observe and measure the voltage at pin 3.
5. Decrease V_{CC} until pin 3 switches, i.e., ≤ 18V. The supply voltage will be the low trip point voltage.

FIGURE 7. OVERVOLTAGE PROTECTION.



When V_{CC} is turned on, IIN should be equal to or greater than 1A. Thermal shutdown will operate properly if the input current drops below 0.5A (0.3A typ.) in 10 to 15 seconds. Cover the unit during this test in the event that the thermal shutdown is not operating properly.

FIGURE 8. THERMAL SHUTDOWN.

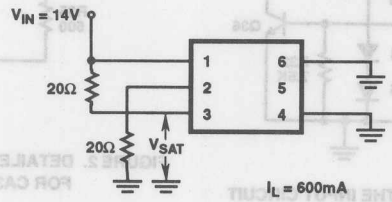
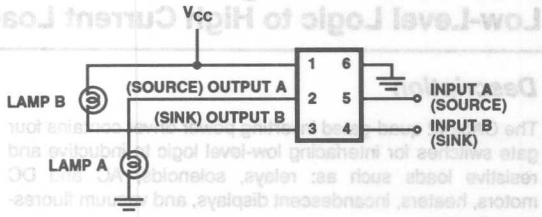


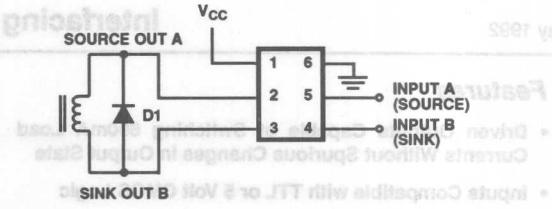
FIGURE 9. OUTPUT SATURATION VOLTAGE.

Typical Applications



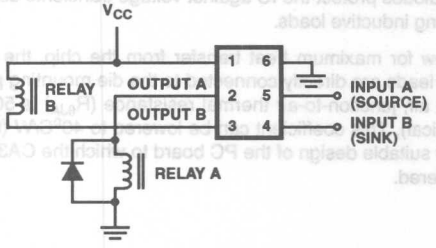
When input A goes low, lamp A will light.
When input B goes low, lamp B will light.

FIGURE 10. LAMP DRIVER.



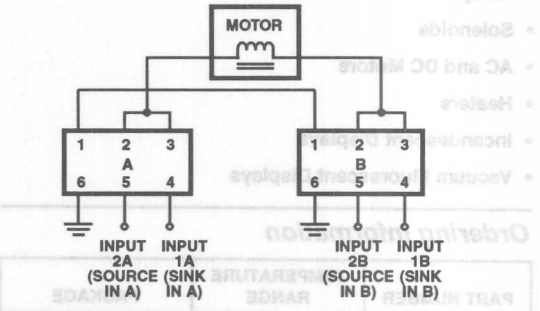
Input A and input B must both be low for the solenoid to switch.

FIGURE 11. NON-LATCHING SOLENOID.



Relay A will close when in input A goes low. Relay B will close when input B goes low. Both relays will close when both inputs go low.

FIGURE 12. RELAY DRIVER.



When opposing inputs go low, the motor will switch direction; if source input A and sink input B both go low, current will flow from A to B. If source input B and sink input A both go low, current will flow from B to A.

FIGURE 13. MOTOR DRIVER OR LATCHING SOLENOID DRIVER.

HARRIS SEMICONDUCTOR

CA3242

Quad-Gated Inverting Power Driver For Interfacing Low-Level Logic to High Current Load

May 1992

Features

- Driven Outputs Capable of Switching 600mA Load Currents Without Spurious Changes in Output State
- Inputs Compatible with TTL or 5 Volt CMOS Logic
- Suitable for Resistive or Inductive Loads
- Output Overload Protection
- Power-Frame Construction for Good Heat Dissipation

Applications

- Relays
- Solenoids
- AC and DC Motors
- Heaters
- Incandescent Displays
- Vacuum Fluorescent Displays

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3242E	-40°C to +105°C	16 Lead Plastic DIP

Description

The CA3242 quad-gated inverting power driver contains four gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent displays, and vacuum fluorescent displays.

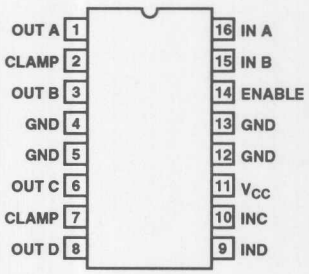
Output overload protection is provided when the load current (approximately 1.2A) causes the output V_{CE}(sat) to rise above 1.3V. A built-in time delay, nominally 25µs, is provided during output turn-on as output drops from V_{DD} to V_{SAT}. That output will be shut down by its protection network without affecting the other outputs. The corresponding Input or Enable must be toggled to reset the output protection circuit.

Steering diodes in the outputs in conjunction with external zener diodes protect the IC against voltage transients due to switching inductive loads.

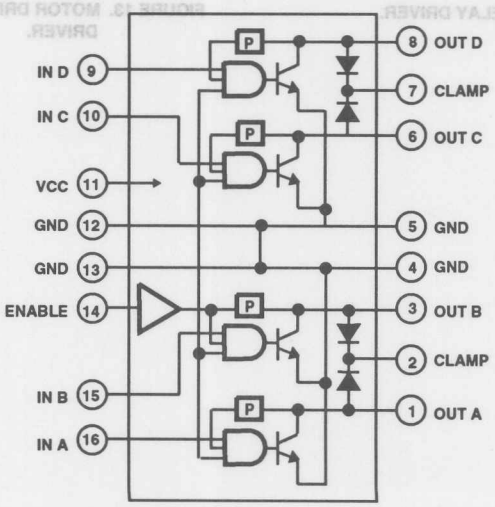
To allow for maximum heat transfer from the chip, the two center leads are directly connected to the die mounting pad. In free air, junction-to-air thermal resistance ($R_{\theta JA}$) is 50°C/W (typical), This coefficient can be lowered to 40°C/W (typical) by suitable design of the PC board to which the CA3242 is soldered.

Pinout

16 LEAD DUAL-IN-LINE PLASTIC PACKAGE (E SUFFIX)
TOP VIEW



Block Diagram



TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **1561.1**

Absolute Information (T_A = +25°C) Unless Otherwise Specified

Logic Supply Voltage, V_{CC} 7V
Logic Input Voltage, V_{IN} 15V
Output Voltage, V_{CEX} . . . . . $50V_{DC}$
Output Sustaining Voltage, V_{CESUS} . . . . . $35V_{DC}$
Output Current, I_O . . . . . $1A_{DC}$
Power Dissipation, P_D
Up to 60°C 1.5W
Above 60°C . . . . . Derate Linearly at 16.6mW/°C
Up to 90°C w/heat sink (PC Board) 1.5W
Above 90°C w/heat sink (PC board) . . Derate Linearly at 25mW/°C

Ambient Temperature Range
Operating . . . . . -40°C to +105°C
Storage . . . . . -55°C to +150°C
Maximum Junction Temperature, T_J . . . . . +150°C
Maximum Thermal Resistance
Junction-to-Air, θ_{JA} . . . . . 60°C/W
Junction-to-Case, θ_{JC} to pins 4, 5, 12, 13 at seat . . . . . 12°C/W
Lead Temperature (During Soldering)
At distance 1/16" ± 1/32" (1.59 ± 0.79mm) from case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At T_A = -40°C to +105°C, V_{CC} = 5V Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Output Leakage Current	I_{CEX}	V_{CE} = 50V, V_{IN} = 0.8V	-	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_C = 100mA, V_{IN} = 0.8V	30	-	V
Collector Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100mA, V_{IN} = 2.4V	-	0.25	V
		I_C = 400mA, V_{IN} = 2.4V	-	0.6	V
		I_C = 600mA, V_{IN} = 2.4V	-	0.8	V
Input Low Voltage	V_{IL}		-	0.8	V
Input Low Current	I_{IL}	V_{IN} = 0.8V	-	±10	µA
Input High Voltage	V_{IH}	I_C = 600mA	2	-	V
Input High Current	I_{IH}	I_C = 700mA, V_{IN} = 4.5V	-	10	µA
Supply Current ON	$I_{CC(ON)}$	I_C = 700mA, V_{CC} = V_{IH} = 5.5V	-	80	mA
Supply Current OFF	$I_{CC(OFF)}$			5	mA
Clamp Diode Leakage Current	I_R	V_R = 50V	-	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 1A	-	1.8	V
		I_F = 1.5A	-	2.5	V
Turn-On Delay	t_{PHL}		-	20	µs
Turn-Off Delay	t_{PLH}		-	30	µs

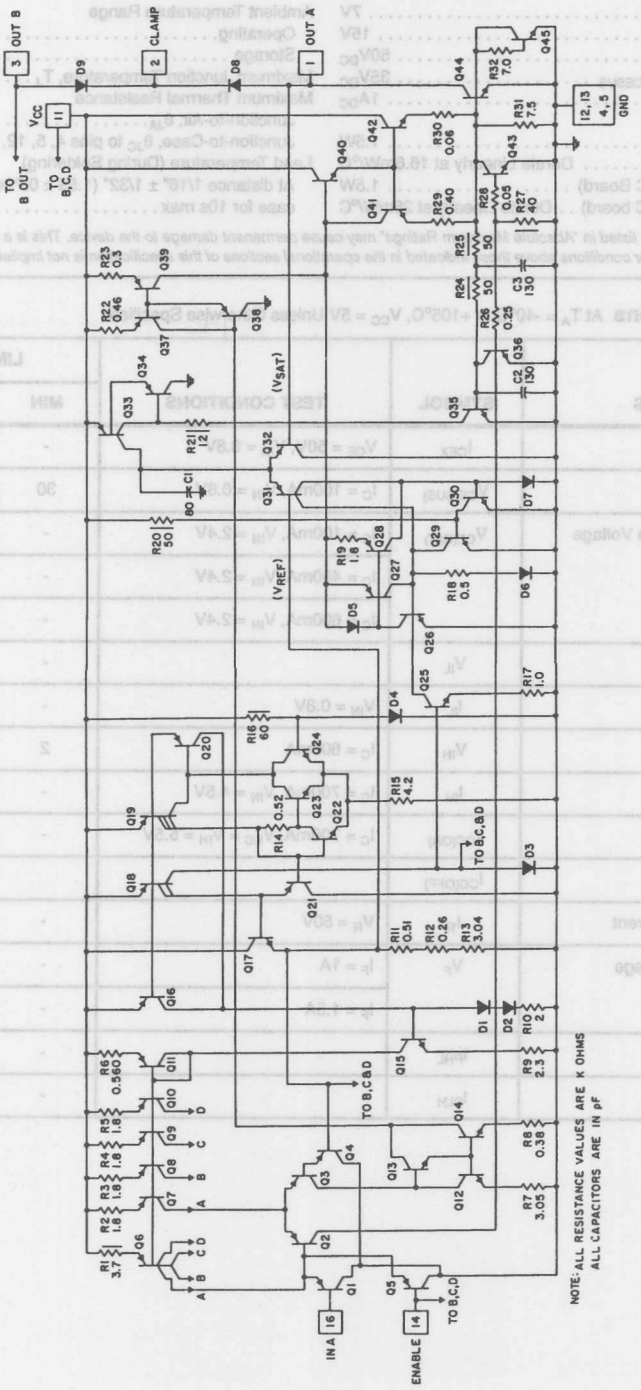


FIGURE 1. SCHEMATIC DIAGRAM OF THE CA3242 (SWITCH SECTION A)

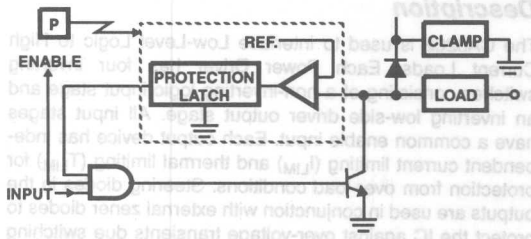


FIGURE 2. LOGIC DIAGRAM FOR EACH OUTPUT

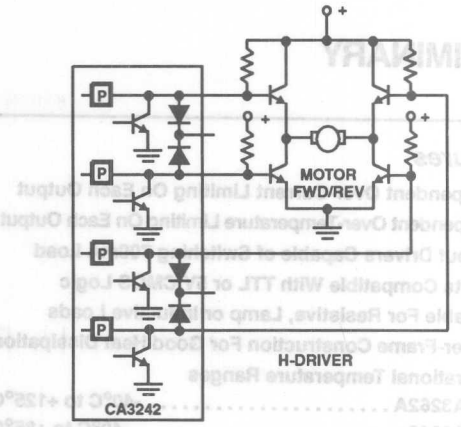


FIGURE 3. TYPICAL APPLICATIONS FOR THE CA3242 QUAD

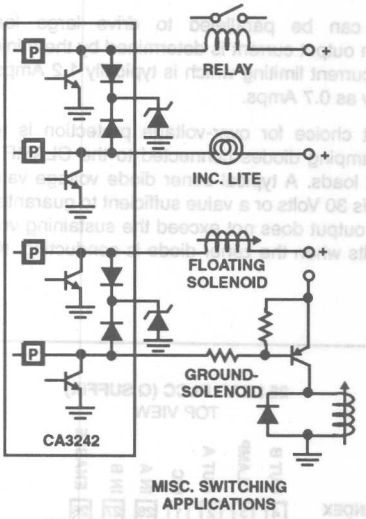


FIGURE 4. TYPICAL APPLICATIONS FOR THE CA3242 QUAD DRIVER

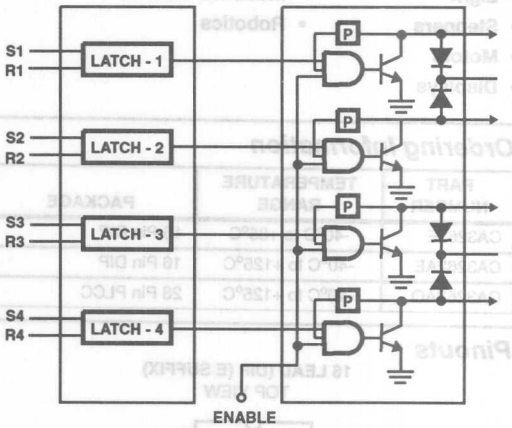


FIGURE 5. TYPICAL APPLICATIONS FOR THE CA3242 QUAD DRIVER

PRELIMINARY

May 1992

Quad-Gated Inverting Power Driver

Features

- Independent Over-Current Limiting On Each Output
- Independent Over-Temperature Limiting On Each Output
- Output Drivers Capable of Switching 700mA Load
- Inputs Compatible With TTL or 5V CMOS Logic
- Suitable For Resistive, Lamp or Inductive Loads
- Power-Frame Construction For Good Heat Dissipation
- Operational Temperature Ranges
  - CA3262A . . . . . -40°C to +125°C
  - CA3262 . . . . . -40°C to +85°C

Applications

- Solenoid
- Relay
- Light
- Steppers
- Motors
- Displays

System Applications

- Automotive
- Appliance
- Industrial Control
- Robotics

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3262E	-40°C to +85°C	16 Pin DIP
CA3262AE	-40°C to +125°C	16 Pin DIP
CA3262AQ	-40°C to +125°C	28 Pin PLCC

Description

The CA3262 is used to interface Low-Level Logic to High Current Loads. Each Power Driver has four inverting switches consisting of a non-inverting logic input stage and an inverting low-side driver output stage. All input stages have a common enable input. Each output device has independent current limiting (I_{LIM}) and thermal limiting (T_{LIM}) for protection from over-load conditions. Steering diodes in the outputs are used in conjunction with external zener diodes to protect the IC against over-voltage transients due switching of inductive loads. To allow for maximum heat transfer from the chip, all ground pins on the DIP and PLCC package are directly connected to the mounting pad of the chip.

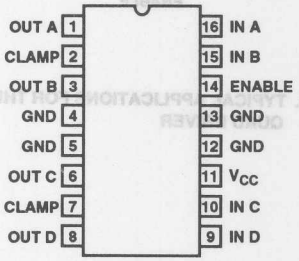
The CA3262 can drive four incandescent lamp loads without modulating their brilliance when the "cold" lamps are energized.

Outputs can be paralleled to drive large loads. The maximum output current is determined by the minimum limit for over-current limiting which is typically 1.2 Amps but may be as low as 0.7 Amps.

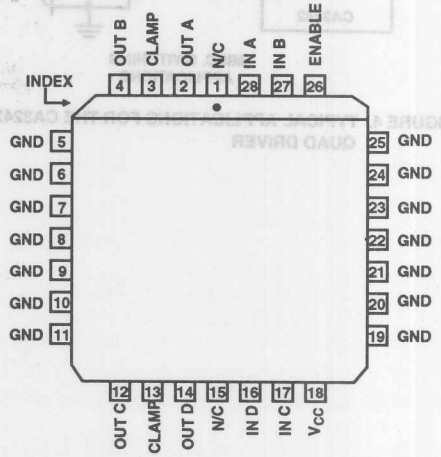
The best choice for over-voltage protection is to provide zener clamping diodes connected to the CLAMP pins with inductive loads. A typical zener diode voltage value for the CA3262 is 30 Volts or a value sufficient to guarantee that the CA3262 output does not exceed the sustaining voltage limit of 40 Volts when the zener diode is conducting. (Continued on 2-8)

Pinouts

16 LEAD (DIP (E SUFFIX)
TOP VIEW



28 LEAD PLCC (Q SUFFIX)
TOP VIEW

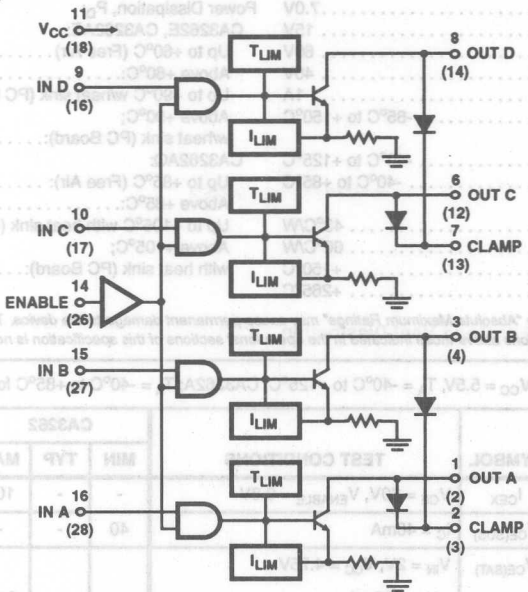


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **1836.1**

Functional Block Diagram



NOTES:

1. Pins 4, 5, 12, 13 ground (Package E)
2. Pins 5-11, 19-25 ground (Package Q)
3. Pin numbers in parentheses apply to the Plastic 28 Leaded Chip Carrier (PLCC)

TRUTH TABLE

ENABLE	IN	OUT
H	5H	L
H	L	H
L	X	H

H = High, L = Low, X = Don't Care

Description (Continued)

Over-voltage protection may or may-not be satisfied by connecting the CLAMP pin to a positive voltage equal or greater than the output load power supply. In many applications transient variations and non-tracking conditions may allow forward conduction through the steering diodes, further up-setting an unstable condition.

Current-limiting is provided as protection for shorted or over-loaded output conditions. Voltage is sampled across a small metal resistor in the emitter of each output stage. When the voltage exceeds a preset comparator level, drive is reduced to the output. Current limiting is sustained unless thermal conditions exceed the preset thermal shutdown temperature of 155°C.

If an output is shorted, the remaining three outputs will continue to function normally unless the continued heat spreading is sufficient to raise the junction temperature at any other output to a level greater than 155°C. High ambient temperature conditions may allow this to happen. The degree of interaction is minimized by separation of the output devices, each to a separate corner of the chip. The output stage does not oscillate when in the current limiting or thermal limiting mode.

As noted, the thermal resistance of both the DIP and PLCC packages are improved by direct connection of the leads to the chip mounting pad. In free air, the junction-to-air thermal resistance, θ_{JA} is 50°C/W (typical) for the DIP package and 40°C/W (typical) for the PLCC package. This coefficient can be lowered to 40°C/W and 30°C/W respectively by suitable design of the PC board to which the CA3262 is soldered.

Absolute Maximum Ratings

Logic Supply Voltage, V_{CC} 7.0V
Logic Input Voltage, V_{IN} 15V
Output Voltage, V_{CEX} 60V
Output Sustaining Voltage, $V_{CE(SUS)}$ 40V
Output Current, I_O 1A
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range:
CA3262AE, CA3262AQ ..... -40°C to +125°C
CA3262E ..... -40°C to +85°C
Thermal Resistance, θ_{ja}:
CA3262AQ ..... 43°C/W
CA3262E, CA3262AE ..... 60°C/W
Maximum Junction Temperature ..... +150°C
Lead Temperature (Soldering 10s) ..... +265°C

Power Dissipation, P_D:
CA3262E, CA3262AE:
Up to +60°C (Free Air) 1.5W
Above +60°C: ..... Derate Linearly at 16.6mW/°C
Up to +90°C w/heat sink (PC Board): 1.5W
Above +90°C;
w/heat sink (PC Board): ..... Derate Linearly at 25mW/°C
CA3262AQ:
Up to +85°C (Free Air): 1.5W
Above +85°C: ..... Derate Linearly at 23mW/°C
Up to +105°C with heat sink (PC Board): 1.5W
Above +105°C;
with heat sink (PC Board): ..... Derate Linearly at 33mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

At V_{CC} = 5.5V, T_A = -40°C to +125°C, CA3262A; T_A = -40°C to +85°C for CA3262

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3262			CA3262A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Leakage Current	I_{CEX}	V_{CE} = 60V, V_{ENABLE} = 0.8V	-	-	100	-	-	50	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_C = 40mA	40	-	-	40	-	-	V
Collector Emitter Saturation Voltage (See Figure 5)	$V_{CE(SAT)}$	V_{IN} = 2V, V_{CC} = 4.75V I_C = 100mA	-	-	0.25	-	-	0.15	V
		I_C = 200mA	-	-	-	-	-	0.2	V
		I_C = 300mA	-	-	-	-	-	0.25	V
		I_C = 400mA	-	-	0.4	-	-	0.3	V
		I_C = 500mA	-	-	-	-	-	0.4	V
		I_C = 600mA	-	-	0.6	-	-	0.5	V
		I_C = 700mA, T_A = -40°C	-	-	0.6	-	-	0.5	V
Input Low Voltage	V_{IL}		-	-	0.8	-	-	0.8	V
Input High Voltage	V_{IH}		2	-	-	2	-	-	V
Input Low Current	I_{IL}	V_{IN} = 0.8V	-	-	10	-	-	10	µA
Input High Current	I_{IH}	V_{IN} = V_{ENABLE} = 5.5V, I_C = 600mA	-	-	10	-	-	10	µA
Supply Current All Outputs ON (See Figure 4)	$I_{CC(ON)}$	V_{IN} = 2V, V_{ENABLE} = 5.5V, I_{OUTA} = I_{OUTB} = I_{OUTC} = I_{OUTD} = 250mA	-	-	70	-	-	55	mA
Supply Current All Outputs OFF (See Figure 4)	$I_{CC(OFF)}$	V_{IN} = 0V	-	-	10	-	-	10	mA
Clamp Diode Leakage Current	I_R	V_R = 50V	-	-	100	-	-	50	µA
Clamp Diode Forward Voltage (See Figure 7)	V_F	I_F = 1A, V_{IN} = 0V	-	-	1.7	-	-	1.7	V
		I_F = 1.5A, V_{IN} = 0V	-	-	2.1	-	-	2.1	V
Turn-On Delay (See Figure 6)	t_{PHL}, t_{PLH}	I_{OUT} = 500mA	-	-	10	-	-	10	µs
Over Current Limiting (Note 1)	I_{LIM}	V_{OUT} = 4.5V to 24.5V	0.7	-	1.8	0.7	-	1.8	A
DESIGN PARAMETER									
Over Temperature Limiting (Junction Temperature)	T_{LIM}		-	155	-	-	155	-	°C

NOTE:

1. With voltage on the collector of the output transistor as indicated (V_{OUT} = 4.5V to 24.5V) and with that output transistor turned on, the current will increase to a limiting value which will be a value of 0.7 A, minimum. That output will shortly thereafter (approx. 5ms) go into over-temperature limiting. (Excessive dissipation during thermal limiting may damage the chip.)

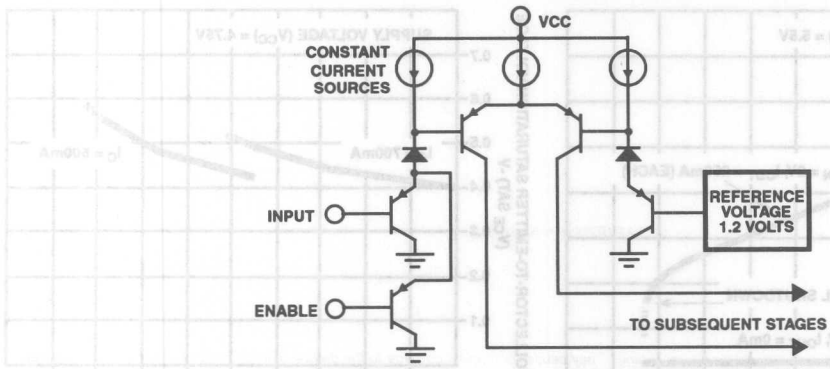


FIGURE 1. CA3262 EQUIVALENT SCHEMATIC OF ONE INPUT STAGE

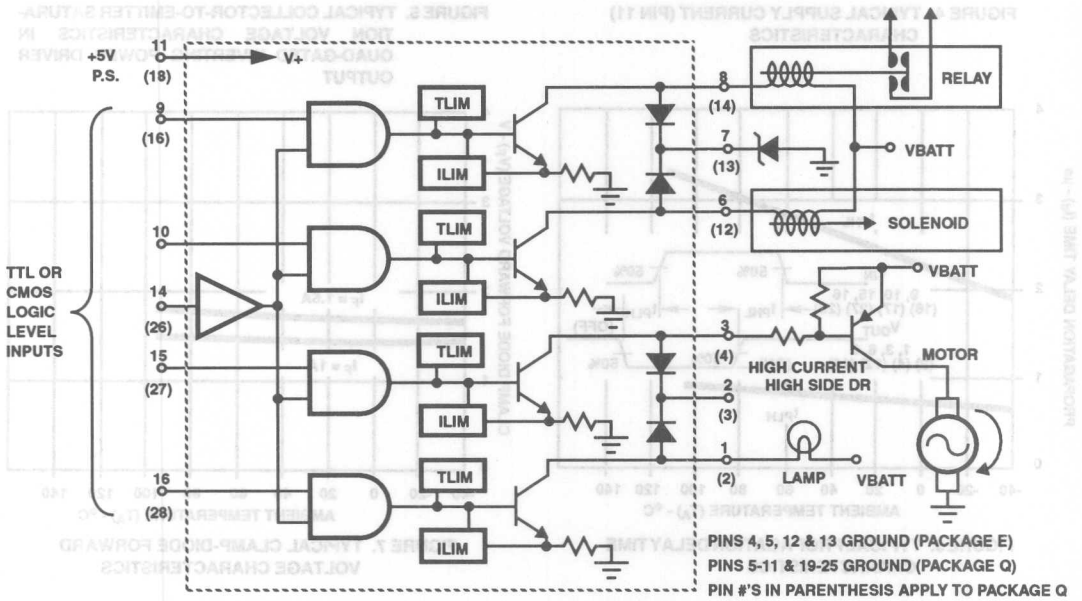


FIGURE 2. QUAD-GATED INVERTING POWER DRIVER (QDR) SCHEMATIC WITH TYPICAL LOAD-DRIVE APPLICATIONS SHOWN. (SEE FIGURE 3)

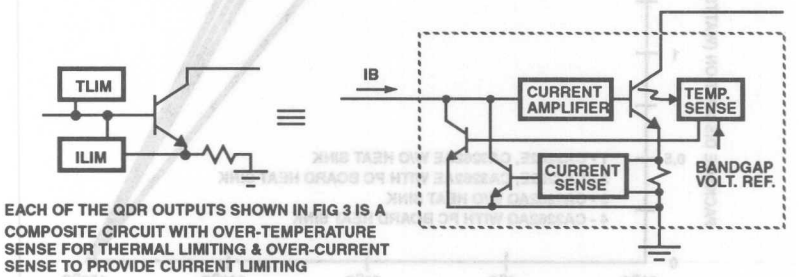


FIGURE 3. QUAD-GATED INVERTING POWER DRIVER (QDR) OUTPUT EQUIVALENT CIRCUIT

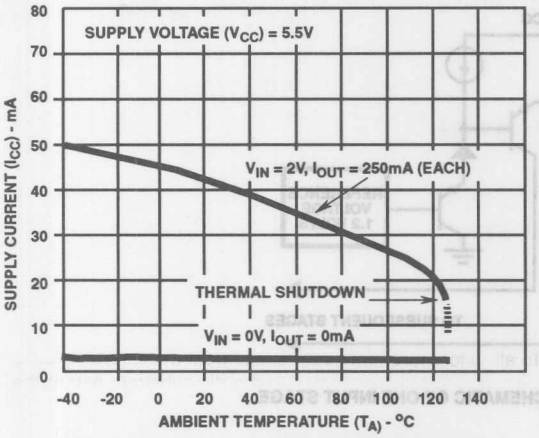


FIGURE 4. TYPICAL SUPPLY CURRENT (PIN 11) CHARACTERISTICS

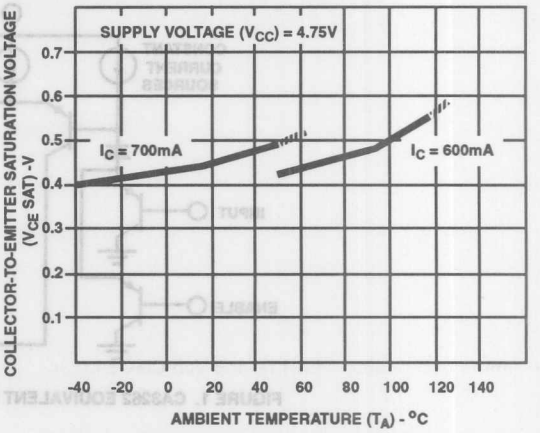


FIGURE 5. TYPICAL COLLECTOR-TO-EMITTER SATURATION VOLTAGE CHARACTERISTICS IN QUAD-GATED INVERTING POWER DRIVER OUTPUT

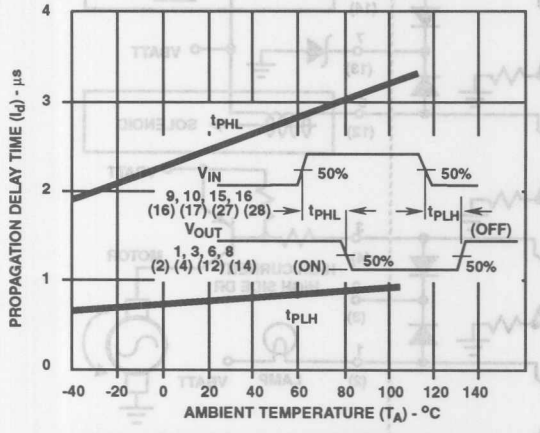


FIGURE 6. TYPICAL PROPAGATION DELAY TIME CHARACTERISTICS

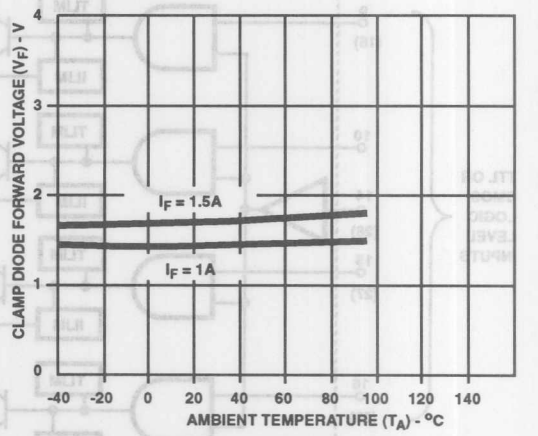


FIGURE 7. TYPICAL CLAMP-DIODE FORWARD VOLTAGE CHARACTERISTICS

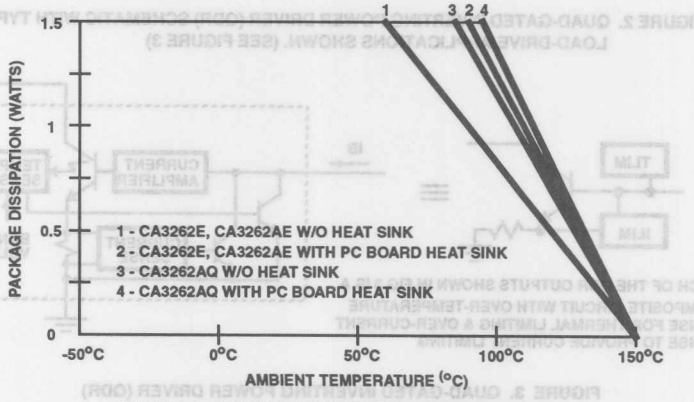


FIGURE 8. PACKAGE DISSIPATION RATING CHART

HARRIS SEMICONDUCTOR

CA3272

Quad-Gated Inverting Power Driver With Fault Mode Diagnostic Flag Output

May 1992

Features

- Independent Over-Current Limiting on Each Output
- Independent Over-Temperature Shutdown With Hysteresis on Each Output
- Capable of Switching 600mA Load Currents
- Inputs Compatible With TTL or 5 Volt CMOS Logic
- Suitable For Resistive or Inductive Loads
- Power-Frame Construction for Good Heat Dissipation
- Fault Mode Output Flag
- Operating Temperature Range . . . . . -40°C to +125°C

Applications

- Solenoid
- Relay
- Light
- Steppers
- Motors
- Displays

System Applications

- Automotive
- Appliance
- Industrial Control
- Robotics

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3272	-40°C to +125°C	28 Lead PLCC

Description

The CA3272 quad-power NAND driver contains four NAND-gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent displays, and vacuum fluorescent displays.

To allow for maximum heat transfer from the chip, all ground leads are directly connected to the die substrate and to the ground bond pads. In free air, junction-to-air thermal resistance ($R_{\theta JA}$) is 40°C/W (typical).

This coefficient can be lowered to 30°C/W (typical) by suitable design of the PC board to which the CA3272 is soldered.

The individual outputs are protected with over-current limiting (I_{LIM}) and over-temperature (T_{LIM}) shutdown. Any one output that faults (see Fault Logic Table) will switch Pin 1 to a constant current pulldown.

If an output load is shorted, the remaining three outputs function normally unless the junction temperature (typically +165°C) of those outputs is exceeded. The output stage does not change state (oscillate) when in the current limit mode.

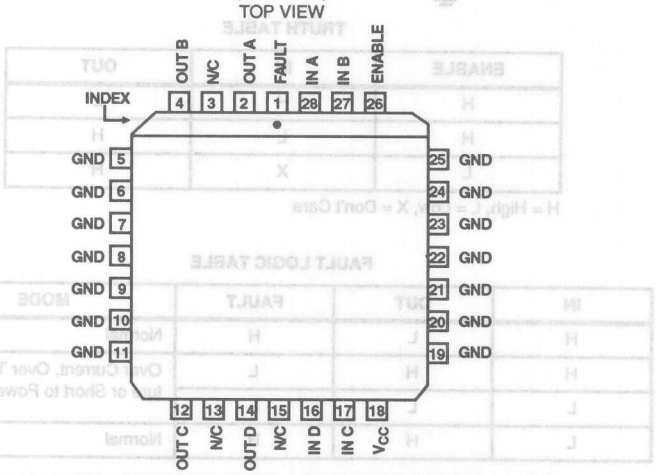
All inputs and enable have internal pulldowns to turn "off" the outputs when inputs are floating.

The CA3272 can drive four incandescent lamp loads without modulating their brilliance when "cold" lamps are energized. Outputs can be "ganged" to drive large loads.

The CA3272 is supplied in a plastic 28 leaded chip carrier, PLCC (Q suffix).

Pinout

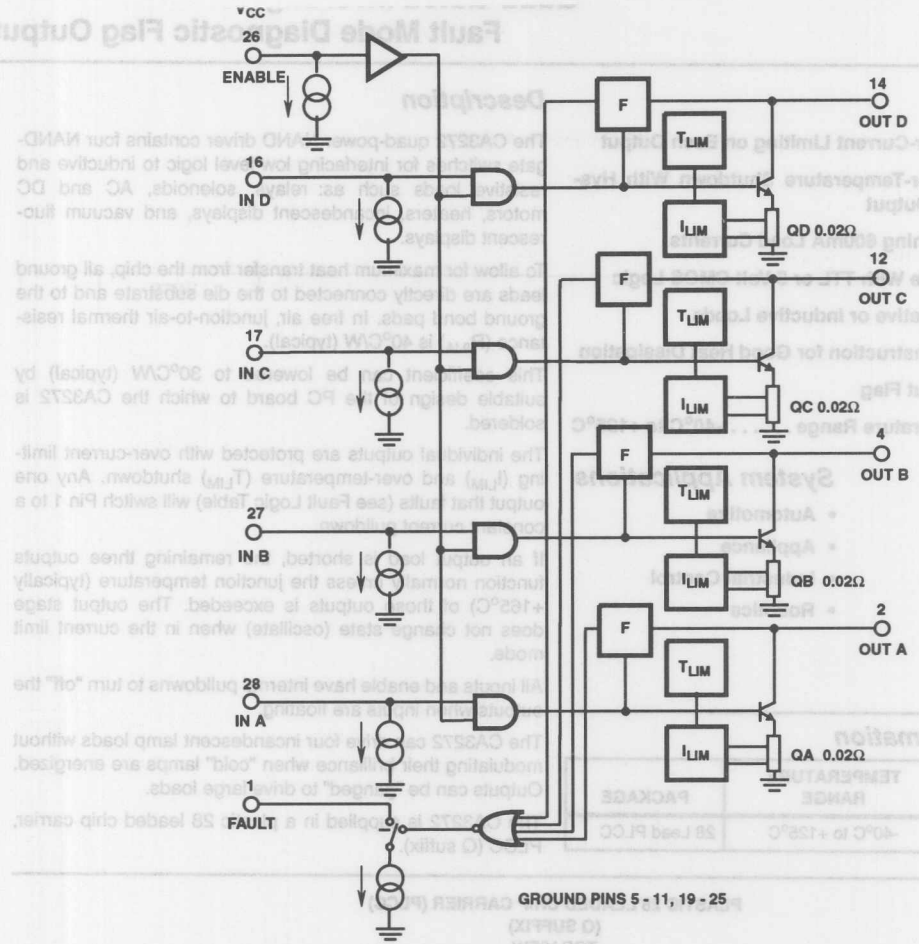
PLASTIC 28 LEADED CHIP CARRIER (PLCC)
(Q SUFFIX)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 2223.1



TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

H = High, L = Low, X = Don't Care

FAULT LOGIC TABLE

IN	OUT	FAULT	MODE
H	L	H	Normal
H	H	L	Over Current, Over Temperature or Short to Power Supply
L	L	L	
L	H	H	Normal

Absolute Maximum Ratings (T_A = +25°C) Unless Otherwise Specified

Logic Supply Voltage, V_{CC} 7V
Logic Input Voltage, V_{IN} 15V
Output Voltage, V_{CEX} . . . . . -12, +50V_{DC}
Output Sustaining Voltage, $V_{CE(SUS)}$ . . . . . 40V_{DC}
Output Current, I_O . . . . . 1.6A_{DC}
Power Dissipation, P_D
Up to 85°C 1.5W
Above 85°C . . . . . Derate Linearly at 23mW/°C
Up to 105°C w/Heat Sink (PC Board) 1.5W
Above 105°C w/Heat Sink (PC Board) . . . Derate Linearly at 33mW/°C

Ambient Temperature Range
Operating . . . . . -40°C to +125°C
Storage . . . . . -55°C to +150°C
Maximum Junction Temperature, T_J . . . . . +150°C
Maximum Thermal Resistance
Junction-to-Air, θ_{JA} . . . . . 43°C/W
Lead Temperature (During Soldering)
At distance $^1/_{16} \pm {}^1/_{32}$" (1.59 ± 0.79mm) from
case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At T_A = -40°C to +125°C, V_{CC} = 5V Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Output Leakage Current	I_{CEX}	V_{CE} = 50V, V_{ENABLE} = 0.8V	-	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_C = 40mA	40	-	V
Collector Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 400mA, V_{IN} = 2V, V_{CC} = 4.75V, T_A = +125°C	-	0.4	V
		I_C = 500mA, V_{IN} = 2V, V_{CC} = 4.75V, T_A = +25°C	-	0.5	V
		I_C = 600mA, V_{IN} = 2V, V_{CC} = 4.75V, T_A = -40°C	-	0.6	V
Input Low Voltage	V_{IL}		-	0.8	V
Input Low Current	I_{IL}	V_{IN} = 0.8V	10	60	µA
Input High Voltage	V_{IH}		2	-	V
Input High Current	I_{IH}	V_{IN} = 5.5V, V_{ENABLE} = 5.5V	10	60	µA
Supply Current ON (All Outputs ON)	$I_{CC(ON)}$	I_{OUT}(A, B, C, D) = 250mA, V_{IN} = 2V V_{ENABLE} = 5.5V	-	60	mA
Supply Current OFF (All Outputs OFF)	$I_{CC(OFF)}$	V_{IN} = 0V	-	10	mA
Turn-On Delay	t_{PHL}, t_{PLH}		-	10	µs
Over Current Limiting* (For Each Output)		V_{OUT} = 4.5V to 24.5V, R_L(Min) = 4Ω	0.7	1.6	A
Fault Output	I_{OL}	I_{LOAD} = 30µA	40	80	µA
	I_{OH}		-	2	µA
	V_{OL}		-	0.4	V
Output Sense Thresholds	V_{HT}	Input = 2V Min	3	5.5	V
	V_{LT}	Input = 0.8V Max	3	5.5	V
DESIGN PARAMETER					
Over Temperature Limiting (Junction Temperature)			165 (Typical)		°C

* With voltage on the collector of the output transistor as indicated (V_{OUT} = 4.5V to 24.5V) and with that output transistor turned on, the current will increase to a limiting value which will be a value of 0.7A minimum. That output will shortly (≈5ms) thereafter go into over temperature shutdown. (Excessive dissipation during thermal shutdown may damage the chip.)

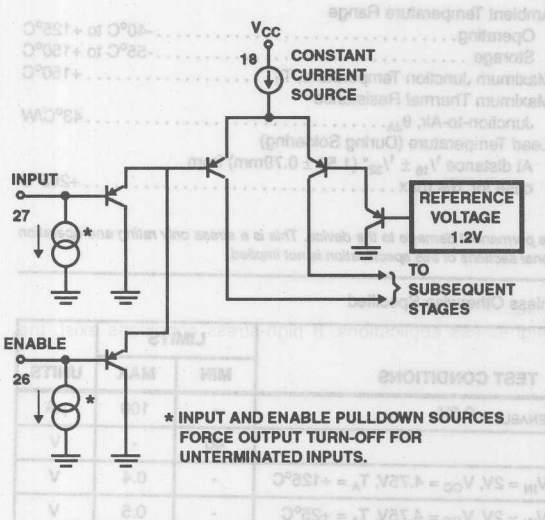


FIGURE 1. SCHEMATIC OF ONE INPUT SECTION

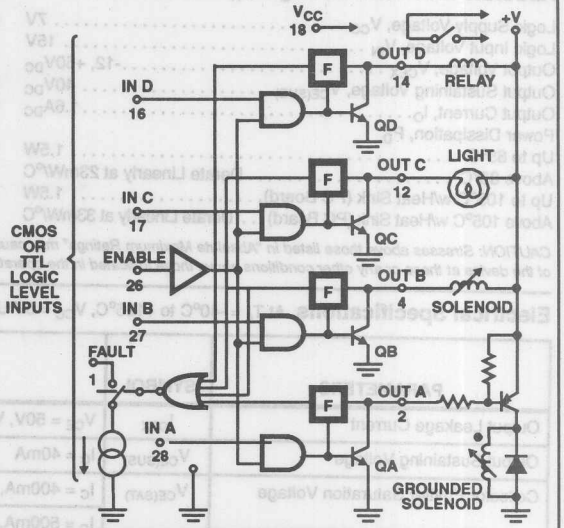


FIGURE 2. QUAD-GATED INVERTING POWER DRIVER (QDR) SCHEMATIC WITH TYPICAL LOAD-DRIVE APPLICATIONS SHOWN (SEE FIGURE 3)

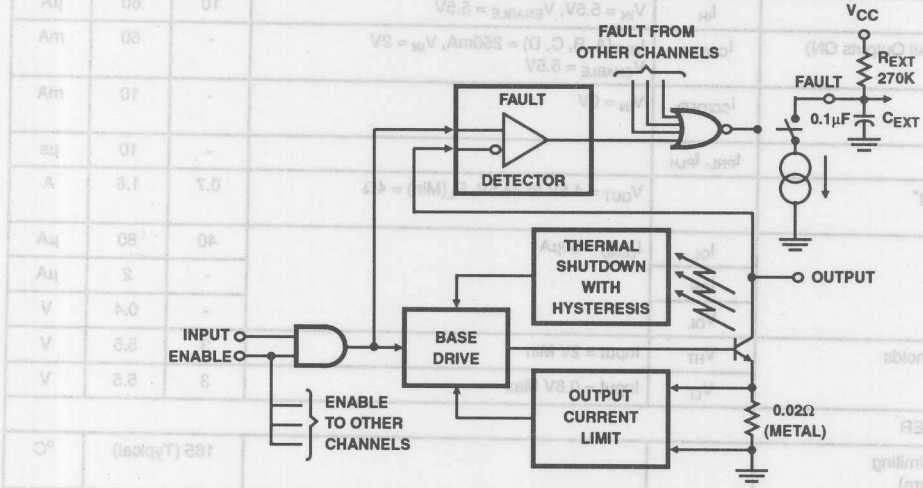


FIGURE 3. QUAD-GATED INVERTING POWER DRIVER (QDR) OUTPUT EQUIVALENT CIRCUIT. THE FAULT OUTPUT REQUIRES A PULL-UP LOAD SUCH AS AN EXTERNAL RESISTOR (R_{EXT}). A CAPACITOR, C_{EXT} SHOULD BE USED TO SUPPRESS SWITCHING SPIKES

HARRIS SEMICONDUCTOR

CA3273

May 1992

High-Side Driver

Features

- Equivalent High Pass p-n-p Transistor
- Current Limiting.....0.6A to 1.2A
- Over-Voltage Shutdown.....+25V to -40V
- Junction Temperature Thermal Limit.....+150°C
- Equivalent beta of 25.....400mA/0.5V
- Internal Bandgap Voltage and Current Reference

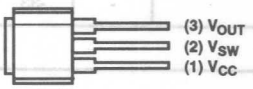
Applications

- Fuel Pump Driver
- Relay Driver
- Solenoid Driver
- Stepper Motor Driver
- Remote Power Switch
- Logic Control Switch

Description

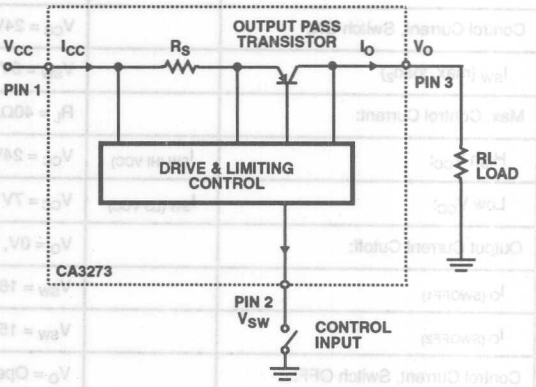
The CA3273 is a power IC equivalent of a p-n-p pass transistor operated as a high-side-driver current switch in either the saturated (ON) or cutoff (OFF) modes. The CA3273 incorporates circuitry to protect the pass currents, excessive input voltage, and thermal overstress. The high-side driver is intended for general purpose, automotive and potentially high-stress applications. If high-stress conditions exist, the use of an external zener diode of 35 volts or less between supply and load terminals may be required to prevent damage due to severe conditions (such as load dump, reverse battery and positive or negative transients). The CA3273 is designed to withstand a nominal reverse-battery (VBAT = 13V) condition without permanent damage to the IC. The CA3273 is supplied in a modified 3-lead TO-202 plastic power package.

Package



MODIFIED TO-202

Block Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE & LEAD FORM
CA3273	-40°C to +85°C	TO-202 MODIFIED

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2113.2**

Absolute Maximum Ratings

Fault Max, V_{CC} (Limited I_{CC}, -40 to +85°C) ..... 25V to 40V
Operating V_{CC} (R_L = 40Ω, -40 to +85°C) 16V
Operating V_{CC} (R_L = 40Ω, -40 to +25°C) 24V
V_O (Output) Inductive Pulse Rating (-40 to +85°C),
V_{SW} Open ..... V_{CC} + 12V
Operating I_{CC} (-40 to +85°C) 1.2A
I_O (-40 to +85°C) 400mA
I_O (-40 to +25°C) 600mA
Dissipation, P_D at +25°C Ambient (Note1) 1.8W
Derate Above +25°C (No Heat Sink) ..... 14.3mW/°C

Thermal Resistance, Junction to Ambient ..... +70°C/W
Junction Temperature (Note 2) ..... +150°C
Ambient Temperature Range:
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -40°C to +150°C
Lead Temperature (During Soldering):
At distance 1/16± 1/32 in. (1.59 ± 0.79 mm)
from case for 12s max. ..... +260 °C

NOTES:
1. $P_D = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{SW}$, $T_J = T_A + P_D \times (\theta_{ja})$
2. Thermal limiting (shutdown) occurs at +150°C on the chip.

Electrical Specifications at T_A = -40°C to +85°C, (See Block Diagram For Test Pin Reference)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Voltage Range	V_{CC}	V_{CC} Reference to V_{SW}	4	-	24	V
Sat. Voltage(V_{CC} - V_O):	V_{SAT}	I_O = -400 mA, V_{SW} = 0V, V_{CC} = 16V	-	-	0.5	V
Operating Load	R_L	V_{CC} = 16V to 24V	40	-	-	W
Overvolt, T_{HD} (Increase V_{CC})	$V_{CC(THD)}$	V_{SW} = 0V, R_L = 1kΩ (V_O goes Low)	25	-	40	V
Current Limiting	$I_O(I_{IM})$	V_{CC} = 16V, V_{SW} = 1V	-	-	1.2	Amp
Control Current, Switch ON:		V_{CC} = 16V, V_{SW} = 0V				
I_{SW} (no load)		I_O = 0mA	-	-15	-	mA
I_{SW} (max. load$_1$)		I_O = -400mA	-	-22	-	mA
Control Current, Switch ON:		V_{CC} = 24V, I_O = -600mA	-	-33	-	mA
I_{SW} (max. load$_2$)		V_{SW} = 0V				
Max. Control Current:		R_L = 40Ω, V_{SW} = 1V				
High V_{CC}:	$I_{SW\ (HI\ VCC)}$	V_{CC} = 24V	-50	-	-	mA
Low V_{CC}:	$I_{SW\ (LO\ VCC)}$	V_{CC} = 7V	-50	-	-	mA
Output Current Cutoff:		V_O = 0V, V_{CC} = 16V				
$I_{O\ (SWOFF1)}$		V_{SW} = 16V	-10	-	+100	µA
$I_{O\ (SWOFF2)}$		V_{SW} = 15V	-100	-	+100	µA
Control Current, Switch OFF:		V_O = Open				
No Load:	$I_{SW\ (HI\ VCC)}$	V_{CC} = 24V, V_{SW} = 23V	-200	-	+50	µA
	$I_{SW\ (LO\ VCC)}$	V_{CC} = 7V, V_{SW} = 6V	-200	-	+50	µA

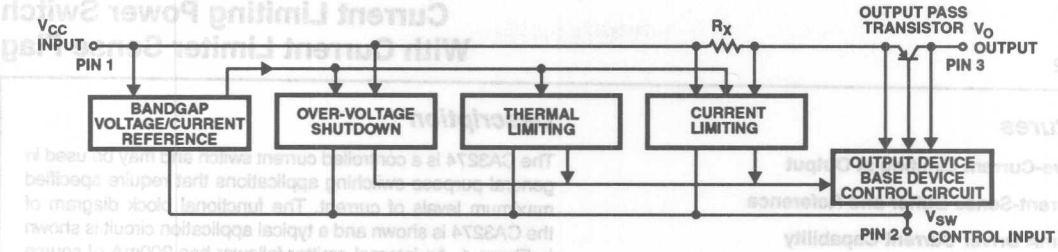


FIGURE 1. FUNCTION BLOCK DIAGRAM OF CA3273

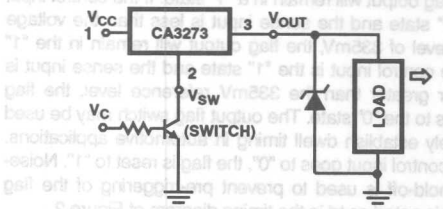


FIGURE 2. TYPICAL APPLICATION WITH ZENER DIODE ($\leq V_{CC}$ +12V) FOR INDUCTIVE SWITCHING PULSE OVER-VOLTAGE PROTECTION

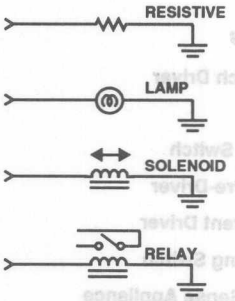


FIGURE 3. TYPICAL LOADS

HARRIS SEMICONDUCTOR

CA3274

Current Limiting Power Switch With Current Limiter Sense Flag

May 1992

Features

- Drive-Current Limiting at Output
- Current-Sense Buffer and Reference
- 200mA Driver Current Capability
- Logic-Level Control Input
- Current Limiting Flag Output
- 50dB Minimum PSRR
- 5μS Typical Switch Time
- Separate Signal and Power Grounds

Applications

- Solenoid Switch Driver
- Relay Driver
- Lamp Control Switch
- Ignition Coil Pre-Driver
- Constant Current Driver
- Current Limiting Switch
- Fault Output Sense Appliance
- Power Supply Fault Mode Control

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3274E	-40°C to +85°C	8 Lead Plastic DIP

Description

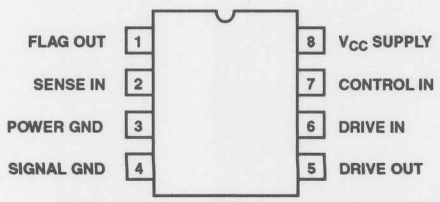
The CA3274 is a controlled current switch and may be used in general purpose switching applications that require specified maximum levels of current. The functional block diagram of the CA3274 is shown and a typical application circuit is shown in Figure 1. An internal emitter follower has 200mA of source drive output capability. The Control Input is a Schmitt trigger buffer amplifier for noise immunity in the environments typical of industrial and automotive control systems.

Current sensing in the emitter circuit of a power-darlington output stage is fed back from a sampling resistor to the sense input of the CA3274 which has a 335mV typical offset. For the example shown in Figure 1, a sampling resistor of 0.056 ohm permits 6.0 amperes (0.335/0.056) of current in the emitter of the output driver. When the current limiter is activated, the flag output changes state conditionally. If the control input is the "0" state, the flag output will remain in a "1" state. If the control input is in the "1" state and the sense input is less than the voltage reference level of 335mV, the flag output will remain in the "1" state. If the control input is the "1" state and the sense input is equal to or greater than the 335mV reference level, the flag output goes to the "0" state. The output flag switch may be used to accurately establish dwell timing in automotive applications. When the control input goes to "0", the flag is reset to "1". Noise-immunity hold-off is used to prevent pre-triggering of the flag output and is noted as td in the timing diagram of Figure 2.

The flag output may be used for diagnostic feedback via the current sense input to detect a fault mode. In this case the sampled drive current is either from the emitter of the CA3274 internal power transistor or an external output amplifier, such as a darlington power transistor or power-FET output stage. The CA3274 has separate power and signal grounds to minimize transient-loop feedback to the input ground and thus prevent false triggering of the output. Optionally, the output from the CA3274 may be taken from the open collector (DRIVE IN) at pin 6. An external resistor at pin 6 may be used to set the level at which Q2 will saturate, providing additional limiting protection for the maximum forward-drive from the CA3274.

Pinout

8 LEAD DUAL-IN-LINE PLASTIC PACKAGE (E SUFFIX)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2222.1**

Block Diagram

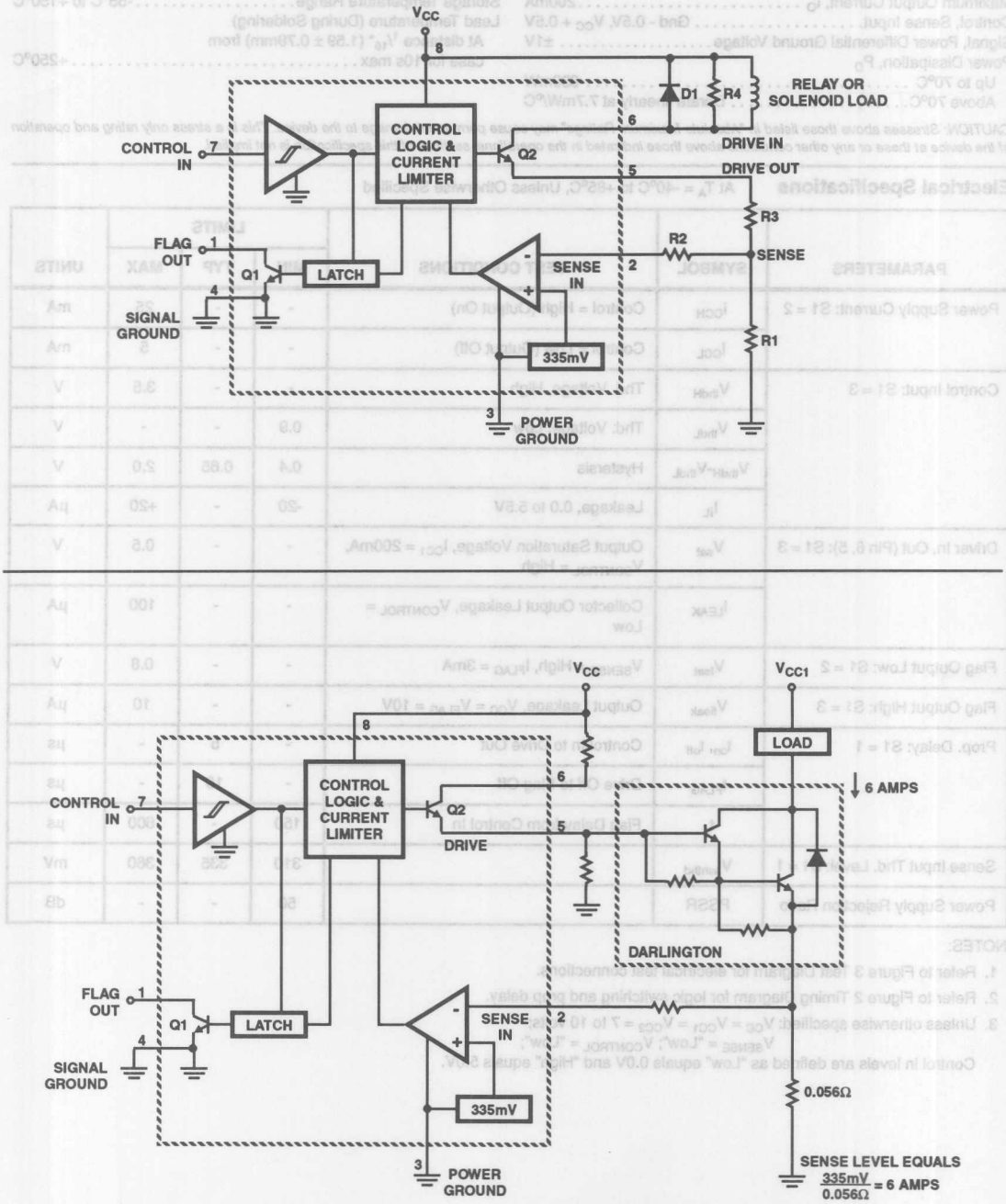


FIGURE 1. TYPICAL APPLICATION AS A POWER SWITCH PRE-DRIVER SWITCH

Absolute Maximum Ratings

Operating Drive Supply, V_{CC} 16V
Maximum Output Current, I_O 200mA
Control, Sense Input..... Gnd - 0.5V, V_{CC} + 0.5V
Signal, Power Differential Ground Voltage..... ±1V
Power Dissipation, P_D
Up to 70°C 630mW
Above 70°C..... Derate linearly at 7.7mW/°C

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -55°C to +150°C
Lead Temperature (During Soldering)
At distance $^1/_{16}$" (1.59 ± 0.79mm) from
case for 10s max..... +250°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

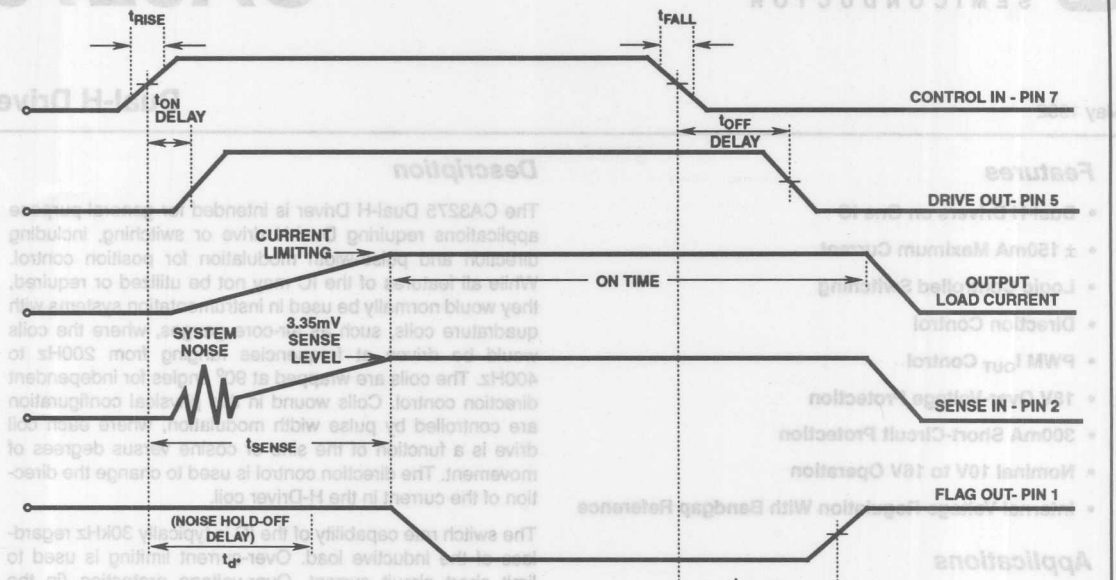
Electrical Specifications

At T_A = -40°C to +85°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Power Supply Current: S1 = 2	I_{CCH}	Control = High (Output On)	-	-	25	mA
	I_{CCL}	Control = Low (Output Off)	-	-	5	mA
Control Input: S1 = 3	V_{thdH}	Thd. Voltage, High	-	-	3.5	V
	V_{thdL}	Thd. Voltage, Low	0.9	-	-	V
	V_{thdH}-V_{thdL}	Hystersis	0.4	0.65	2.0	V
	I_{IL}	Leakage, 0.0 to 5.5V	-20	-	+20	µA
Driver In, Out (Pin 6, 5): S1 = 3	V_{sat}	Output Saturation Voltage, I_{CC1} = 200mA, $V_{CONTROL}$ = High	-	-	0.5	V
	I_{LEAK}	Collector Output Leakage, $V_{CONTROL}$ = Low	-	-	100	µA
Flag Output Low: S1 = 2	V_{fsat}	V_{SENSE} = High, I_{FLAG} = 3mA	-	-	0.8	V
Flag Output High: S1 = 3	V_{fleak}	Output Leakage, V_{CC} = V_{FLAG} = 10V	-	-	10	µA
Prop. Delay: S1 = 1	t_{on}, t_{off}	Control In to Drive Out	-	5	-	µs
	t_{FLAG}	Drive Off to Flag Off	-	10	-	µs
	t_d	Flag Delay from Control In	150	-	600	µs
Sense Input Thd. Level: S1 = 1	V_{senthd}		310	335	360	mV
Power Supply Rejection Ratio	PSSR		50	-	-	dB

NOTES:

1. Refer to Figure 3 Test Diagram for electrical test connections.
2. Refer to Figure 2 Timing Diagram for logic switching and prop delay.
3. Unless otherwise specified: V_{CC} = V_{CC1} = V_{CC2} = 7 to 10 volts;
V_{SENSE} = "Low"; $V_{CONTROL}$ = "Low";
Control in levels are defined as "Low" equals 0.0V and "High" equals 5.0V.



* For V_{CC} = 7V to 10V; t_{dr} (MAX) = 600µS if Control In = High, Sense In = High; Pin 1, Flag Out can go low only if $t_{SENSE} \geq t_d$

FIGURE 2. CA3274 TIMING DIAGRAM

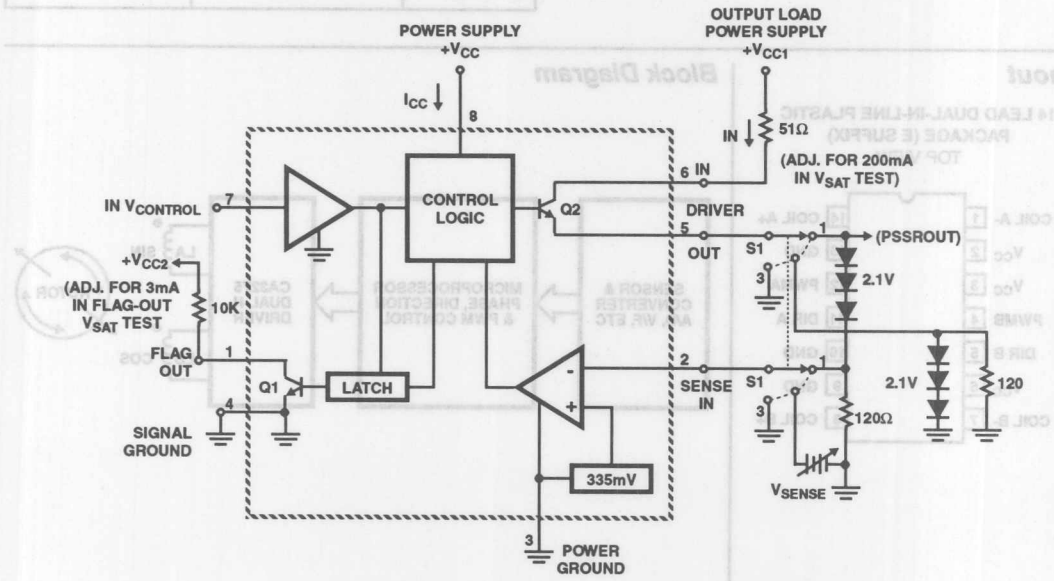


FIGURE 3. CA3274 TEST CIRCUIT

HARRIS SEMICONDUCTOR

CA3275

May 1992

Dual-H Driver

Features

- Dual-H Drivers on One IC
- ± 150mA Maximum Current
- Logic Controlled Switching
- Direction Control
- PWM I_{OUT} Control
- 18V Over-Voltage Protection
- 300mA Short-Circuit Protection
- Nominal 10V to 16V Operation
- Internal Voltage Regulation With Bandgap Reference

Applications

- Dual H-Switch For Air Core Gauge Instrumentation
- µP Controlled Sensor Data Displays
- Speedometer Displays
- Tachometer Displays
- Stepper Motors
- Slave Position Indicators

Description

The CA3275 Dual-H Driver is intended for general-purpose applications requiring Dual-H drive or switching, including direction and pulse-width modulation for position control. While all features of the IC may not be utilized or required, they would normally be used in instrumentation systems with quadrature coils, such as air-core gauges, where the coils would be driven at frequencies ranging from 200Hz to 400Hz. The coils are wrapped at 90° angles for independent direction control. Coils wound in this physical configuration are controlled by pulse width modulation, where each coil drive is a function of the sine or cosine versus degrees of movement. The direction control is used to change the direction of the current in the H-Driver coil.

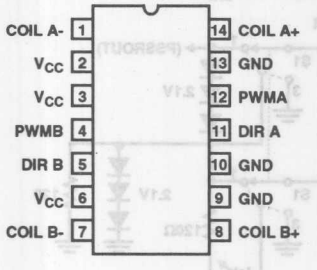
The switch rate capability of the IC is typically 30kHz regardless of the inductive load. Over-current limiting is used to limit short circuit current. Over-voltage protection (in the range of 18V to 40V) causes the device to shut down the output current drive. Thermal shutdown limits power dissipation on the chip. The CA3275 is supplied in a 14 lead dual-in-line plastic package.

Ordering Information

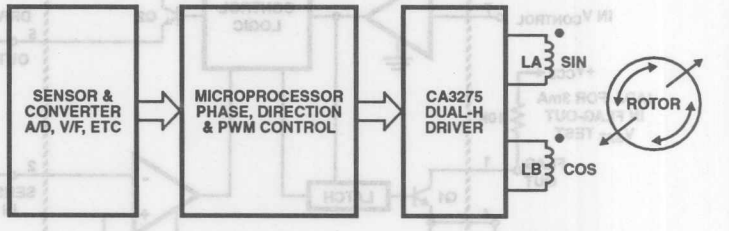
PART	TEMPERATURE	PACKAGE
CA3275E	-40°C to +85°C	14 Lead Plastic DIP

Pinout

14 LEAD DUAL-IN-LINE PLASTIC PACKAGE (E SUFFIX)
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2159.1**

Absolute Information (T_C = +25°C) Unless Otherwise Specified

Operating V_{CC} 16V
Transient V_{CC}, 30 Seconds Maximum 24V
Peak V_{CC}, 0.4 Seconds Maximum 40V
Maximum Continuous Output Current, Each Drive . . . . . ±100mA
Maximum PWM Output Switching Current, Each Drive . . . . . ±150mA
Power Dissipation, P_D
Up to +70°C 750mW
Above +70°C . . . . . Derate Linearly at 11.1mW/°C

Ambient Temperature Range
Operating . . . . . -40°C to +85°C
Storage . . . . . -55°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At distance 1/16 ± 1/32" (1.59 ± 0.79mm) from case for 10s max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At T_A = +25°C, V_{CC} = 16V Unless Otherwise Specified

PARAMETERS	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage Range	V_{CC}	8	-	16	V
Supply Current (Note 1)	I_{CC}	-	8	20	mA
INPUT LEVELS					
Logic Input, Low Voltage	V_{IL}	-	-	0.8	V
Logic Input, High Voltage	V_{IH}	3.5	-	-	V
Logic Input, Low Current, V_{IL} = 0V	I_{IL}	-10	-	-	µA
Logic Input, High Current, V_{IH} = 5V	I_{IH}	-	-	10	µA
OUTPUT: RLA = RLB = 138Ω					
Maximum Source Saturated Voltage	V_{SAT} - High	-	1.2	1.75	V
Maximum Sink Saturated Voltage	V_{SAT} - Low	-	0.25	0.5	V
Differential V_{SAT} Voltage, Both Outputs Saturated	Diff - V_{SAT}	-	10	100	mV

Switching Specifications

PARAMETERS	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
SOURCE CURRENT (See Figure 3)					
Turn-Off Delay	T_{SC-OFF}	-	-	2	µs
Fall Time	T_{SC-F}	-	-	2.2	µs
Turn-On Time	T_{SC-ON}	-	-	1	µs
Rise Time	T_{SC-R}	-	-	0.4	µs
SINK CURRENT (See Figure 4)					
Turn-Off Delay	$T_{SCK-OFF}$	-	-	1.6	µs
Fall Time	T_{SCK-F}	-	-	0.4	µs
Turn-On Time	T_{SCK-ON}	-	-	0.6	µs
Rise Time	T_{SCK-R}	-	-	0.2	µs

NOTE:
1. No load, PWMA = PWMB = 5V, DIR A = DIR B = 0V

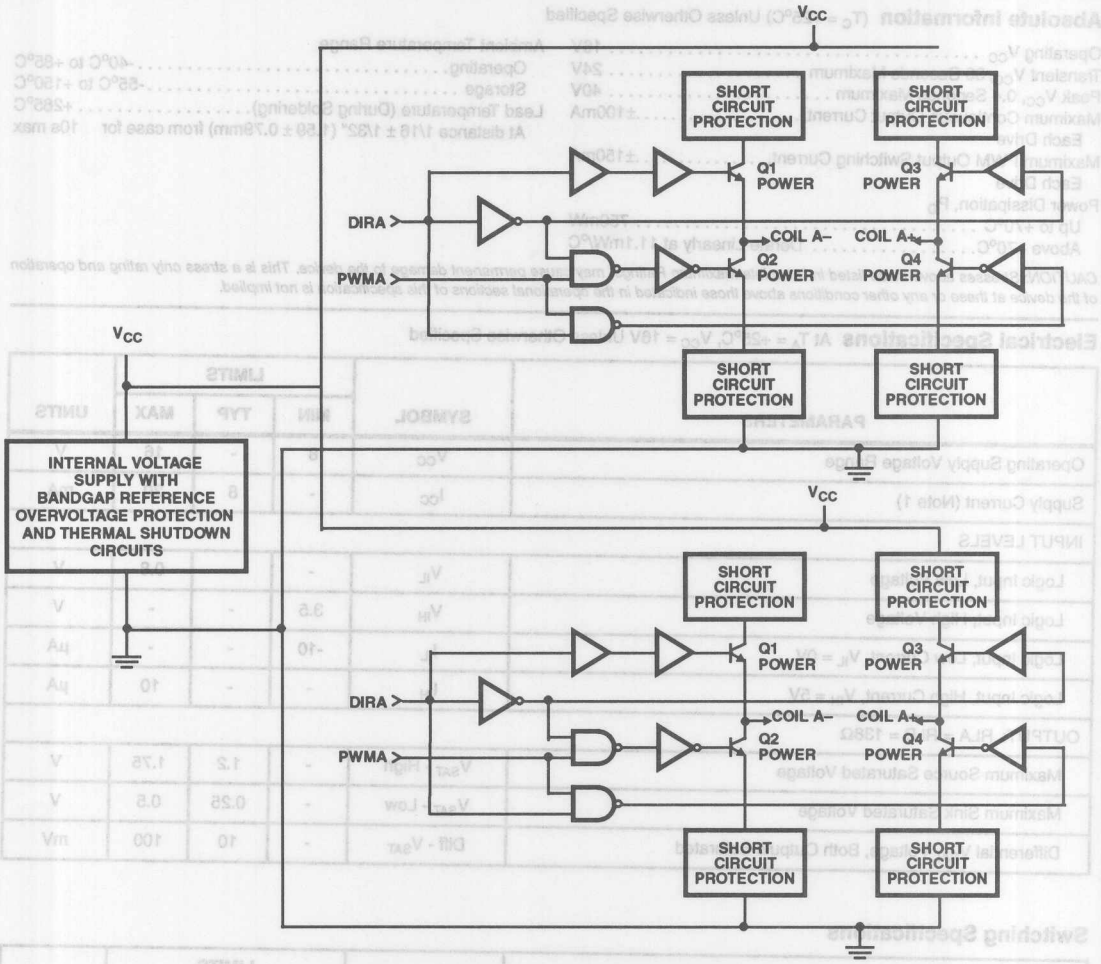


FIGURE 1. CA3275 DUAL-H DRIVER SCHEMATIC

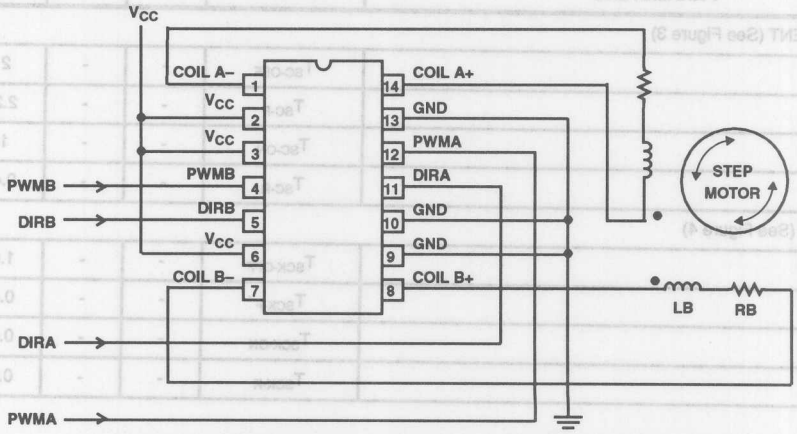


FIGURE 2. QUADRATURE STEP-MOTOR APPLICATION SCHEMATIC

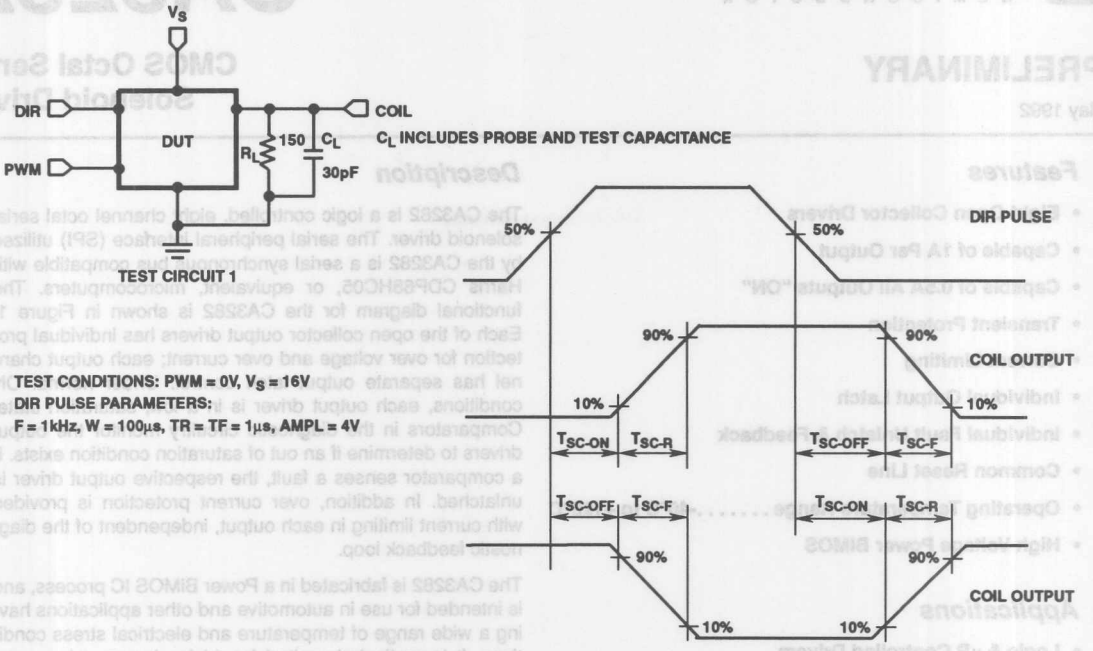


FIGURE 3. SOURCE SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

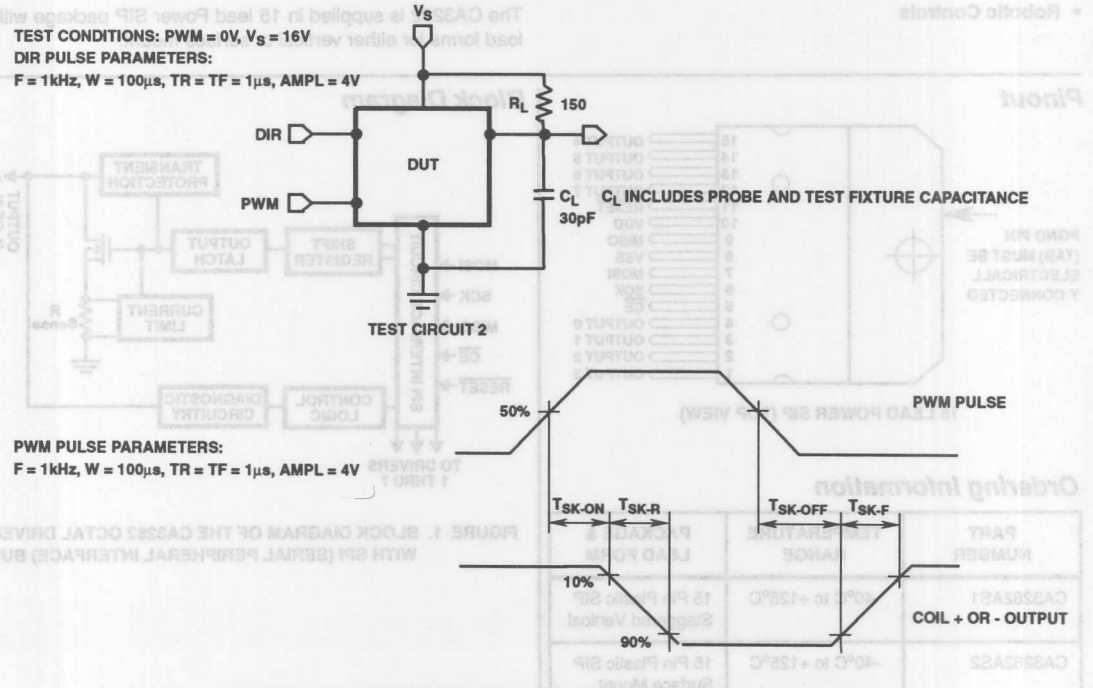


FIGURE 4. SINK SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

CA3282

PRELIMINARY

May 1992

CMOS Octal Serial Solenoid Driver

Features

- Eight Open Collector Drivers
- Capable of 1A Per Output
- Capable of 0.5A All Outputs "ON"
- Transient Protection
- Current Limiting
- Individual Output Latch
- Individual Fault Unlatch & Feedback
- Common Reset Line
- Operating Temperature Range . . . . . -40°C to +125°C
- High Voltage Power BiMOS

Applications

- Logic & µP Controlled Drivers
- Solenoids, Relays & Lamp Drivers
- Automotive & Industrial Systems
- Robotic Controls

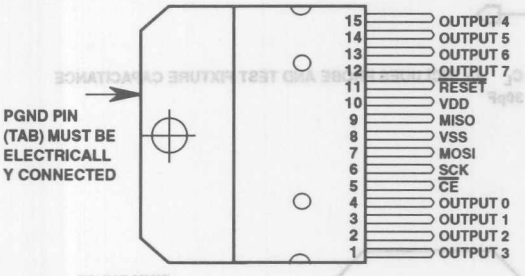
Description

The CA3282 is a logic controlled, eight channel octal serial solenoid driver. The serial peripheral interface (SPI) utilized by the CA3282 is a serial synchronous bus compatible with Harris CDP68HC05, or equivalent, microcomputers. The functional diagram for the CA3282 is shown in Figure 1. Each of the open collector output drivers has individual protection for over voltage and over current; each output channel has separate output latch control. Under normal ON conditions, each output driver is in a low, saturation state. Comparators in the diagnostic circuitry monitor the output drivers to determine if an out of saturation condition exists. If a comparator senses a fault, the respective output driver is unlatched. In addition, over current protection is provided with current limiting in each output, independent of the diagnostic feedback loop.

The CA3282 is fabricated in a Power BiMOS IC process, and is intended for use in automotive and other applications having a wide range of temperature and electrical stress conditions. It is particularly suited for driving lamps, relays, and solenoids in applications where low operating power, high breakdown voltage, and high output current at high temperatures is required.

The CA3282 is supplied in 15 lead Power SIP package with lead forms for either vertical or surface mount.

Pinout



15 LEAD POWER SIP (TOP VIEW)

Block Diagram

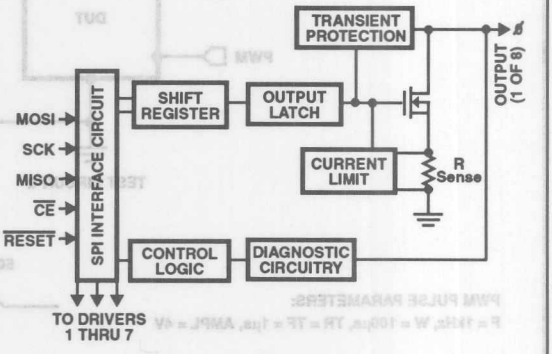


FIGURE 1. BLOCK DIAGRAM OF THE CA3282 OCTAL DRIVER WITH SPI (SERIAL PERIPHERAL INTERFACE) BUS

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE & LEAD FORM
CA3282AS1	-40°C to +125°C	15 Pin Plastic SIP Staggered Vertical
CA3282AS2	-40°C to +125°C	15 Pin Plastic SIP Surface Mount

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2767.2**

Absolute Maximum Ratings

DC Logic Supply, V_{DD} . . . . . -0.7V to +7.0V
Output Voltage, V_O . . . . . -0.7V to 40V
Output Current, I_{LOAD} . . . . . 1A Max
Input Voltage, V_{IN} . . . . . 7V Max
Operating Temperature Range . . . . . -40°C to +150°C
Storage Temperature Range (T_{stg}) . . . . . -55°C to +150°C

Thermal Characteristics

Thermal Resistance Junction-Case, θ_{JC} . . . . . +3°C/W Max
Thermal Resistance Junction-Ambient, θ_{JA} . . . . . +35°C/W Max
Lead Temperature (During Soldering):
At distance $^1/_{16}$ $\pm^1/_{32}$ In. (1.59 ± 0.79mm)
from case for 10s max . . . . . +265°C

Electrical Specifications V_{DD} = -5V ± 5%, T_j = -40°C to +125°C; Unless Otherwise Specified.

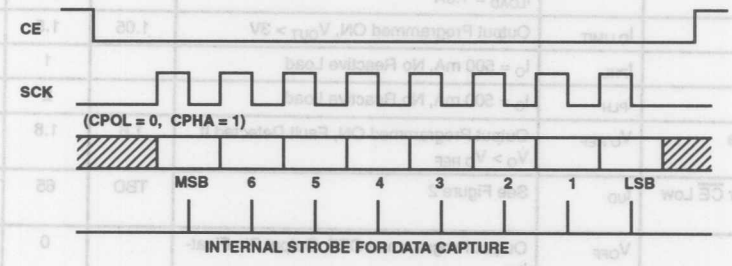
PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Quiescent Supply Current	I_{DD}	All Outputs ON, 0.5A Load Per Output		5	10	mA
Output Clamping Voltage	V_{OC}	I_{LOAD} = 0.5A, Output Programmed OFF	30	32	40	V
Output Clamping Energy	E_{OC}	I_{LOAD} = 0.5A, Output ON	20			mJ
Output Leakage Current	$I_{O\ LEAK}$	Output Programmed OFF				
		V_O = 24V		150	1000	µA
		V_O = 14V		150	500	µA
		V_O = 5V		150	200	µA
Output Saturation Voltage	V_{SAT}	Output Programmed ON				
		I_{LOAD} = 0.5A		0.3	0.5	V
		I_{LOAD} = 0.75A		0.4	1.25	V
		I_{LOAD} = 1.0A		0.6	2.0	V
Output Current Limit	$I_{O\ LIMIT}$	Output Programmed ON, V_{OUT} > 3V	1.05	1.5		A
Turn-On Delay	t_{PHL}	I_O = 500 mA, No Reactive Load		1	10	µs
Turn-Off Delay	t_{PLH}	I_O = 500 mA, No Reactive Load		2	10	µs
Fault Reference Voltage	$V_{O\ REF}$	Output Programmed ON, Fault Detected If $V_O > V_{O\ REF}$	1.6	1.8	2.0	V
Fault Reset Delay (After $\overline{CE}$ Low to High Transition)	t_{UD}	See Figure 2	TBD	65	250	µs
Output OFF Voltage	V_{OFF}	Output Programmed OFF, Output Pin Floating		0	1	V
LOGIC INPUTS (MOSI, $\overline{CE}$, SCK and $\overline{RESET}$)						
Threshold Voltage at Falling Edge	V_{T-}	V_{DD} = 5V ±10%	$0.2V_{DD}$	$0.3V_{DD}$		V
Threshold Voltage at Rising Edge	V_{T+}	V_{DD} = 5V ±10%		$0.6V_{DD}$	$0.7V_{DD}$	V
Hysteresis Voltage	V_H	$V_{T+} - V_{T-}$	0.85	1.4	2.25	V
Input Current	I_I	V_{DD} = 5.5V, 0 < V_I < V_{DD}	-10		+10	µA
Input Capacitance	C_I	0 < V_I < V_{DD}			20	pF
LOGIC OUTPUT (MISO)						
Output LOW Voltage	V_{OL}	I_{OL} = 1.6 mA		0.2	0.4	V
Output HIGH Voltage	V_{OH}	I_{OL} = 0.8 mA	V_{DD} -1.3V	V_{DD} -0.2V		V
Output Tristate Leakage Current	I_{OL}	V_{DD} = 5.25V, 0 < V_O < V_{DD}, $\overline{CE}$ Pin Held High	-10		+10	µA
Output Capacitance	C_{OUT}	0 < V_O < V_{DD}, $\overline{CE}$ Pin Held High			20	pF

Serial Peripheral Interface Timing (See Figure 2)

PARAMETERS	SYMBOL		TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Frequency		f_{OPER}		D.C.	Note 1	1.0	MHz
Cycle Time	(1)	t_{CYC}		1.0	0.1		µs
Enable Lead Time	(2)	t_{LEAD}			<100	1000	ns
Enable Lag Time	(3)	t_{LAG}			<100	1000	ns
Clock HIGH Time	(4)	t_{wSCKH}		410	50		ns
Clock LOW Time	(5)	t_{wSCKL}		410	50		ns
Data Setup Time	(6)	t_{SU}		150	20		ns
Data Hold Time	(7)	t_H		150	20		ns
Enable Time	(8)	t_{EN}			50	1000	ns
Disable Time	(9)	t_{DIS}			150	1000	ns
Data Valid Time	(10)	t_V			75	360	ns
Output Data Hold Time	(11)	t_{HO}		0	50		ns
Rise Time (MISO Output)	(12)	t_{rSO}	V_{DD} = 20% to 70%, C_L = 200pF		35	150	ns
Rise Time SPI Inputs (SCK, MOSI, $\overline{CE}$)	(12)	t_{rSI}	V_{DD} = 20% to 70%, C_L = 200pF			90	ns
Fall Time (MISO Output)	(13)	t_{fSO}	V_{DD} = 20% to 70%, C_L = 200pF		45	150	ns
Fall Time SPI Inputs (SCK, MOSI, $\overline{CE}$)	(13)	t_{fSI}	V_{DD} = 20% to 70%, C_L = 200pF			90	ns

NOTE:

1. Operating Frequency is typically greater than 10MHz but it is application limited primarily by external SPI input rise/fall times and MISO output loading.



DATA AND CLOCK TIMING

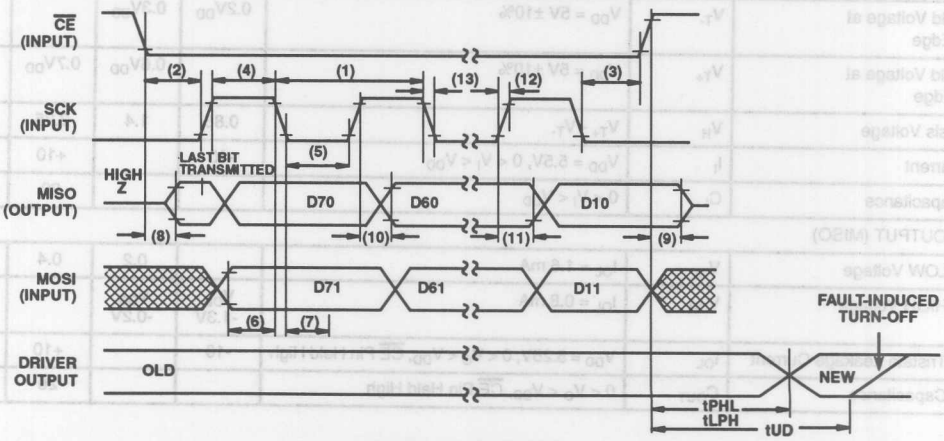


FIGURE 2. SPI TIMING

Signal Descriptions

Output 0 - Output 7 - Power Output Drivers. The input and output bits corresponding to Output 0 thru Output 7 are transmitted and received most significant bit (MSB) first via the SPI bus. The outputs are provided with current limiting and voltage sense functions for fault indication and protection. The nominal load current for these outputs is 500mA, with current limiting set to a minimum of 1.05A. An on chip clamp circuit capable of handling 500mA is provided at each output for clamping inductive loads.

$\overline{\text{RESET}}$ - Active low reset input. When this input line is low, the shift register and output latches are configured to turn off all output drivers. A power on clear function may be implemented by connecting this pin to V_{DD} with an external resistor, and to V_{SS} with an external capacitor. In any case, this pin must not be left floating.

$\overline{\text{CE}}$ - Active low chip enable. Data is transferred from the shift register to the outputs on the rising edge of this signal. The falling edge of $\overline{\text{CE}}$ loads the shift register with the output voltage sense bits coming from the output stages. The output driver for the MISO pin is enabled when this pin is low. $\overline{\text{CE}}$ must be a logic low prior to the first serial clock (SCK) and must remain low until after the last (eighth) serial clock cycle. A low level on $\overline{\text{CE}}$ also activates an internal disable circuit used for unlatching output states that are in a fault mode as sensed by an out of saturation condition. A high on $\overline{\text{CE}}$ forces MISO to a high impedance state. Also, when $\overline{\text{CE}}$ is high, the octal driver ignores the SCK and MOSI signals.

SCK, MISO, MOSI - See Serial Peripheral Interface (SPI) section in this data sheet.

V_{DD} and V_{SS} - Positive and negative power supply lines.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) utilized by the CA3282 is a serial synchronous bus for control and data transfers. The clock (SCK), which is generated by the microcomputer, is active only during data transfers. In systems using CDP68HC05 family microcomputers, the inactive clock polarity is determined by the CPOL bit in the microcomputer's control register. The CPOL bit is used in conjunction with the clock phase bit, CPHA to produce the desired clock data relationship between the microcomputer and octal driver. The CPHA bit in general selects the clock edge which captures data and allows it to change states. For the CA3282, the CPOL bit must be set to a logic zero and the CPHA bit to a logic one. Configured in this manner, MISO (output) data will appear with every rising edge of SCK, and MOSI (input) data will be latched into the shift register with every falling edge of SCK. Also, the steady state value of the inactive serial clock, SCK, will be at a low level. Timing diagrams for the serial peripheral interface are shown in Figure 2.

SPI Signal Descriptions

MOSI (Master Out/Slave In) - Serial data input. Data bytes are shifted in at this pin, most significant bit (MSB) first. The data is passed directly to the shift register which in turn controls the latches and output drivers. A logic "0" on this pin will program the corresponding output to be ON, and a logic "1" will turn it OFF.

MISO (Master In/ Slave Out) - Serial data output. Data bytes are shifted out at this pin, most significant bit (MSB) first. This pin is the serial output from the shift register and is tri stated when CE is high. A high for a data bit on this pin indicates that the corresponding output is high. A low on this pin for a data bit indicates that the output is low. Comparing the serial output bits with the previous input bits, the microcomputer implements the diagnostic data supplied by the CA3282.

SCK - Serial clock input. This signal clocks the shift register. New MISO (output) data will appear on every rising edge of SCK and new MOSI (input) data will be latched into the shift register on every falling edge of SCK. The SCK phase bit, CPHA, and polarity bit, CPOL, must be set to 1 and 0, respectively in the microcomputer's control register.

Functional Description

The CA3282 is a low operating power, high voltage, high current, octal, serial solenoid driver featuring eight channels of open collector drivers. The drivers have low saturation voltage and output short circuit protection, suitable for driving resistive or inductive loads such as lamps, relays and solenoids. Data is transmitted to the device serially using the Serial Peripheral Interface (SPI) protocol. Each channel is independently controlled by an output latch and a common $\overline{\text{RESET}}$ line that disables all eight outputs. Byte timing with asynchronous reset is shown in Figure 3. The circuit receives 8 bit serial data by means of the serial input (MOSI), and stores this data in an internal register to control the output drivers. The serial output (MISO) provides 8 bit diagnostic data representing the voltage level at the driver output. This allows the microcomputer to diagnose the condition at the output drivers. The device is selected when the chip enable ($\overline{\text{CE}}$) line is low. When $\overline{\text{CE}}$ is high, the device is deselected and the serial output (MISO) is placed in a tri state mode. The device shifts serial data on the rising edge of the serial clock (SCK), and latches data on the falling edge. On the rising edge of chip enable ($\overline{\text{CE}}$), new input data from the shift register is latched in the output drivers. The falling edge of chip enable ($\overline{\text{CE}}$) transfers the output driver fault information back to the shift register. The output drivers have low ON voltage at rated current, and are monitored by a comparator for an out of saturation condition, in which case the output driver with the fault becomes unlatched and diagnostic data is sent to the microcomputer via the MISO line. A typical microcomputer interface circuit is shown in Figure 4. This circuit is also cascadable with another octal driver.

Shift Register

The shift register has both serial and parallel inputs and outputs. Serial output and input data are simultaneously transferred to and from the SPI bus. The parallel outputs are latched into the output latch in the CA3282 at the end of a data transfer. The parallel inputs jam diagnostic data into the shift register at the beginning of a data transfer cycle.

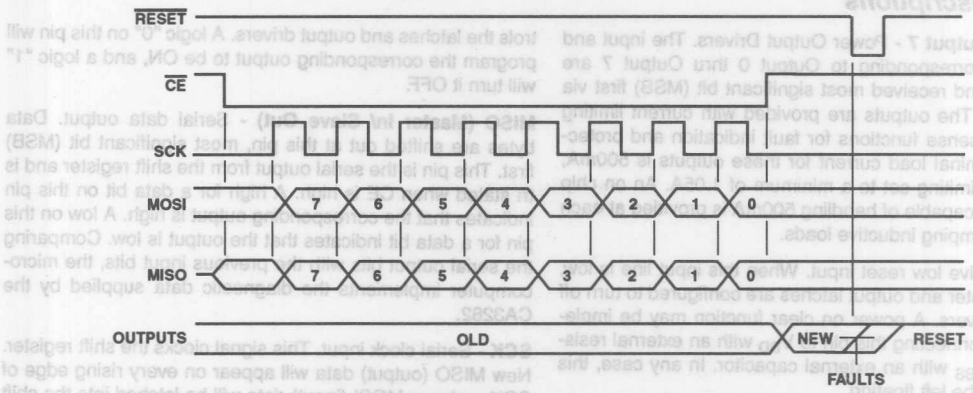


FIGURE 3. BYTE TIMING WITH ASYNCHRONOUS RESET

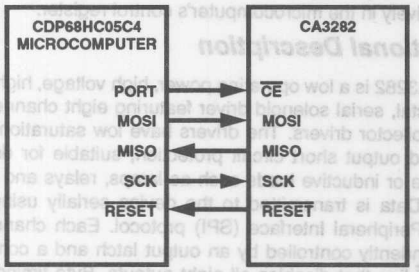


FIGURE 4. TYPICAL MICROCOMPUTER INTERFACE WITH THE CA3282

Output Latch

The output latch holds input data from the shift register which is used to activate the outputs. The latch circuit may be cleared by a fault condition (to protect the overloaded outputs), or by the $\overline{\text{RESET}}$ signal.

Output Drivers

The output drivers provide an active low output of 500mA nominal with current limiting set to 1.05A to allow for high inrush currents. In addition, each output is provided with a voltage clamp circuit to limit inductive transients. Each output driver is also monitored by a comparator for an out of saturation condition. If the output voltage of an ON output pin exceeds the saturation voltage limit, a fault condition is assumed and the latch driving this output is reset, turning the output off. The output comparators, which also provide diagnostic feedback data to the shift register, contain an internal pulldown current which will cause the cell to indicate a low output voltage if the output is programmed OFF and the output pin is open circuited.

$\overline{\text{CE}}$ High to Low Transition

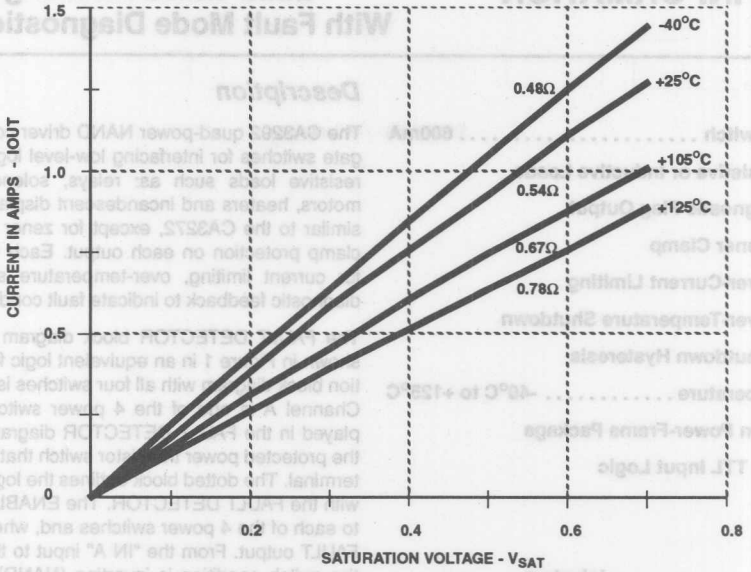
When $\overline{\text{CE}}$ is low, the tri-state MISO pin is enabled. On the falling edge of $\overline{\text{CE}}$, diagnostic data from the output voltage comparators will be latched into the shift register. If an output is high, a logic one will be loaded into that bit in the shift register. If the output is low, a logic zero will be loaded. During the time that $\overline{\text{CE}}$ is low, data bytes controlling the output drivers are shifted in at the MOSI pin most significant bit (MSB) first. A logic zero on this pin will program the corresponding output to be ON, and a logic one will turn it OFF

$\overline{\text{CE}}$ Low to High Transition

When the last data bit has been shifted into the CA3282, the $\overline{\text{CE}}$ pin should be pulled high. At the rising edge of $\overline{\text{CE}}$, shift register data is latched into the output latch and the outputs are activated with the new data. An internal 150msec delay timer will start at this rising edge to compensate for high inrush currents in lamps and inductive loads. During this period, the outputs will be protected only by the analog current limiting circuits since resetting of the output latches by fault conditions will be inhibited during this time. This allows the device to handle inrush currents immediately after turn on. When the 150msec delay has elapsed, the out-put voltages are sensed by the comparators and any out of saturation outputs are latched off. The serial clock input pin (SCK) should be low during $\overline{\text{CE}}$ transitions to avoid false clocking of the shift register. The SCK input is gated by $\overline{\text{CE}}$ so that the SCK input is ignored when $\overline{\text{CE}}$ is high.

Detecting Fault Conditions

Fault conditions may be checked as follows. Clock in a new control byte and wait approximately 150msec to allow the outputs to settle. Clock in the same control byte and note the diagnostic data output at the MISO pin. The diagnostic bits should be identical to the data clocked in. Any differences will indicate a fault at the corresponding outputs. For example, if an output was programmed ON by clocking in a zero, and the corresponding diagnostic bit for that output is a one, indicating the driver output is still high, then a short circuit or overload condition may have caused the output to unlatch. Alternatively, if the output was programmed OFF by clocking in one, and the diagnostic bit for that output shows a zero, then the probable cause is an open circuit resulting in a floating output.



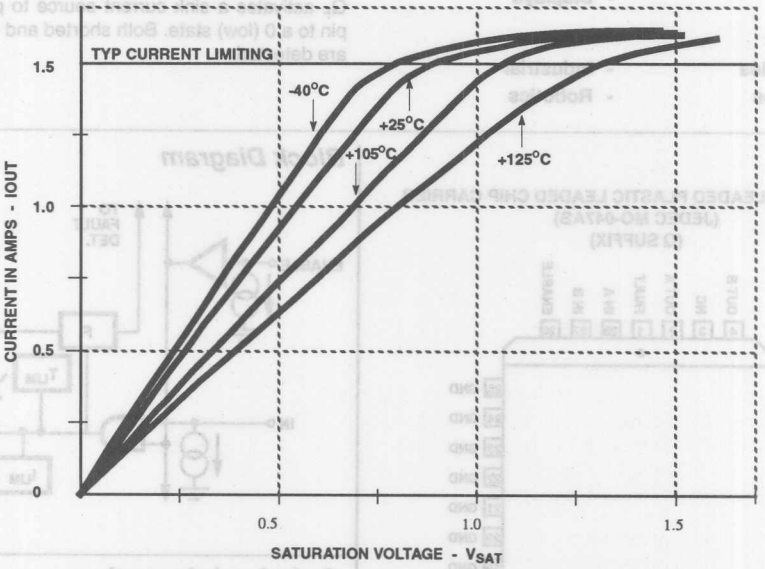


FIGURE 5. CA3282 TYPICAL OUTPUT DRIVER vs V_{SAT}

HARRIS SEMICONDUCTOR

CA3292

ADVANCED INFORMATION

May 1992

Quad-Gated Inverting Power Driver With Fault Mode Diagnostic Flag Output

Features

- Load Current Switch 600mA
- Suitable for Resistive or Inductive Loads
- Fault Mode Diagnostic Flag Output
- Over-Voltage Zener Clamp
- Independent Over-Current Limiting
- Independent Over-Temperature Shutdown
- Temperature Shutdown Hysteresis
- Operating Temperature ..... -40°C to +125°C
- High Dissipation Power-Frame Package
- 5 Volt CMOS or TTL Input Logic

Applications

- Drivers For:
  - Solenoids
  - Relays
  - Power Output
  - Lamps
  - Injectors
  - Steppers
  - Motors
  - Displays
- System Use:
  - Automobiles
  - Appliances
  - Industrial
  - Robotics

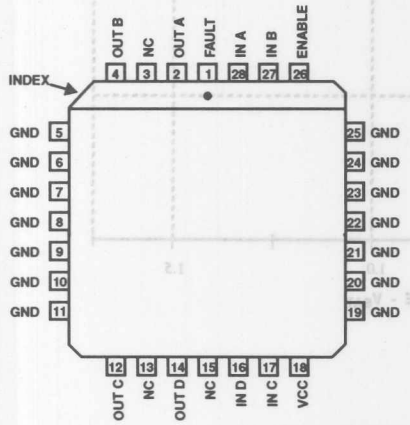
Description

The CA3292 quad-power NAND driver contains four NAND-gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters and incandescent displays. The CA3292 is similar to the CA3272, except for zener diode over-voltage clamp protection on each output. Each output is protected for current limiting, over-temperature shutdown and has diagnostic feedback to indicate fault conditions.

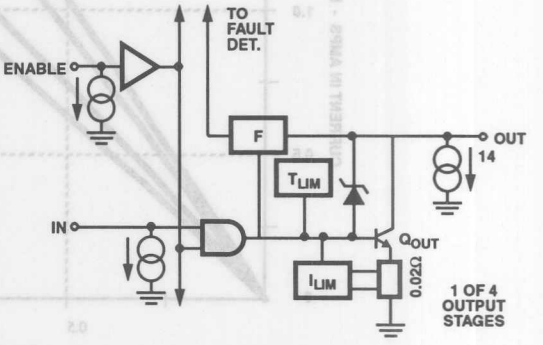
The FAULT DETECTOR block diagram of the CA3292 is shown in Figure 1 in an equivalent logic form while the function block diagram with all four switches is shown in Figure 2. Channel A is one of the 4 power switching functions displayed in the FAULT DETECTOR diagram. Transistor Q_A is the protected power transistor switch that drives the "OUT A" terminal. The dotted block outlines the logic block associated with the FAULT DETECTOR. The ENABLE input is common to each of the 4 power switches and, when low, disables the FAULT output. From the "IN A" input to the "OUT A" output, the switch condition is inverting (NAND). When IN is high, OUT is low and the switch is conducting. The FAULT DETECTOR senses the IN and OUT states and switches Q_F "ON" if a fault is detected. When a fault is detected, transistor Q_F activates a sink current source to pull-down the FAULT pin to a 0 (low) state. Both shorted and open load conditions are detected.

Pinout

PLASTIC 28-LEADED PLASTIC LEADED CHIP CARRIER
(JEDEC MO-047AB)
(Q SUFFIX)



Block Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3292Q	-40°C +125°C	28 Lead PLCC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2946**

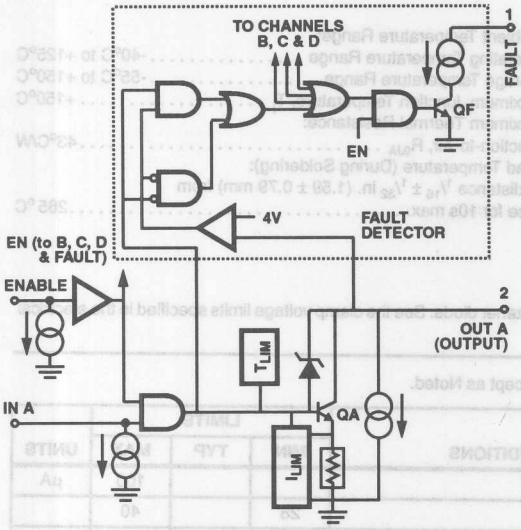
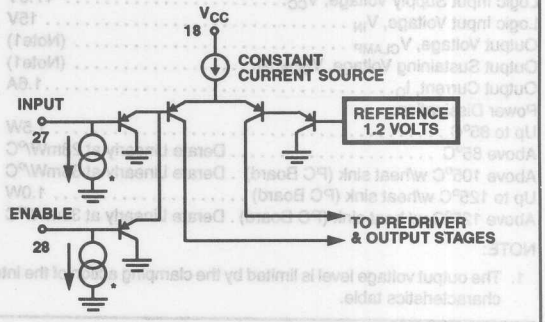


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF THE CA3292 FAULT DETECTOR



*INPUT AND ENABLE PULLDOWN SOURCES FORCE OUTPUT TURN-OFF FOR ALL UNDETERMINATED INPUTS

FIGURE 3. SCHEMATIC OF ONE INPUT STAGE

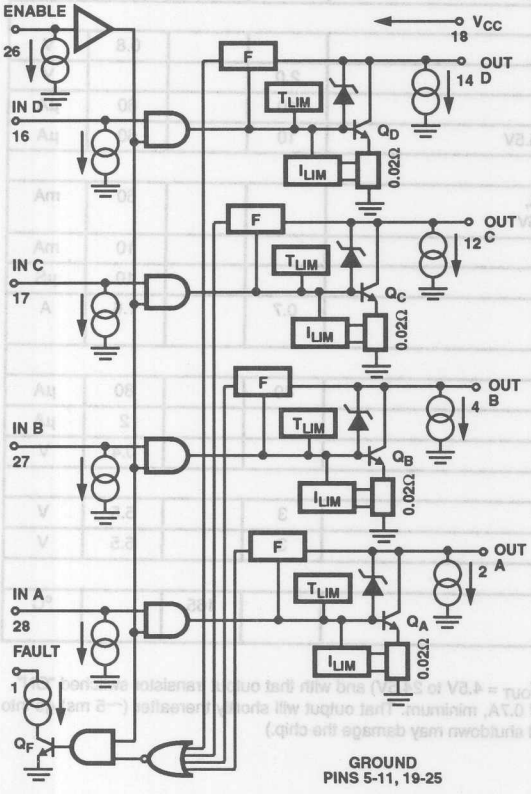


FIGURE 2. CA3292 FUNCTIONAL BLOCK DIAGRAM SHOWING ALL OUTPUTS

TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	DON'T CARE	H

FAULT LOGIC TABLE

IN	OUT	FAULT	MODE
H	L	H	NORMAL
H L	H L	L L	Over current or over temperature or output short to power supple
L	H	H	Normal

Absolute Maximum Ratings

Logic Input Supply Voltage, V_{CC} ..... +7.0V
Logic Input Voltage, V_{IN} 15V
Output Voltage, V_{CLAMP} ..... (Note1)
Output Sustaining Voltage, $V_{CE(SUS)}$ ..... (Note1)
Output Current, I_O 1.6A
Power Dissipation:
Up to 85°C 1.5W
Above 85°C ..... Derate Linearly at 23mW/°C
Above 105°C w/heat sink (PC Board) . Derate Linearly at 33mW/°C
Up to 125°C w/heat sink (PC Board) 1.0W
Above 125°C w/ heat sink (PC Board) . Derate Linearly at 33mW/°C

Ambient Temperature Range:
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Maximum Junction Temperature, T_j ..... +150°C
Maximum Thermal Resistance:
Junction-to-Air, $R_{\theta JA}$ ..... 43°C/W
Lead Temperature (During Soldering):
At distance $^1/_{16} \pm {}^1/_{32}$ in. (1.59 ± 0.79 mm) from case for 10s max. ..... 265 °C

NOTE:

1. The output voltage level is limited by the clamping action of the internal zener diode. See the clamp voltage limits specified in the electrical characteristics table.

Electrical Specifications

At T_A = -40°C to +125°C, V_{CC} = 5.5V Except as Noted.

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Leakage Current	I_{CEX}	V_{CE} 24V, V_{ENABLE} = 0.8V			100	µA
Output Clamp Voltage	V_{CLAMP}	I_{CE} = 300µA	28		40	
COLLECTOR EMITTER SATURATION VOLTAGE:	$V_{CE(SAT)}$	I_C = 400mA, V_{IN} 2V, V_{CC} = 4.75V, T_A = +125°C			0.4	V
		I_C = 500mA, V_{IN} 2V, V_{CC} = 4.75V, T_A = +25°C			0.5	V
		I_C = 600mA, V_{IN} 2V, V_{CC} = 4.75V, T_A = -40°C			0.6	V
LOGIC INPUT THRESHOLDS:						
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	V_{IN} = 0.8V	10		60	µA
Input High Current	I_{IH}	V_{IN} = 5.5V, V_{ENABLE} = 5.5V	10		60	µA
SUPPLY CURRENT:						
All Outputs ON	$I_{CC(ON)}$	I_{OUT}(A,B,C,D) = 250mA, V_{IN} = 2V, V_{ENABLE} = 5.5V			60	mA
All Outputs OFF	$I_{CC(OFF)}$				10	mA
Turn-On Delay	t_{PHL}, t_{PLH}				10	µS
Over-Current Limiting for each Output (Note 1)		V_{OUT} = 4.5V to 24.5V, R_L = (Min.) = 4Ω	0.7		1.6	A
FAULT OUTPUT, I_{LOAD} = 30µA:						
Output Low Current	I_{OL}		40		80	µA
Output High Current	I_{OH}				2	µA
Output Low Voltage	V_{OL}	I_{OL} = 30µA			0.4	V
Output Sense Thresholds:						
Output High Threshold	V_{HT}	V_{IN} = 2.0V (Min.)	3		5.5	V
Output Low Threshold	V_{LT}	V_{IN} = 0.8V (Max.)	3		5.5	V
OVER-TEMPERATURE SHUTDOWN (DESIGN PARAMETER):						
Typical Junction Temperature at Thermal Shutdown				165		°C

NOTE:

1. With voltage on the collector of the output transistor as indicated (V_{OUT} = 4.5V to 24.5V) and with that output transistor switched "ON", the current will increase to a limiting value which will be a value of 0.7A, minimum. That output will shortly thereafter (~5 ms) go into Over-Temperature shutdown. (Excessive dissipation during thermal shutdown may damage the chip.)

HARRIS SEMICONDUCTOR

HIP0080
HIP0081

ADVANCE INFORMATION

May 1992

Quad Inverting Power Driver With Diagnostic Interface

Features

- Low Side Power MOSFET Output Drivers
- Output Driver Protection:
  - Over-Current Shutdown
  - Over-Temperature Shutdown
  - Over-Voltage Internal Clamp
- Load Currents Switching Capability with All Outputs ON:
  - HIP0081 . . . . . 1 Amp Each
  - HIP0080 . . . . . 0.5 Amp Each
- Regulated 5V Logic Interface
- 5 Volt CMOS Inputs logic
- Fault Mode Output for Shorts, Opens & Over-Temperature
- 16 Bit Serial Diagnostic Register
- SPI Bus Compatible Data Readout
- 3°C/W - 15 Lead Power SIP Package
- -40°C to +125°C Operating Temperature

Applications

- Drivers For:
  - Solenoids
  - Relays
  - Power Output
  - Lamps
  - Injectors
  - Steppers
  - Motors
  - Displays
- System Use:
  - Automotive
  - Appliances
  - Industrial
  - Robotics

Description

The HIP0080/0081 Quad Power Drivers contain four individually protected NDMOS power output transistor switches to drive inductive and resistive loads such as: relays, solenoids, injection drivers, AC and DC motors, heaters and incandescent displays. The 4 Power Drivers are low-side switches driven by CMOS logic input control stages. The output drivers are protected against over-current, over-temperature and over-voltage. An internal drain-to-gate zener diode provides the clamping protection for over-voltage. Diagnostic circuits provide ground short, supply short, open load and thermal overload detection for each of the 4 output stages. Each of the 4 input drivers and their respective diagnostic filters are controlled by one ENABLE input.

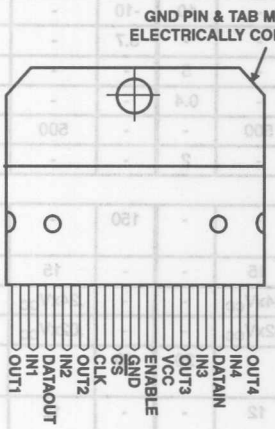
The inputs are CMOS logic compatible and individually control the output drivers with an active high state for turn-on. All other control inputs are active high with the exception of the Chip Select ($\overline{CS}$) which is active low. The DATAIN and DATAOUT are positive logic and the Clock (CLK) input for the Serial Interface is active on the rising edge of the CLK pulse. All inputs include a nominal level of hysteresis. IN1, IN2, IN3, IN4 and ENABLE have pull-down resistors of approximately 100kΩ. This switches off any channel that has an unterminated input.

Ordering Information

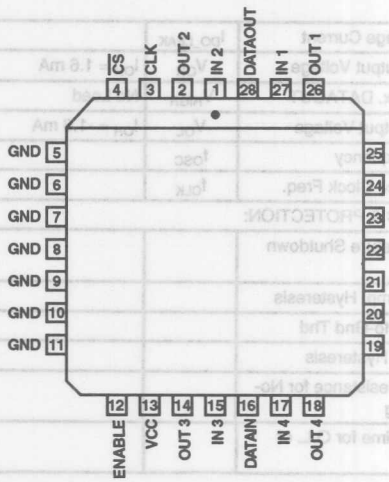
PART NUMBER	TEMPERATURE RANGE	PACKAGE & LEAD FORM
HIP0081AS1	-40°C to +125°C	15 Pin Plastic SIP Staggered Vert.
HIP0081AS2	-40°C to +125°C	15 Pin Plastic SIP Surface Mount
HIP0080AM	-40°C to +125°C	28 Pin PLCC

Pinouts

15 LEAD PLASTIC SIP
TOP VIEW



28 LEAD PLCC
TOP VIEW



11 POWER DRIVERS AND SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3018

Absolute Maximum Ratings

Supply Voltage, V_{CC} ..... -16V to 45V
Output Voltage V_O ..... -0.5 to V_{CLAMP}
Input Voltage, V_{IN} ..... -0.5V to 7V
Output Current, I_{OUT} ..... -2A to +3A
Operating Temperature Range ..... -40°C to +125°C
Operating Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range, T_{STG} ..... -55°C to +150°C

Thermal Resistance	θ_{ja}	θ_{jc}
HIP0080, HIP0081	35°C/W	3°C/W

Lead Temperature (During Soldering)
At distance $^1/_{16} \pm {}^1/_{32}$" (1.59 ± 0.79mm) from case for 10s max ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{CC} = 5.5 to 25V ± 5%, T_A = -40°C to +125°C; Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			HIP0080			HIP0081			
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER OUTPUTS:									
Output ON Resistance	R_{ON}	V_{CC} 10 to 25V, I_{OUT} = 1A V_{CC} 5.5 to 10V, I_{OUT} = 0.7A	-	-	1.0 2.0	-	-	0.5 1.0	Ω Ω
Output Over-Voltage Clamp Range	V_{CLAMP}	Output Programmed OFF	27	-	43	73	-	85	V
Output Short Prot. Current Range	I_{SC}		1.5	-	2.1	3	-	4.1	A
Output Short Circuit Det. Delay	t_{SCDLY}		-	6	-	-	6	-	µs
Output ON-OFF Voltage Ramp Rate		(Resistive load)	-	10	-	-	10	-	V/µs
Turn-On Delay	t_{PHL}	V_{CC} = 14V, R_{LOAD} =14Ω	-	-	8	-	-	8	µs
Turn-Off Delay	t_{PLH}	V_{CC} = 14V, R_{LOAD} =14Ω	-	-	8	-	-	8	µs
SUPPLY:									
Power Supply Current	I_{CC}		-	20	-	-	20	-	mA
Power Supply Reset Active	V_{CC_RST}		3	-	4	3	-	4	V
Shut-Down Current Mode	I_{SHTDN}	Enable LOW	-	20	-	-	N/A	-	µA
INPUTS:									
Low-Level Input Voltage	V_{IL}		-	-	1	-	-	1	V
High-Level Input Voltage	V_{IH}		3.5	-	-	3.5	-	-	V
Input Hysteresis Threshold	V_{IN_HYS}		0.85	-	2.25	0.85	-	2.25	V
Input Pull-Down Resistance	R_{pd}		-	100k	-	-	100k	-	Ω
DATAOUT:									
Tristate Leakage Current	I_{DO_LEAK}		-10	-	10	-10	-	10	µA
Logic High Output Voltage	V_{OH}	I_{OH} = 1.6 mA	3.7	-	-	3.7	-	-	V
Unloaded Max. DATAOUT	V_{HIGH}	No Load	-	-	5	-	-	5	V
Logic Low Output Voltage	V_{OL}	I_{OH} = -1.6 mA	-	-	0.4	-	-	0.4	V
Oscillator Frequency	f_{OSC}		-	500	-	-	500	-	kHz
Serial Interface Clock Freq.	f_{CLK}		-	-	2	-	-	2	MHz
DIAGNOSTIC & PROTECTION:									
Over-Temperature Shutdown Threshold			150	-	-	150	-	-	°C
Shutdown Temp. Hysteresis			-	15	-	-	15	-	°C
Output Short-to-Gnd Thd			-	.24xV_{CC}	-	-	.24xV_{CC}	-	V
Short-to-Gnd Hysteresis			-	.02xV_{CC}	-	-	.02xV_{CC}	-	V
Open-Load Resistance for No-Load Warning			10	-	20	10	-	20	kΩ
Filter Delay Time for O.L. or Short-to-Gnd			-	12	-	-	12	-	µs

Overview

As shown in the Functional Block Diagram, each output stage has voltage and temperature sensors with comparators and delay filters. Four bits of diagnostic information is provided as feedback from each of the four stages. The diagnostic data for all outputs is converted to a serial sequence of 16 bits which is output to a diagnostic register. The data may be read when the Chip Select, $\overline{CS}$ is low and the Clock, CLK transitions positive. With $\overline{CS}$ low, the CLK clock input synchronously shifts the register data while new data is shifted in from the DATAIN input. After 16 clocks, the DATAIN information is shifted to the DATAOUT output. The diagnostic register is cleared after the falling edge of $\overline{CS}$ to allow new diagnostic data to be stored while the existing serial data is read. Figure 2 shows a complete functional signal flow diagram. In each switching channel, the diagnostic sense circuits set 1 bit in the diagnostic register for each of the 4 diagnostics fault conditions as follows:

Bit 1 - indicates a thermal overload when the sensed junction temperature of the output is greater than 150°C. When over-temperature is sensed, the sensor output directly gates-off the drive to the power output and the respective fault bit is set in the diagnostic register. When the chip is sufficiently cooled, the output is gated-on if the input remains ON.

Bit 2 - indicates the fault condition for an output-to-supply short (shorted load). A small value of resistance (~0.01Ω) in the source-to-ground line of the output stage is used to sense the output short. A comparator senses the voltage level and filters the output to provide an input to the control stage and to the diagnostic register. The control state directly shuts down the output when an over-current condition is sensed. Under this condition of fault, the input driver is latched off. To restore the output drive, the short must be removed and the input toggled OFF and then ON.

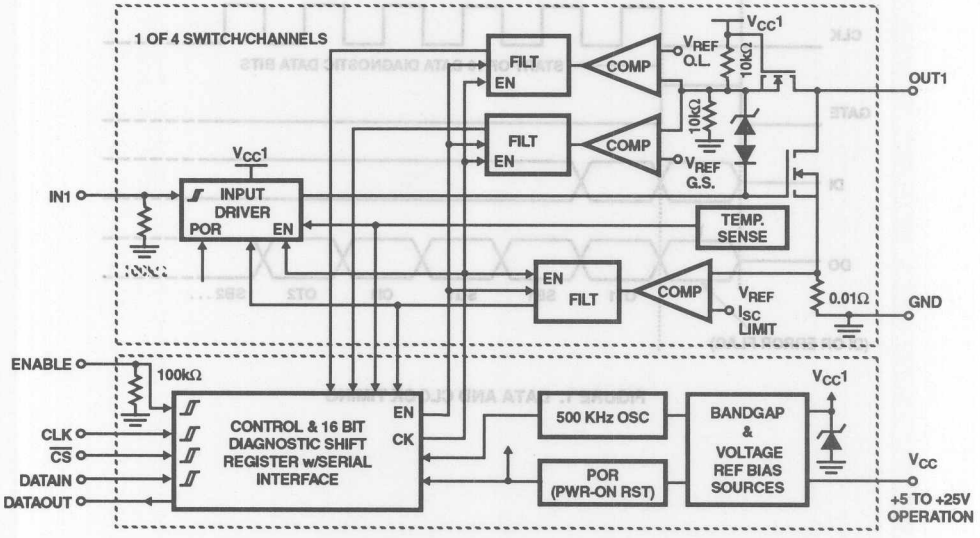
Bit 3 - indicates the condition of an output to ground short. Each output stage has drain-to-supply ($V_{CC}1$) and drain-to-ground pull-up and pull-down resistors of approximately 10kΩ to sense this condition. When the output is off and the sense level is low, an output-to-ground short is detected by the comparator.

Bit 4 - indicates the condition of an open load on the output. The same divider noted above is used to set the output level. If the sense level is at or near the mid-range of the voltage supply, $V_{CC}1$ when the output is in the off condition, a no-load condition is detected.

For normal operating conditions, a Reset turns off all outputs when the V_{CC} level drops below 3.5 volts. The internal bandgap and bias supply function includes a 5V regulated supply for the low voltage signal and logic circuits.

Filters are used on the outputs of the fault sensing comparators to avoid the detection of short duration transient spikes. The on chip oscillator is used to clock an internal shift register in each filter. If the fault condition is longer than a preset number of clock cycles, the fault condition is recognized and the respective bit is set in the diagnostic register. No filter is used in the thermal-overload feedback circuit and the bit is set when thermal shutdown occurs.

Functional Block Diagram



Switching Channel 1:

1	Over-temperature	OT1
2	Short to Supply	SB1
3	Short to Ground	SG1
4	Open Load	OI1

Switching Channel 2:

5	Over-temperature	OT2
6	Short to Supply	SB2
7	Short to Ground	SG2
8	Open Load	OI2

Switching Channel 3:

9	Over-temperature	OT3
10	Short to Supply	SB3
11	Short to Ground	SG3
12	Open Load	OI3
14	Short to Supply	SB4
15	Short to Ground	SG4
16	Open Load	OI4

Referring to figure 1, the error bits are jammed from DI (DATAIN) to DO (DATAOUT) when enabled by $\overline{CS}$ going low (active). The GATE is an internal control signal that goes high when $\overline{CS}$ goes low. The CLK signal starts when activated to read the first diagnostic data bit (OT1). The first DO bit following the $\overline{CS}$ low and GATE high is a fault error flag which goes high if any one of the 16 fault bits have been set HIGH. This Fault Flag data bit precedes the 16 fault bits and is ORed with the fault bits. In cascaded operation (See Fig 3), the DI input for the first of the selected chips should be tied to ground. When cascaded, the error flags are also cascaded. A fault condition is immediately evident without reading all bits. However, all bits must be read to determine on which chip the diagnostic bit has been set.

The diagnostic interfaces to the HIP0080 and HIP0081 are SPI compatible. The microcontroller is programmed to control the read and respond action based on the diagnostic readout. The Error Flag bit requires a separate input back to the microcontroller. When the CLK signal starts, the serial sequence starting with the first diagnostic bit (OT1) is input to the microcontroller.

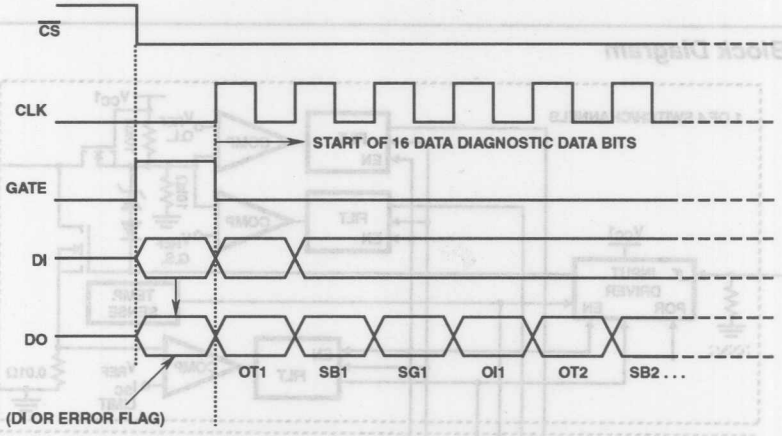


FIGURE 1. DATA AND CLOCK TIMING

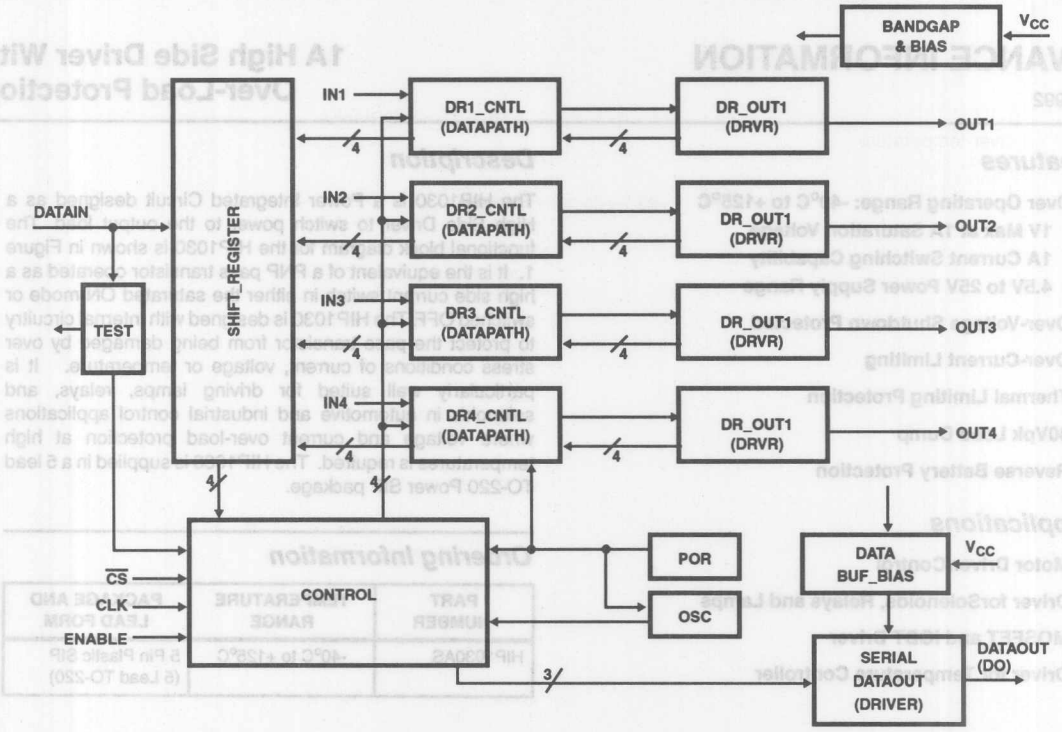


FIGURE 2. FUNCTIONAL SIGNAL FLOW DIAGRAM

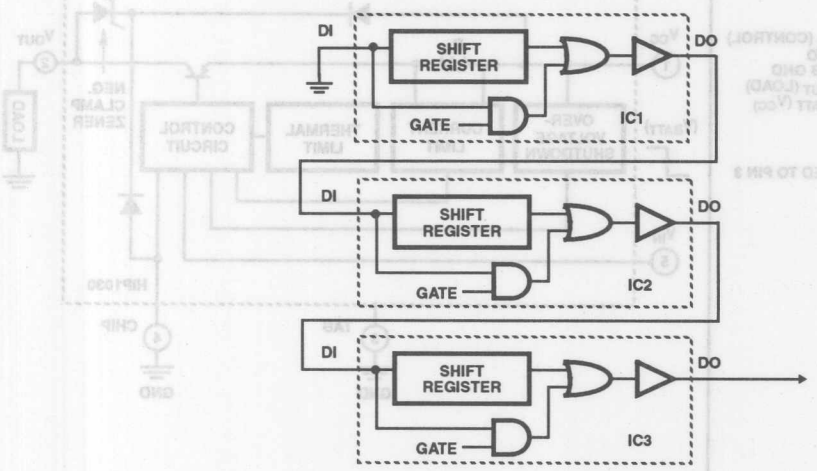


FIGURE 3. CASCADED CHIP OPERATION TO READ DIAGNOSTIC DATA

HARRIS SEMICONDUCTOR

HIP1030

ADVANCE INFORMATION

May 1992

1A High Side Driver With Over-Load Protection

Features

- Over Operating Range: -40°C to +125°C
  - 1V Max at 1A Saturation Voltage
  - 1A Current Switching Capability
  - 4.5V to 25V Power Supply Range
- Over-Voltage Shutdown Protected
- Over-Current Limiting
- Thermal Limiting Protection
- 80Vpk Load Dump
- Reverse Battery Protection

Applications

- Motor Driver/Control
- Driver forSolenoids, Relays and Lamps
- MOSFET and IGBT Driver
- Driver for Temperature Controller

Description

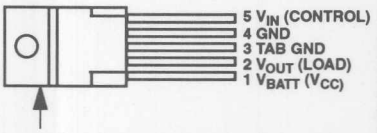
The HIP1030 is a Power Integrated Circuit designed as a High Side Driver to switch power to the output load. The functional block diagram for the HIP1030 is shown in Figure 1. It is the equivalent of a PNP pass transistor operated as a high side current switch in either the saturated ON mode or switched OFF. The HIP1030 is designed with internal circuitry to protect the pass transistor from being damaged by over stress conditions of current, voltage or temperature. It is particularly well suited for driving lamps, relays, and solenoids in automotive and industrial control applications where voltage and current over-load protection at high temperatures is required. The HIP1030 is supplied in a 5 lead TO-220 Power SIP package.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE AND LEAD FORM
HIP1030AS	-40°C to +125°C	5 Pin Plastic SIP (5 Lead TO-220)

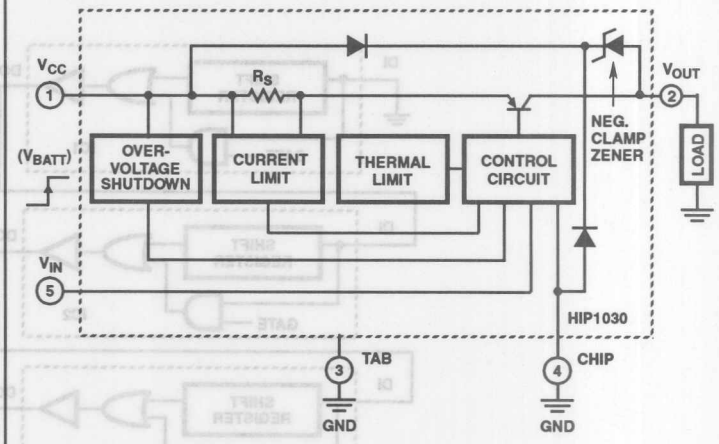
Pinout

TO-220 5 LEAD
TOP VIEW



TAB (GND) INTERNALLY CONNECTED TO PIN 3

Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2788.3**

Absolute Maximum Ratings

Continuous Supply Voltage 25V
Input Voltage, V_{IN} ..... -1V to +7V
Load Current, I_{OUT} ..... Internally Limiting 1.4A
Load Dump (Survival) ..... ±80Vpk

Thermal Resistance (θ_{jc}) ..... 4°C/W
Junction Temperature ..... 150°C
Ambient Operating Temperature ..... -40°C to +125°C
Storage Temperature ..... -40°C to +150°C
Lead Temperature (Soldering 10s max) ..... 265°C

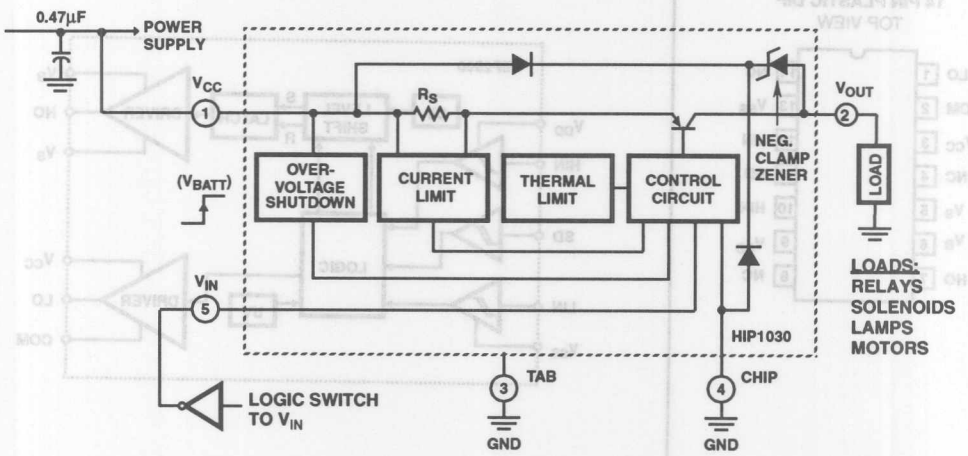
NOTE: $Pd = (V_{CC} - V_{OUT})(I_{OUT}) + (V_{CC})(I_{GND})$
$T_j = T_A + (Pd)(\text{Thermal Resistance})$

Electrical Specifications

T_A = -40°C to +125°C, V_{IN} = 2V; I_{OUT} = 0.5A, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Voltage Range	V_{CC}		4.5	-	24	V
Over-Voltage Shutdown	V_{OVSD}		26	-	36	V
Over-Temperature Limiting	T_{LIMIT}		-	150	-	°C
Negative Pulse Output Clamp Voltage	V_{CLAMP}		V_{CC}	-	V_{CC} - 28	V
Input Bias Current	I_{IN}	V_{IN} = 0.8V	-	-	30	µA
Input Control OFF	V_{IL}		-	-	0.8	V
Input Control ON	V_{IH}		2.0	-	-	V
Short Circuit Current Limiting	I_{SC}		-1.4	-	-3.0	A
Supply Current - Full Load	I_{CCMax}	I_{OUT} = 1A	-	-	1.1	A
Supply Current - No Load	$I_{QUIENSCENT}$	V_{IN} = 0V; I_{OUT} = 0A; V_{CC} = 12V	-	-	100	µA
Output Saturation Voltage	V_{SAT}	I_{OUT} = 1A	-	-	100	µA
Output Leakage	I_{OFF}	V_{IN} = 0.8V	-50	-	-	µA

Typical Application



HARRIS SEMICONDUCTOR

HIP2500

PRELIMINARY

May 1992

Half-Bridge 500V_{DC} Driver

Features

- Maximum Rating 500V
- Ability to Interface and Drive N-Channel Power Devices
- Floating Bootstrap Power Supply for Upper Rail Drive
- CMOS S4chmitt-Triggered Inputs with Hysteresis and Pull-Down
- 100kHz Operation
- Single Low Current Bias Supply Operation . . . . 7mA Typ
- Latch-up Immune CMOS Logic
- Peak Drive. . . . . Up to 2.0A
- Gate Drive Switching Time . . . . . < 150ns Typ

Applications

- High Frequency Switch-Mode Power Supply
- Induction Heating and Welding
- Switch Mode Amplifiers
- AC and DC Motor Drives
- Electronic Lamp Ballasts
- Battery Chargers
- UPS Inverters

Description

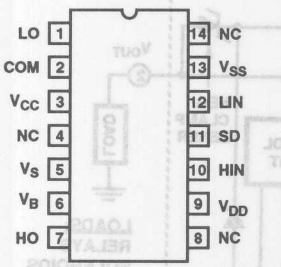
The HIP2500 is a high voltage integrated circuit (HVIC) optimized to drive MOS gated power devices in half-bridge topologies. It provides the necessary control for PWM motor drive, power supply, and UPS applications.

Ordering Information

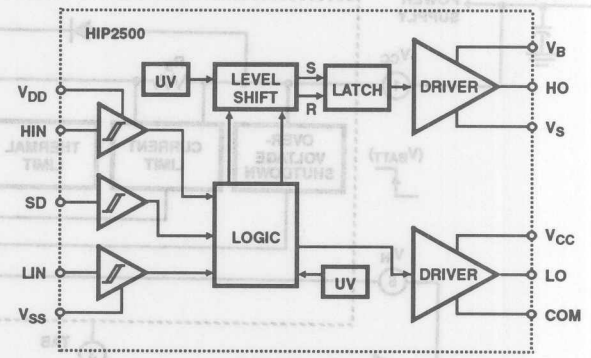
PART	TEMPERATURE	PACKAGE
HIP2500IP	-40°C to +85°C	14 Lead Plastic DIP

Pinout

14 PIN PLASTIC DIP
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2801.1**

Absolute Maximum Ratings

Full Temperature Range Unless Otherwise Noted, All Voltages Referenced to V_{SS} Unless Otherwise Noted.

Floating Supply Voltage, V_B . . . . . V_S-0.5V to V_S+16.5V (Positive Terminal)
Floating Supply Voltage, V_S . . . . . 500V (Common Terminal)
High Side Channel Output Voltage, V_{HO} . . . . . -0.5V to V_B+0.5V
Fixed Supply Voltage, V_{CC} . . . . . -0.5V to 16.5V
Low Side Channel Output Voltage, V_{LO} . . . . . -0.5V to V_{CC}+0.5V
Logic Supply Voltage, V_{DD} . . . . . -0.5V to 16.5V
Logic Input Voltage, V_{IN} . . . . . -0.5V to V_{DD}+0.5V [HIN, LIN & SD (Shutdown)]

Thermal Characteristics

Thermal Resistance, Junction-to-Ambient θ_{ja}
Plastic DIP Package . . . . . 75°C/W
Maximum Package Power Dissipation at +85°C
Plastic DIP Package 500mW
Maximum Junction Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range, T_S . . . . . -40°C to +150°C
Operating Ambient Temperature Range, T_A . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended DC Operating Conditions

Floating Supply Voltage, V_B . . . . . V_S+10V to V_S+15V (Floating Terminal)
High Side Channel Output Voltage, V_{HO} . . . . . 10V to V_B (With Respect to V_S)
Fixed Supply Voltage, V_{CC} . . . . . 10V to 15V
Low Side Channel Output Voltage, VLO . . . . . 0V to V_{CC}
Logic Supply Voltage, V_{DD} . . . . . 4V to V_{CC}
Floating Supply Voltage, V_S . . . . . -4.0V to 500V (Common Terminal)

Electrical Specifications

$V_{CC} = (V_B - V_S) = V_{DD} = 15V$, $C_{OM} = V_{SS} = 0$ and $T_A = +25°C$, Unless Otherwise Noted

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
Quiescent V_{CC} Current	I_{QCC}	-	1.4	1.7	mA
Quiescent V_{BS} Current	I_{QBS}	-	280	400	µA
Quiescent V_{DD} Current	I_{QDD}	-	0.1	1	µA
Logic Input Bias Current, $V_{IN} = V_{DD}$ (HIN, LIN, SD)	IN+	-	12	20	µA
Logic Input Leakage Current, $V_{IN} = V_{SS}$ (HIN, LIN, SD)	IN-	-	0	1	µA
Logic Input Positive Going Threshold	V_{TH}+	7.5	8.0	8.5	V
Logic Input Negative Going Threshold	V_{TH}-	5.5	5.9	6.3	V
Undervoltage Positive Going Threshold	UV+	6.8	8.3	9.85	V
Undervoltage Negative Going Threshold	UV-	6.3	8.2	9.5	V
Output High Open Circuit Voltage (HO, LO)	V_{OUT}+	-	-	15	V
Output Low Open Circuit Voltage (HO, LO)	V_{OUT}-	-	-	0.1	V
Output High Short Circuit Current (Sourcing)	I_{OUT}+	1.9	2.3	-	A
Output Low Short Circuit Current (Sinking)	I_{OUT}-	2	2.5	-	A

Switching Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
HIGH SIDE CHANNEL WITH 500V OFFSET, CL = 1000pF					
High Side Turn-On Propagation Delay	t_{ON}	350	420	500	ns
High Side Turn-Off Propagation Delay	t_{OFF}	300	365	450	ns
High Side Turn-On Rise Time	t_R	20	28	35	ns
High Side Turn-Off Fall Time	t_F	20	28	35	ns
LOW SIDE CHANNEL, CL = 1000pF					
Low Side Turn-on Propagation Delay	t_{ON}	275	350	425	ns
Low Side Turn-off Propagation Delay	t_{OFF}	225	275	330	ns
Low Side Turn-on Rise Time	t_R	20	27	35	ns
Low Side Turn-off Fall Time	t_F	20	27	35	ns
Shutdown Propagation Delay High Side Shutdown	t_{SDHO}	300	385	450	ns
Low Side Shutdown	t_{SDLO}	240	300	360	ns
HIGH SIDE CHANNEL WITH 500V OFFSET, CL = 1000pF					
Propagation Delay Matching (Between HO and LO)	M_t	0	-	75	ns
Minimum On Output Pulse Width (HO, LO)	$PW_{OUT(MIN)}$	-	35	50	ns
Minimum Input Pulse Width (ON)	$PW_{ON(MIN)}$	-	200	250	ns
Minimum Input Pulse Width (OFF)	$PW_{OFF(MIN)}$	-	245	350	ns
Deadtime LO Turn-off to HO Turn-on	DHt_{ON}	125	145	170	ns
Deadtime HO Turn-off to LO Turn-on	DLt_{ON}	15	25	120	ns
MAXIMUM TRANSIENT CONDITIONS					
Offset Supply Operating Transient	dV_S/dt	-	-	50	V/ns

Logic Truth Table

HIN	LIN	UV_H	UV_L	SD	HO	LO	COMMENTS
0	0	0	0	0	0	0	Normal Off
0	1	0	0	0	0	1	Lower On
1	0	0	0	0	1	0	Upper On
1	1	0	0	0	1	1	Both On
X	X	X	X	1	0	0	Chip Disabled
X	X	1	1	X	0	0	V_{CC} UV Lockout and V_{BS} Lockout
X	1	1	0	0	0	1	V_{BS} UV Lockout
1	X	0	1	0	1	0	V_{CC} UV Lockout

HARRIS SEMICONDUCTOR

HIP4010

ADVANCE INFORMATION

May 1992

Power H-Switch

Features

- Two Independent 1/2 H-Switch Drivers
- Single Supply . . . . . +4V to +15V
- Dual Supplies . . . . . ±2V to ±7.5V
- Switching Capabilities 0.5A
- CMOS Input (TTL Compatible)
- Complementary (CMOS) Switching Circuit
- Over-Temperature Protection
- Current-Overload Protection
- "Dynamic Braking" Circuit
- Rds_{ON} . . . . . 0.5Ω per Switching MOSFET

Applications:

- Motor Control
- Relay Driver
- Solenoid Driver
- Stepper Motors

Description

In the Functional Block Diagram of the HIP4010 the four switches and a load are arranged in an H-configuration so that the polarity of the dc supply voltage (from terminals V_{DDA} and V_{SSA}) applied to the load can be selected by switching; thereby directing the flow of load current in either direction. This is commonly known as 4-quadrant load control. As drawn in the Functional Block Diagram, switches P1 and N2 are "closed;" when current flows from V_{DDA} through P1, through the load, and then through N2 to terminal V_{SSA}; where load terminal OUT1 is at a positive potential with respect to OUT2. Switches P1 and N2 are operated synchronously by the control logic. The control logic switches P2 and N1 to an "open" state when P1 and N2 are "ON". When the switch states are reversed, P1 and N2 are open and N1 and P2 are closed. Consequently, current then flows from V_{DDA} through P2, through the load, and through N1 to terminal V_{SSA}, where load terminal OUT2 is then at a positive potential with respect to OUT1.

The HIP4010 POWER H-Switch is designed in a high speed BiMOS-E technology, using both CMOS and bipolar transistors. The BiMOS-E process adds a drain extension implant to 3μ poly-gate CMOS transistors, enhancing the device voltage capabilities. Vertical bipolar transistors, having high gain-bandwidth and transconductance, are standard in the BiMOS-E technology.

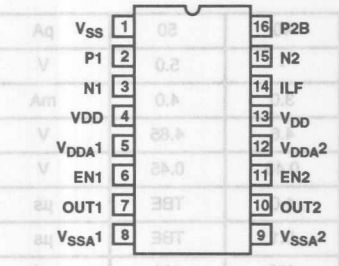
The HIP4010 POWER H-Switch is available in a 16 Lead Dual-In-Line Plastic Package with heat spreading frame construction to enhance thermal dissipation. Under normal conditions, the HIP4010 can dissipate 1.5W (typ.) in free air at +60°C and can dissipate 1.5W (typ.) at +105°C with a PC-Board as a heat-sink.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE & LEAD FORM
HIP4010MP	-55°C to +125°C	16 Lead DIP

Pinout

16 LEAD DUAL-IN-LINE PLASTIC PACKAGE
TOP VIEW



NOTE: Terminals 4, 5, 12 and 13 are interconnected

Functional Truth Table

HIP4010 H-SWITCH

SWITCH DRIVER 1				SWITCH DRIVER 2			
INPUTS			OUTPUT	INPUTS			OUTPUT
P1	N1	EN1	OUT1	P2B	N2	EN2	OUT2
H	L	H	OH	L	L	H	OH
L	L	H	OL	H	L	H	OL
H	H	H	OL	L	H	H	OL
L	H	H	OL	H	H	H	OL
X	X	L	Z	L	H	H	OL

L = Low logic level; H = High logic level
Z = High Impedance (off state)
OH = Output High (sourcing current to the output terminal)
OL = Output Low (sinking current from the output terminal)
X = Don't care

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3176

DC Supply Voltage (Between V_{DD} and V_{SS} Terminals) 16V
DC Input Voltage 16V
Input Terminal Current 1mA
Recommended DC Operating Voltage Range
(V_{DD} to V_{SS}, $V_{DDA}1$ to $V_{SSA}1$, $V_{DDA}2$ to $V_{SSA}2$) ..... +4V to +15V
Operating Temperature Range ..... -55°C to +125°C
Junction Temperature, T_J ..... +150°C
Lead Temperature (During Soldering) ..... +265°C

Above +60°C ..... Derate linearly at 16.6mW/°C
Up to +90°C, with Heat Sink (PC Board) 1.5W
Above +90°C ..... Derate linearly at 25mW/°C
Maximum Thermal Resistance (Free Air*) Junction-to-Air .... +60°C/W

* In free air, the junction-to-air thermal resistance ($R_{\theta JA}$) is typically +50°C/W. This coefficient can be lowered to 40°C/W by suitable design of the PC board to which the HIP4010 package is soldered.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Typical Values Intended Only for Design Guidance

T_A = +25°C, $V_{DDA}1$, $V_{DDA}2$, and V_{DD} = +12V; $V_{SSA}1$, $V_{SSA}2$, and V_{SS} = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
Output Current			0.5	A
Input Resistance			0.5	TΩ
Saturation Voltage I_{SINK} = 0.5A	V_{SAT}		0.25	V
Response Time Rise	t_r	C_L = 5pF, R_L = 1MΩ	1.0	µs
Response Time Fall	t_f		0.2	µs

Electrical Specifications

T_A = +25°C, $V_{SSA}1$, $V_{SSA}2$, and V_{SS} = 0V, Unless Otherwise Specified

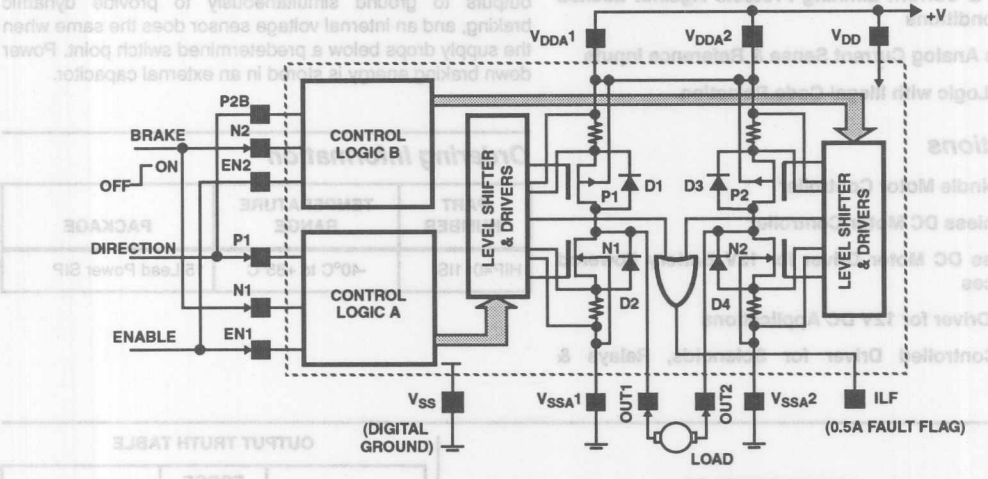
PARAMETERS	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
$V_{DDA}1$, $V_{DDA}2$, and V_{DD} = +12V:					
Input Current	CI1	-	40	50	pA
Input Voltage Range	VI	0.0	-	12.0	V
Idle Supply Current; I_{OUT} = 0	I_{SUPPLY}	-	10	15	mA
Output Voltage High; (V_{SAT}) I_{SOURCE} = 0.5A	V_{OH}	11.65	11.7	11.75	V
Output Voltage Low; (V_{SAT}) I_{SINK} = 0.5A	V_{OL}	0.25	0.30	0.35	V
Response Time Rising Edge	t_{DR}	-	1.0	TBE	µs
Response Time Falling Edge	t_{DF}	-	0.1	TBE	µs
Output Source Current		-	500	530	mA
Output Sink Current		450	500	530	mA
$V_{DDA}1$, $V_{DDA}2$, and V_{DD} = +5V:					
Input Current	CI1	-	40	50	pA
Input Voltage Range	VI	0.0	-	5.0	V
Idle Supply Current; I_{OUT} = 0	I_{SUPPLY}	-	3.0	4.0	mA
Output Voltage High; I_{SOURCE} = 0.5A	V_{OH}	4.55	4.6	4.65	V
Output Voltage Low; (V_{SAT}) I_{SINK} = 0.5A	V_{OL}	0.35	0.40	0.45	V
Response Time Rising Edge	t_{DR}	-	1.0	TBE	µs
Response Time Falling Edge	t_{DF}	-	0.1	TBE	µs
Output Source Current		450	500	530	mA
Output Sink Current		450	500	530	mA

Application

The Functional Block Diagram shows an application block diagram of a motor-driver circuit using HIP4010 as a "Full" H-Switch. The "left" and "right" H-Switch's are driven from the control input terminals to the output switching transistors of the HIP4010. The circuit is intended to safely start, stop, and provide control of rotational direction for a motor requiring no more than 0.5 A of supply current. The stop function includes a "dynamic braking" feature.

With the "ENABLE" terminal LOW, MOSFET Switches P1 and P2 are "off;" i.e., supply current is cut off. With the "BRAKE" terminal LOW and "ENABLE" transitioned HIGH, either P1, N2 or P2, N1 can be driven into conduction; the CMOS-pair chosen for conduction is determined by the logic level applied to the "DIRECTION" terminal; resulting in either clockwise (CW) or counterclockwise (CCW) shaft rotation. When the "BRAKE" terminal is transitioned HIGH (while holding ENABLE at HIGH), the gates of both N1 and N2 are driven HIGH. Thus, if current was flowing through N1 (from the motor terminal OUT1) at the moment of "dynamic braking," it would continue to flow through N1 to the $V_{SSA}1/V_{SSA}2$ external ground tie, then continue through diode D4 to motor terminal OUT2; the resistance of the motor winding (and the series-connected path) dissipates the kinetic energy stored in the system. Reversing rotation, current flowing through N2 (from the motor terminal OUT2), at the moment of "dynamic braking", would continue to flow through N2 to the $V_{SSA}2/V_{SSA}1$ tie, then continue through diode D2 to the motor terminal OUT1, to dissipate the stored kinetic energy as previously described.

Functional Block Diagram



Terminal Assignment Information

$V_{DDA}1$	Positive terminal-pin for power-supply; $V_{DDA}1$ is internally connected to $V_{DDA}2$ and V_{DD}.
$V_{DDA}2$	Positive terminal-pin for power-supply; $V_{DDA}2$ is internally connected to $V_{DDA}1$ and V_{DD}.
V_{DD}	Positive terminal-pin for power-supply suited to digital circuits; V_{DD} is internally connected to $V_{DDA}1$ and $V_{DDA}2$.
$V_{SSA}1$	Negative terminal-pin for power-supply; used in conjunction with Switch Driver 1.
$V_{SSA}2$	Negative terminal-pin for power-supply; used in conjunction with Switch Driver 2.
V_{SS}	Negative terminal-pin for power-supply suited for digital circuits.
P1, P2B	Input pins used to control the direction of output current flow in Switch Driver 1 and Switch Driver 2, respectively.
N1, N2	Input pins used to activate the Dynamic Braking of Switch Driver 1 and Switch Driver 2, respectively.
EN1, EN2	Input pins used to enable Switch Driver 1 and Switch Driver 2, respectively.
OUT1, OUT2	Output pins for Switch Driver 1 and Switch Driver 2, respectively.
ILF	Output pin (flag); high logic level signify that Switch Driver1, Switch Driver2, or both are in "Current Limit" state

NOTES:

1. Terminals P1, P2, N1, N2, P2B, EN1 and EN2 are internally connected to protection circuits intended to guard the CMOS gate-oxides against damage due to electrostatic discharge. However, these devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
2. For maintenance of performance and reliability, Harris Semiconductor strongly recommends that the "IC Handling Procedures", located in Section 1 of the current Analog Products Data Book, be followed closely by any activity involved with IC products.

HARRIS SEMICONDUCTOR

HIP4011

PRELIMINARY

May 1992

Three-Phase Brushless DC Motor Controller

Features

- 3A DC, 5A Peak Output Current
- 16V Max. Rated Supply Voltage
- Built-in "Free-Wheeling" Diodes
- Output dv/dt Limited to Reduce EMI
- External Dynamic Brake Control Switch With Undervoltage Sense
- Thermal & Current Limiting Protects Against Locked Rotor Conditions
- Provides Analog Current Sense & Reference Inputs
- Decode Logic with Illegal Code Rejection

Applications

- Drive Spindle Motor Controller
- 3ϕ Brushless DC Motor Controller
- Brushless DC Motor Driver for 12V Battery Powered Appliances
- Phased Driver for 12V DC Applications
- Logic Controlled Driver for Solenoids, Relays & Lamps

Description

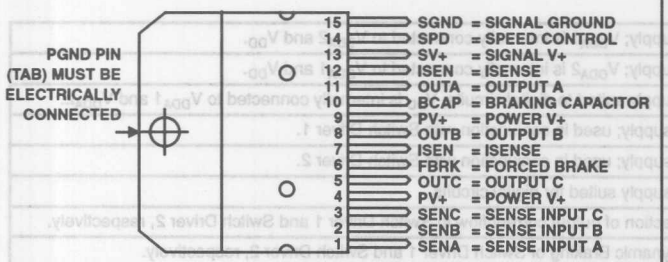
The HIP4011 motor driver is intended for three phase brushless motor control at continuous output currents up to 3A. It accepts inputs from buffered Hall effect sensors and drives three motor windings, regulating the current through an external current sensing resistor, according to an analog control input. Output "freewheeling" diodes are built in and output dv/dt is limited to decrease the generated EMI. Thermal and current limiting are used to protect the device from locked rotor conditions. A brake control input forces all outputs to ground simultaneously to provide dynamic braking, and an internal voltage sensor does the same when the supply drops below a predetermined switch point. Power down braking energy is stored in an external capacitor.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP4011IS	-40°C to +85°C	15 Lead Power SIP

Pinout

15 LEAD POWER SIP
TOP VIEW



OUTPUT TRUTH TABLE

SENSOR INPUTS			FORCE BRAKE INPUT*	OUTPUTS		
A	B	C	FBRK	A	B	C
0	0	0	0	OFF	OFF	OFF
1	0	0	0	1	OFF	0
0	1	0	0	0	1	OFF
1	1	0	0	OFF	1	0
0	0	1	0	OFF	0	1
1	0	1	0	1	0	OFF
0	1	1	0	0	OFF	1
1	1	1	0	OFF	OFF	OFF
X	X	X	1	0	0	0

* Undervoltage and Force Brake logic truth table entries are identical.

"X" = Don't Care

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2939.1**

Absolute Maximum Ratings

Supply Voltage, SV+ or PV+ . . . . . -1V to +16V
Referred to SGND or PGND (Note 1)
Output Current, Continuous 3A
Output Current, Peak (Note 2) 5A
Substrate (PGND) Current 1A
Logic Input Current . . . . . -20mA to +20mA
(Clamped to SV+ and SGND)

Dissipation/Temperature Ratings

Power Dissipation (Note 3) 25W
Junction Temperature Range, Operating . . . . . +150°C
Storage Temperature Range . . . . . -55°C to +150°C

NOTES:

1. PV+ and SV+ are to be tied together, as are PGND and SGND.
2. Operating above the continuous current rating causes a decrease in operating life.
3. Derate power dissipation above case temperature of +75°C at 0.33 Watts/°C.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C and SV+ = PV+ = 10.4V to 13.2V, Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITION	LIMITS			UNITS
		MIN	TYP	MAX	
SUPPLY (SV+) CURRENT					
No Drive	Outputs Off			10	mA
With Drive	Outputs On			15	mA
LOGIC INPUT CURRENT					
Sensor Inputs	SENA, SENB & SENC = 0V to 3V	-0.5		-1.5	mA
Brake Input	FBRK = 0.8V to 2.4V	50		150	µA
LOGIC INPUT THRESHOLDS					
Sensor Inputs	Logic "0" Input Voltage			1.8	V
Sensor Inputs	Logic "1" Input Voltage	3			V
Brake Input	Logic "0" Input Voltage			0.8	V
Brake Input	Logic "1" Input Voltage	2.4			V
AMPLIFIER INPUT (SPD)					
Bias Current				700	nA
Offset Voltage				3	mV
Input Range (Linear)		0		1	V
Input Impedance		1			MΩ
SYSTEM BANDWIDTH	(Note 1)		35		kHz
CURRENT LIMIT	Rsense = 0.20Ω		5		A
THERMAL LIMIT					
Threshold			155		°C
Hysteresis			40		°C
OUTPUT DRIVERS					
On Saturation (See Note 5)	Iout = 3A, Vpmos + Vnmos			2.2	V
On Saturation (See Note 5)	Iout = 0.6A, Vpmos + Vnmos			0.44	V
Off Leakage	PV+ > Vout > PGND or Isen			1	mA
Slew Rate	(See Note 2)		0.5		V/µS
FREEWHEEL DIODES					
Forward Drop	Iout = 1A			1.5	V

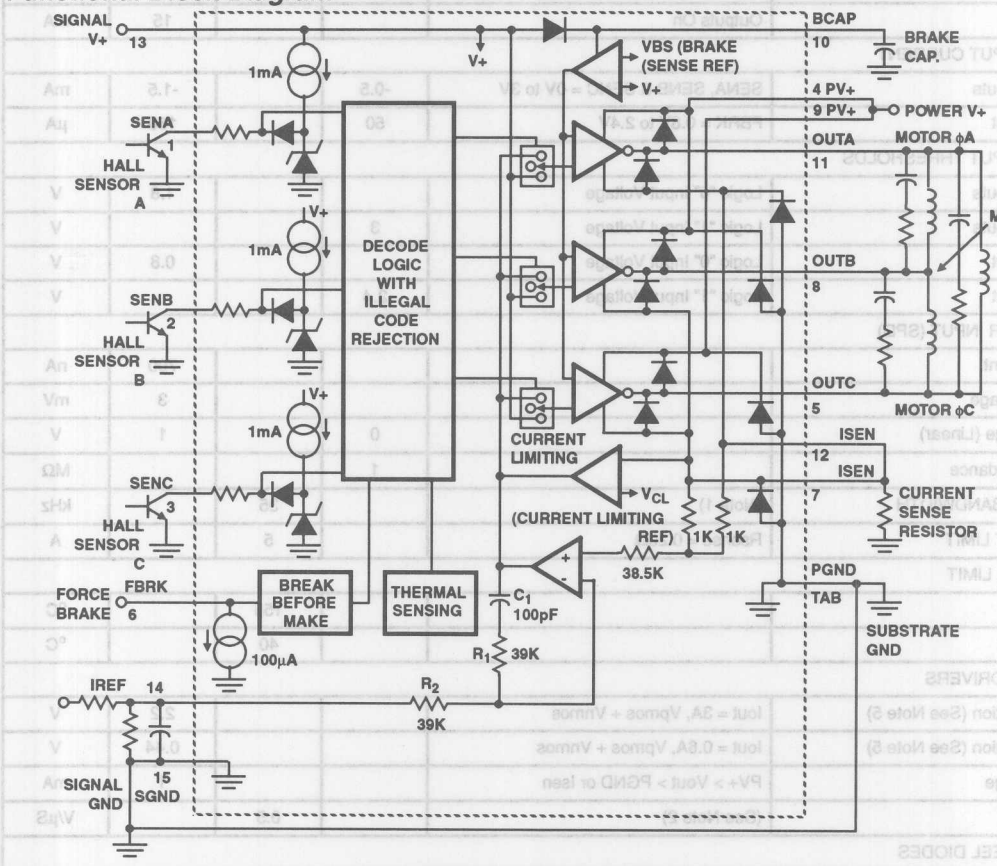
Electrical Specifications T_A = +25°C and SV+ = PV+ = 10.4V to 13.2V, Unless Otherwise Specified (Continued)

CHARACTERISTIC	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
INTERNAL BRAKE DRIVER					
Undervoltage Trip Point, PV+	(See Note 3)	2.7		3.3	V
Hysteresis	(See Note 4)	40		60	%
On Saturation	Each Nmos, Iout = 3A			0.4	V
BRAKE CAPACITOR (BCAP)					
Discharge Leakage	SV+ = PV+ = 3V to 12V, BCAP = 10V			5	µA

NOTES:

1. The system bandwidth is fixed by an internal RC network around the amplifier.
2. Internal limiting of turn on and turn off drive is used to limit output dv/dt.
3. The braking action starts at the given trip point with a falling supply voltage.
4. Hysteresis causes the brake to be removed at a higher trip point with a rising supply voltage.
5. This value includes the combined voltage drops of one upper plus one lower switch at the indicated current.

Functional Block Diagram



THREE-PHASE BRUSHLESS CONTROLLER

HARRIS SEMICONDUCTOR

HIP4080

ADVANCE INFORMATION

May 1992

High Frequency H-Bridge Driver

Features

- High Voltage Capability; Bootstrap Supply Max Voltage to 95VDC
- Bus Voltage .....80V (Max)
- Small Surface Mount Package
- Drives 1000pF Load at 450KHz in Free Air at 50°C with Rise and Fall Times of Typically 10ns
- User-Programmable Dead Time
- Drives 4 N-Channel Devices in H-Bridge Configuration
- On-chip Charge-Pumps Maintain Bootstrap Supplies
- HEN Pin can PWM Upper Switches Only
- HEN (High Enable) and DIS (Disable) Pins Override Input Control
- Proprietary Circuitry Minimizes On-Chip Switching Losses
- Input Logic Thresholds Compatible with 5 and 15 volt Logic Levels
- On-Chip Control Circuit Initializes Bootstrap Capacitors upon Chip Enable

Applications

- Medium/Large Voice Coil Motors
- H-Bridge Power Supplies
- Digital Power Amplifiers for Hi-Fi systems
- High Speed Stepper Motor controls

Description

The HIP4080 is a high frequency, medium voltage H-Bridge N-Channel MOSFET driver IC, packaged in a 20 or 24 pin plastic SOIC. Due to its ability to switch at frequencies greater than 500KHz,the HIP4080 is particularly well suited for driving Voice Coil Motors for medium and large computer disk drives, switching amplifiers in high-efficiency switching audio amplifiers and H-Bridge power supplies depending on load and cooling techniques.

Short propagation delays of approximately 70ns and dead times of typically 40ns coupled with "minimum on times" of about 100ns allow a nearly distortionless, ripple-free current waveform and maximum control loop crossover frequencies providing rapid, fine control of the driven load.

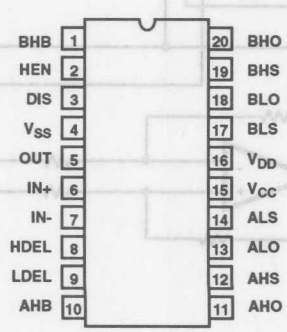
HIP4080 can also drive any small, medium voltage brush motor, and two HIP4080s can be used to drive high performance stepper motors, since the short minimum "on-time" can provide fine micro-stepping capability.

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
HIP4080IP	-40°C to +85°C	20 Pin Plastic DIP
HIP4080IB	-40°C to +85°C	20 Pin Plastic SOIC

Pinout

20 PIN PLASTIC DIP
20 PIN SOIC
TOP VIEW



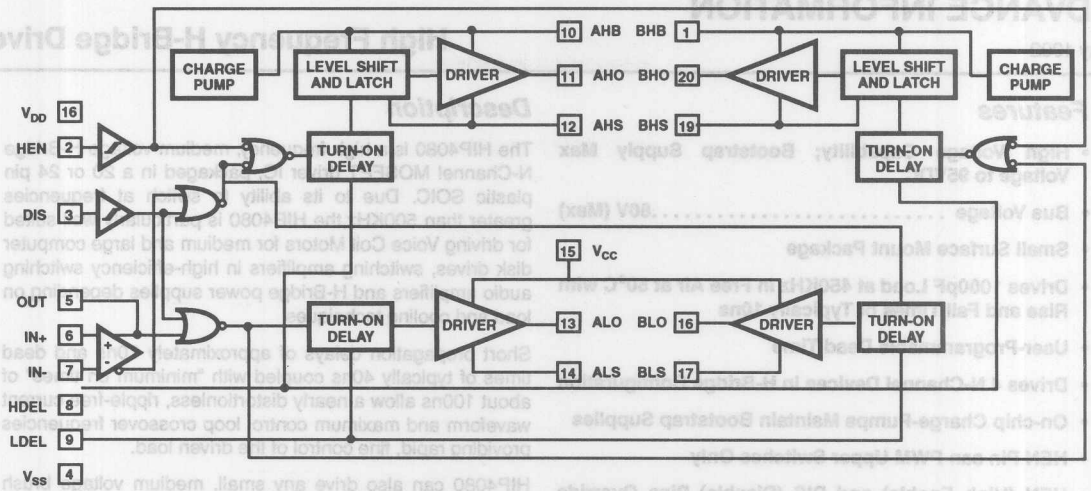
11 POWER DRIVERS AND SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

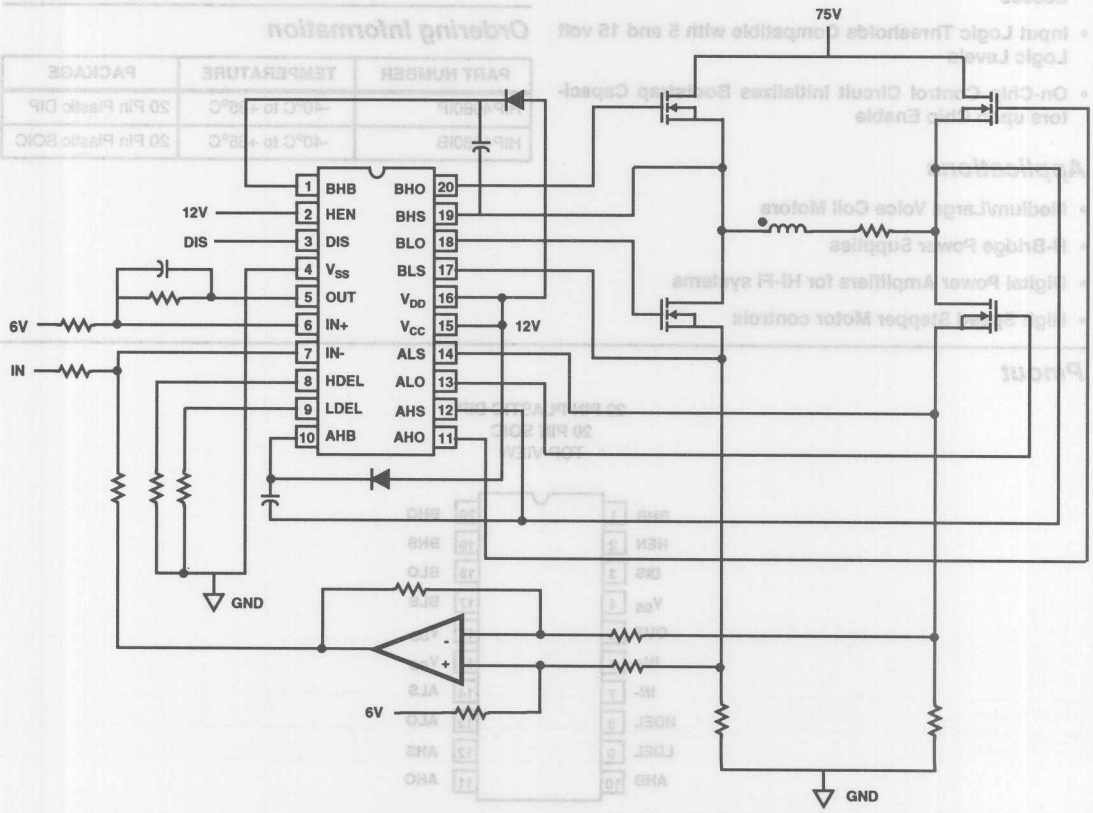
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File Number 3178

Functional Block Diagram



Typical Application



Absolute Maximum Ratings

Supply Voltage, V_{DD} and V_{CC} ..... -0.3V to 16V
Input, Output or I/O Voltage ..... -0.3V to V_{DD}+0.3V
Voltage on AHS, BHS ..... -2.0V (Transient) to 80V
Voltage on ALS, BLS ..... -2.0V (Transient) to +2.0V (Transient)
Voltage on AHB, BHB ..... $V_{AHS, BHS}$-0.3V to $V_{AHS, BHS}$+16V
Voltage on ALO, BLO ..... $V_{ALS, BLS}$-0.3V to V_{CC}+0.3V
Voltage on AHO, BHO ..... $V_{AHS, BHS}$-0.3V to $V_{AHB, BHB}$+0.3V

Input Current, HDEL and LDEL ..... -5mA to 0mA
Phase Slew Rate ..... .20V/ns
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
Maximum Package Power Dissipation at +25°C (Note 1)
SOIC Package 750mW

NOTE:

1. Derate power dissipation above ambient temperature of 25°C by 7mW/°C. $P_{diss} = 0.144 + 0.2e^{-6} f_{PWM} + 2 V_{CC}^2 C_L (f_{PWM} + f_{DIR})$ where f_{PWM} = pwm frequency and f_{DIR} = direction change frequency (in Hertz) C_L = load capacitance (in Farads)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage, V_{DD} and V_{CC} ..... +10V to +15V
Voltage on ALS, BLS ..... -1.0V +1.0V
Voltage on AHS, BHS ..... -1V to 75V

Voltage on AHB, BHB ..... $V_{AHS, BHS}$+10V to $V_{AHS, BHS}$+15V
Input Current, HDEL and LDEL ..... -500µA to -50µA
Operating Temperature Range ..... 0°C to +125°C

Electrical Specifications

Specifications apply over recommended operating conditions, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
QUIESCENT SUPPLY CURRENTS (specified with static inputs that fully switch outputs)						
V_{DD} Current	I_{DD}		8	12	20	mA
V_{CC} Current	I_{CC}	$I_{ALO} = I_{BLO} = 0$	0	100	200	µA
AHB Current	I_{AHB}	$I_{AHO} = 0$	-40	-20	0	µA
BHB Current	I_{BHB}	$I_{BHO} = 0$	-40	-20	0	µA
AHS Current	I_{AHS}	$I_{AHO} = 0$	-5	0	1	µA
BHS Current	I_{BHS}	$I_{BHO} = 0$	-5	0	1	µA
INPUT COMPARATOR						
Offset Voltage	V_{OS}		-5	0	+5	mV
Input Bias Current	I_{IB}		0	1	4	µA
Input Offset Current	I_{OS}		-1	0	+1	µA
Input Common Mode Voltage Range	CMVR		1	-	V_{DD}-1.5	V
Voltage Gain	AVOL		10	25	-	V/mV
OUTPUT (OUT)						
High Level Output Voltage	V_{OH}	IN+>IN-, I_{OH} = -300µA	V_{DD}-0.4	-	-	V
Low Level Output Voltage	V_{OL}	IN+<IN-, I_{OL} = 300µA	-	-	0.4	V
High Level Output Current	I_{OH}	$V_{OUT}=V_{DD}/2$	-	-	-2.4	mA
Low Level Output Current	I_{OL}	$V_{OUT} = V_{DD}/2$	4.5	-	-	mA
DIS, HEN						
Low Level Input Threshold Voltage	V_{TL}		1.4	2.1	-	V
High Level Input Threshold Voltage	V_{TH}		-	2.4	2.7	V
Input Hysteresis	V_{HYS}		-	0.3	-	V
GATE DRIVER OUTPUTS						
Peak Pullup Current	I_{O+}	V_{CC} = 12V	-	2	-	A
Peak Pulldown Current	I_{O-}	V_{CC} = 12V	-	2	-	A

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Input Pulse Width	T_{PWIN}	IHDEL = -100 µA ILDEL = -50 µA	-	100	-	ns
Mimimum Output Pulse Width	T_{PWOUT}	IHDEL = -100 µA ILDEL = -50 µA	-	100	-	ns
HEN Prop. Delay	T_{PHEN}	IHDEL = -100 µA ILDEL = -50 µA	-	70	-	ns
Upper Prop. Delay (Turn-Off)	T_{PH}	IHDEL = -100 µA ILDEL = -50 µA	-	70	-	ns
Lower Prop. Delay (Turn-t_{OFF})	T_{PL}	IHDEL = -100 µA ILDEL = -50 µA	-	70	-	ns
DISable Prop. Delay	T_{PDIS}	IHDEL = -100 µA ILDEL = -50 µA	-	150	-	ns
Dead Time	T_{DTLH}	IHDEL = -100 µA ILDEL = -50 µA Lower off toUpper on, C_L = 1000 pF	-	40	-	ns
Dead Time	T_{DTHL}	IHDEL = -100 µA ILDEL = -50 µA Upper off toLower on, C_L = 1000 pF	-	40	-	ns
Rise Time	T_R	C_L=2500pf	-	20	-	ns
		C_L=1000pf	-	10	-	ns
Fall Time	T_F	C_L=2500pf	-	20	-	ns
		C_L=1000pf	-	10	-	ns

HARRIS SEMICONDUCTOR

HV400

May 1992

High Current MOSFET Driver

Features

- Fast Fall Times.....16ns at 10,000pF
- No Supply Current In Quiescent State
- Peak Source Current.....6A
- Peak Sink Current.....30A
- High Frequency Operation.....300kHz

Applications

- Switch Mode Power Supplies
- DC/DC Converters
- Motor Controllers
- Uninterruptible Power Supplies

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HV400CP	0°C to +75°C	8 Pin Plastic Mini-DIP
HV400CB	0°C to +75°C	8 Pin Plastic SOIC
HV400IP	-40°C to +85°C	8 Pin Plastic Mini-DIP
HV400IB	-40°C to +85°C	8 Pin Plastic SOIC
HV400MJ/883*	-55°C to +125°C	8 Pin CerDIP
HV400Y	+25°C	DICE

* Contact Harris for availability date.

Description

The HV400 is a single monolithic, non-inverting high current driver designed to drive large capacitive loads at high slew rates. The device is optimized for driving single or parallel connected N-channel power MOSFETs with total gate charge from 5nC to >1000nC. It features two output stages pinned out separately allowing independent control of the MOSFET gate rise and fall times. The current sourcing output stage is an NPN capable of 6A. An SCR provides over 30A of current sinking. The HV400 achieves rise and fall times of 54ns and 16ns respectively driving a 10,000pF load.

Special features are included in this part to provide a simple, high speed gate drive circuit for power MOSFETs. The HV400 requires no quiescent supply current, however, the input current is approximately 15mA while in the high state. With the internal current steering diodes (pin 7) and an external capacitor, both the timing and MOSFET gate power come from the same pulse transformer; no special external supply is required for high side switches. No high voltage diode is required to charge the bootstrap capacitor.

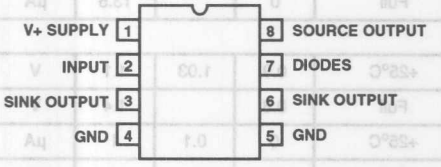
The HV400 in combination with the MOSFET and pulse transformer makes an isolated power switch building block for applications such as high side switches, secondary side regulation and synchronous rectification. The HV400 is also suitable for driving IGBTs, MCTs, BJTs and small GTOs.

The HV400 is a type of buffer; it does not have input logic level switching threshold voltages. This single stage design achieves propagation delays of 20ns. The output NPN begins to source current when the voltage on pin 2 is approximately 2V more positive than the voltage at pin 8.

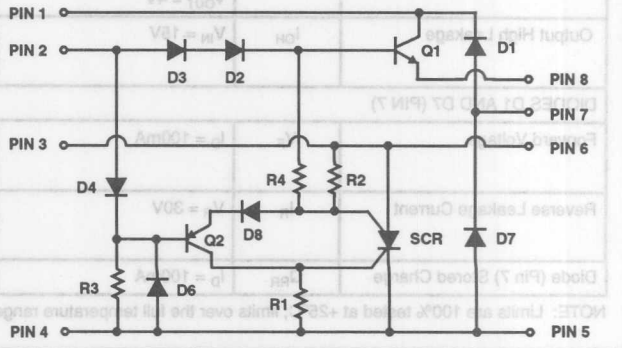
The output SCR switches on when the input pin 2 voltage is 1V more negative than the voltage at pins 3/6. Due to the use of the SCR for current sinking, once the output switches low, the input must not go high again until all the internal SCR charge has dissipated, 0.5µs - 1.5µs later.

Pinout

HV400 (PLASTIC MINI-DIP AND SOIC)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 2850

Absolute Maximum Ratings

Voltage Between Pin1 and Pin 4/5 ..... 35V
Input Voltage Pin 7 (Max) ..... Pin 1 + 1.5V
Input Voltage Pin 7 (Min) ..... Pin 4/5 -1.5V
Input Voltage Pin 2 to Pin 4/5 ..... +/- 35V
Input Voltage Pin 2 to Pin 6 ..... -35V
Maximum Clamp Current (Pin 7) ..... ±300mA
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... $-65°C < T_A < +150°C$

Thermal Resistance ..... θ_{ja} θ_{jc}
PDIP ..... 93.8°C/W 31.5°C/W
SOIC ..... 157.1°C/W 42.8°C/W
Power Dissipation at T_A = +25°C ..... 1.33W Mini-DIP
Power Dissipation at T_A = +25°C ..... 0.8W SOIC
Operating Temperature Range
HV400CP/CB ..... $0°C < T_A < +70°C$
HV400IP/IB ..... $-40°C < T_A < +85°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications V_{SUPPLY} = 15V

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
INPUT (PIN 2)							
Input High Differential Voltage (Pin 2 - Pin 8)	V_{IH}	V_{OUT} = 0V, I_{OUT} HI = 10mA	+25°C	0.6	1.7	2.8	V
			Full	0.5	-	3.5	V
Input Low Differential Voltage (Pin 2 - Pin 3/6)	V_{IL}	V_{OUT} = 12V, I_{OUT} LO = -3mA	+25°C	-1.1	-0.9	-0.8	V
			Full	-1.26	-	-0.65	V
Input High Current	I_{IH}	$V_{PIN\ 1,\ 2}$ = 30V, I_{SOURCE} = 0	+25°C	15	18	20	mA
			Full	15		22	mA
Input High Current Peak	I_{IHP}	I_{SOURCE} = 6A, 1µs pulse, V_{IN} = 9V, V_{OUT} = 0V	+25°C		700		mA
Input Low Current	I_{IL}	$V_{PIN\ 2}$ = -30V	+25°C	-80	-50		µA
			Full	-120			µA
SOURCE OUTPUT (PIN 8)							
High Output Voltage	V_{OH}	V_{IN} = +V, I_{OUT} = 150mA	+25°C	12.1	12.8	13.4	V
			Full	12.0		13.5	V
Peak Output Current	I_{OP8}	V_{IN} = 9V, 1µs Pulse, V_{OUT} = 0V	+25°C		6		A
Output Low Leakage	I_{OL}	V_{OUT} = 0V, V_{IN} = 0V	+25°C	0	10	50	µA
			Full			55	µA
SINK OUTPUT (PIN 3/6)							
Low Output Voltage	V_{OL}	V_{IN} = 0V, I_{OUT} = -150mA	+25°C	0.8	0.89	1.0	V
			Full	0.8		1.05	V
Peak Output Current	I_{OP6}	V_{IN} = 0V, 5µs Pulse, V_{OUT} = 4V	+25°C		30		A
Output High Leakage	I_{OH}	V_{IN} = 15V	+25°C	0	0.3	2	µA
			Full	0		13.5	µA
DIODES D1 AND D7 (PIN 7)							
Forward Voltage	V_F	I_D = 100mA	+25°C	0.9	1.03	1.1	V
			Full	0.8		1.4	V
Reverse Leakage Current	I_R	V_R = 30V	+25°C	0	0.1	1	µA
			Full	0		1	µA
Diode (Pin 7) Stored Charge	Q_{RR}	I_D = 100mA	+25°C		6.5		nC

NOTE: Limits are 100% tested at +25°C; limits over the full temperature range are guaranteed but not tested.

Pin Descriptions

SYMBOL	DESCRIPTION
DC INPUT PARAMETERS	
V_{IH}	The differential voltage between the input (Pin 2) to the output (Pin 8) required to source 10mA
V_{IL}	The differential voltage between the input (Pin 2) to the output (Pins 3, 6) required to sink 3mA
I_{IH}	The current required to maintain the input (Pin 2) high with I_{OUT} = 0A
I_{IHP}	The input (Pin 2) current for a given pulsed output current
I_{IL}	The current require to maintain the input (Pin 2) low
DC OUTPUT PARAMETERS	
V_{OH}	The output (Pin 8) voltage with input (Pin 2) = V+
I_{OP8}	The pulsed peak source current form output (Pin 8)
I_{OL}	The output (Pin 8) leakage current with the input (Pin 2) = Ground
V_{OL}	The output (Pins 3, 6) voltage with the input (Pin 2) = Ground
I_{OP6}	The pulsed peak sink current into output (Pins 3, 6)
I_{OH}	The output (Pins 3, 6) leakage current with the input (Pin 2) = V+
V_F	The forward voltage of diode D1 or D7
I_R	The reverse leakage current of diode D1 or D7
Q_{RR}	The time integral of the reverse current at turn off
AC PARAMETERS (See Switching Time Specifications)	
T_R	The low to high transition of the output
T_F	The high to low transition of the output
T_{DR}	The output propagation delay from the input (Pin 2) rising edge
T_{DF}	The output propagation delay from the input (Pin 2) falling edge
T_{OR}	The minimum time required after an output high to low transition before the next input low to high transition

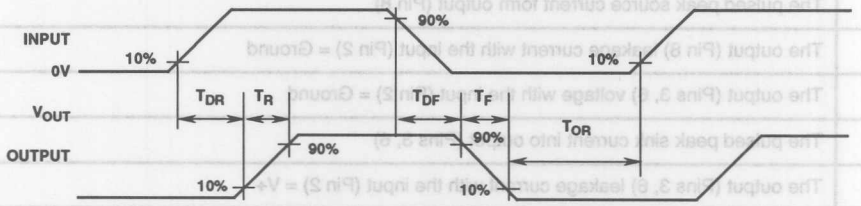
Switching Time Specifications V_{SUPPLY} = 15V

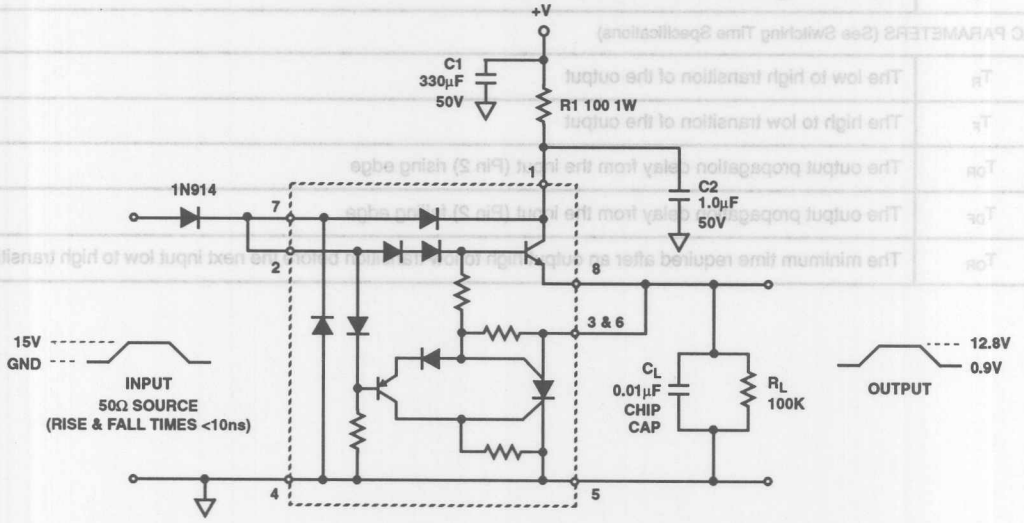
PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS			UNITS
				MIN	TYP	MAX	
Rise Time	T_R	See Switching Test Circuit	Full		50	66	ns
Fall Time	T_F	See Switching Test Circuit	Full		15	24	ns
Delay Time (Lo to Hi)	T_{DR}	See Switching Test Circuit	Full		20	25	ns
Delay Time (Hi to Lo)	T_{DF}	See Switching Test Circuit	Full		17	28	ns
Minimum Off Time	T_{OR}	See Switching Test Circuit	Full		900	1500	ns

NOTES:

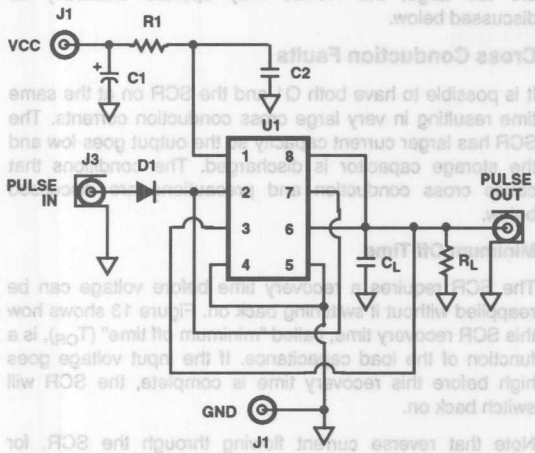
1. Switching times are guaranteed but not tested
2. Typical values are for +25°C

Switching Diagram and Test Circuit



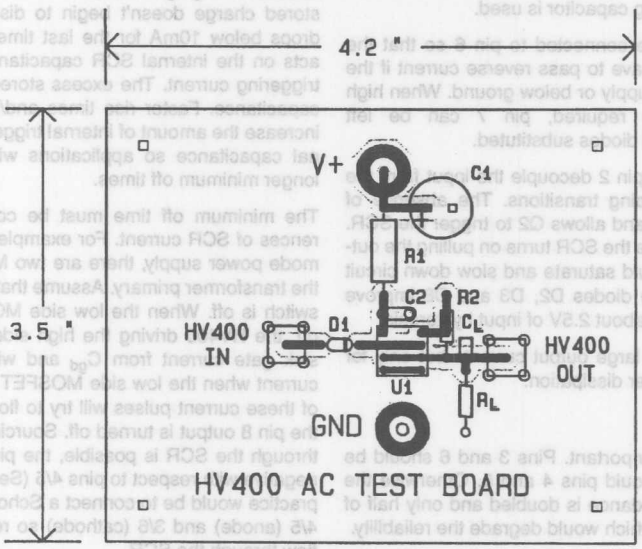


HV400 Switching Test Circuit



Parts List

R1 100Ω, 1W Carbon Resistor
R2 Wire
R_L 100KΩ, 1/8W Carbon Resistor
C1 330µF, 50V Capacitor
C2 1µF, 50V Capacitor
C_L 0.01µF, 50V Chip Capacitor
D1 1N914 Diode
J1, J2 PC Mount Banana Jack Johnson 108-0740-001
J3, J4 PC Mount SMA Connector Johnson EFJ142
U1 Harris HV400 I.C.



Application Information

Circuit Operation

The HV400's operation is easily explained by referring to the schematic. The control signal is applied to pin 2. If the control signal is about 2V above pin 8, the output NPN Q1 turns on charging the MOSFET gate from a capacitor connected to pin 1. Resistor R4 helps keep the SCR off by applying a reverse bias to the SCR anode gate.

When the control input drops about 1V below pin 3/6, PNP Q2 turns on which triggers the SCR by driving both the anode and cathode gates. The SCR discharges the MOSFET gate and when its current becomes less than 10mA, it turns off. Transistor Q2 conducts any gate leakage currents, through resistors R1 and R2, once the SCR turns off. Figure 7 shows the output characteristics before the SCR turns on and after it turns off. When the SCR turns on, resistor R4 provides a path to remove Q1 base charge. Resistor R3 provides the base current for Q2 to reduce the turn off delay time. Resistors R1 and R2 reduce the SCR recovery time.

The two diodes connected to the diode input pin 7 provide some operation flexibility. With pins 2 and 7 connected together, diode D1 provides a path to recharge the storage capacitor once the MOSFET gate is pulled high and, along with diodes D2 and D3, keeps Q1 from going into hard saturation which would increase delay times. Diode D7 would clamp the input near ground and provide a current path if an input DC blocking capacitor is used.

Alternatively, pin 7 can be connected to pin 6 so that the SCR and NPN Q1 don't have to pass reverse current if the output "rings" above the supply or below ground. When high performance diodes are required, pin 7 can be left disconnected and external diodes substituted.

The diodes in series with pin 2 decouple the input from the output during negative going transitions. The absence of input current turns off Q1 and allows Q2 to trigger the SCR. Diode D8 turns off Q2 once the SCR turns on pulling the output low, otherwise Q2 would saturate and slow down circuit operation. In addition, the diodes D2, D3 and D8 improve noise immunity by adding about 2.5V of input hysteresis.

The HV400 is capable of large output currents but only for brief durations due to power dissipation.

Circuit Board Layout

PC board layout is very important. Pins 3 and 6 should be connected together as should pins 4 and 5. Otherwise the internal interconnect impedance is doubled and only half of the bond wires are used which would degrade the reliability.

The bootstrap capacitor should hold at least 10x the charge of the MOSFET and should be connected between pins 1 and 4/5 with minimum lead lengths and spacings. Likewise, the HV400 should be as close to the MOSFET as possible. Any long PC traces (parasitic inductances) between the MOSFET gate and pins 8 or 3/6 or between the source and pins 4/5 should be avoided. Inductance between the HV400 and the MOSFET limit the MOSFET switching time. If they are too large, the HV400 may operate erratically as discussed below.

Cross Conduction Faults

It is possible to have both Q1 and the SCR on at the same time resulting in very large cross conduction currents. The SCR has larger current capacity so the output goes low and the storage capacitor is discharged. The conditions that cause cross conduction and precautions are discussed below.

Minimum Off Time

The SCR requires a recovery time before voltage can be reapplied without it switching back on. Figure 13 shows how this SCR recovery time, called "minimum off time" (T_{OR}), is a function of the load capacitance. If the input voltage goes high before this recovery time is complete, the SCR will switch back on.

Note that reverse current flowing through the SCR, for example due to load inductance ringing, extends the minimum off time. Since the minimum off time is really dependent upon how much stored charge remains in the SCR when the anode (pin 3/6) is taken positive, it may vary for different applications. Figure 13 indirectly shows that the minimum off time increases with larger currents. It also increases at elevated temperatures as shown in Figure 14. Excessive ringing increases the minimum off time since the stored charge doesn't begin to dissipate until the current drops below 10mA for the last time. Rising anode voltage acts on the internal SCR capacitance to generate its own triggering current. The excess stored charge increases this capacitance. Faster rise times and/or higher voltages also increase the amount of internal trigger current from the internal capacitance so applications with larger dV/dt require longer minimum off times.

The minimum off time must be considered for all occurrences of SCR current. For example, in a half bridge switch mode power supply, there are two MOSFET's connected to the transformer primary. Assume that the high side MOSFET switch is off. When the low side MOSFET switch is turned on, the HV400 driving the high side MOSFET will have to sink gate current from C_{gd} and will have to source gate current when the low side MOSFET switches back off. Both of these current pulses will try to flow through pin 3/6 since the pin 8 output is turned off. Sourcing current from pins 3/6 through the SCR is possible, the pin 3/6 voltage becoming negative with respect to pins 4/5 (See Figure 8). But a better practice would be to connect a Schottky diode between pins 4/5 (anode) and 3/6 (cathode) so reverse current does not flow through the SCR.

False SCR Triggering

The SCR may be triggered inadvertently. The output may overshoot the input due to inductive loading or over driving the output NPN (allowing it to saturate). Whenever pin 6 is more positive than pin 2 by 1V, the SCR is triggered on. Also,

if the output rises too rapidly, greater than 0.5V/nS, the SCR may self trigger. Both issues are resolved by minimizing the load inductance and inserting sufficient resistance, usually 0.1 to 10 ohms, between pin 8 and the load.

A very fast negative going input voltage can result in minimum off times of about 2.5µs. If the output can not keep up with the falling input, the stored charge of diode D4 is transferred into the base of Q2. This excess charge in Q2 must have time to dissipate. Otherwise, when pin 3/6 goes positive, Q2 will turn on and trigger the SCR. An external diode in series with pin 2, as shown in Figure 1, will prevent D4 from discharging into the base of Q2 but that will also reduce the output voltage by the forward voltage of that diode.

Internal Diodes

The internal diodes connected to pin 7 are provided for convenience but may not be suitable for large currents. Since they are part of the integrated circuit, they are physically small, operate at high current densities, and have long recovery times. Figure 15 shows that their forward characteristics degrade above 100mA. In addition, Figure 16 shows their reverse recovery charge as a function of forward current. The product of this charge, the applied reverse voltage and the frequency is the additional power dissipation due to the diodes. For stored charge calculations, use the peak forward current within 100ns of the application of reverse bias. In addition to the extra power dissipation, the capacitance of these diodes may extend the switching delay times.

Power Dissipation Calculations

The power required to drive the MOSFET is the product of its total gate charge times the gate supply voltage (maximum voltage on HV400 pin 1, 2 or 7) times the frequency. Assuming that the MOSFET gate resistance is negligible, this power is dissipated within the HV400. If resistors are placed between the HV400 and the MOSFET, then some of the power is dissipated in the resistors, the percentage depending upon the ratio of resistors to HV400 output impedance.

There are two other sources of power dissipation to consider. First there is the power in R3 which is the product of the input pin 2 current and voltage (with no output current) times the duty cycle. Second is the product of the pin 7 diode stored charge, which is dependent upon the forward current, times the applied diode reverse voltage times the frequency. This information is available from figures 3 and 16 in this data sheet.

Applications Circuits

The HV400 was designed to interface a pulse transformer to a power MOSFET. There must be some means to balance the transformer volt-second product over a cycle. The unipolar drive shown in Figure 1 lets the core magnetization inductance reverse the primary and secondary voltages. The zener diode on the primary side limits this voltage and must be capable of dissipating the energy stored in the transformer. The load may be connected to either the power MOSFET drain or source.

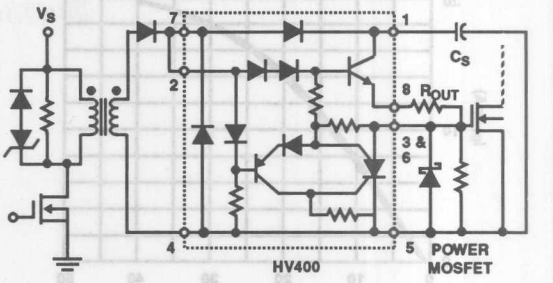


FIGURE 1. UNIPOLAR DRIVE

A diode is added in series with pins 2 and 7 to allow the transformer secondary to go negative. The charge storage of the pin 7 diode may cause the turn off delay time to be too long. Alternatively, pin 7 could be left disconnected and a second external diode connected between the transformer (anode) and pin 1 (cathode). In some applications the diode in series with pin 2 may be unnecessary but the -35V input to output or ground maximum rating should be observed.

Sometimes the volt-second balance is achieved by a push-pull drive on the pulse transformer primary. This is especially useful if there are two secondary windings driving two HV400's out of phase such as in a half-bridge configuration

Other times it is more convenient to achieve volt-second balance by using capacitors to block DC in the primary and secondary windings as shown in Figure 2. The pin 7 diodes provide a path for discharging the secondary side DC blocking capacitor. Both capacitors, C_{IN} and C_S, should be at least 10 times the equivalent MOSFET gate capacitance.

The HV400 can be used as a current booster for low side switches by connecting directly to the PWM output. The circuit would be similar to the switching time test circuit.

It is worth restating that some consideration (and experimentation) should be given to the choice of external components, i.e. resistors, capacitors and diodes, to optimize performance in a given application.

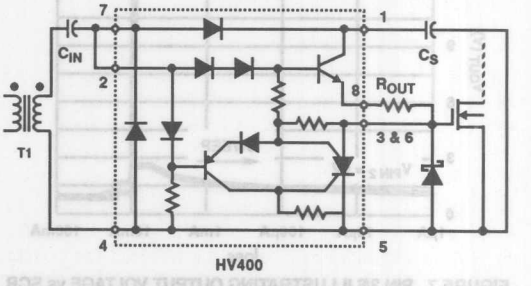


FIGURE 2. BIPOLAR DRIVE WITH DC BLOCKING CAPACITOR

Typical Performance Curves T_A = +25°C Unless Otherwise Specified

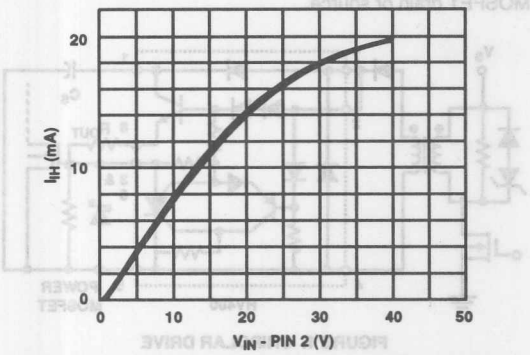


FIGURE 3. PIN 2 INPUT CURRENT vs INPUT VOLTAGE WITH ZERO OUTPUT CURRENT

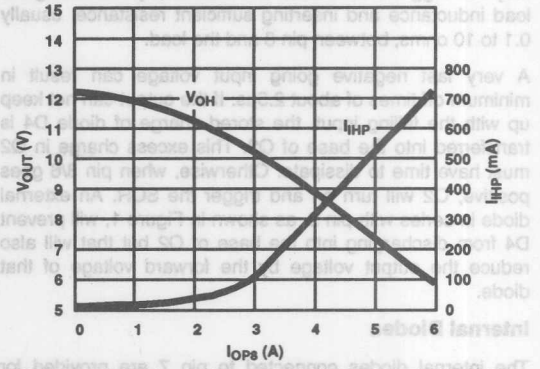


FIGURE 4. PIN 2 I_{IHP} & V_{OH} vs OUTPUT SOURCE CURRENT

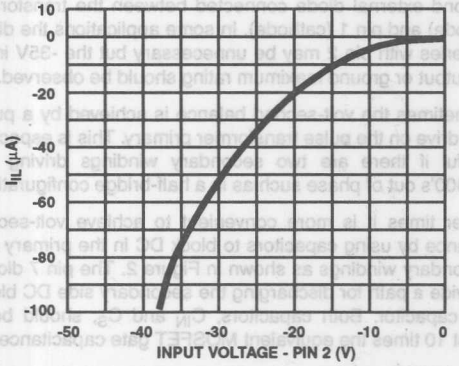


FIGURE 5. PIN 2 I_{IL} vs INPUT VOLTAGE



FIGURE 6. V_{OL} vs I_{OP6} (5µs PULSES)

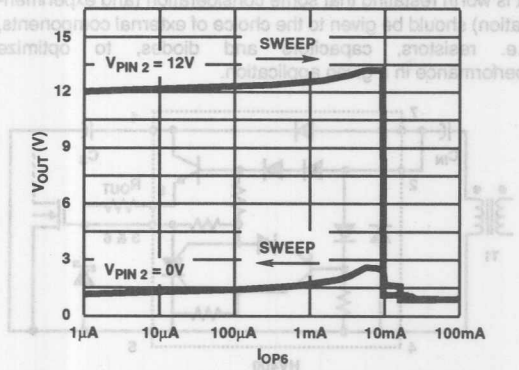


FIGURE 7. PIN 3/6 ILLUSTRATING OUTPUT VOLTAGE vs SCR OUTPUT SINK LATCHING AND HOLDING CURRENT

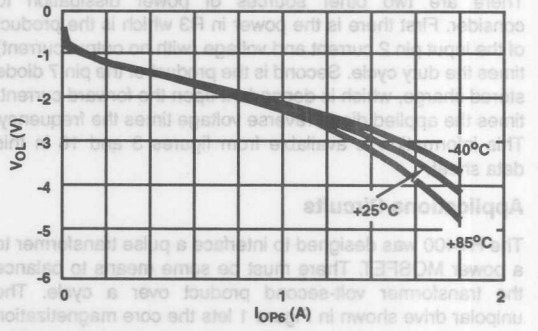


FIGURE 8. PIN 3/6 VOLTAGE vs REVERSE CURRENT 300µs PULSES

Typical Performance Curves T_A = +25°C Unless Otherwise Specified (Continued)

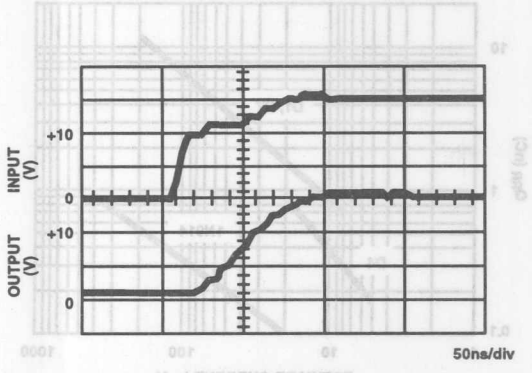


FIGURE 9. LOW TO HIGH TRANSIENT RESPONSE WAVEFORMS (C_L = 10nF)

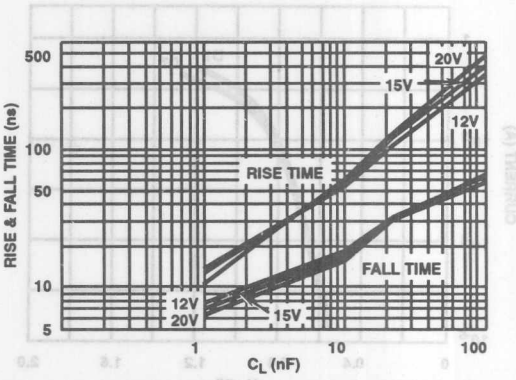


FIGURE 10. RISE & FALL TIMES vs C_L(V+ = 12V, 15V, 20V)

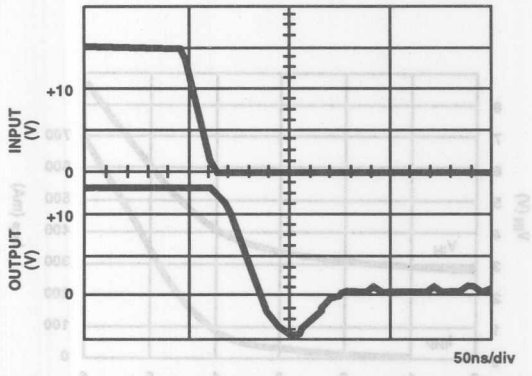


FIGURE 11. HIGH TO LOW TRANSIENT RESPONSE WAVEFORMS (C_L = 10nF)

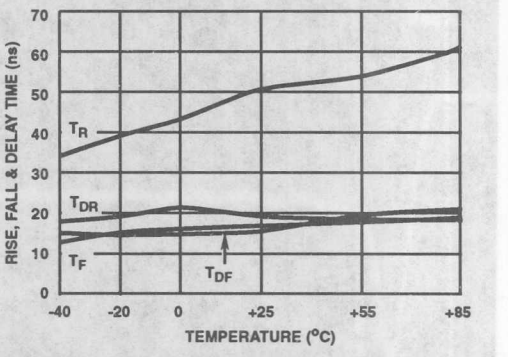


FIGURE 12. RISE, FALL & DELAY TIMES vs TEMPERATURE

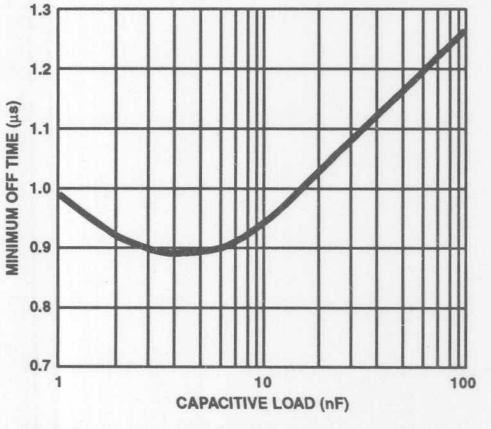


FIGURE 13. MINIMUM OFF TIME (T_{OR}) vs C_L AT +25°C

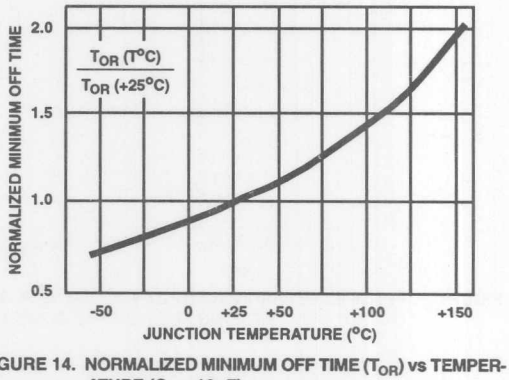


FIGURE 14. NORMALIZED MINIMUM OFF TIME (T_{OR}) vs TEMPERATURE (C_L = 10nF)

Typical Performance Curves T_A = +25°C Unless Otherwise Specified (Continued)

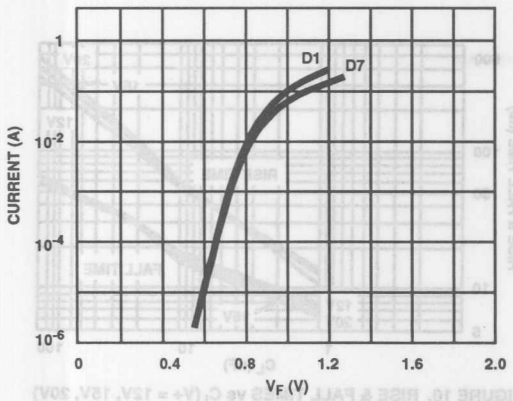


FIGURE 15. DIODE D1 & D7 CURRENT vs V_F

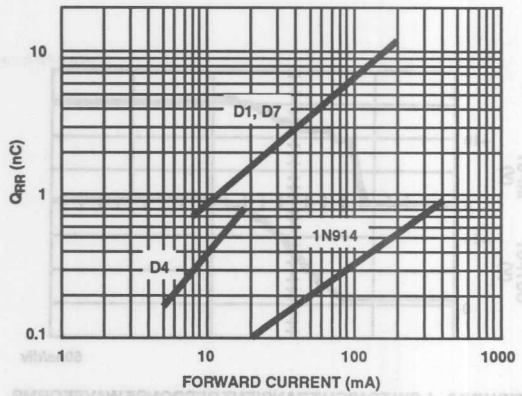
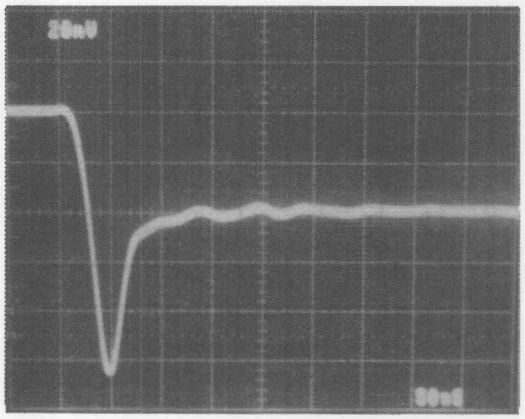


FIGURE 16. DIODE Q_{RR} vs FORWARD CURRENT



Vertical 100mA/div
Horizontal 50ns/div

FIGURE 17. DIODE D1 REVERSE RECOVERY WAVEFORM
I_F = 200mA, 20V REVERSE BIAS

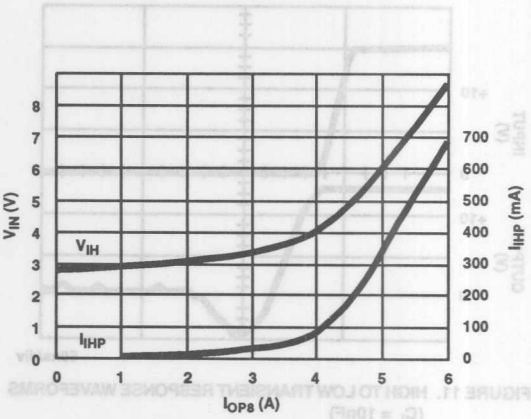


FIGURE 18. V_{IH} & I_{IHP} vs I_{OP8} [V_{OUT} (PIN 8) = 0, V+ = 15V, 1µs PULSE]

Metallization Topology

DIE DIMENSIONS:
66.9 x 71.65 x 19 mils
(1700 x 1820 x 483µm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

SUBSTRATE POTENTIAL (POWERED UP):
Unbiased

GLASSIVATION:
Type: Silox
Thickness: 12kÅ ± 2kÅ
Type: Nitride
Thickness: 3.5kÅ ± 2.5kÅ

TRANSISTOR COUNT: 3

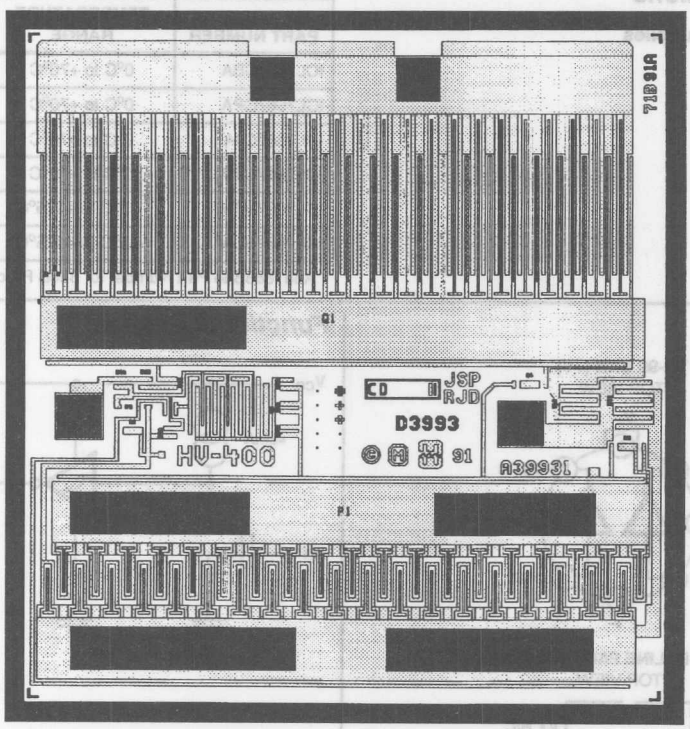
PROCESS: HFSB Linear Dielectric Isolation

Metallization Mask Layout

HV400Y

(8) SOURCE OUTPUT

(8) SOURCE OUTPUT



V+ (1)

INPUT (2)

SINK OUTPUT (3)

GROUND (4)

(7) DIODES

(6) SINK OUTPUT

(5) GROUND

NOTE: Pin Numbers Correspond to Mini-DIP and SOIC Packages Only.

Dual Power MOSFET Driver

Features

- **Fast Rise and Fall Times**
  - **30ns with 1000pF Load**
- **Wide Supply Voltage Range**
  - **V_{CC} = 4.5 to 15V**
- **Low Power Consumption**
  - **4mW with Inputs Low**
  - **20mW with Inputs High**
- **TTL/CMOS Input Compatible Power Driver**
  - **R_{OUT} = 7Ω Typ**
- **Direct Interface with Common PWM Control ICs**
- **Pin Equivalent to DS0026/DS0056; TSC426**

Typical Applications

- **Switching Power Supplies**
- **DC/DC Converters**
- **Motor Controllers**

Description

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters. The ICL7667's high current outputs minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitance. The ICL7667's input are TTL compatible and can be directly driven by common pulse-width modulation control ICs.

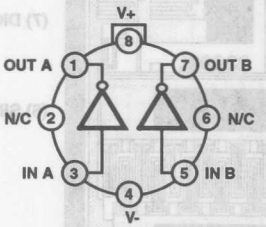
Order Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7667CBA	0°C to +70°C	8 Pin SOIC
ICL7667CPA	0°C to +70°C	8 Pin Plastic
ICL7667CJA	0°C to +70°C	8 Pin Ceramic DIP
ICL7667CTV	0°C to +70°C	TO-99 Can
ICL7667MTV*	-55°C to +125°C	TO-99 Can
ICL7667MJA*	-55°C to +125°C	8 Pin Ceramic DIP

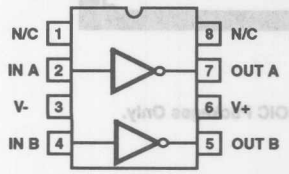
* Add /883B to Part Number for 883B Processing

Pinouts

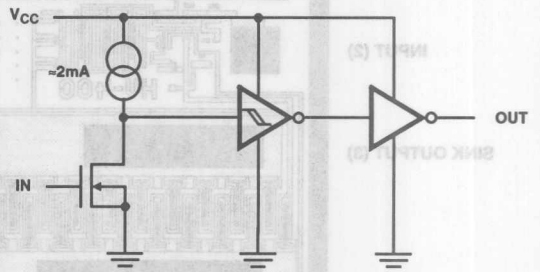
TO-99 CAN (TV)
TOP VIEW



8 LEAD DUAL-IN-LINE PACKAGE (PA, JA, BA)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
Copyright © Harris Corporation 1992

Absolute Maximum Ratings

Supply Voltage V+ to V- 15V
Input Voltage ..... V- -0.3V to V+ +0.3V
Package Dissipation, T_A +25°C 500mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Linear Derating Factors
TO-99 ..... 6.7mW/°C above 50°C
Plastic DIP Package ..... 5.6mW/°C above 36°C
Ceramic DIP Package ..... 6.7mW/°C above 50°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Temperature Range

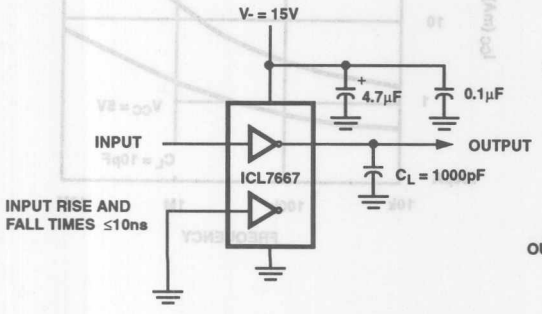
ICL7667C ..... 0°C to +70°C
ICL7667M ..... -55°C to +125°C

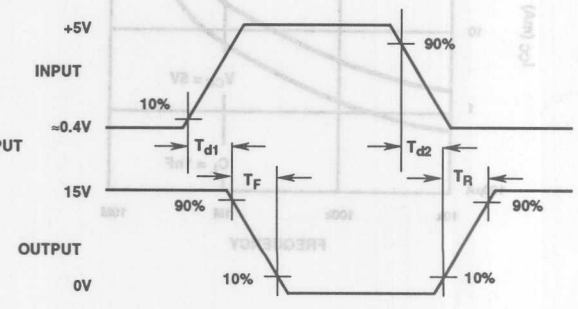
Electrical Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	ICL7667C, M T_A = +25°C			ICL7667M -55°C ≤ T_A ≤ +125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC SPECIFICATIONS									
Logic 1 Input Voltage	V_{IH}	V_{CC} = 4.5V	2.0	-	-	2.0	-	-	V
Logic 1 Input Voltage	V_{IH}	V_{CC} = 15V	2.0	-	-	2.0	-	-	V
Logic 0 Input Voltage	V_{IL}	V_{CC} = 4.5V	-	-	0.8	-	-	0.5	V
Logic 0 Input Voltage	V_{IL}	V_{CC} = 15V	-	-	0.8	-	-	0.5	V
Input Current	I_{IL}	V_{CC} = 15V, V_{IN} = 0V and 15V	-0.1	-	0.1	-0.1	-	0.1	µA
Output Voltage High	V_{OH}	V_{CC} = 4.5V and 15V	V_{CC} -0.05	V_{CC}	-	V_{CC} -0.1	-	-	V
Output Voltage Low	V_{OL}	V_{CC} = 4.5V and 15V	-	0	0.05	-	-	0.1	V
Output Resistance	R_{OUT}	V_{IN} = V_{IL}, I_{OUT} = -10mA, V_{CC} = 15V	-	7	10	-	-	12	Ω
Output Resistance	R_{OUT}	V_{IN} = V_{IH}, I_{OUT} = 10mA, V_{CC} = 15V	-	8	12	-	-	13	Ω
Power Supply Current	I_{CC}	V_{CC} = 15V, V_{IN} = 3V both inputs	-	5	7	-	-	8	mA
Power Supply Current	I_{CC}	V_{CC} = 15V, V_{IN} = 0V both inputs	-	150	400	-	-	400	µA
SWITCHING SPECIFICATIONS									
Delay Time	T_{D2}	Figure 3	-	35	50	-	-	60	ns
Rise Time	T_R	Figure 3	-	20	30	-	-	40	ns
Fall Time	T_F	Figure 3	-	20	30	-	-	40	ns
Delay Time	T_{D1}	Figure 3	-	20	30	-	-	40	ns

* NOTE: All typical values have been characterized but are not tested.

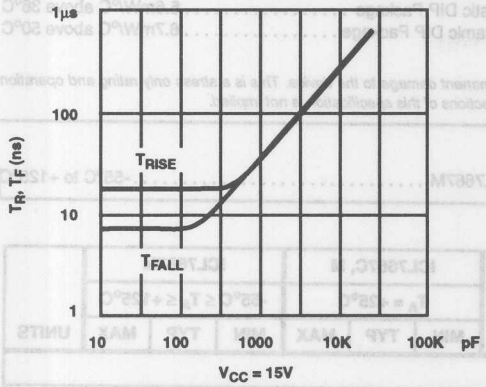
Test Circuits



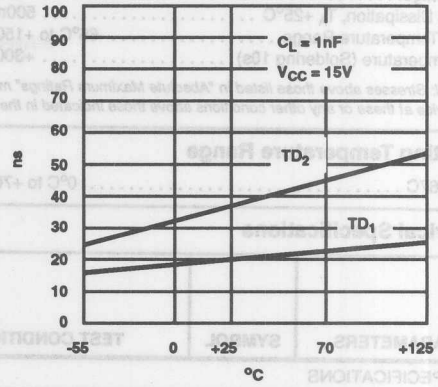


Typical Performance Characteristics

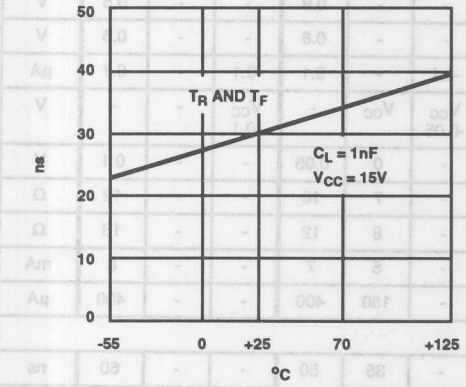
RISE AND FALL TIMES vs. C_L



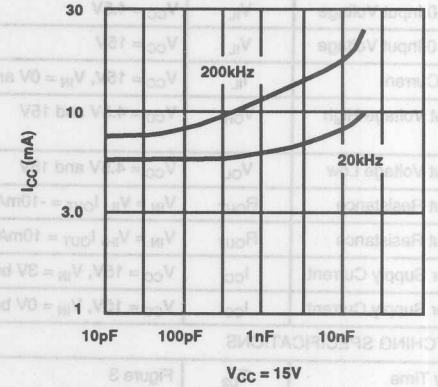
T_{D1}, T_{D2} vs. TEMPERATURE



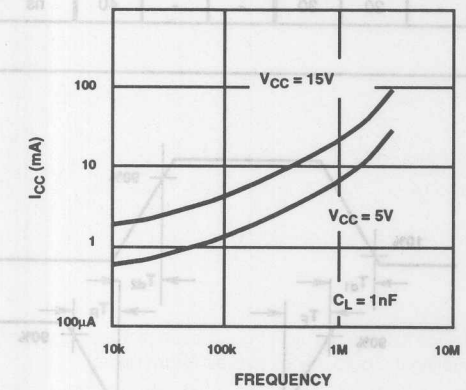
T_R, T_F vs. TEMPERATURE



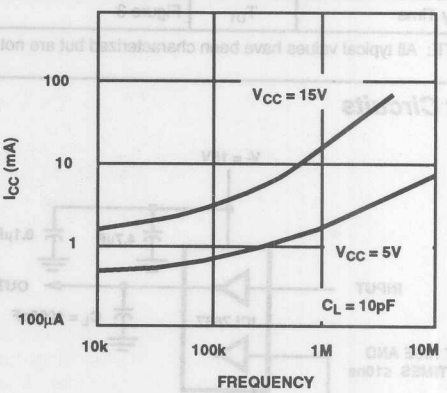
I_{CC} vs. C_L



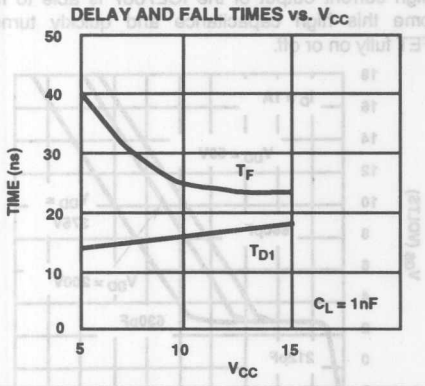
I_{CC} vs. FREQUENCY

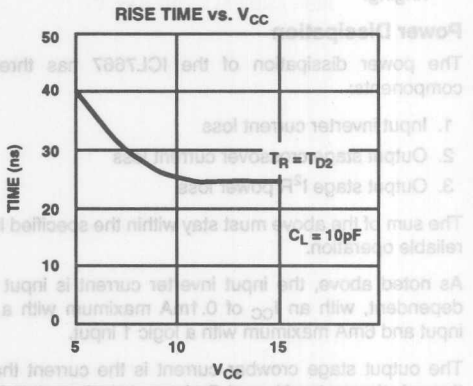


NO LOAD I_{CC} vs. FREQUENCY



Typical Performance Characteristics (Continued)





Detailed Description

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 15V. Its high output current enables it to rapidly charge and discharge the gate capacitance of power MOSFETs, minimizing the switching losses in switchmode power supplies. Since the output stage is CMOS, the output will swing to within millivolts of both ground and V_{CC} without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at V_{CC} = 15V, the propagation delays and specifications are almost independent of V_{CC}.

In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

Input Stage

The input stage is a large N-channel FET with a P-channel constant-current source. This circuit has a threshold of about 1.5V, relatively independent of the V_{CC} voltage. This means that the inputs will be directly compatible with TTL over the entire 4.5V - 15V V_{CC} range. Being CMOS, the inputs draw less than 1µA of current over the entire input voltage range of ground to V_{CC}. The quiescent current or no load supply current of the ICL7667 is affected by the input voltage, going to nearly zero when the inputs are at the 0 logic level and rising to 7mA maximum when both inputs are at the 1 logic level. A small amount of hysteresis, about 50mV to 100mV at the input, is generated by positive feedback around the second stage.

Output Stage

The ICL7667 output is a high-power CMOS inverter, swinging between ground and V_{CC}. At V_{CC} = 15V, the output impedance of the inverter is typically 7Ω. The high peak current capability of the ICL7667 enables it to drive a 1000pF load with a rise time of only 40ns. Because the output stage impedance is very low, up to 300mA will flow through the series N- and P-channel output devices (from V_{CC} to ground) during output transitions. This crossover current is responsible for a significant portion of the internal power dissipation of the ICL7667 at high frequencies. It can be minimized by keeping the rise and fall times of the input to the ICL7667 below 1µs.

Application Notes

Although the ICL7667 is simply a dual level-shifting inverter, there are several areas to which careful attention must be paid.

Grounding

Since the input and the high current output current paths both include the ground pin, it is very important to minimize and common impedance in the ground return. Since the ICL7667 is an inverter, any common impedance will generate negative feedback, and will degrade the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ICL7667 as is possible.

Bypassing

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A 4.7µF tantalum capacitor in parallel with a low inductance 0.1µF capacitor is usually sufficient bypassing.

Output Damping

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

1. Reduce inductance by making printed circuit board traces as short as possible.
2. Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
3. Use a 10Ω to 30Ω resistor in series with the output of the ICL7667. Although this reduces ringing, it will also slightly increase the rise and fall times.

components:

1. Input inverter current loss
2. Output stage crossover current loss
3. Output stage I^2R power loss

The sum of the above must stay within the specified limits for reliable operation.

As noted above, the input inverter current is input voltage dependent, with an I_{CC} of 0.1mA maximum with a logic 0 input and 6mA maximum with a logic 1 input.

The output stage crowbar current is the current that flows through the series N- and P-channel devices that form the output. This current, about 300mA, occurs only during output transitions. **Caution:** The inputs should never be allowed to remain between V_{IL} and V_{IH} since this could leave the output stage in a high current mode, rapidly leading to destruction of the device. If only one of the drivers is being used, be sure to tie the unused input to a ground. **NEVER** leave an input floating. The average supply current drawn by the output stage is frequency dependent, as can be seen in I_{CC} vs. Frequency graph in the Typical Characteristics Graphs.

The output stage I^2R power dissipation is nothing more than the product of the output current times the voltage drop across the output device. In addition to the current drawn by any resistive load, there will be an output current due to the charging and discharging of the load capacitance. In most high frequency circuits the current used to charge and discharge capacitance dominates, and the power dissipation is approximately

$$P_{AC} = CV_{CC}^2f$$

where C = Load Capacitance, f = Frequency

In cases where the load is a power MOSFET and the gate drive requirement are described in terms of gate charge, the ICL7667 power dissipation will be

$$P_{AC} = Q_GV_{CC}f$$

where Q_G = Charge required to switch the gate, in Coulombs,
f = Frequency.

Power MOS Driver Circuits

Power MOS Driver Requirements

Because it has a very high peak current output, the ICL7667 the at driving the gate of power MOS devices. The high current output is important since it minimizes the time the power MOS device is in the linear region. Figure 4 is a typical curve of charge vs. gate voltage for a power MOSFET. The flat region is caused by the Miller capacitance, where the drain-to-gate capacitance is multiplied by the voltage gain of the FET. This increase in capacitance occurs while the power MOSFET is in the linear

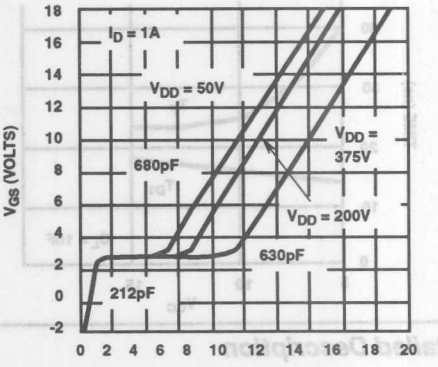


FIGURE 4: MOSFET GATE DYNAMIC CHARACTERISTICS

Direct Drive of MOSFETs

Figure 6 shows interfaces between the ICL7667 and typical switching regulator ICs. Note that unlike the DS0026, the ICL7667 does not need a dropping resistor and speedup capacitor between it and the regulator IC. The ICL7667, with its high slew rate and high voltage drive can directly drive the gate of the MOSFET. The 1527 IC is the same as the 1525 IC, except that the outputs are inverted. This inversion is needed since ICL7667 is an inverting buffer.

Transformer Coupled Drive of MOSFETs

Transformers are often used for isolation between the logic and control section and the power section of a switching regulator. The high output drive capability of the ICL7667 enables it to directly drive such transformers. Figure 6 shows a typical transformer coupled drive circuit. PWM ICs with either active high or active low output can be used in this circuit, since any inversion required can be obtained by reversing the windings on the secondaries.

Buffered Drivers for Multiple MOSFETs

In very high power applications which use a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge and discharge quickly. Figure 8 shows a circuit which works very well with very large capacitance loads. When the input of the driver is zero, Q1 is held in conduction by the lower half of the ICL7667 and Q2 is clamped off by Q1. When the input goes positive, Q1 is turned off and a current pulse is applied to the gate of Q2 by the upper half of the ICL7667 through the transformer, T1. After about 20ns, T1 saturates and Q2 is held on by its own C_{gs} and the bootstrap circuit of C1, D1 and R1. This bootstrap circuit may not be needed at frequencies greater than 10kHz since the input capacitance of Q2 discharges slowly.

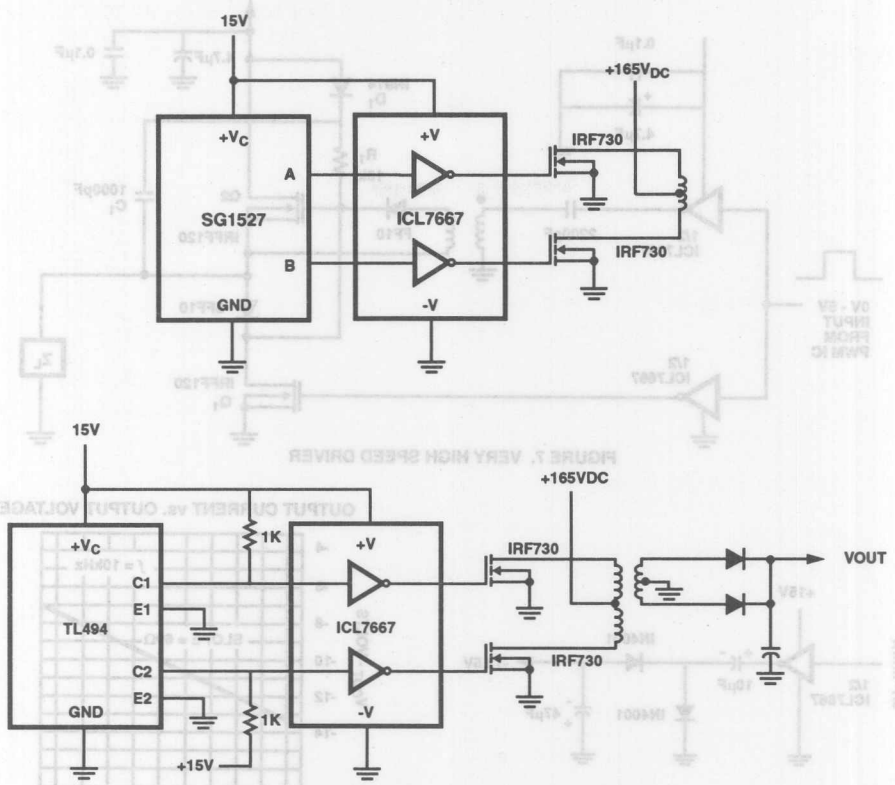


FIGURE 5. DIRECT DRIVE OF MOSFET GATES

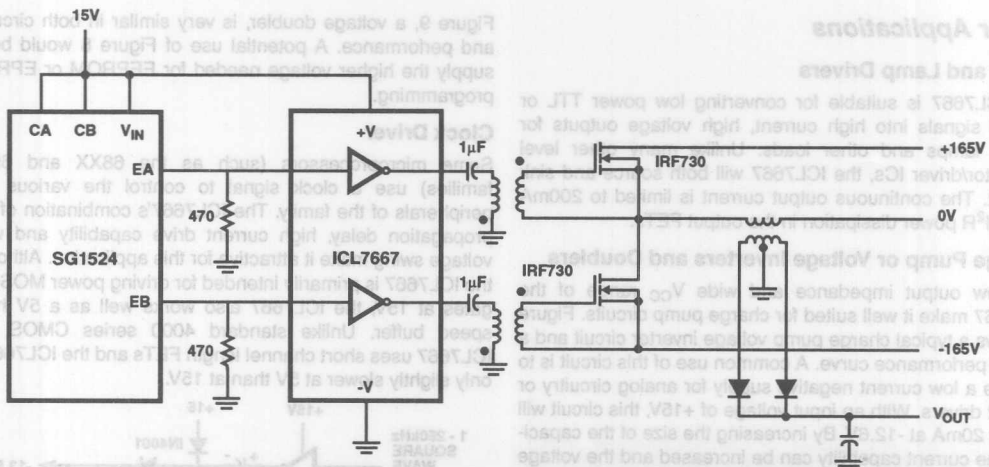


FIGURE 6. TRANSFORMER COUPLED DRIVE CIRCUIT

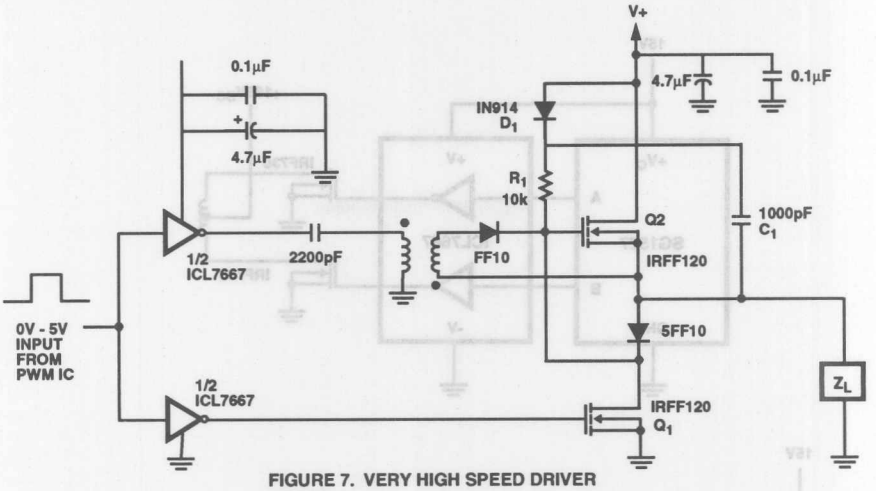


FIGURE 7. VERY HIGH SPEED DRIVER

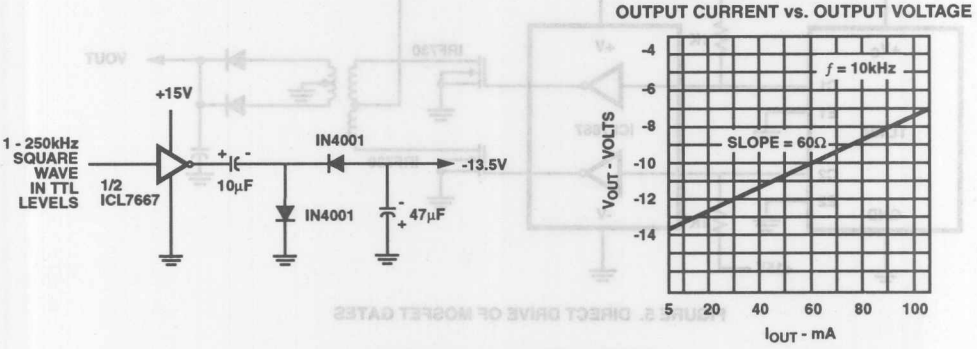


FIGURE 8. VOLTAGE INVERTER

Other Applications

Relay and Lamp Drivers

The ICL7667 is suitable for converting low power TTL or CMOS signals into high current, high voltage outputs for relays, lamps and other loads. Unlike many other level translator/driver ICs, the ICL7667 will both source and sink current. The continuous output current is limited to 200mA by the I^2R power dissipation in the output FETs.

Charge Pump or Voltage Inverters and Doublers

The low output impedance and wide V_{CC} range of the ICL7667 make it well suited for charge pump circuits. Figure 8 shows a typical charge pump voltage inverter circuit and a typical performance curve. A common use of this circuit is to provide a low current negative supply for analog circuitry or RS232 drivers. With an input voltage of +15V, this circuit will deliver 20mA at -12.6V. By increasing the size of the capacitors, the current capability can be increased and the voltage loss decreased. The practical range of the input frequency is 500Hz to 250kHz. As the frequency goes up, the charge pump capacitors can be made smaller, but the internal losses in the ICL7667 will rise, reducing the circuit efficiency.

Figure 9, a voltage doubler, is very similar in both circuitry and performance. A potential use of Figure 8 would be to supply the higher voltage needed for EEPROM or EPROM programming.

Clock Driver

Some microprocessors (such as the 68XX and 65XX families) use a clock signal to control the various LSI peripherals of the family. The ICL7667's combination of low propagation delay, high current drive capability and wide voltage swing make it attractive for this application. Although the ICL7667 is primarily intended for driving power MOSFET gates at 15V, the ICL7667 also works well as a 5V high-speed buffer. Unlike standard 4000 series CMOS, the ICL7667 uses short channel length FETs and the ICL7667 is only slightly slower at 5V than at 15V.

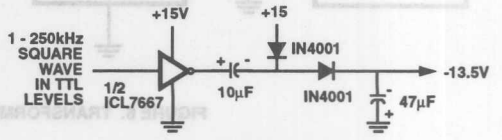


FIGURE 9. VOLTAGE DOUBLER

HARRIS SEMICONDUCTOR

SP600

May 1992

Half-Bridge 500V_{DC} Driver

Features

- Maximum Rating 500V
- Ability to Interface and Drive Standard and Current Sensing n-Channel Power MOSFET/IGBT Devices
- Creation and Management of a Floating Power Supply for Upper Rail Drive
- Simultaneous Conduction Lockout
- Overcurrent Protection
- Single Low Current Bias Supply Operation
- Latch Immune CMOS Logic
- Peak Drive in Excess of 0.5 Amp

Description

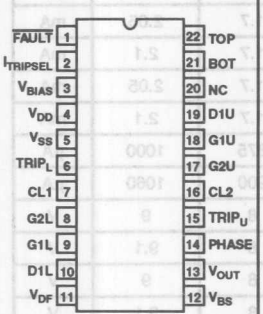
The SP600 is a smart power high voltage integrated circuit (HVIC) optimized to drive MOS gated power devices in half-bridge topologies. It provides the necessary control and management for PWM motor drive, power supply, and UPS applications.

Ordering Information

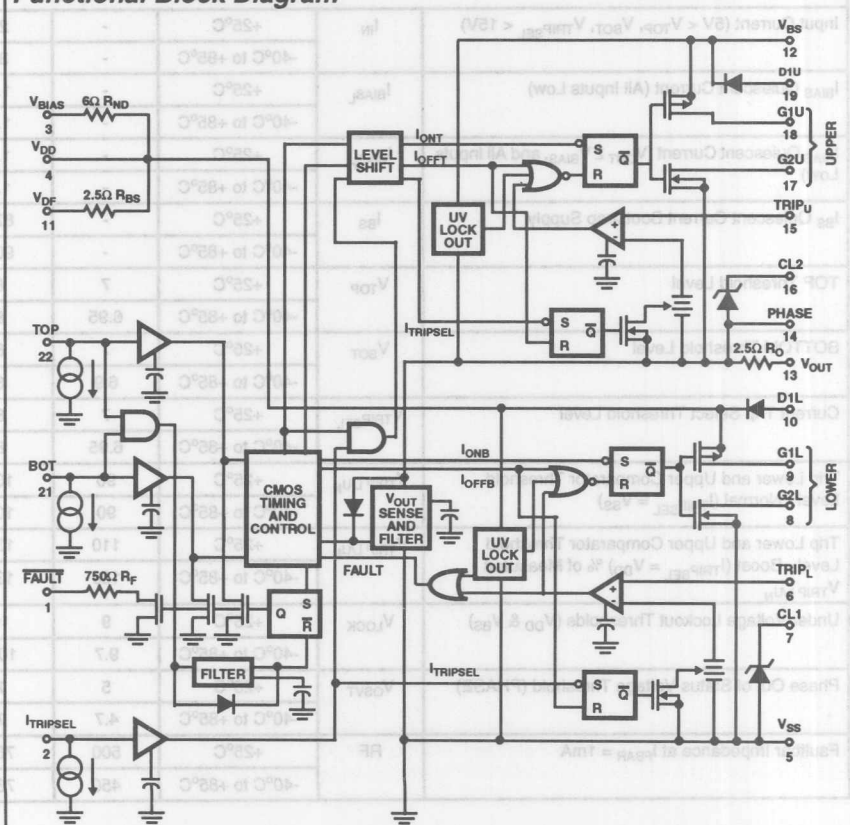
PART	TEMPERATURE	PACKAGE
SP600	-40°C to +85°C	22 Pin Plastic DIP

Pinout

22 PIN DIP
TOP VIEW



Functional Block Diagram



11 POWER DRIVERS AND SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2428.2**

Absolute Maximum Ratings

Full Temperature Range, All Voltage Referenced to V_{SS} Unless Otherwise Noted. Notes 1, 2.

Low Voltage Power Supply, V_{BIAS} (Note 1) . . . . . $18V_{DC}$
Floating Low Voltage Boot Strap . . . . . $18V_{DC}$
Power Supply to Phase, V_{BS}
Low Voltage Signal Pins
Fault, $I_{TRIP\ SEL}$, V_{DD}, $TRIP_L$, CL1, G2L . . . . . $-0.5V_{DC}$ to V_{DD} +0.5
G1L, D1L, V_{DF}, TOP, BOT
CL2, $TRIP_U$, G1U, G2U, D1U to Phase . . . . . -0.5_{VDC} to V_{BS}+0.5
High Voltage Pins
Phase, V_{PHASE} . . . . . $500V_{DC}$
(V_{BS}, V_{OUT}, $TRIP_U$, CL2, G2U & D1U: 0V-18V Higher Than Phase)
Dynamic High Voltage Rating Phase, ... 10,000V/µs
$DV_{PHASE/dt}$

Power Dissipation and Thermal Characteristics

Thermal Resistance, Junction-to-Ambient θ_{ja}
Plastic DIP Package 75°C/W
Maximum Package Power Dissipation at T_A = +85°C, P_O
Plastic DIP Package 500mW
Operating Ambient Temperature Range, T_A . . . . . -25°C to +85°C
Storage Temperature Range, T_S . . . . . -40°C to +150°C

NOTES:

1. Care must be taken in the application of V_{BIAS} as not to impose high peak dissipation demands on a relatively small metallized noise dropping resistor (R_{ND}). Prolonged high peak currents may result if $+15V_{DC}$ is applied abruptly and/or if the local bypass capacitor C_{DD} is large. It is suggested that C_{DD} be ≤ 10MFD. If it is desirable to switch the $15V_{DC}$ source or if a C_{DD} is larger, additional series impedance may be required.
2. Consult factory for additional package offerings.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

(V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, & V_{BS} Referenced to PHASE. DF: V_{DF} to V_{BS}, CF: V_{BS} to PHASE

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Input Current (5V < V_{TOP}, V_{BOT}, $V_{TRIP_{SEL}}$ < 15V)	I_{IN}	+25°C	-	20	30	µA
		-40°C to +85°C	-	30	33	µA
I_{BIAS} Quiescent Current (All Inputs Low)	I_{BIAS_L}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BIAS} Quiescent Current ($V_{OUT} \geq V_{BIAS}$, and All Inputs Low)	I_{BIAS_H}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BS} Quiescent Current Bootstrap Supply	I_{BS}	+25°C	-	875	1000	µA
		-40°C to +85°C	-	900	1060	µA
TOP Threshold Level	V_{TOP}	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
BOTTOM Threshold Level	V_{BOT}	+25°C	7	8	9	V
		-40°C to +85°C	6.9	8	9.1	V
Current Trip Select Threshold Level	$V_{TRIP_{SEL}}$	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
Trip Lower and Upper Comparator Threshold Level - Normal ($I_{TRIP_{SEL}} = V_{SS}$)	$V_{TRIP\ L/U_N}$	+25°C	90	105	125	mV
		-40°C to +85°C	90	105	127	mV
Trip Lower and Upper Comparator Threshold Level - Boost ($I_{TRIP_{SEL}} = V_{DD}$) % of Measured $V_{TRIP\ L/U_N}$	$V_{TRIP\ L/U_B}$	+25°C	110	130	150	%
		-40°C to +85°C	109	130	152	%
Under Voltage Lockout Thresholds (V_{DD} & V_{BS})	V_{LOCK}	+25°C	9	10	11.5	V
		-40°C to +85°C	9.7	10.5	11.8	V
Phase Out of Status Voltage Threshold (PHASE)	V_{OSVT}	+25°C	5	7	9	V
		-40°C to +85°C	4.7	7	9.6	V
Faultbar Impedance at I_{FBAR} = 1mA	RF	+25°C	500	760	1000	Ω
		-40°C to +85°C	450	760	1100	Ω

Electrical Specifications (V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, & V_{BS} Referenced to PHASE. DF: V_{DF} to V_{BS}, CF: V_{BS} to PHASE

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Upper/Lower Source Impedances (I_{Source} = 10mA)	$R_{SO\ L/U}$	+25°C	12	17	23	Ω
		-40°C to +85°C	7	17	29	Ω
Upper/Lower Sink Impedances (I_{SINK} = 10mA)	$R_{SI\ L/U}$	+25°C	8	12	16	Ω
		-40°C to +85°C	5	12	20	Ω
Bootstrap Supply Current Limiting Impedance	R_{BS}	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω
Noise Dropping Resistor Impedance	R_{ND}	+25°C	6	10	14	Ω
		-40°C to +85°C	5.4	10	14.6	Ω
High Voltage Leakage (500V V_{BS}, V_{OUT}, PHASE, $TRIP_U$, CL2, G1U, G2U, & D1U to V_{SS}. All other Pins at V_{SS})	I_{LK}	+25°C	-	1	3	µA
		-40°C to +85°C	-	1	3	µA
Miller Clamp Diodes; D1U and D1L (I_D = 10mA)	$V_{D1U/L}$	+25°C	1.05	1.4	1.7	V
		-40°C to +85°C	1.05	1.4	1.7	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 10mA)	$V_{CL2/1\text{-}Low}$	+25°C	6.35	6.61	6.85	V
		-40°C to +85°C	6.15	6.61	7.15	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 50mA)	$V_{CL2/1\text{-}High}$	+25°C	7.7	8.1	8.7	V
V_{OUT} Limiting Resistance	R_O	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω

NOTE: Maximum Steady State + 15V_{DC} Supply Current = I_{BIAS_L} + I_{BS}

Switching Characteristics (All Referenced to V_{ss}, Except: $Trip_u$, Cl2, G1u, G2u, And D1u Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE)

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Refresh One Shot Timer	t_{REF}	+25°C	200	350	500	µs
		-40°C to +85°C	180	350	540	µs
Delay Time of Trip I/u Voltage (I_{TRIP} sel. low) to G2U/G2L Low (50% Overdrive	$t_{OFF_{TN}}$	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Trip I Voltage (I_{TRIP} sel. low) to Faultbar Low	t_{FN}	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Phase Out of Status to Faultbar Low (TOP High)	t_{OSVF}	+25°C	500	700	900	ns
		-40°C to +85°C	400	700	1050	ns
Minimum Logic Input Pulse Width: TOP & BOTTOM	t_{MINIW}	+25°C	300	430	600	ns
		-40°C to +85°C	275	430	660	ns
Minimum G1U/G1L On Time	t_{ON}	+25°C	1.6	2.3	3.1	µs
		-40°C to +85°C	1.5	2.4	3.4	µs
Minimum Pulsed Off Time, G2U/G2L	t_{OFF}	+25°C	1.3	2.0	3.4	µs
		-40°C to +85°C	1.05	2.1	3.9	µs
Turn On Delay Time of G1U (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs
Turn On Delay Time of G1L (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs

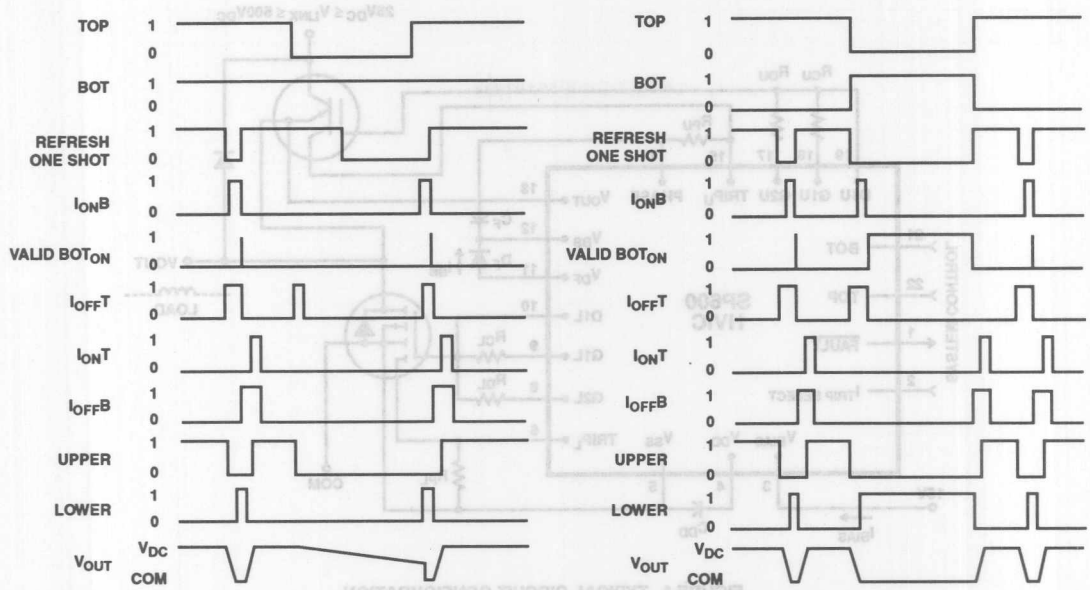
Switching Characteristics (All Referenced to V_{ss}, Except: $Trip_U$, Cl2, G1u, G2u, And D1u Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE) **(Continued)**

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Turn On Delay Time of G1U (TRISTATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn On Delay Time of G1L (TRISTATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn Off Delay Time of G2U and G2L	t_{OFF_D}	+25°C	0.75	1.0	1.45	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Minimum Dead Time: G1U off to G1L on, or G1L off to G1U on (BISTATE MODE)	$t_{D.T.}$	+25°C	1.5	2.5	3.5	µs
		-40°C to +85°C	1.2	2.6	4	µs
Fault Reset Delay to Clear Faultbar	$t_{R.T.}$	+25°C	3.4	4.5	6.6	µs
		-40°C to +85°C	3.15	4.8	7.4	µs
Rise Time of Upper & Lower Driver (Load = 2000pF)	$t_{R\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns
Fall Time of Upper & Lower Driver (Load = 2000pF)	$t_{F\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns

Recommended Operating Conditions and Functional Pin Description (All Voltages Referenced to V_{SS}, Unless Otherwise Noted. See Figure 1)

PARAMETER	CONDITION
Faultbar	Open Drain Fault Indicator Output
$I_{TRIP\ SELECT}$	Digital Input Command to Increase TRIP L and U Threshold by 30%
V_{BIAS}	14.5V to 16.5V with 15V nominal, ≅ 1.5mA DC BIAS Current
V_{DD}	C_{DD} to V_{SS}
V_{SS}	COMMON
Trip I	100mV Signal to Shut Off LOWER Drive and Trigger a Fault Output
CL1	Lower Noise Clamp Zener
G2L & G1L	Low Impedance Driver Designed to Drive Power MOS Transistors (LOWER)
V_{DF}	Current Limiting Charging Resistor for Bootstrap Capacitor Power Supply
V_{BS}	Bootstrap Supply, Normally a Diode Drop Below V_{DD} Voltage with Respect to the Floating PHASE Reference
V_{OUT}	Load Connection Node
Phase	Floating Reference Point for High Side Control Circuitry: V_{BS}, $TRIP_U$, CL2, G1U, G2U & D1U
$Trip_U$	100mV Signal, Referenced to PHASE, to Shut Off UPPER Drive
CL2	Upper Noise Clamp Zener
G2U & G1U	Low Impedance Driver Designed to Drive Power MOS Transistors (UPPER)
Top	Digital Input to Command the UPPER On
Bot	Digital Input to Command the LOWER On
D1U	Miller Clamp UPPER to V_{BS}
D1L	Miller Clamp LOWER to V_{DD}

Timing Diagram



TRISTATE MODE SLOWER THAN REFRESH ONE SHOT TIMER **BISTATE MODE SLOWER THAN REFRESH ONE SHOT TIMER**

NOTE: BOT switching not relevant.

Typical Circuit Configuration

TRUTH TABLE

Applicable to Typical Circuit Configuration (Figure 1)

INPUTS						OUTPUTS		
TOP	BOT	$TRIP_L$	$TRIP_U$	PHASE	V_{BIAS}	UPPER	LOWER	FAULT BAR
0	0	0	X	X	1	0	0	1
1	1	0	0	1	1	1	0	1
1	1	0	1	1	1	0	0	0
1	1	0	X	0	1	0	0	0
X	X	1	X	X	1	0	0	0
0	1	0	X	X	1	0	1	1
1	0	0	X	X	1	0	0	1
X	X	X	X	X	0	0	0	0

NOTE: 0 = False, 1 = True, X = Don't Care

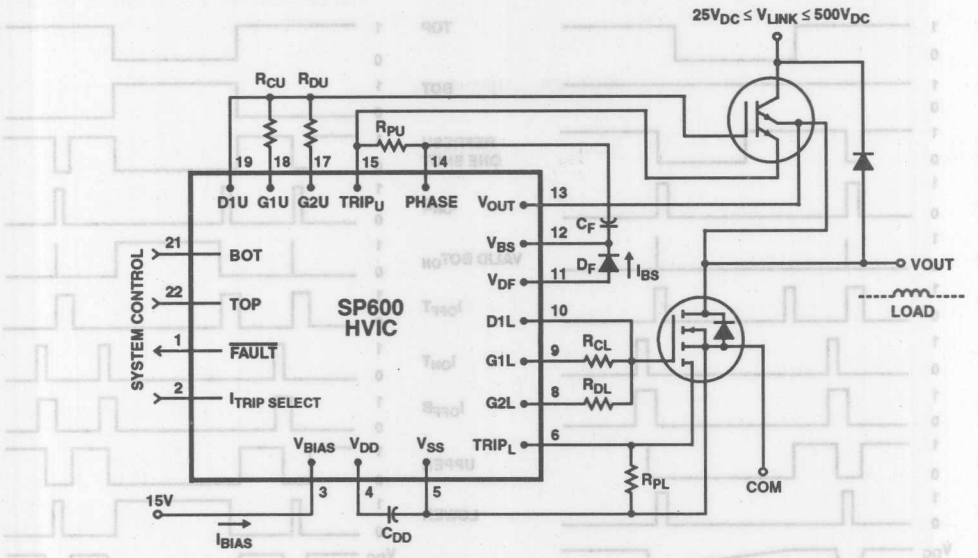


FIGURE 1. TYPICAL CIRCUIT CONFIGURATION

LEGEND		
Application Specific	R_{CU}	Upper Gate Charging Resistor
Application Specific	R_{DU}	Upper Gate Discharge Resistor
Application Specific	R_{PU}	Upper Current Pilot Resistor
Application Specific	R_{CL}	Lower Gate Charging Resistor
Application Specific	R_{DL}	Lower Gate Discharging Resistor
Application Specific	R_{PL}	Lower Current Pilot Resistor
3µF @ ≥ 15DC	C_{DD}	Local LV Filter Capacitor
0.22µF Ceramic X7R @ ≥ $15V_{DC}$	C_F	Flying Capacitor for Bootstrap Supply
Harris P/N A114M or Equiv PRV ≥ V_{LINK}	D_F	Flying Diode for Bootstrap Supply

Refer to 'Additional Product Offerings' for information concerning power output devices.

Functional Description

The SP600 provides a flexible, digitally controlled power function which is intended to be used as PWM drivers of n-channel MOSFETs and/or IGBTs for up to 240VAC line rectified totem-pole applications. The CMOS driveable inputs are filtered and captured by the control logic to determine the output state. The logic includes fixed timing to prohibit simultaneous conduction of the external power switches and, thru the V_{OUT} sense detector, verifies the output voltage state is in agreement with the controlled inputs. The > 11VDC floating power supply required to drive the upper rail external power device is created and managed by the HVIC through Cf and Df. This capacitor is refreshed from the V_{DD} supply each time V_{OUT} goes low. If the upper channel is commanded on for a long period of time, the bootstrap capacitor Cf is automatically refreshed by bringing V_{OUT} low. This is accomplished by turning off the upper rail MOSFET/IGBT, momentarily turning on the lower rail output device, followed by returning control back to the upper switch. Otherwise, Cf would gradually deplete its charge allowing the upper switch to come out of saturation. The upper and lower gate drivers allow for controlled charge and discharge rates as well as facilitate the use of nearly lossless current sensing power MOS devices. The over current trip level can be boosted 30% on a pulse by pulse basis by logic level '1' applied to $I_{TRIP\ SELECT}$. A $\overline{FAULT}$ output signal is generated when any of the following occurs:

V bias is low
Over current is detected
V phase doesn't agree with the input signal

Reset of $\overline{FAULT}$ is provided by externally removing power or by holding both TOP and BOT inputs low for the required reset time (trt_{MAX}).

Each application can be individually optimized by the selection of external components tailored to ensure proper overall system operation including:

Determining the ratings and sizing of MOSFETs and IGBTs, mixed or matched, as well as flyback diodes (FBD).

The selection of separate gate charge (R_C) & discharge (R_D) impedance chosen per the load capacitance, frequency of operation, and D_I/D_T dependent recovery characteristics of the associated FBDs. R_D should also be sized to prevent simultaneous bridge conduction by ensuring gate discharge in the allotted turn off pulse width ($t_{OFF\ MIN}$).

The selection of over current detection resistors (R_P), compatible with current sense MOSFETs/IGBTs or shunt(s) may be used.

For the floating bootstrap supply D_F & C_F must be determined. D_F must support the worse case system bus voltage and handle the charging currents of C_F. Proper selection should take into consideration T_{RR} and T_{FR} per the desired operating frequency. Proper selection of C_F is a trade off between the minimum t_{ON} time of the lower rail to charge up the capacitor, the amount of charge transfer required by the load, and cost. Due to automatic refresh the capacitor is replenished every 350µs TYP (or even sooner if input commands the TOP to switch at a faster repetition rate).

The local filter capacitor (C_{DD}) should be sized sufficiently large enough to transfer the charge to C_F without causing a significant droop in V_{DD}. As a rule of thumb it should be at least 10 times larger than C_F and be located adjacent to the V_{DD} and V_{SS} pins to minimize series resistance and inductance.

Refer to Application Note AN-8829 for more details about module operation and selection of external components.

HARRIS SEMICONDUCTOR

SP601

May 1992

Half-Bridge 500V$_{DC}$ Driver

Features

- Maximum Rating 500V
- Ability to Interface and Drive Standard and Current Sensing N-Channel Power MOSFET/IGBT Devices
- Creation and Management of a Floating Power Supply for Upper Rail Drive
- Simultaneous Conduction Lockout
- Overcurrent Protection
- Single Low Current Bias Supply Operation
- Latch Immune CMOS Logic
- Peak Drive in Excess of 0.5 Amp

Description

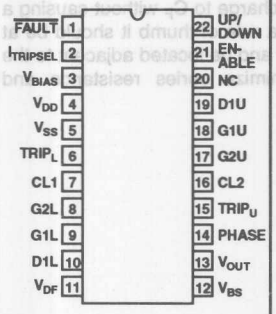
The SP601 is a smart power high voltage integrated circuit (HVIC) optimized to drive MOS gated power devices in half-bridge topologies. It provides the necessary control and management for PWM motor drive, power supply, and UPS applications.

Ordering Information

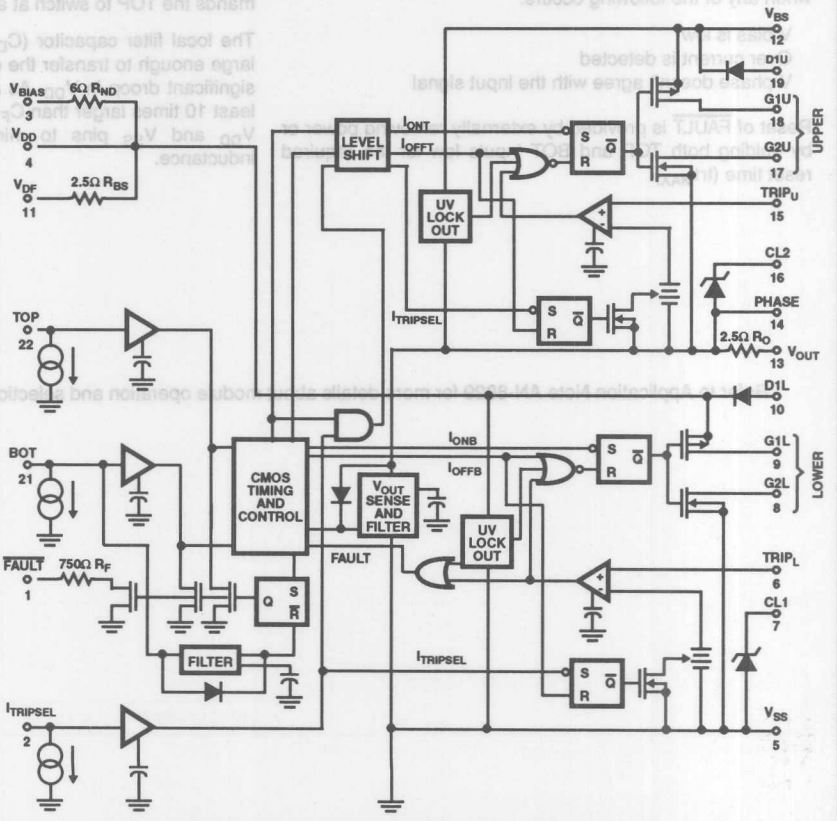
PART	TEMPERATURE	PACKAGE
SP601	-40°C to +85°C	22 Pin Plastic DIP

Pinout

22 PIN DIP
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2429.2**

Absolute Maximum Ratings

Full Temperature Range, All Voltage Referenced to V_{SS} Unless Otherwise Noted. Notes 1, 2.

Low Voltage Power Supply, V_{BIAS} (Note 1) ..... $18V_{DC}$
Floating Low Voltage Boot Strap Power Supply to Phase, V_{BS} ..... $18V_{DC}$
Low Voltage Signal Pins
Fault, $I_{TRIP\ SEL}$, V_{DD}, $TRIP_L$, CL1, G2L ..... $-0.5V_{DC}$ to V_{DD} +0.5
G1L, D1L, V_{DF}, TOP, BOT
CL2, $TRIP_U$, G1U, G2U, D1U to Phase ..... -0.5_{VDC} to V_{BS}+0.5
High Voltage Pins
Phase, V_{PHASE} ..... $500V_{DC}$
(V_{BS}, V_{OUT}, $TRIP_U$, CL2, G2U & D1U: 0V-18V Higher Than Phase)
Dynamic High Voltage Rating Phase, $DV_{PHASE/dt}$ 10,000V/µs

Power Dissipation and Thermal Characteristics

Thermal Resistance, Junction-to-Ambient θ_{ja}
Plastic DIP Package 75°C/W
Maximum Package Power Dissipation at T_A = +85°C, P_O
Plastic DIP Package 500mW
Operating Ambient Temperature Range, T_A ..... -25°C to +85°C
Storage Temperature Range, T_S ..... -40°C to +150°C

NOTES:
1. Care must be taken in the application of V_{BIAS} as not to impose high peak dissipation demands on a relatively small metallized noise dropping resistor (R_{ND}). Prolonged high peak currents may result if $+15V_{DC}$ is applied abruptly and/or if the local bypass capacitor C_{DD} is large. It is suggested that C_{DD} be ≤ 10MFD. If it is desirable to switch the $15V_{DC}$ source or if a C_{DD} is larger, additional series impedance may be required.
2. Consult factory for additional package offerings.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

(V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, & V_{BS} Referenced to PHASE. DF: V_{DF} to V_{BS}, CF: V_{BS} to PHASE

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Input Current (5V < V_{TOP}, V_{BOT}, $V_{TRIP_{SEL}}$ < 15V)	I_{IN}	+25°C	-	20	30	µA
		-40°C to +85°C	-	30	33	µA
I_{BIAS} Quiescent Current (All Inputs Low)	I_{BIAS_L}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BIAS} Quiescent Current ($V_{OUT} \geq V_{BIAS}$, and All Inputs Low)	I_{BIAS_H}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BS} Quiescent Current Bootstrap Supply	I_{BS}	+25°C	-	875	1000	µA
		-40°C to +85°C	-	900	1060	µA
ENABLE Threshold Level	V_{TOP}	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
UP/DN Threshold Level	V_{BOT}	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
Current Trip Select Threshold Level	$V_{TRIP_{SEL}}$	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
Trip Lower and Upper Comparator Threshold Level - Normal ($I_{TRIP_{SEL}}$ = V_{SS})	$V_{TRIP\ L/U_N}$	+25°C	90	105	125	mV
		-40°C to +85°C	90	105	127	mV
Trip Lower and Upper Comparator Threshold Level - Boost ($I_{TRIP_{SEL}}$ = V_{DD}) % of Measured $V_{TRIP\ L/U_N}$	$V_{TRIP\ L/U_B}$	+25°C	110	130	150	%
		-40°C to +85°C	109	130	152	%
Under Voltage Lockout Thresholds (V_{DD} & V_{BS})	V_{LOCK}	+25°C	9	10	11.5	V
		-40°C to +85°C	9.7	10.5	11.8	V
Phase Out of Status Voltage Threshold (PHASE)	V_{OSVT}	+25°C	5	7	9	V
		-40°C to +85°C	4.7	7	9.6	V
Faultbar Impedance at I_{FBAR} = 1mA	RF	+25°C	500	760	1000	Ω
		-40°C to +85°C	450	760	1100	Ω

Electrical Specifications .(V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, & V_{BS} Referenced to PHASE. DF: V_{DF} to V_{BS}, CF: V_{BS} to PHASE **(Continued)**

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Upper/Lower Source Impedances (I_{Source} = 10mA)	$R_{SO\ L/U}$	+25°C	12	17	23	Ω
		-40°C to +85°C	7	17	29	Ω
Upper/Lower Sink Impedances (I_{SINK} = 10mA)	$R_{SI\ L/U}$	+25°C	8	12	16	Ω
		-40°C to +85°C	5	12	20	Ω
Bootstrap Supply Current Limiting Impedance	R_{BS}	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω
Noise Dropping Resistor Impedance	R_{ND}	+25°C	6	10	14	Ω
		-40°C to +85°C	5.4	10	14.6	Ω
High Voltage Leakage (500V V_{BS}, V_{OUT}, PHASE, $TRIP_U$, CL2, G1U, G2U, & D1U to V_{SS}. All other Pins at V_{SS})	I_{LK}	+25°C	-	1	3	µA
		-40°C to +85°C	-	1	3	µA
Miller Clamp Diodes; D1U and D1L (I_D = 10mA)	$V_{D1U/L}$	+25°C	1.05	1.4	1.7	V
		-40°C to +85°C	1.05	1.4	1.7	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 10mA)	$V_{CL2/1\text{-}Low}$	+25°C	6.35	6.61	6.85	V
		-40°C to +85°C	6.15	6.61	7.15	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 50mA)	$V_{CL2/1\text{-}High}$	+25°C	7.7	8.1	8.7	V
V_{OUT} Limiting Resistance	R_O	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω

NOTE: Maximum Steady State + 15V_{DC} Supply Current = I_{BIAS_L} + I_{BS}

Switching Characteristics (All Referenced to V_{ss}, Except: $Trip_u$, Cl2, G1u, G2u, And D1u Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE)

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Refresh One Shot Timer	t_{REF}	+25°C	200	350	500	µs
		-40°C to +85°C	180	350	540	µs
Delay Time of Trip I/u Voltage (I_{TRIP} sel. low) to G2U/G2L Low (50% Overdrive	$t_{OFF\text{-}TN}$	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Trip I Voltage (I_{TRIP} sel. low) to Faultbar Low	t_{FN}	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Phase Out of Status to Faultbar Low (TOP High)	t_{OSVF}	+25°C	500	700	900	ns
		-40°C to +85°C	400	700	1050	ns
Minimum Logic Input Pulse Width: TOP & BOTTOM	t_{MINIW}	+25°C	300	430	600	ns
		-40°C to +85°C	275	430	660	ns
Minimum G1U/G1L On Time	t_{ON}	+25°C	1.6	2.3	3.1	µs
		-40°C to +85°C	1.5	2.4	3.4	µs
Minimum Pulsed Off Time, G2U/G2L	t_{OFF}	+25°C	1.3	2.0	3.4	µs
		-40°C to +85°C	1.05	2.1	3.9	µs
Turn On Delay Time of G1U (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs
Turn On Delay Time of G1L (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs

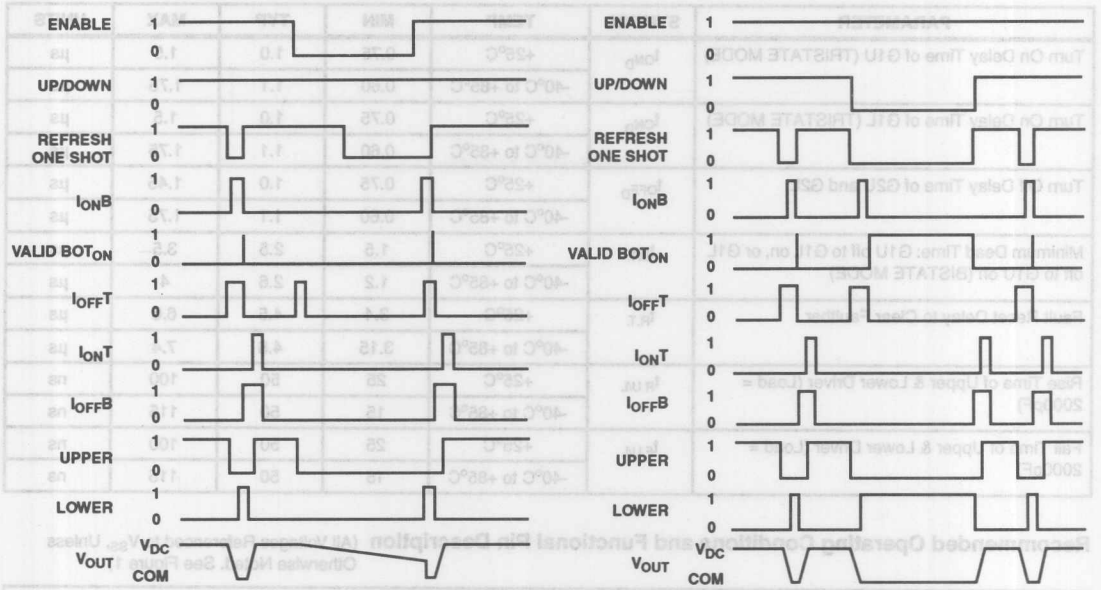
Switching Characteristics (All Referenced to V_{ss}, Except: $Trip_u$, Cl2, G1u, G2u, And D1u Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE) **(Continued)**

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Turn On Delay Time of G1U (TRISTATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn On Delay Time of G1L (TRISTATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn Off Delay Time of G2U and G2L	t_{OFF_D}	+25°C	0.75	1.0	1.45	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Minimum Dead Time: G1U off to G1L on, or G1L off to G1U on (BISTATE MODE)	$t_{D.T.}$	+25°C	1.5	2.5	3.5	µs
		-40°C to +85°C	1.2	2.6	4	µs
Fault Reset Delay to Clear Faultbar	$t_{R.T.}$	+25°C	3.4	4.5	6.6	µs
		-40°C to +85°C	3.15	4.8	7.4	µs
Rise Time of Upper & Lower Driver (Load = 2000pF)	$t_{R\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns
Fall Time of Upper & Lower Driver (Load = 2000pF)	$t_{F\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns

Recommended Operating Conditions and Functional Pin Description (All Voltages Referenced to V_{SS}, Unless Otherwise Noted. See Figure 1)

PARAMETER	CONDITION
Faultbar	Open Drain Fault Indicator Output
$I_{TRIP\ SELECT}$	Digital Input Command to Increase TRIP L and U Threshold by 30%
V_{BIAS}	14.5V to 16.5V with 15V nominal, ≅ 1.5mA DC BIAS Current
V_{DD}	C_{DD} to V_{SS}
V_{SS}	COMMON
Trip I	100mV Signal to Shut Off LOWER Drive and Trigger a Fault Output
CL1	Lower Noise Clamp Zener
G2L & G1L	Low Impedance Driver Designed to Drive Power MOS Transistors (LOWER)
V_{DF}	Current Limiting Charging Resistor for Bootstrap Capacitor Power Supply
V_{BS}	Bootstrap Supply, Normally a Diode Drop Below V_{DD} Voltage with Respect to the Floating PHASE Reference
V_{OUT}	Load Connection Node
Phase	Floating Reference Point for High Side Control Circuitry: V_{BS}, $TRIP_U$, CL2, G1U, G2U & D1U
$Trip_U$	100mV Signal, Referenced to PHASE, to Shut Off UPPER Drive
CL2	Upper Noise Clamp Zener
G2U & G1U	Low Impedance Driver Designed to Drive Power MOS Transistors (UPPER)
ENABLE	Digital Input to ENABLE the UP/DN Command to Turn on Top/Bottom Devices
UP/DN	Digital Input to Top/Bottom Device (If ENABLE is High)
D1U	Miller Clamp UPPER to V_{BS}
D1L	Miller Clamp LOWER to V_{DD}

Timing Diagram



TRISTATE MODE SLOWER THAN REFRESH ONE SHOT TIMER **BISTATE MODE SLOWER THAN REFRESH ONE SHOT TIMER**

NOTE: BOT switching not relevant.

Typical Circuit Configuration

TRUTH TABLE

Applicable to Typical Circuit Configuration (Figure 1)

INPUTS						OUTPUTS		
UP/DN	ENABLE	$TRIP_L$	$TRIP_U$	PHASE	V_{BIAS}	UPPER	LOWER	FAULT BAR
0	0	0	X	X	1	0	0	1
1	1	0	0	1	1	1	0	1
1	1	0	1	1	1	0	0	0
1	1	0	X	0	1	0	0	0
X	X	1	X	X	1	0	0	0
0	1	0	X	X	1	0	1	1
1	0	0	X	X	1	0	0	1
X	X	X	X	X	0	0	0	0

NOTE: 0 = False, 1 = True, X = Don't Care

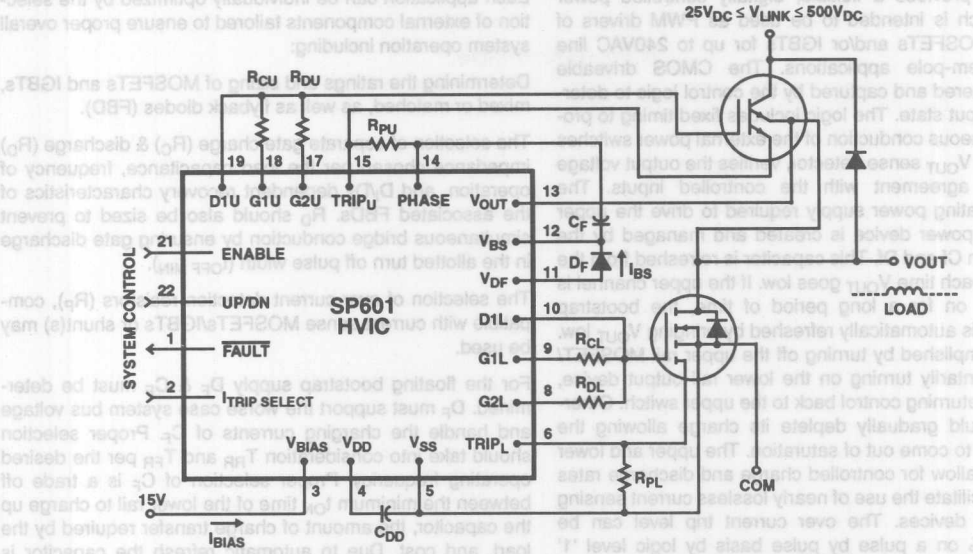


FIGURE 1. TYPICAL CIRCUIT CONFIGURATION

LEGEND		
Application Specific	R_{CU}	Upper Gate Charging Resistor
Application Specific	R_{DU}	Upper Gate Discharge Resistor
Application Specific	R_{PU}	Upper Current Pilot Resistor
Application Specific	R_{CL}	Lower Gate Charging Resistor
Application Specific	R_{DL}	Lower Gate Discharging Resistor
Application Specific	R_{PL}	Lower Current Pilot Resistor
3µF @ ≥ 15DC	C_{DD}	Local LV Filter Capacitor
0.22µF Ceramic X7R @ ≥ $15V_{DC}$	C_F	Flying Capacitor for Bootstrap Supply
Harris P/N A114M or Equiv PRV ≥ V_{LINK}	D_F	Flying Diode for Bootstrap Supply

Refer to 'Additional Product Offerings' for information concerning power output devices.

n-channel MOSFETs and/or IGBTs for up to 240VAC line rectified totem-pole applications. The CMOS driveable inputs are filtered and captured by the control logic to determine the output state. The logic includes fixed timing to prohibit simultaneous conduction of the external power switches and, thru the V_{OUT} sense detector, verifies the output voltage state is in agreement with the controlled inputs. The > 11VDC floating power supply required to drive the upper rail external power device is created and managed by the HVIC through Cf and Df. This capacitor is refreshed from the V_{DD} supply each time V_{OUT} goes low. If the upper channel is commanded on for a long period of time, the bootstrap capacitor Cf is automatically refreshed by bringing V_{OUT} low. This is accomplished by turning off the upper rail MOSFET/IGBT, momentarily turning on the lower rail output device, followed by returning control back to the upper switch. Otherwise, Cf would gradually deplete its charge allowing the upper switch to come out of saturation. The upper and lower gate drivers allow for controlled charge and discharge rates as well as facilitate the use of nearly lossless current sensing power MOS devices. The over current trip level can be boosted 30% on a pulse by pulse basis by logic level '1' applied to $I_{TRIP\ SELECT}$. A $\overline{FAULT}$ output signal is generated when any of the following occurs:

V bias is low
Over current is detected
V phase doesn't agree with the input signal

Reset of $\overline{FAULT}$ is provided by externally removing power or by holding the ENABLE input low for the required reset time (trt_{MAX}).

system operation including:

Determining the ratings and sizing of MOSFETs and IGBTs, mixed or matched, as well as flyback diodes (FBD).

The selection of separate gate charge (R_C) & discharge (R_D) impedance chosen per the load capacitance, frequency of operation, and D_I/D_T dependent recovery characteristics of the associated FBDs. R_D should also be sized to prevent simultaneous bridge conduction by ensuring gate discharge in the allotted turn off pulse width ($t_{OFF\ MIN}$).

The selection of over current detection resistors (R_P), compatible with current sense MOSFETs/IGBTs or shunt(s) may be used.

For the floating bootstrap supply D_F & C_F must be determined. D_F must support the worse case system bus voltage and handle the charging currents of C_F. Proper selection should take into consideration T_{RR} and T_{FR} per the desired operating frequency. Proper selection of C_F is a trade off between the minimum t_{ON} time of the lower rail to charge up the capacitor, the amount of charge transfer required by the load, and cost. Due to automatic refresh the capacitor is replenished every 350µs TYP (or even sooner if the UP/DN input switches at a faster repetition rate).

The local filter capacitor (C_{DD}) should be sized sufficiently large enough to transfer the charge to C_F without causing a significant droop in V_{DD}. As a rule of thumb it should be at least 10 times larger than C_F and be located adjacent to the V_{DD} and V_{SS} pins to minimize series resistance and inductance.

Refer to Application Note AN-8829 for more details about module operation and selection of external components.

POWER MOSFETs 12

ULTRA-FAST RECTIFIERS

DATA SHEETS		PAGE
MUR810, MUR815, MUR820 RUR810, RUR815, RUR820	8A High-Speed, High-Efficiency Epitaxial Silicon Rectifiers	12-3
MUR840, MUR850, MUR860 RUR840, RUR850, RUR860	8A High-Speed, High-Voltage, High-Efficiency Epitaxial Silicon Rectifiers	12-5
MUR870E/880E/890E/8100E RUR870/880/890/8100	8A Ultrafast Diode With Soft Recovery Characteristic	12-8
MUR1510/1515/1520 RUR1510/1515/1520	15A Ultrafast Diode With Soft Recovery Characteristic	12-11
MUR1540/1550/1560 RUR1540/1550/1560	15A Ultrafast Diode With Soft Recovery Characteristic	12-14
RUR1570, RUR1580 RUR1590, RUR15100	15A Ultrafast Diode With Soft Recovery Characteristic	12-17
RUR3010/3015/3020	30A Ultrafast Diode With Soft Recovery Characteristic	12-20
RUR3040/3050/3060	30A Ultrafast Diode With Soft Recovery Characteristic	12-23
RUR3070/3080/3090/30100	30A Ultrafast Diode With Soft Recovery Characteristic	12-26
RURD810/815/820	Dual 8A High-Speed, High-Efficiency Epitaxial Silicon Rectifiers	12-29
MUR1610CT, MUR1615CT, MUR1620CT, RUR1610CT, RUR1615CT, RUR1620CT	Dual 8A High-Speed, High-Efficiency Epitaxial Silicon Rectifiers	12-31
MUR3010PT, MUR3015PT, MUR3020PT, RURD1510, RURD1515, RURD1520	15A Ultrafast Dual Diode With Soft Recovery Characteristic	12-35
MUR3040PT, MUR3050PT, MUR3060PT, RURD1540, RURD1550, RURD1560	15A Ultrafast Dual Diode With Soft Recovery Characteristic	12-38
RURD1610/1615/1620	Dual 16A High-Speed, High-Efficiency Epitaxial Silicon Rectifiers	12-41
RURD3010/3015/3020	30A Ultrafast Dual Diode With Soft Recovery Characteristics	12-43
RURD3040/3050/3060	30A Ultrafast Dual Diode With Soft Recovery Characteristics	12-46

POWER MOSFETs 12

ULTRA-FAST RECTIFIERS

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MUR1540/1550/1560 RUR1540/1550/1560	15A Ultrafast Diode With Soft Recovery Characteristic	12-14
RUR1570, RUR1580 RUR1590, RUR15100	15A Ultrafast Diode With Soft Recovery Characteristic	12-17
RUR3010/3015/3020	30A Ultrafast Diode With Soft Recovery Characteristic	12-20
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MUR3040PT, MUR3050PT, MUR3060PT, RUR1540, RUR1550, RUR1560	15A Ultrafast Dual Diode With Soft Recovery Characteristic	12-38
RURD1610/1615/1620	Dual 16A High-Speed, High-Efficiency Epitaxial Silicon Rectifiers	12-41
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HARRIS

MUR810 RUR810
MUR815 RUR815
MUR820 RUR820

8A High-Speed, High-Efficiency Epitaxial Silicon Rectifiers

August 1991

Features

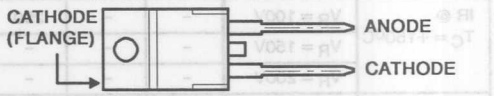
- Ultrafast Recovery Time (t_{rr} < 35ns)
- Low Forward Voltage
- Low Thermal Resistance
- Planar Design
- Wire-Bonded Construction

Applications

- General Purpose
- Power Switching Circuits to 100kHz
- Output Rectification in Switchng Power Supplies

Package

TO-220AC
TOP VIEW



Symbol



Description

MUR810, MUR815, MUR820 and RUR810, RUR815, RUR820 are low forward voltage drop ultrafast recovery rectifiers (t_{rr} < 35ns). They use a glass-passivated ion-implanted, epitaxial construction.

These devices are intended for use as output rectifiers and flywheel diodes in a variety of high-frequency pulse-width modulated switching regulators. Their low stored charge and attendant fast reverse-recovery behavior minimize electrical noise generation and in many circuits markedly reduce the turn-on dissipation of the associated power switching transistors.

All are supplied in TO-220AC packages.

Absolute Maximum Ratings (T_C = +25°C)

		MUR810 RUR810	MUR815 RUR815	MUR820 RUR820
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Average Rectified Forward Current				
T_A = 25°C (No Heat Sink)	$I_{F(AV)}$	3A	3A	3A
T_A = 25°C (With Heat Sink)*	$I_{F(AV)}$	8A	8A	8A
T_A = 150°C	$I_{F(AV)}$	8A	8A	8A
Nonrepetitive Peak Surge Current (8.3ms, ½ cycle)	I_{FSM}	100A	100A	100A
Operating and Storage Temperature	T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C
Maximum Lead Temperature During Solder (At distance > ⅛" (3.17mm) from case or 10s max)	T_L	260°C	260°C	260°C

*Wakefield type 295 heat sink with convection cooling.

12 ULTRA-FAST RECTIFIERS

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File Number 1355.2

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS									UNITS
		MUR810, RUR810			MUR815, RUR815			MUR820, RUR820			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 8A T_C = +150°C	–	–	0.83	–	–	0.83	–	–	0.85	V
	I_F = 8A T_C = +25°C	–	–	0.975	–	–	0.975	–	–	1	V
IR @ T_C = +150°C	V_R = 100V	–	–	250	–	–	–	–	–	–	µA
	V_R = 150V	–	–	–	–	–	250	–	–	–	µA
	V_R = 200V	–	–	–	–	–	–	–	–	250	µA
IR @ T_C = +25°C	V_R = 100V	–	–	5	–	–	–	–	–	–	µA
	V_R = 150V	–	–	–	–	–	5	–	–	–	µA
	V_R = 200V	–	–	–	–	–	–	–	–	5	µA
t_{rr}	I_F = 1A*	–	–	35	–	–	35	–	–	35	ns
$R_{\Theta jc}$		–	–	3	–	–	3	–	–	2	°C/W
$R_{\Theta ja}$		–	–	60	–	–	60	–	–	60	°C/W
C_J	V_R = 10V I_F = 0A	–	40	–	–	40	–	–	40	–	pF

*dI_F/dt = 40A/µs, I_{RM} (rec) < 1A, I_{RR} = 0.25A.

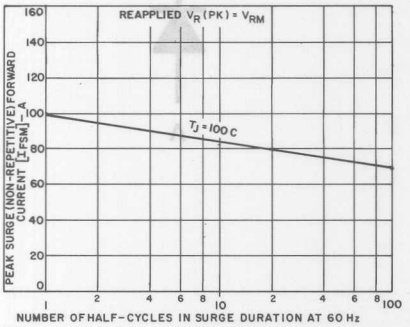


FIGURE 1. PEAK SURGE FORWARD CURRENT vs SURGE DURATION

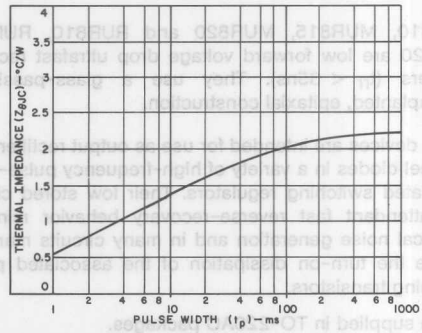


FIGURE 2. THERMAL IMPEDANCE vs PULSE WIDTH

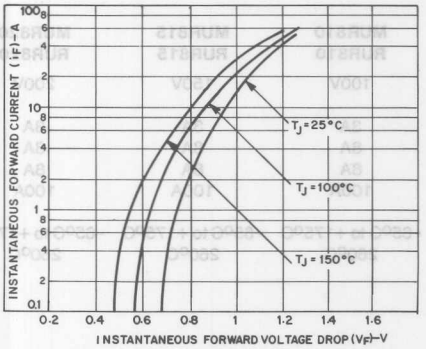


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

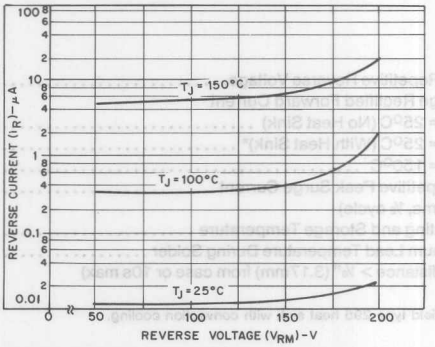


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

HARRIS

MUR840 RUR840
MUR850 RUR850
MUR860 RUR860

8A High-Speed, High-Voltage, High Efficiency Epitaxial Silicon Rectifiers

August 1991

Features

- Ultrafast Recovery Time (t_{rr} < 50ns)
- Low Forward Voltage
- Low Thermal Resistance
- Hard Glass Passivation
- Wire-Bonded Construction

Applications

- General Purpose
- Power Switching Circuits to 100kHz
- Output Rectification in Switchng Power Supplies

Description

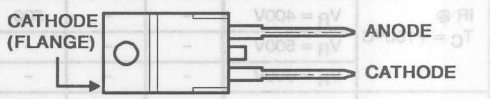
MUR840, MUR850, MUR860 and RUR840, RUR850, RUR860 are low forward voltage drop ultrafast recovery rectifiers (t_{rr} < 50ns). They use a glass-passivated ion-implanted, epitaxial construction.

These devices are intended for use as output rectifiers and flywheel diodes in a variety of high-frequency pulse-width modulated switching regulators. Their low stored charge and attendant fast reverse-recovery behavior minimize electrical noise generation and in many circuits markedly reduce the turn-on dissipation of the associated power switching transistors.

All are supplied in TO-220AC packages.

Package

TO-220AC
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		MUR840 RUR840	MUR850 RUR850	MUR860 RUR860
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage, V_{RWM} DC Blocking Voltage, V_R	V_{RRM}	400V	500V	600V
Average Rectified Forward Current Total Device, (Rated V_R), T_C = 150°C	$I_{F(AV)}$	8A	8A	8A
Peak Repetitive Forward Curent (Rated V_R, Square Wave, 20kHz), T_C = 150°C	I_{FM}	16A	16A	16A
Nonrepetitive Peak Surge Current (Surge Applied at Rated Load Conditions Halfwave, Single Phase, 60Hz)	I_{FSM}	100A	100A	100A
Operating and Storage Temperature	T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C
Maximum Lead Temperature During Solder (At distance > ⅛" (3.17mm) from case or 10s max)	T_L	260°C	260°C	260°C

12

ULTRA-FAST RECTIFIERS

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File Number 2091.1

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS									UNITS
		MUR840, RUR840			MUR850, RUR850			MUR860, RUR860			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 8A T_C = +150°C	–	–	1.0	–	–	1.2	–	–	1.2	V
	I_F = 8A T_C = +25°C	–	–	1.3	–	–	1.5	–	–	1.5	V
IR @ T_C = +150°C	V_R = 400V	–	–	500	–	–	–	–	–	–	µA
	V_R = 500V	–	–	–	–	–	500	–	–	–	µA
	V_R = 600V	–	–	–	–	–	–	–	–	500	µA
IR @ T_C = +25°C	V_R = 400V	–	–	10	–	–	–	–	–	–	µA
	V_R = 500V	–	–	–	–	–	10	–	–	–	µA
	V_R = 600V	–	–	–	–	–	–	–	–	10	µA
t_{rr}	I_F = 1A*	–	–	60	–	–	60	–	–	60	ns
	I_F = 0.5**	–	–	50	–	–	50	–	–	50	ns
$R_{\Theta jc}$		–	–	2	–	–	2	–	–	2	°C/W

*dI_F/dt = 50A/µs

**I_R =1.0A, I_{REC} = 0.25A.

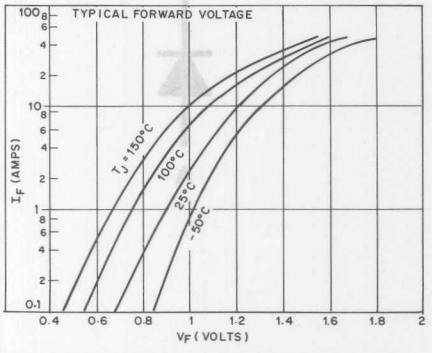


FIGURE 1. TYPICAL FORWARD VOLTAGE (MUR840, RUR840)

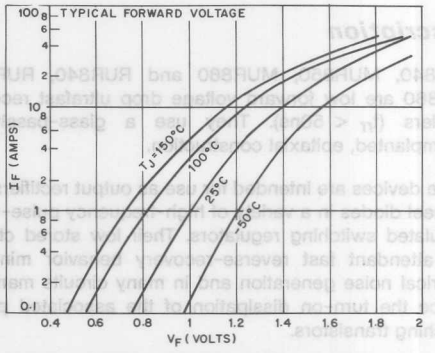


FIGURE 2. TYPICAL FORWARD VOLTAGE (MUR850, MUR860, RUR850, AND RUR860)

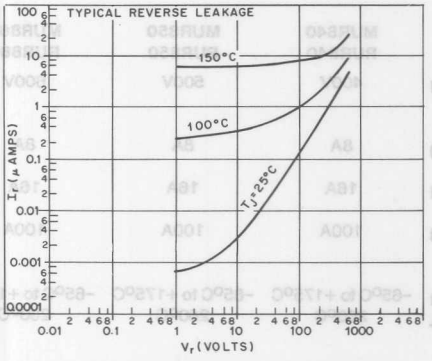


FIGURE 3. TYPICAL REVERSE LEAKAGE (MUR840, RUR840)

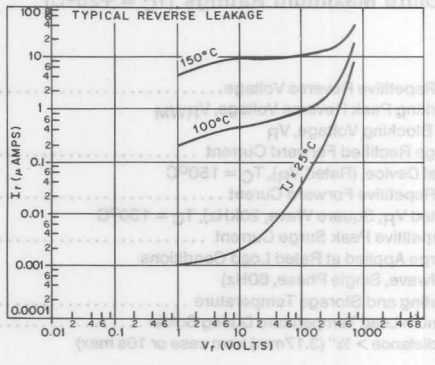


FIGURE 4. TYPICAL REVERSE LEAKAGE (MUR850, MUR860, RUR850, AND RUR860)

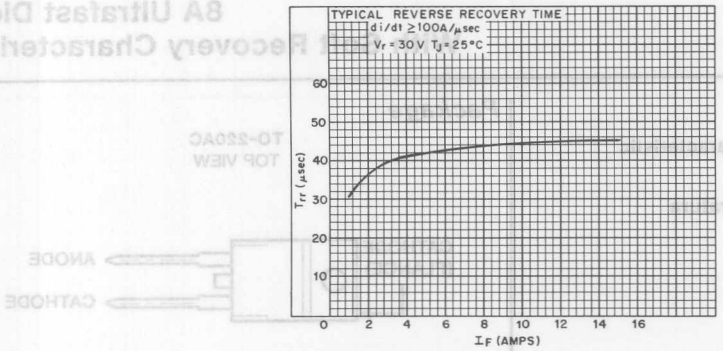


FIGURE 5. TYPICAL REVERSE RECOVERY TIME (ALL TYPES)

HARRIS

MUR870E, MUR880E, MUR890E MUR8100E, RUR870, RUR880 RUR890, RUR8100

8A Ultrafast Diode With Soft Recovery Characteristic

May 1991

Features

- Ultrafast with Soft Recovery Characteristic (t_{rr} < 75ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 1000V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

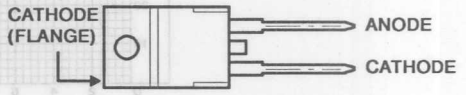
MUR870E, MUR880E, MUR890E, MUR8100E and RUR870, RUR880, RUR890, RUR8100 are ultrafast dual diodes (t_{rr} < 75ns) with soft recovery characteristics ($t_a/t_b \approx 0.5$). They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

All are supplied in TO-220AC packages.

Package

TO-220AC
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

	MUR870E RUR870	MUR880E RUR880	MUR890E RUR890	MUR8100E RUR8100
Peak Repetitive Reverse Voltage ..... V_{RRM}	700V	800V	900V	1000V
Working Peak Reverse Voltage ..... V_{RWM}	700V	800V	900V	1000V
DC Blocking Voltage ..... V_R	700V	800V	900V	1000V
Average Rectified Forward Current ..... $I_{F(AV)}$ (Total device forward current at rated V_R and T_C = 150°C)	8A	8A	8A	8A
Peak Forward Repetitive Current ..... I_{FRM} (Rated V_R, square wave 20kHZ)	16A	16A	16A	16A
Nonrepetitive Peak Surge Current ..... I_{FSM} (Surge applied at rated load condition halfwave 1phase 60Hz)	100A	100A	100A	100A
Operating and Storage Temperature ..... T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

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File Number 2780.1

Electrical Characteristics At Case Temperature (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS												UNITS
		MUR870E, RUR870			MUR880E, RUR880			MUR890E, RUR890			MUR8100E, RUR8100			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 8A T_C = +150°C			1.50			1.50			1.50			1.50	V
	I_F = 8A T_C = +25°C			1.80			1.80			1.80			1.8	V
IR @ T_C = +150°C	V_R = 700V			500										µA
	V_R = 800V						500							µA
	V_R = 900V									500				µA
	V_R = 1000V												500	µA
IR @ T_C = +25°C	V_R = 700V			25										µA
	V_R = 500V						25							µA
	V_R = 600V									25				µA
	V_R = 1000V												25	µA
t_{rr}	I_F = 1A			100			100			100			100	ns
	I_F = 8A			110			110			110			110	ns
t_a	I_F = 1A		40			40			40			40		ns
	I_F = 8A		45			45			45			45		ns
t_b	I_F = 1A		20			20			20			20		ns
	I_F = 8A		20			20			20			20		ns
$R_{\Theta jc}$				2.0			2.0			2.0			2.0	°C/W
W_{avl}	see Fig. 7&8			20			20			20			20	mj

Definitions

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current (pw = 300µs, D = 2%).

t_{rr} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_a + t_b$.

t_a = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM}. (See Figure 2)

$R_{\Theta jc}$ = Thermal resistance junction to case.

W_{avl} = Controlled avalanche energy (See Figures 7 & 8).

pw = pulse width.

D = duty cycle.

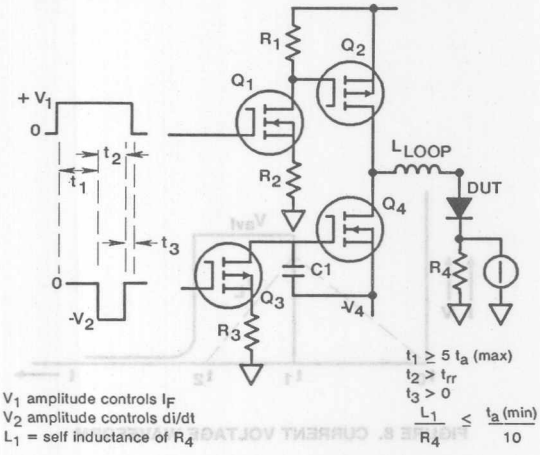


FIGURE 1. t_{rr} TEST CIRCUIT

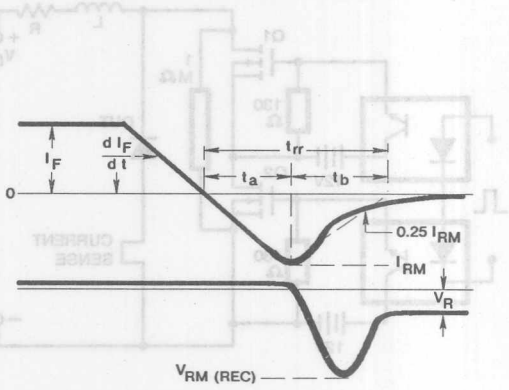


FIGURE 2. DEFINITIONS OF t_{rr}, t_a AND t_b

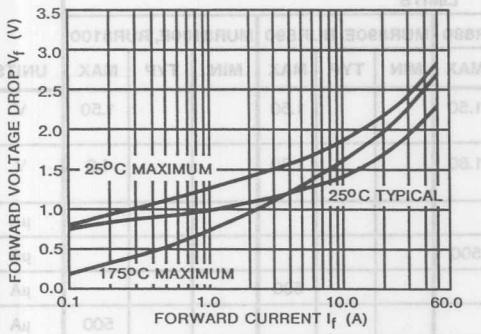


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

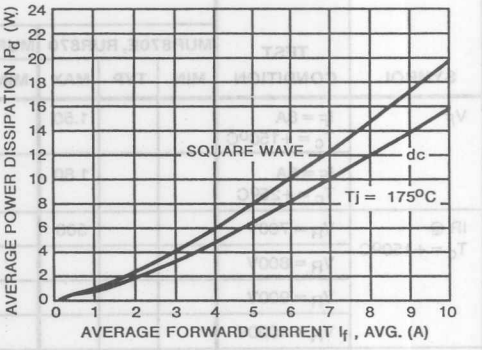


FIGURE 4. AVERAGE FORWARD CURRENT vs AVERAGE POWER DISSIPATION

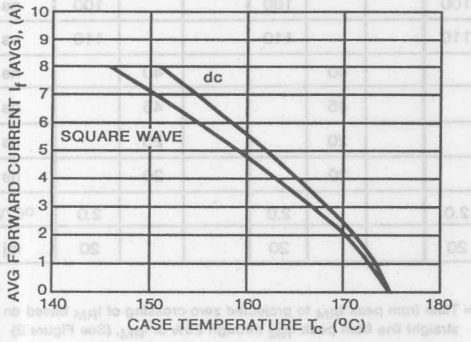


FIGURE 5. AVERAGE FORWARD CURRENT vs CASE TEMPERATURE

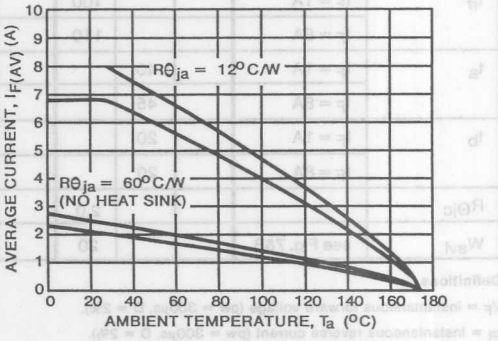


FIGURE 6. AVERAGE FORWARD CURRENT vs AMBIENT TEMPERATURE

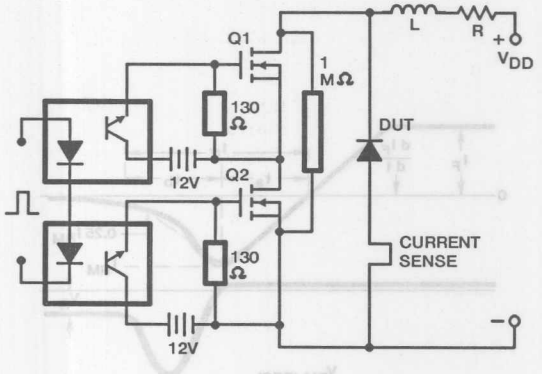


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

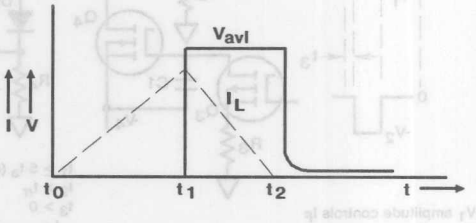


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L peak$ = 1A, L = 40mH, R < 0.1Ω, $W_{avl} = (1/2)\ LI^2[V_{avl}/(V_{avl}-V_{dd})]$

HARRIS

MUR1510 RUR1510
MUR1515 RUR1515
MUR1520 RUR1520

15A Ultrafast Diode With Soft Recovery Characteristic

May 1991

Features

- Ultrafast with Soft Recovery Characteristic (t_{rr} < 30ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 200V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

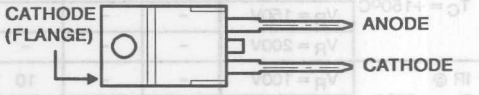
MUR1510, MUR1515, MUR1520 and RUR1510, RUR1515, RUR1520 are ultrafast dual diodes (t_{rr} < 30ns) with soft recovery characteristics ($t_a/t_b \approx 1$). They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

All are supplied in TO-220AC packages.

Package

TO-220AC
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		MUR1510 RUR1510	MUR1515 RUR1515	MUR1520 RUR1520
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Working Peak Reverse Voltage	V_{RWM}	100V	150V	200V
DC Blocking Voltage	V_R	100V	150V	200V
Average Rectified Forward Current (Total device forward current at rated V_R and T_C = 150°C)	$I_{F(AV)}$	15A	15A	15A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHZ)	I_{FRM}	30A	30A	30A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1phase 60Hz)	I_{FSM}	200A	200A	200A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

12

ULTRA-FAST RECTIFIERS

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File Number **2779.1**

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS									UNITS
		MUR1510, RUR1510			MUR1515, RUR1515			MUR1520, RUR1520			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A T_C = +150°C	–	–	0.85	–	–	0.85	–	–	0.85	V
	I_F = 15A T_C = +25°C	–	–	1.05	–	–	1.05	–	–	1.05	V
IR @ T_C = +150°C	V_R = 100V	–	–	500	–	–	–	–	–	–	µA
	V_R = 150V	–	–	–	–	–	500	–	–	–	µA
	V_R = 200V	–	–	–	–	–	–	–	–	500	µA
IR @ T_C = +25°C	V_R = 100V	–	–	10	–	–	–	–	–	–	µA
	V_R = 150V	–	–	–	–	–	10	–	–	–	µA
	V_R = 200V	–	–	–	–	–	–	–	–	10	µA
t_{rr}	I_F = 1A	–	–	30	–	–	30	–	–	30	ns
	I_F = 15A	–	–	35	–	–	35	–	–	35	ns
t_a	I_F = 1A	–	18	–	–	18	–	–	18	–	ns
	I_F = 15A	–	20	–	–	20	–	–	20	–	ns
t_b	I_F = 1A	–	9	–	–	9	–	–	9	–	ns
	I_F = 15A	–	10	–	–	10	–	–	10	–	ns
$R_{\Theta jc}$		–	–	1.5	–	–	1.5	–	–	1.5	°C/W
W_{avl}	see Fig. 7&8	–	–	20	–	–	20	–	–	20	mj

Definitions

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current (pw = 300µs, D = 2%).

t_{rr} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of t_a + t_b.

t_a = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

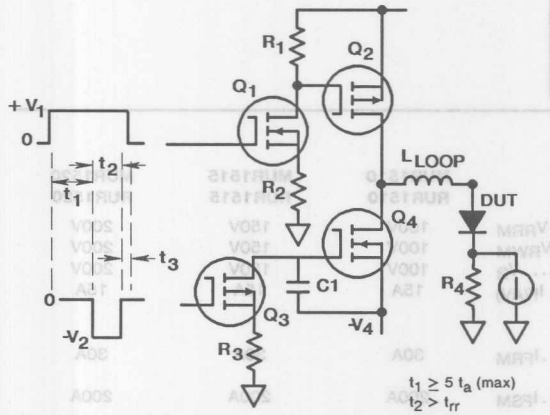
t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM}. (See Figure 2)

$R_{\Theta jc}$ = Thermal resistance junction to case.

W_{avl} = Controlled avalanche energy (See Figures 7 & 8).

pw = pulse width.

D = duty cycle.



V_1 amplitude controls I_F
V_2 amplitude controls di/dt
L_1 = self inductance of R_4

FIGURE 1. t_{rr} TEST CIRCUIT

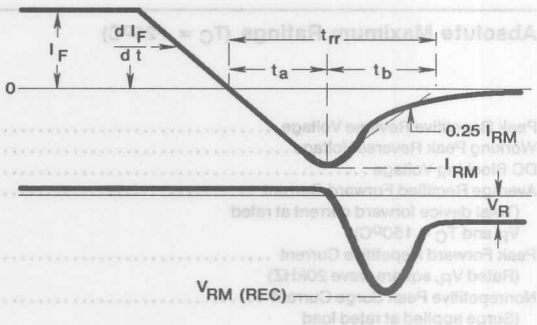


FIGURE 2. DEFINITIONS OF t_{rr}, t_a AND t_b

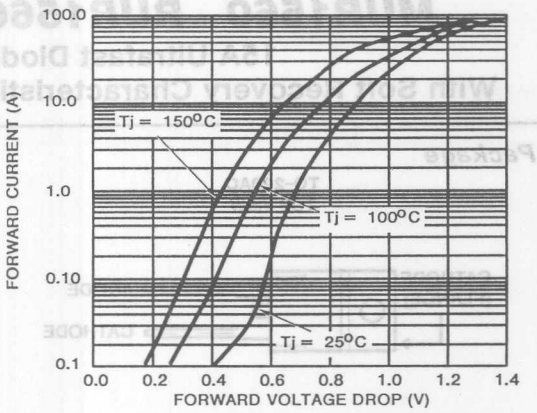


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

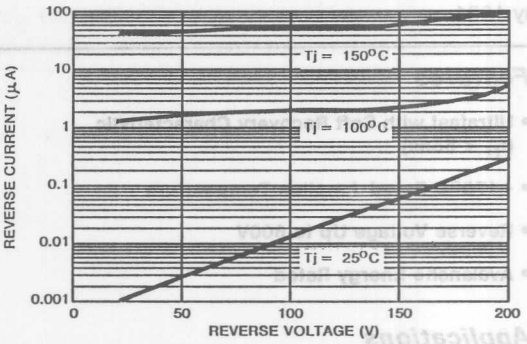


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

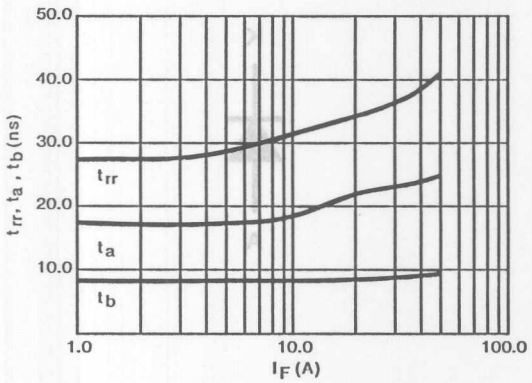


FIGURE 5. TYPICAL t_{rr}, t_a, t_b vs FORWARD CURRENT

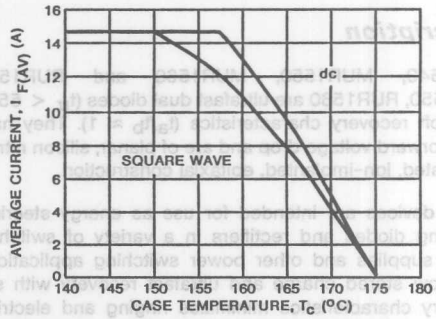


FIGURE 6. TYPICAL CURRENT DERATING CURVE w.r.t. CASE TEMPERATURE

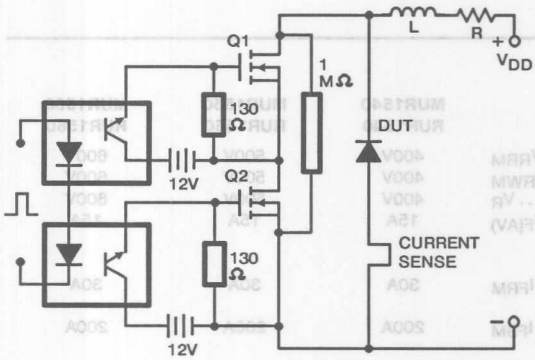


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

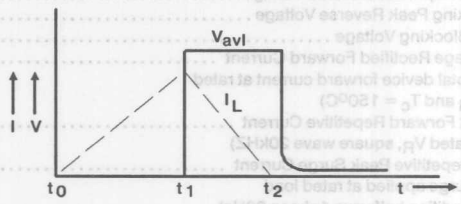


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $W_{avl} = (1/2)\ LI^2[V_{avl}/(V_{avl}-V_{dd})]$

HARRIS

MUR1540 RUR1540
MUR1550 RUR1550
MUR1560 RUR1560

15A Ultrafast Diode With Soft Recovery Characteristic

May 1991

Features

- Ultrafast with Soft Recovery Characteristic (t_{rr} < 55ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 600V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

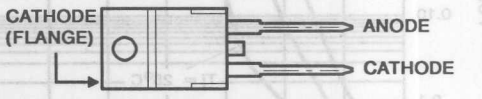
MUR1540, MUR1550, MUR1560 and RUR1540, RUR1550, RUR1560 are ultrafast dual diodes (t_{rr} < 55ns) with soft recovery characteristics ($t_a/t_b \approx 1$). They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

All are supplied in TO-220AC packages.

Package

TO-220AC
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		MUR1540 RUR1540	MUR1550 RUR1550	MUR1560 RUR1560
Peak Repetitive Reverse Voltage	V_{RRM}	400V	500V	600V
Working Peak Reverse Voltage	V_{RWM}	400V	500V	600V
DC Blocking Voltage	V_R	400V	500V	600V
Average Rectified Forward Current (Total device forward current at rated V_R and T_C = 150°C)	$I_{F(AV)}$	15A	15A	15A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHZ)	I_{FRM}	30A	30A	30A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1phase 60Hz)	I_{FSM}	200A	200A	200A
Operating and Storage Temperature	Ts, Tj	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

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File Number 2778.1

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS									UNITS
		MUR1540, RUR1540			MUR1550, RUR1550			MUR1560, RUR1560			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A T_C = +150°C	–	–	1.12	–	–	1.20	–	–	1.20	V
	I_F = 15A T_C = +25°C	–	–	1.25	–	–	1.50	–	–	1.50	V
IR @ T_C = +150°C	V_R = 400V	–	–	500	–	–	–	–	–	–	μA
	V_R = 500V	–	–	–	–	–	500	–	–	–	μA
	V_R = 600V	–	–	–	–	–	–	–	–	500	μA
IR @ T_C = +25°C	V_R = 400V	–	–	10	–	–	–	–	–	–	μA
	V_R = 500V	–	–	–	–	–	10	–	–	–	μA
	V_R = 600V	–	–	–	–	–	–	–	–	10	μA
t_{rr}	I_F = 1A	–	–	55	–	–	55	–	–	55	ns
	I_F = 15A	–	–	60	–	–	60	–	–	60	ns
t_a	I_F = 1A	–	20	–	–	20	–	–	20	–	ns
	I_F = 15A	–	30	–	–	30	–	–	30	–	ns
t_b	I_F = 1A	–	15	–	–	15	–	–	15	–	ns
	I_F = 15A	–	17	–	–	17	–	–	20	–	ns
$R_{\Theta jc}$		–	–	1.5	–	–	1.5	–	–	1.5	°C/W
W_{avl}	see Fig. 7&8	–	–	20	–	–	20	–	–	20	mj

Definitions

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current (pw = 300μs, D = 2%).

t_{rr} = Reverse recovery time at dI_F/dt = 100A/μs (See Figure 2), summation of $t_a + t_b$.

t_a = Time to reach peak reverse current at dI_F/dt = 100A/μs (See Figure 2).

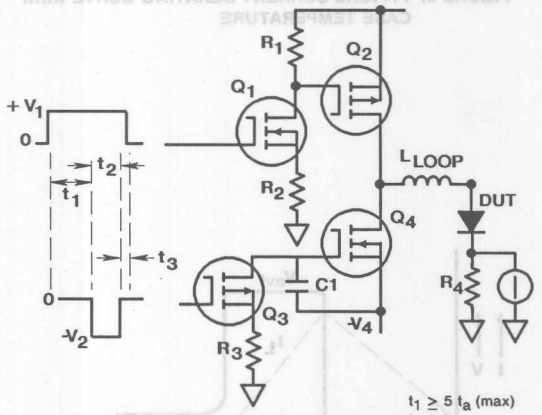
t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM}. (See Figure 2)

$R_{\Theta jc}$ = Thermal resistance junction to case.

W_{avl} = Controlled avalanche energy (See Figures 7 & 8).

pw = pulse width.

D = duty cycle.



$t_1 \geq 5\ t_a$ (max)
$t_2 > t_{rr}$
$t_3 > 0$
$\frac{L_1}{R_4} \leq \frac{t_a(min)}{10}$

V_1 amplitude controls i_F
V_2 amplitude controls di/dt
L_1 = self inductance of R_4

FIGURE 1. t_{rr} TEST CIRCUIT

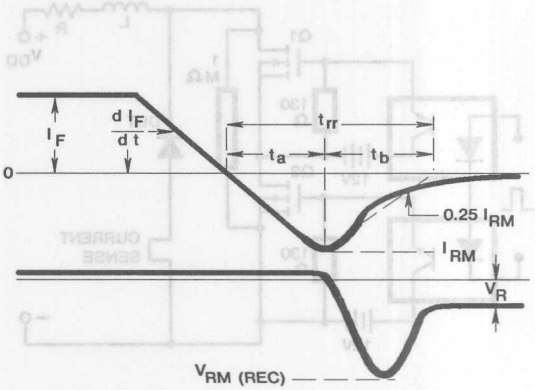


FIGURE 2. DEFINITIONS OF t_{rr}, t_a AND t_b

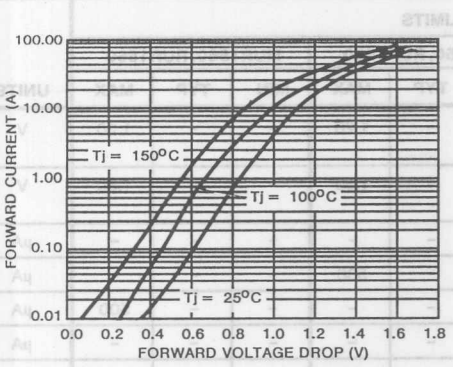


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

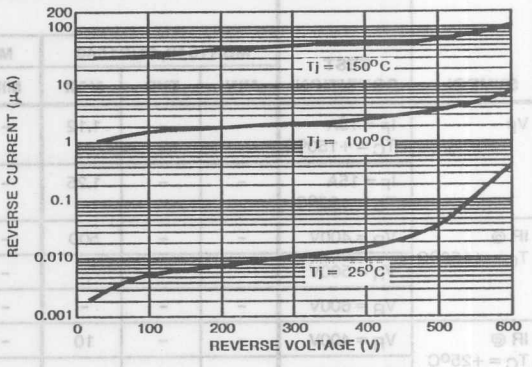


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

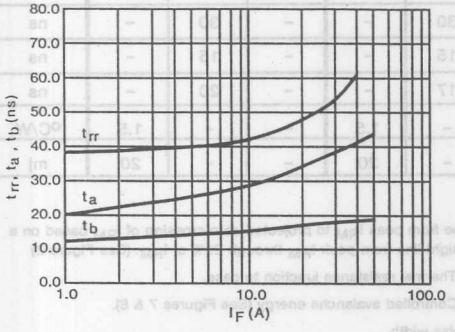


FIGURE 5. TYPICAL t_{rr}, t_a, t_b vs FORWARD CURRENT

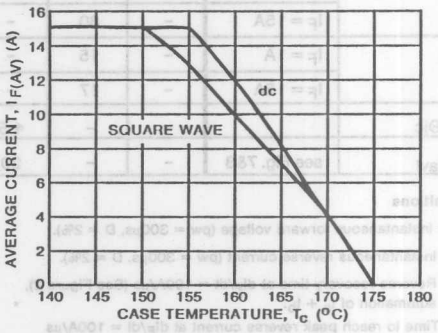


FIGURE 6. TYPICAL CURRENT DERATING CURVE w.r.t. CASE TEMPERATURE

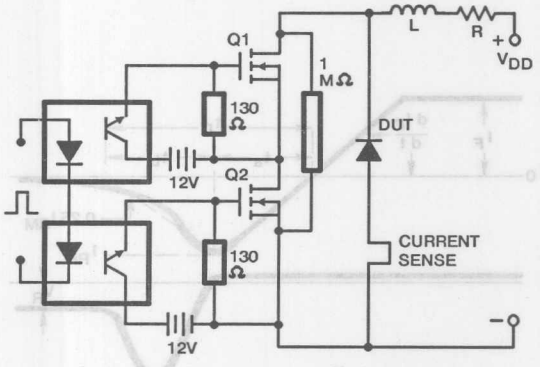


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

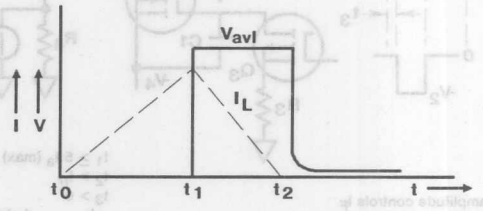


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L peak = 1A$, $L = 40mH$, $R < 0.1\Omega$, $W_{avl} = (1/2)\, LI^2[V_{avl}/(V_{avl}-V_{dd})]$

HARRIS

RUR1570/1580, RUR1590/15100

15A Ultrafast Diode With Soft Recovery Characteristic

August 1991

Features

- Ultrafast with Soft Recovery Characteristic (t_{rr} < 100ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

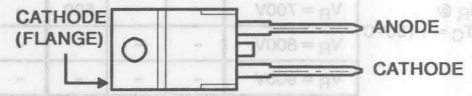
RUR1570, RUR1580, RUR1590, RUR15100 are ultrafast diodes with soft recovery characteristics (t_{rr} < 100ns). They have a low forward voltage drop and are silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as flywheel/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

All are supplied in TO-220AC packages.

Package

TO-220AC
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		RUR1570	RUR1580	RUR1590	RUR15100
Peak Repetitive Reverse Voltage	V_{RRM}	700V	800V	900V	1000V
Working Peak Reverse Voltage	V_{RWM}	700V	800V	900V	1000V
DC Blocking Voltage	V_R	700V	800V	900V	1000V
Average Rectified Forward Current (T_C = +141.25°C)	$I_{F(AV)}$	15A	15A	15A	15A
Peak Forward Repetitive Current (Square wave 20kHZ)	I_{FRM}	30A	30A	30A	30A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1phase 60Hz)	I_{FSM}	200A	200A	200A	200A
Maximum Power Dissipation	P_D	100W	100W	100W	100W
Operating and Storage Temperature	T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C

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ULTRA-FAST RECTIFIERS

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File Number 2878

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS												UNITS
		RUR1570			RUR1580			RUR1590			RUR15100			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A, T_C = +150°C	-	-	1.50	-	-	1.50	-	-	1.50	-	-	1.50	V
	I_F = 15A, T_C = +25°C	-	-	1.80	-	-	1.80	-	-	1.80	-	-	1.80	V
I_R @ T_C = +150°C	V_R = 700V	-	-	500	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V	-	-	-	-	-	500	-	-	-	-	-	-	µA
	V_R = 900V	-	-	-	-	-	-	-	-	500	-	-	-	µA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	500	µA
I_R @ T_C = +25°C	V_R = 700V	-	-	100	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V	-	-	-	-	-	100	-	-	-	-	-	-	µA
	V_R = 900V	-	-	-	-	-	-	-	-	100	-	-	-	µA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	100	µA
t_{rr}	I_F = 1A	-	-	100	-	-	100	-	-	100	-	-	100	ns
	I_F = 15A	-	-	125	-	-	125	-	-	125	-	-	125	ns
t_a	I_F = 15A	-	75	-	-	75	-	-	75	-	-	75	-	ns
t_b	I_F = 15A	-	40	-	-	40	-	-	40	-	-	40	-	ns
$R_{\Theta JC}$		-	-	1.5	-	-	1.5	-	-	1.5	-	-	1.5	°C/W
W_{avl}		-	-	20	-	-	20	-	-	20	-	-	20	mj

Definitions

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current (pw = 300µs, D = 2%).

t_{rr} = Reverse recovery time at dI_F/dt = 100A/µs, summation of $t_a + t_b$.

t_a = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM}. (See Figure 2)

$R_{\Theta jc}$ = Thermal resistance junction to case.

W_{avl} = Controlled avalanche energy (See Figures 7 & 8).

pw = pulse width.

D = duty cycle.

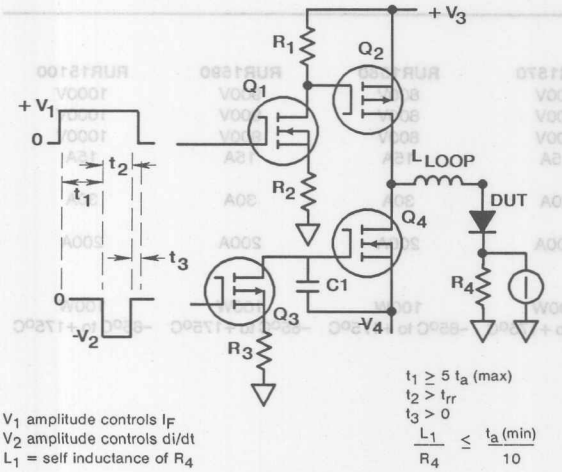


FIGURE 1. t_{rr} TEST CIRCUIT

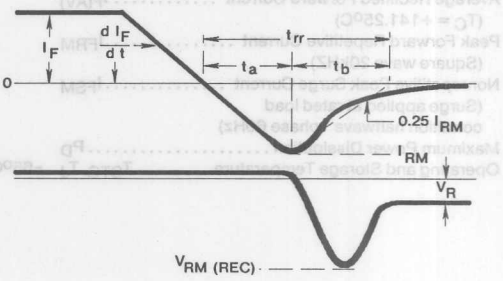


FIGURE 2. DEFINITIONS OF t_{rr}, t_a AND t_b

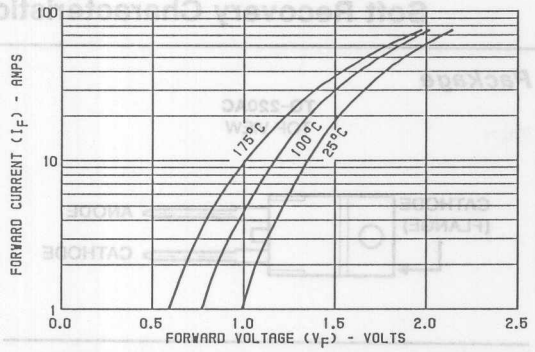


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

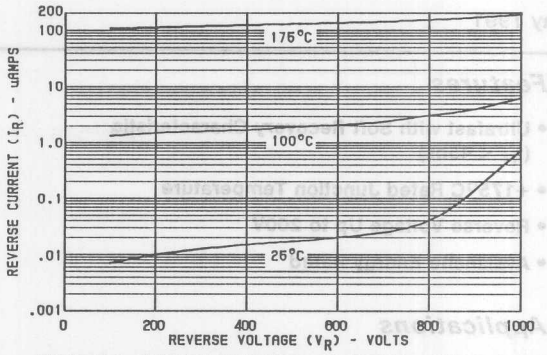


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

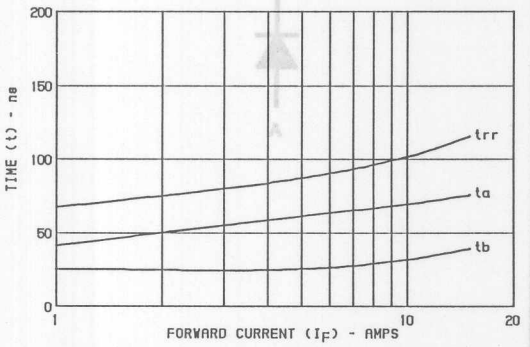


FIGURE 5. TYPICAL t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

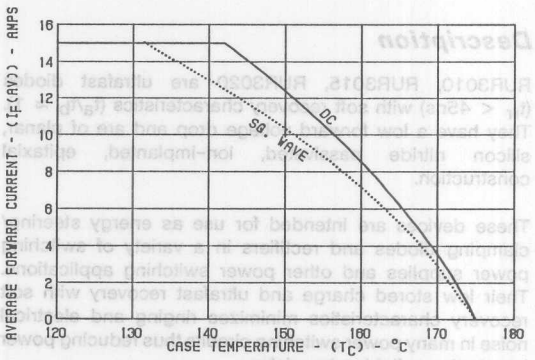


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

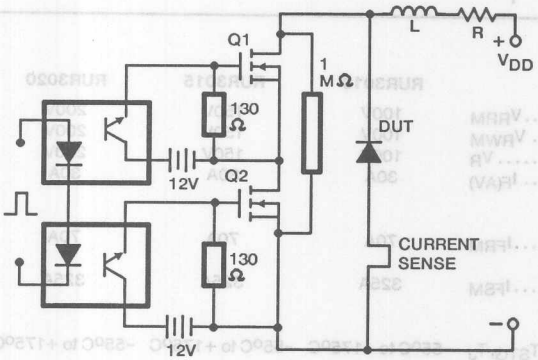


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

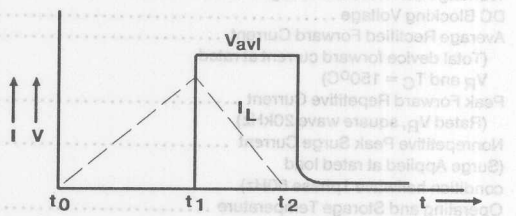


FIGURE 8. AVALANCHE CURRENT & VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $W_{avl} = (1/2)\ LI^2[V_{avl}/(V_{avl}-V_{dd})]$
Q1 and Q2 are 1000V MOSFETs

HARRIS

RUR3010
RUR3015
RUR3020

30A Ultrafast Diode With Soft Recovery Characteristic

May 1991

Features

- Ultrafast with Soft Recovery Characteristic (t_{rr} < 45ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 200V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

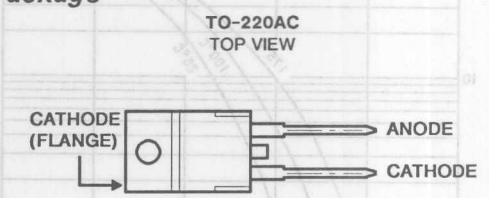
Description

RUR3010, RUR3015, RUR3020 are ultrafast diodes (t_{rr} < 45ns) with soft recovery characteristics ($t_a/t_b \approx 1$). They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

All are supplied in TO-220AC packages.

Package



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		RUR3010	RUR3015	RUR3020
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Working Peak Reverse Voltage	V_{RWM}	100V	150V	200V
DC Blocking Voltage	V_R	100V	150V	200V
Average Rectified Forward Current (Total device forward current at rated V_R and T_C = 150°C)	$I_{F(AV)}$	30A	30A	30A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHz)	I_{FRM}	70A	70A	70A
Nonrepetitive Peak Surge Current (Surge Applied at rated load condition halfwave 1phase 60Hz)	I_{FSM}	325A	325A	325A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

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File Number 2777.2

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	RUR3010 LIMITS			RUR3015 LIMITS			RUR3020 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +150°C	–	–	0.85	–	–	0.85	–	–	0.85	V
	I_F = 30A, T_C = +25°C	–	–	1.00	–	–	1.00	–	–	1.00	V
IR @ T_C = +150°C	V_R = 100V	–	–	500	–	–	–	–	–	–	µA
	V_R = 150V	–	–	–	–	–	500	–	–	–	µA
	V_R = 200V	–	–	–	–	–	–	–	–	500	µA
IR @ T_C = +25°C	V_R = 100V	–	–	30	–	–	–	–	–	–	µA
	V_R = 150V	–	–	–	–	–	30	–	–	–	µA
	V_R = 200V	–	–	–	–	–	–	–	–	30	µA
t_{rr}	I_F = 1A	–	–	45	–	–	45	–	–	45	ns
	I_F = 30A	–	–	50	–	–	50	–	–	50	ns
t_a	I_F = 1A	–	24	–	–	24	–	–	24	–	ns
	I_F = 30A	–	28	–	–	28	–	–	28	–	ns
t_b	I_F = 1A	–	17	–	–	17	–	–	17	–	ns
	I_F = 30A	–	20	–	–	20	–	–	20	–	ns
$R_{\Theta jc}$		–	–	1.2	–	–	1.2	–	–	1.2	°C/W
W_{avl}	see Fig. 7&8	–	–	20	–	–	20	–	–	20	mj

Definitions

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current (pw = 300µs, D = 2%).

t_{rr} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_a + t_b$.

t_a = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

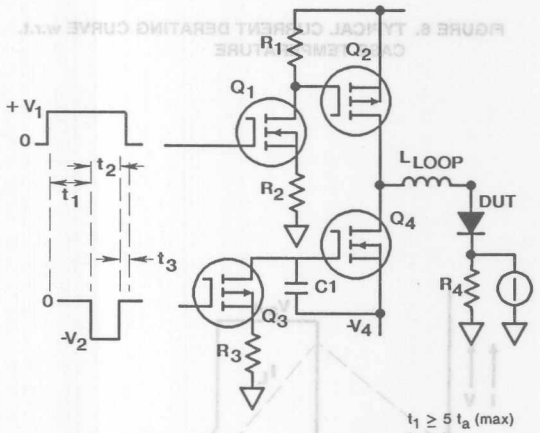
t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM}. (See Figure 2)

$R_{\Theta jc}$ = Thermal resistance junction to case.

W_{avl} = Controlled avalanche energy (See Figures 7 & 8).

pw = pulse width.

D = duty cycle.



$t_1 \geq 5\ t_a$ (max)
$t_2 > t_{rr}$
$t_3 > 0$
$\frac{L_1}{R_4} \leq \frac{t_a\ (min)}{10}$

V_1 amplitude controls I_F
V_2 amplitude controls di/dt
L_1 = self inductance of R_4

FIGURE 1. t_{rr} TEST CIRCUIT

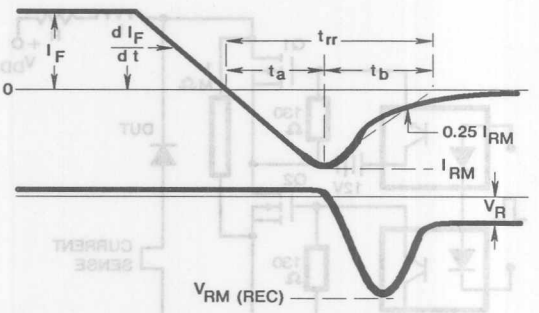


FIGURE 2. DEFINITIONS OF t_{rr}, t_a AND t_b

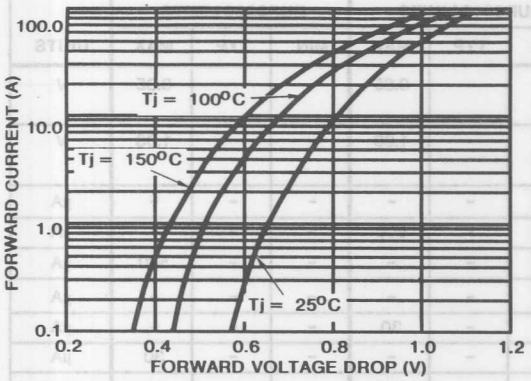


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

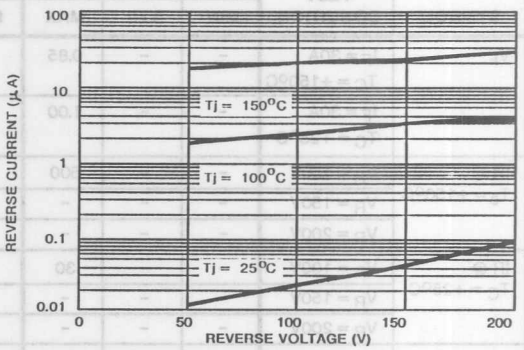


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

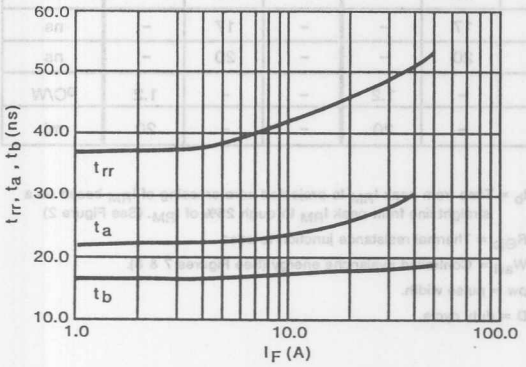


FIGURE 5. TYPICAL t_{rr}, t_a, t_b vs FORWARD CURRENT

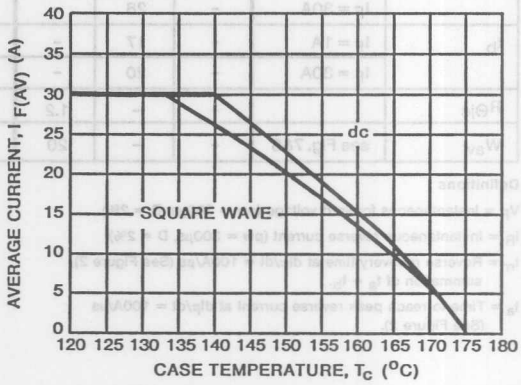


FIGURE 6. TYPICAL CURRENT DERATING CURVE w.r.t. CASE TEMPERATURE

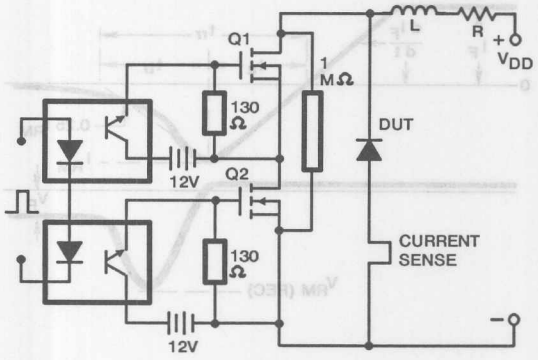


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

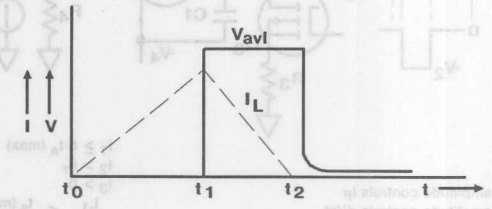


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_{L}peak = 1A$, $L = 40mH$, $R < 0.1\Omega$, $W_{avl} = (1/2)\ LI^2[V_{avl}/(V_{avl}-V_{dd})]$

HARRIS

RUR3040
RUR3050
RUR3060

30A Ultrafast Diode With Soft Recovery Characteristic

May 1991

Features

- Ultrafast with Soft Recovery Characteristic (t_{rr} < 55ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 600V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

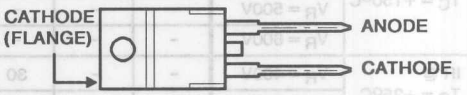
RUR3040, RUR3050, RUR3060 are ultrafast diodes (t_{rr} < 55ns) with soft recovery characteristics ($t_a/t_b \approx 1$). They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

All are supplied in TO-220AC packages.

Package

TO-220AC
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		RUR3040	RUR3050	RUR3060
Peak Repetitive Reverse Voltage	V_{RRM}	400V	500V	600V
Working Peak Reverse Voltage	V_{RWM}	400V	500V	600V
DC Blocking Voltage	V_R	400V	500V	600V
Average Rectified Forward Current (Total device forward current at rated V_R and T_C = 150°C)	$I_{F(AV)}$	30A	30A	30A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHz)	I_{FRM}	70A	70A	70A
Nonrepetitive Peak Surge Current (Surge Applied at rated load condition halfwave 1phase 60Hz)	I_{FSM}	325A	325A	325A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

12

ULTRA-FAST RECTIFIERS

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File Number 2776.1

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	RUR3040 LIMITS			RUR3050 LIMITS			RUR3060 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +150°C	-	-	1.30	-	-	1.30	-	-	1.30	V
	I_F = 30A, T_C = +25°C	-	-	1.50	-	-	1.50	-	-	1.50	V
IR @ T_C = +150°C	V_R = 400V	-	-	1	-	-	-	-	-	-	mA
	V_R = 500V	-	-	-	-	-	1	-	-	-	mA
	V_R = 600V	-	-	-	-	-	-	-	-	1	mA
IR @ T_C = +25°C	V_R = 400V	-	-	30	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	30	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	30	µA
t_{rr}	I_F = 1A	-	-	55	-	-	55	-	-	55	ns
	I_F = 30A	-	-	60	-	-	60	-	-	60	ns
t_a	I_F = 1A	-	20	-	-	20	-	-	20	-	ns
	I_F = 30A	-	38	-	-	38	-	-	38	-	ns
t_b	I_F = 1A	-	15	-	-	15	-	-	15	-	ns
	I_F = 30A	-	20	-	-	20	-	-	20	-	ns
$R_{\Theta jc}$		-	-	1.2	-	-	1.2	-	-	1.2	°C/W
W_{avl}	see Fig. 7&8	-	-	20	-	-	20	-	-	20	mj

Definitions

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current (pw = 300µs, D = 2%).

t_{rr} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_a + t_b$.

t_a = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

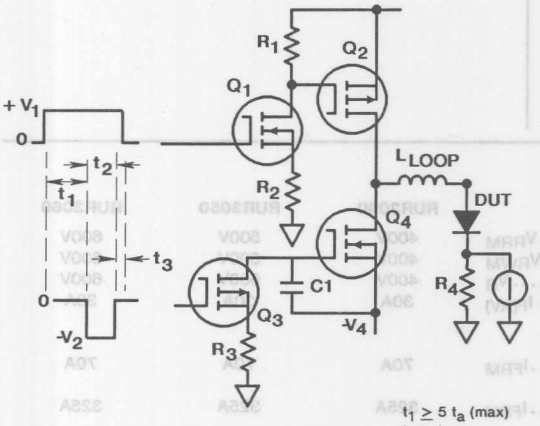
t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM}. (See Figure 2)

$R_{\Theta jc}$ = Thermal resistance junction to case.

W_{avl} = Controlled avalanche energy (See Figures 7 & 8).

pw = pulse width.

D = duty cycle.



V_1 amplitude controls I_F
V_2 amplitude controls di/dt
L_1 = self inductance of R_4

$t_1 \geq 5\ t_a$ (max)
$t_2 > t_{rr}$
$t_3 > 0$
$\frac{L_1}{R_4} \leq \frac{t_a\ (min)}{10}$

FIGURE 1. t_{rr} TEST CIRCUIT

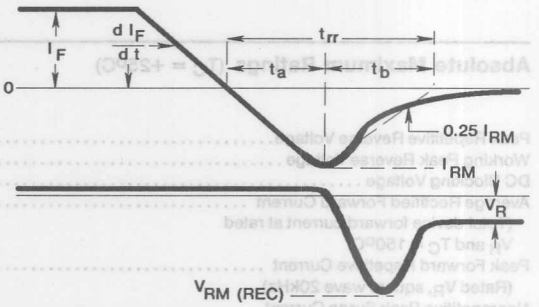


FIGURE 2. DEFINITIONS OF t_{rr}, t_a AND t_b

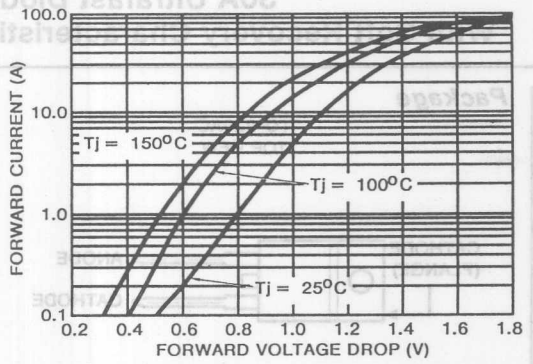


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

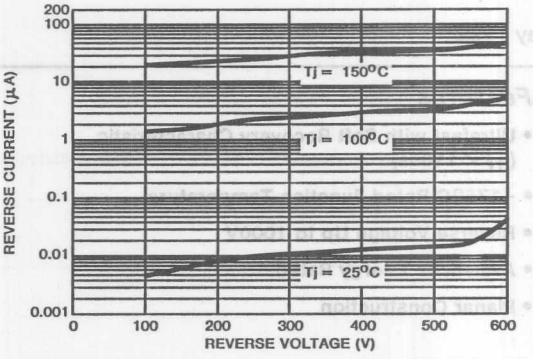


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

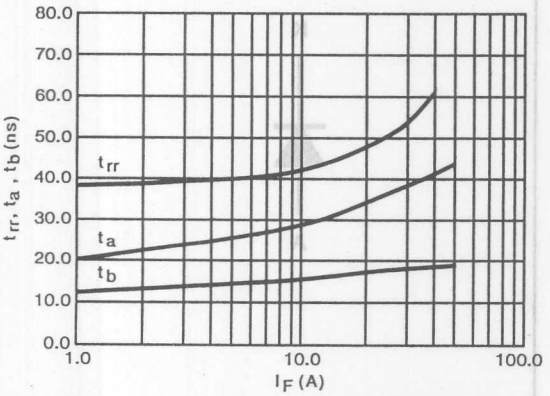


FIGURE 5. TYPICAL t_{rr}, t_a, t_b vs FORWARD CURRENT

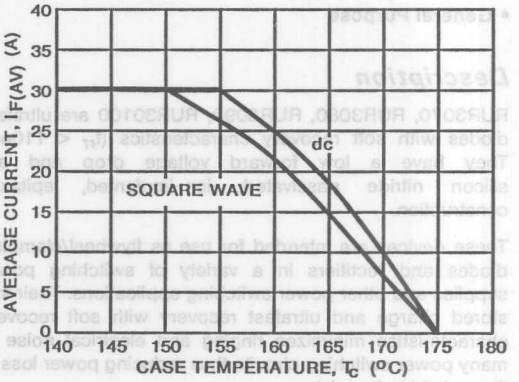


FIGURE 6. TYPICAL CURRENT DERATING CURVE w.r.t. CASE TEMPERATURE

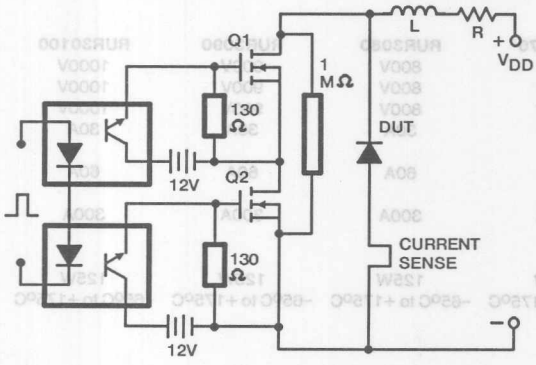


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

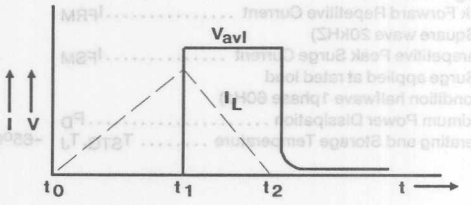


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $W_{avl} = (1/2)\ LI^2[V_{avl}/(V_{avl}-V_{dd})]$

HARRIS

RUR3070/3080, RUR3090/30100

30A Ultrafast Diode With Soft Recovery Characteristic

May 1992

Features

- Ultrafast with Soft Recovery Characteristic (t_{rr} < 110ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

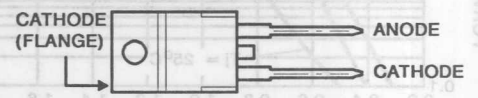
RUR3070, RUR3080, RUR3090, RUR30100 are ultrafast diodes with soft recovery characteristics (t_{rr} < 110ns). They have a low forward voltage drop and are silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as flywheel/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

All are supplied in TO-220AC packages.

Package

TO-220AC
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

	RUR3070	RUR3080	RUR3090	RUR30100
Peak Repetitive Reverse Voltage ..... V_{RRM}	700V	800V	900V	1000V
Working Peak Reverse Voltage ..... V_{RWM}	700V	800V	900V	1000V
DC Blocking Voltage ..... V_R	700V	800V	900V	1000V
Average Rectified Forward Current ..... $I_{F(AV)}$ (T_C = +121°C)	30A	30A	30A	30A
Peak Forward Repetitive Current ..... I_{FRM} (Square wave 20kHZ)	60A	60A	60A	60A
Nonrepetitive Peak Surge Current ..... I_{FSM} (Surge applied at rated load condition halfwave 1phase 60Hz)	300A	300A	300A	300A
Maximum Power Dissipation ..... P_D	125W	125W	125W	125W
Operating and Storage Temperature ..... T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C

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File Number 2877.1

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS												UNITS
		RUR3070			RUR3080			RUR3090			RUR30100			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +150°C	-	-	1.60	-	-	1.60	-	-	1.60	-	-	1.60	V
	I_F = 30A, T_C = +25°C	-	-	1.80	-	-	1.80	-	-	1.80	-	-	1.8	V
I_R @ T_C = +150°C	V_R = 700V	-	-	1	-	-	-	-	-	-	-	-	-	mA
	V_R = 800V	-	-	-	-	-	1	-	-	-	-	-	-	mA
	V_R = 900V	-	-	-	-	-	-	-	-	1	-	-	-	mA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	1	mA
I_R @ T_C = +25°C	V_R = 700V	-	-	100	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V	-	-	-	-	-	100	-	-	-	-	-	-	µA
	V_R = 900V	-	-	-	-	-	-	-	-	100	-	-	-	µA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	100	µA
t_{rr}	I_F = 1A	-	-	110	-	-	110	-	-	110	-	-	110	ns
	I_F = 30A	-	-	150	-	-	150	-	-	150	-	-	150	ns
t_a	I_F = 30A	-	90	-	-	90	-	-	90	-	-	90	-	ns
t_b	I_F = 30A	-	45	-	-	45	-	-	45	-	-	45	-	ns
$R_{\Theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	-	-	1.2	°C/W
W_{avl}		-	-	20	-	-	20	-	-	20	-	-	20	mj

Definitions

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current (pw = 300µs, D = 2%).

t_{rr} = Reverse recovery time at dI_F/dt = 100A/µs, summation of $t_a + t_b$.

t_a = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

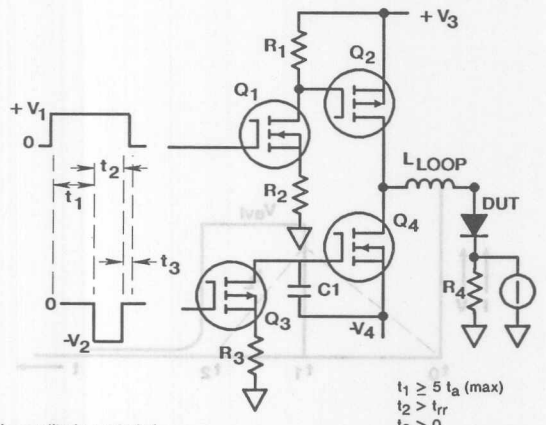
t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM}. (See Figure 2)

$R_{\Theta jc}$ = Thermal resistance junction to case.

W_{avl} = Controlled avalanche energy (See Figures 7 & 8).

pw = pulse width.

D = duty cycle.



V_1 amplitude controls I_F
V_2 amplitude controls di/dt
L_1 = self inductance of R_4

$t_1 \geq 5\ t_a$ (max)
$t_2 > t_{rr}$
$t_3 > 0$
$\frac{L_1}{R_4} \leq \frac{t_a\ (min)}{10}$

FIGURE 1. t_{rr} TEST CIRCUIT

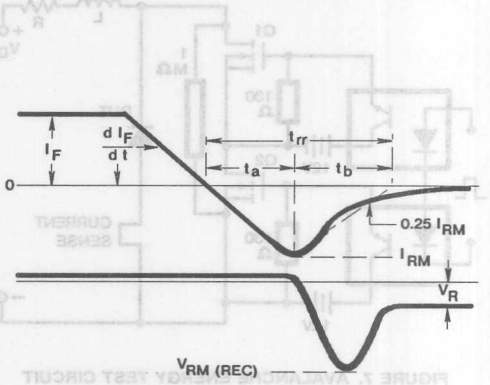


FIGURE 2. DEFINITIONS OF t_{rr}, t_a AND t_b

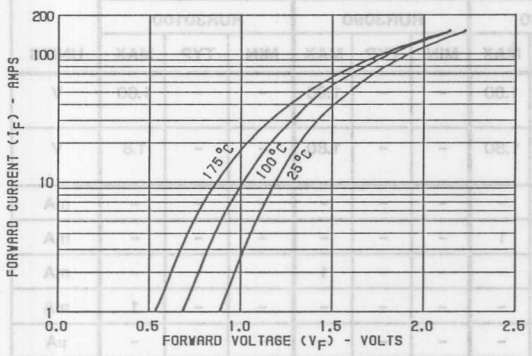


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

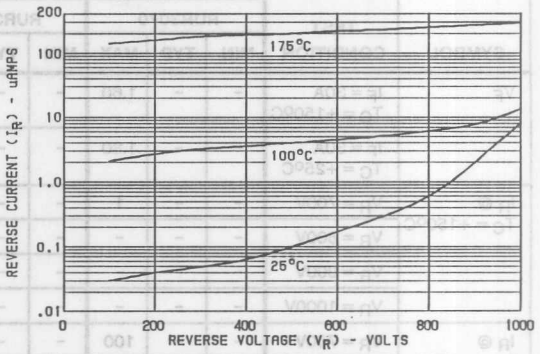


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

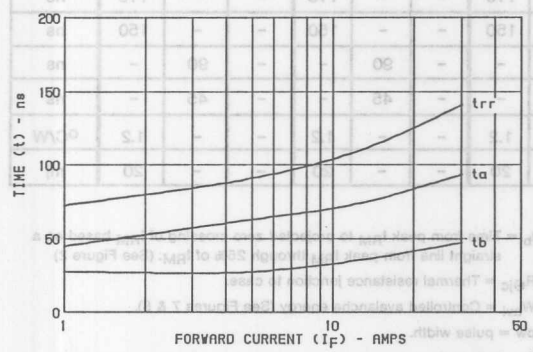


FIGURE 5. TYPICAL t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

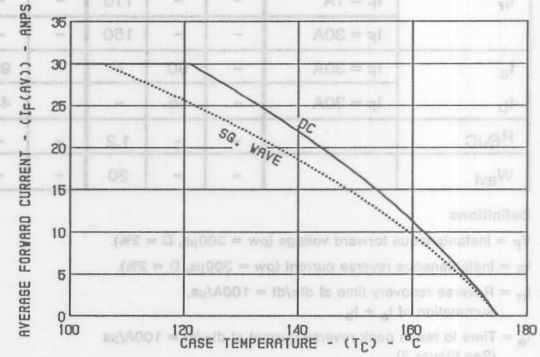


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

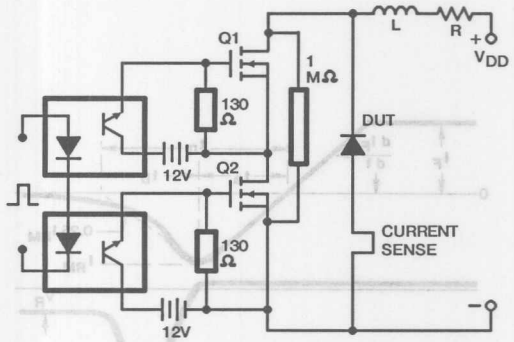


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

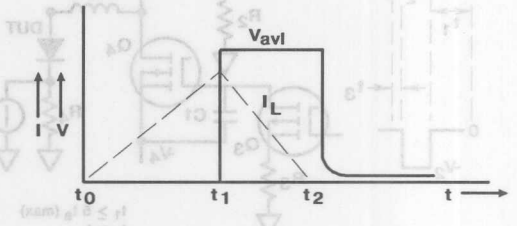


FIGURE 8. AVALANCHE CURRENT & VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $W_{avl} = (1/2)\ LI^2[V_{avl}/(V_{avl}-V_{dd})]$
Q1 and Q2 are 1000V MOSFETs

RURD810
RURD815
RURD820

Dual 8A High-Speed, High-Efficiency Epitaxial Silicon Rectifiers

August 1991

Features

- Ultrafast Recovery Time (t_{rr} < 35ns)
- Low Forward Voltage
- Low Thermal Resistance
- Planar Design
- Wire-Bonded Construction

Applications

- General Purpose
- Power Switching Circuits to 100kHz
- Full-Wave Rectification

Description

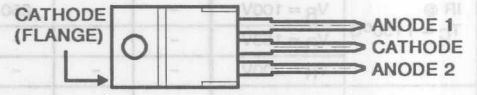
The RURD810, RURD815, RURD820 are low forward voltage drop ultrafast rectifiers (t_{rr} < 35ns). They use a glass passivated ion-implanted, epitaxial construction.

These devices are intended for use as output rectifiers and flywheel diodies in a variety of high frequency pulse width modulated and switching regulators. Their low stored charge and attendant fast reverse recovery behavior minimize electrical noise generation and in many circuits markedly reduce the turn-on dissipation of the associated power switching transistors.

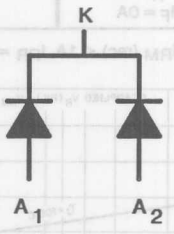
All are supplied in TO-220AB plastic packages.

Package

TO-220AB
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		RURD810	RURD815	RURD820
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Average Rectified Forward Current				
T_A = 25°C (No Heat Sink)	$I_{F(AV)}$	3A	3A	3A
T_A = 25°C (With Heat Sink)*	$I_{F(AV)}$	8A	8A	8A
T_A = 125°C	$I_{F(AV)}$	8A	8A	8A
Nonrepetitive Peak Surge Current (8.3ms, ½ cycle)	I_{FSM}	100A	100A	100A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C
Maximum Lead Temperature During Solder (At distance > ⅛" (3.17mm) from case or 10s max)	T_L	260°C	260°C	260°C

*Wakefield type 295 heat sink with convection cooling.

12 ULTRA-FAST RECTIFIERS

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File Number 1356.2

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURD810			RURD815			RURD820			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 8A, T_C = +150°C	–	–	0.83	–	–	0.83	–	–	0.85	V
	I_F = 8A, T_C = +25°C	–	–	0.975	–	–	0.975	–	–	1	V
IR @ T_C = +150°C	V_R = 100V	–	–	250	–	–	–	–	–	–	µA
	V_R = 150V	–	–	–	–	–	250	–	–	–	µA
	V_R = 200V	–	–	–	–	–	–	–	–	250	µA
IR @ T_C = +25°C	V_R = 100V	–	–	5	–	–	–	–	–	–	µA
	V_R = 150V	–	–	–	–	–	5	–	–	–	µA
	V_R = 200V	–	–	–	–	–	–	–	–	5	µA
t_{rr}	I_F = 8A*	–	–	35	–	–	35	–	–	35	ns
$R_{\Theta jc}$		–	–	2.25	–	–	2.25	–	–	2.25	°C/W
$R_{\Theta ja}$		–	–	60	–	–	60	–	–	60	°C/W
C_J	V_R = 10V, I_F = 0A	–	40	–	–	40	–	–	40	–	pF

*dI_F/dt = 40A/µs, I_{RM} (rec) < 1A, I_{RR} = 0.25A.

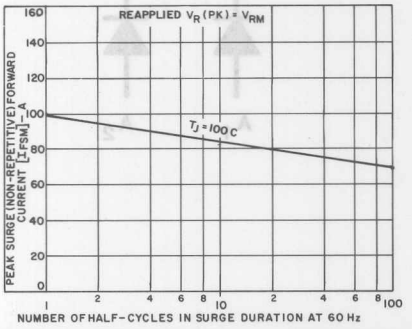


FIGURE 1. PEAK SURGE FORWARD CURRENT vs SURGE DURATION

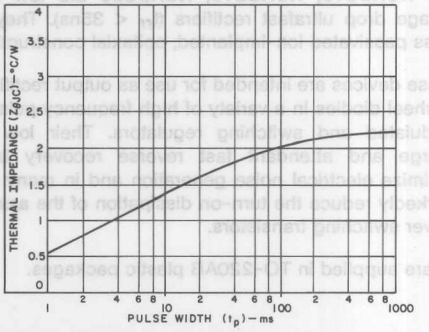


FIGURE 2. THERMAL IMPEDANCE vs PULSE WIDTH (PER JUNCTION)

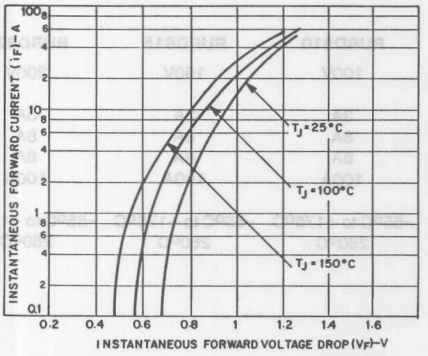


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

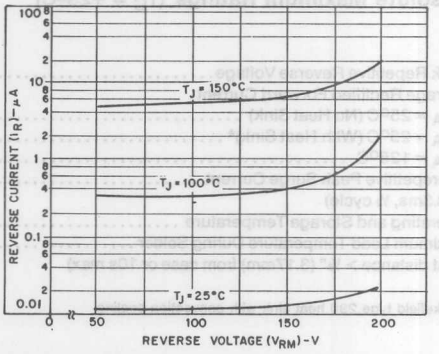


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

HARRIS

MUR1610CT RUR1610CT
MUR1615CT RUR1615CT
MUR1620CT RUR1620CT

Dual 8A High-Speed, High-Efficiency Epitaxial Silicon Rectifiers

August 1991

Features

- Ultrafast Recovery Time (t_{rr} < 35ns)
- Low Forward Voltage
- Low Thermal Resistance
- Hard Glass Passivation
- Wire-Bonded Construction

Applications

- General Purpose
- Power Switching Circuits to 100kHz
- Full-Wave Rectification

Description

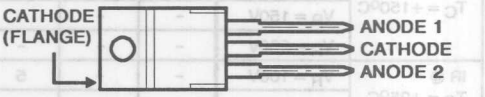
The MUR1610CT, MUR1615CT, MUR1620CT, RUR1610CT, RUR1615CT, RUR1620CT are low forward voltage drop ultrafast rectifiers (t_{rr} < 35ns). They use a glass passivated ion-implanted, epitaxial construction.

These devices are intended for use as output rectifiers and flywheel diodies in a variety of high frequency pulse width modulated and switching regulators. Their low stored charge and attendant fast reverse recovery behavior minimize electrical noise generation and in many circuits markedly reduce the turn-on dissipation of the associated power switching transistors.

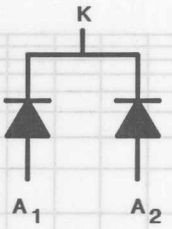
All are supplied in TO-220AB plastic packages.

Package

TO-220AB
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		MUR1610CT RUR1610CT	MUR1615CT RUR1615CT	MUR1620CT RUR1620CT
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Working Peak Reverse Voltage	V_{RWM}	100V	150V	200V
DC Blocking Voltage	V_R	100V	150V	200V
Average Rectified Forward Current (Per Leg)	$I_{F(AV)}$	8A	8A	8A
(Total device, (Rated V_R), T_C = 150°C		16A	16A	16A
Peak Forward Repetitive Current (Per Diode Leg) (Rated V_R, Square Wave, 20kHZ), T_C = 150°C	I_{FRM}	16A	16A	16A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave, single phase, 60Hz)	I_{FSM}	100A	100A	100A
Operating and Storage Temperature	T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C
Maximum Lead Temperature During Soldering (At distance > 1/8" (3.17mm) from case for 10s max)	T_L	260°C	260°C	260°C

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ULTRA-FAST RECTIFIERS

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File Number 1885.1

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS									UNITS
		MUR1610CT, RUR1610CT			MUR1615CT, RUR1615CT			MUR1620CT, RUR1620CT			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 8A T_C = +150°C	–	–	0.83	–	–	0.83	–	–	0.85	V
	I_F = 8A T_C = +25°C	–	–	0.975	–	–	0.975	–	–	1	V
IR @ T_C = +150°C	V_R = 100V	–	–	250	–	–	–	–	–	–	µA
	V_R = 150V	–	–	–	–	–	250	–	–	–	µA
	V_R = 200V	–	–	–	–	–	–	–	–	250	µA
IR @ T_C = +25°C	V_R = 100V	–	–	5	–	–	–	–	–	–	µA
	V_R = 150V	–	–	–	–	–	5	–	–	–	µA
	V_R = 200V	–	–	–	–	–	–	–	–	5	µA
t_{rr}	I_F = 1A*	–	–	35	–	–	35	–	–	35	ns
	I_F = 0.5**	–	–	25	–	–	25	–	–	25	ns
$R_{\Theta jc}$		–	–	3	–	–	3	–	–	3	°C/W

* dI_F/dt = 50A/µs ** I_R =1.0A, I_{REC} = 0.25A.

MUR1610CT, MUR1615CT, RUR1610CT, RUR1615CT

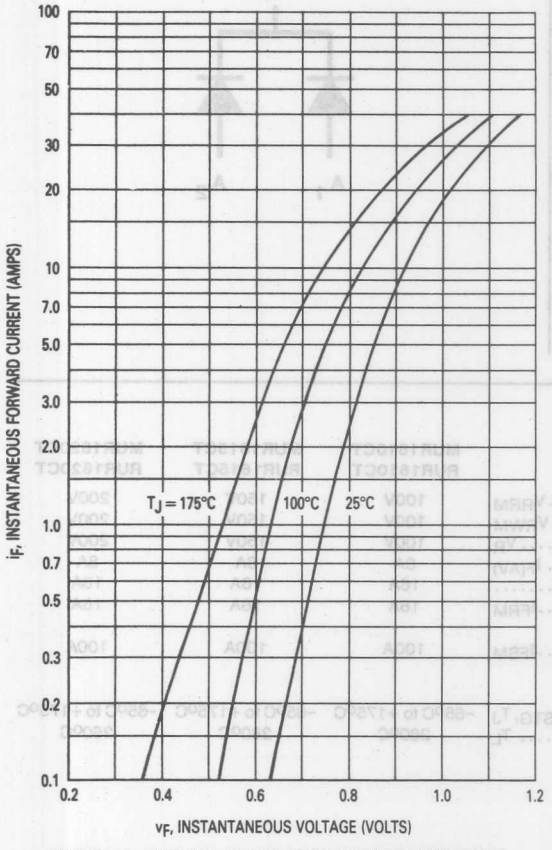


FIGURE 1. TYPICAL FORWARD VOLTAGE (PER LEG)

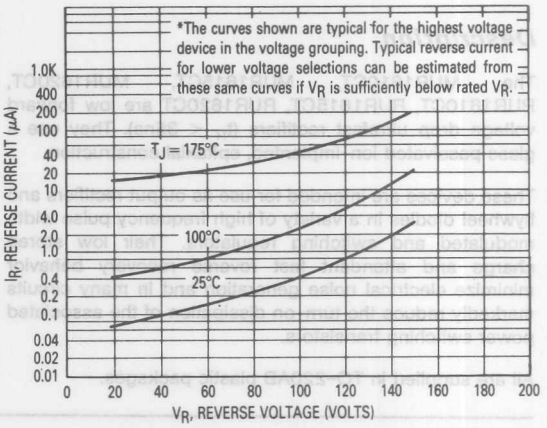


FIGURE 2. TYPICAL REVERSE CURRENT (PER LEG*)

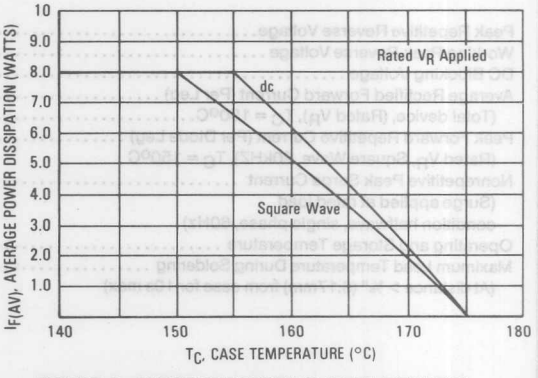


FIGURE 3. CURRENT DERATING CASE (PER LEG)

MUR1610CT, MUR1615CT, RUR1610CT, RUR1615CT (CONTINUED)

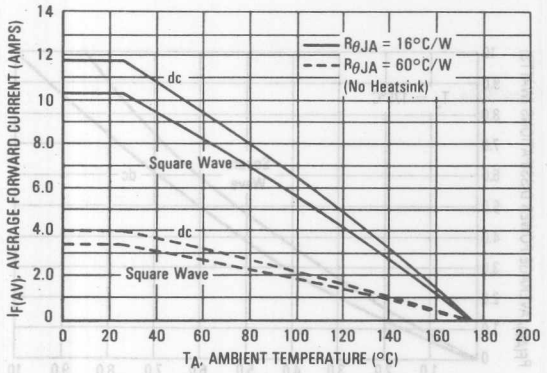


FIGURE 4. CURRENT DERATING, AMBIENT (PER LEG)

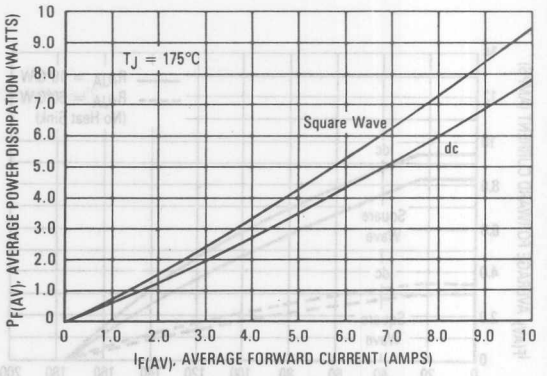


FIGURE 5. POWER DISSIPATION (PER LEG)

MUR1620CT, RUR1620CT

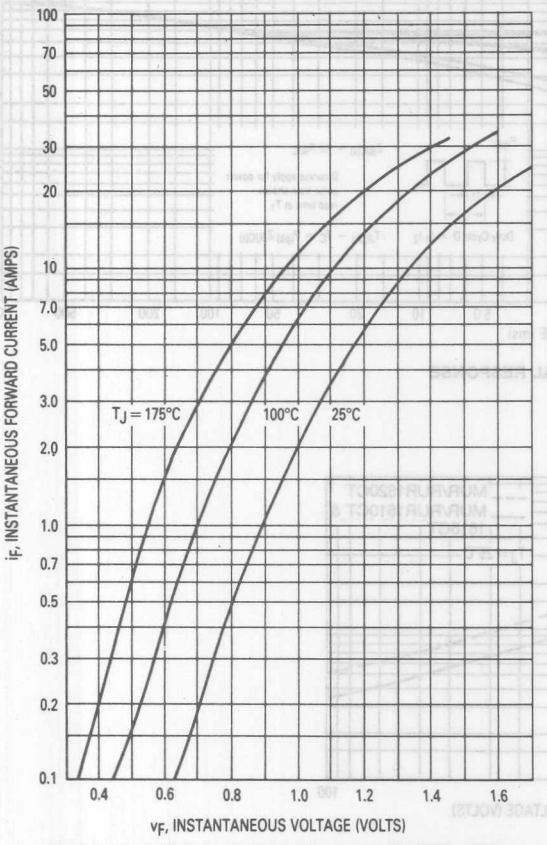


FIGURE 6. TYPICAL FORWARD VOLTAGE (PER LEG)

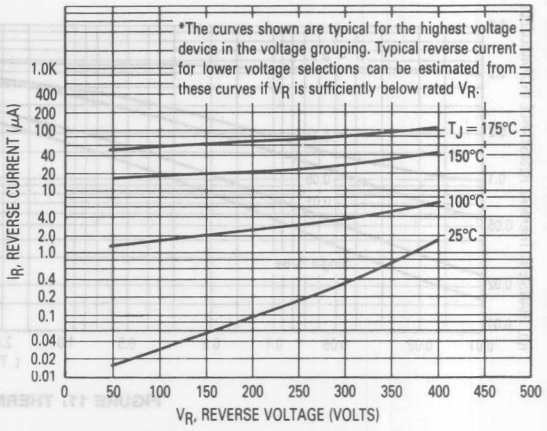


FIGURE 7. TYPICAL REVERSE CURRENT (PER LEG)*

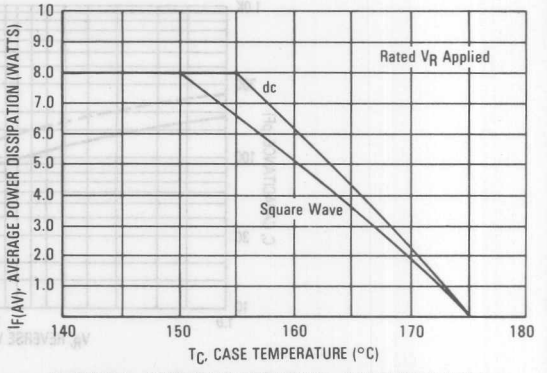


FIGURE 8. CURRENT DERATING, CASE (PER LEG)

12 ULTRA-FAST RECTIFIERS

MUR1620CT, RUR1620CT (CONTINUED)

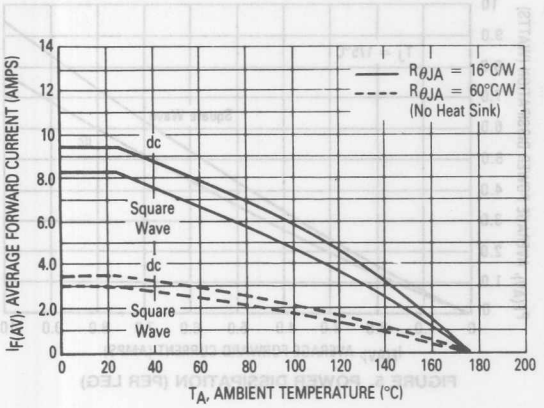


FIGURE 9. CURRENT DERATING AMBIENT (PER LEG)

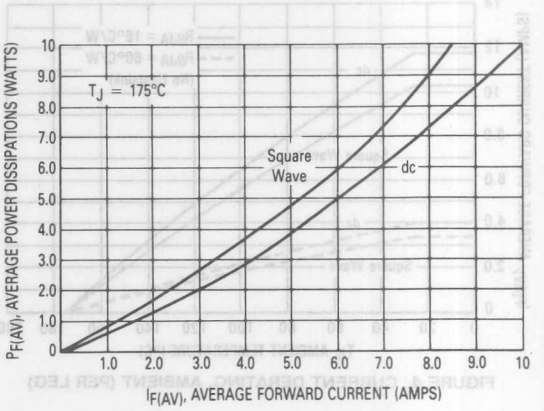


FIGURE 10. POWER DISSIPATION (PER LEG)

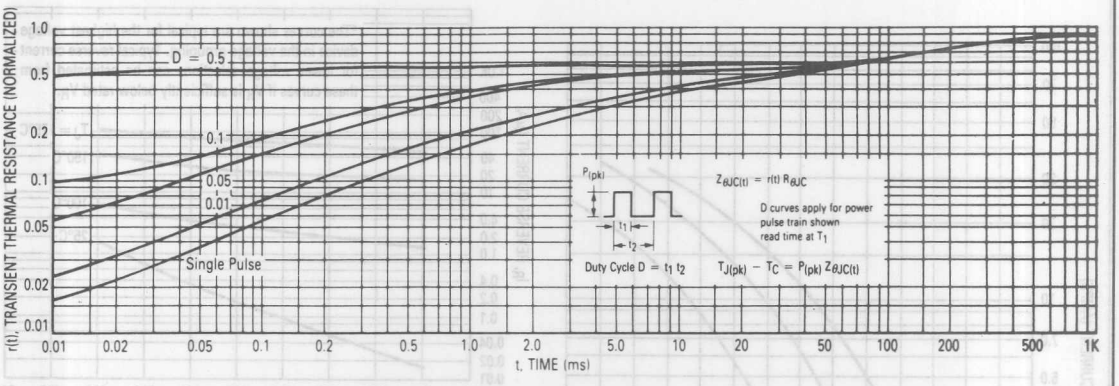


FIGURE 11. THERMAL RESPONSE

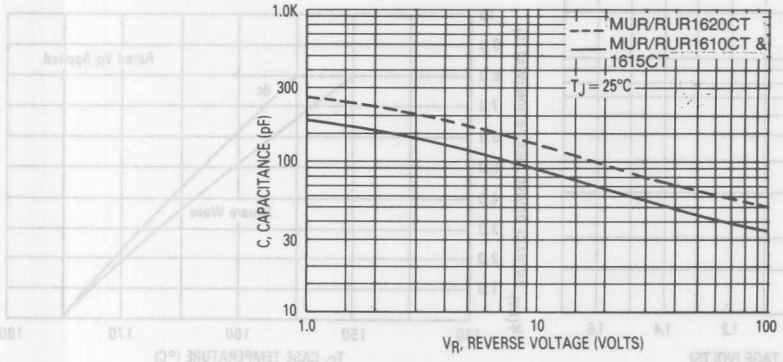


FIGURE 12. TYPICAL CAPACITANCE (PER LEG)

HARRIS

MUR3010PT RURD1510
MUR3010PT RURD1515
MUR3020PT RURD1520

15A Ultrafast Dual Diode With Soft Recovery Characteristic

May 1991

Features

- Ultrafast with Soft Recovery Characteristic (t_{rr} < 30ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 200V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

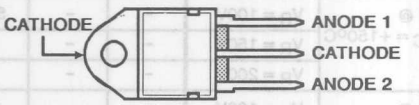
MUR3010PT, MUR3010PT, MUR3020PT and RURD1510, RURD1515, RURD1520 are ultrafast dual diodes (t_{rr} < 30ns) with soft recovery characteristics ($t_a/t_b \approx 1$). They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

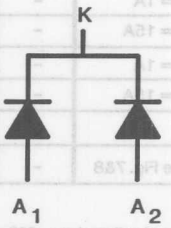
All are supplied in TO-218AC packages.

Package

TO-218AC
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		MUR3010PT RURD1510	MUR3010PT RURD1515	MUR3020PT RURD1520
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Working Peak Reverse Voltage	V_{RWM}	100V	150V	200V
DC Blocking Voltage	V_R	100V	150V	200V
Average Rectified Forward Current (Total device forward current at rated V_R and T_C = 150°C)	$I_{F(AV)}$	15A	15A	15A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHZ)	I_{FRM}	30A	30A	30A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1phase 60Hz)	I_{FSM}	200A	200A	200A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

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ULTRA-FAST RECTIFIERS

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File Number 2775.2

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS									UNITS
		MUR3010PT, RURD1510			MUR3015PT, RURD1515			MUR3020PT, RURD1520			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A T_C = +150°C	-	-	0.85	-	-	0.85	-	-	0.85	V
	I_F = 15A T_C = +25°C	-	-	1.05	-	-	1.05	-	-	1.05	V
IR @ T_C = +150°C	V_R = 100V	-	-	500	-	-	-	-	-	-	µA
	V_R = 150V	-	-	-	-	-	500	-	-	-	µA
	V_R = 200V	-	-	-	-	-	-	-	-	500	µA
IR @ T_C = +25°C	V_R = 100V	-	-	10	-	-	-	-	-	-	µA
	V_R = 150V	-	-	-	-	-	10	-	-	-	µA
	V_R = 200V	-	-	-	-	-	-	-	-	10	µA
t_{rr}	I_F = 1A	-	-	30	-	-	30	-	-	30	ns
	I_F = 15A	-	-	35	-	-	35	-	-	35	ns
t_a	I_F = 1A	-	18	-	-	18	-	-	18	-	ns
	I_F = 15A	-	20	-	-	20	-	-	20	-	ns
t_b	I_F = 1A	-	9	-	-	9	-	-	9	-	ns
	I_F = 15A	-	10	-	-	10	-	-	10	-	ns
$R_{\Theta jc}$		-	-	1.5	-	-	1.5	-	-	1.5	°C/W
W_{avl}	see Fig. 7&8	-	-	20	-	-	20	-	-	20	mj

Definitions

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current (pw = 300µs, D = 2%).

t_{rr} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_a + t_b$.

t_a = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

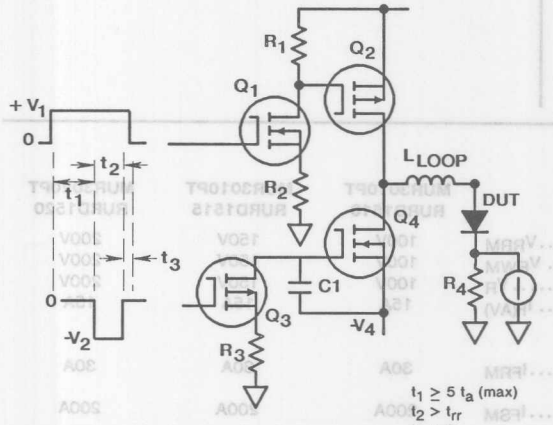
t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM}. (See Figure 2)

$R_{\Theta jc}$ = Thermal resistance junction to case.

W_{avl} = Controlled avalanche energy (See Figures 7 & 8).

pw = pulse width.

D = duty cycle.



V_1 amplitude controls I_F
V_2 amplitude controls di/dt
L_1 = self inductance of R_4

$t_1 \geq 5\ t_a$ (max)
$t_2 > t_{rr}$
$t_3 > 0$
$\frac{L_1}{R_4} \leq \frac{t_a\ (min)}{10}$

FIGURE 1. t_{rr} TEST CIRCUIT

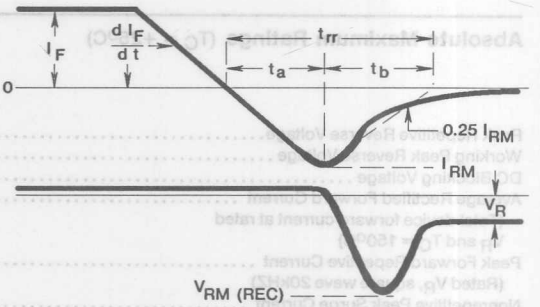


FIGURE 2. DEFINITIONS OF t_{rr}, t_a AND t_b

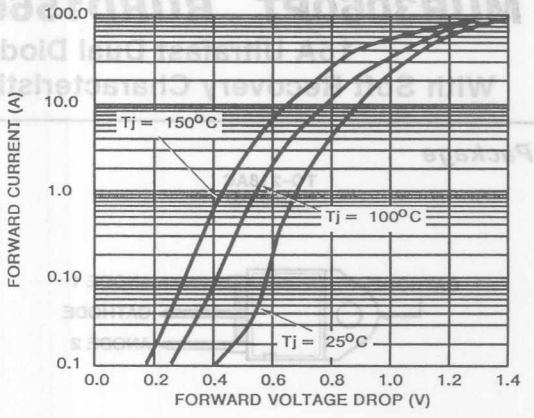


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

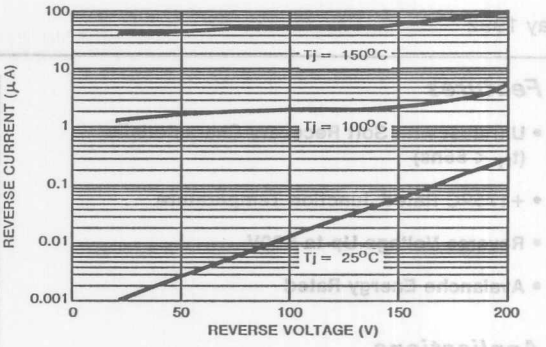


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

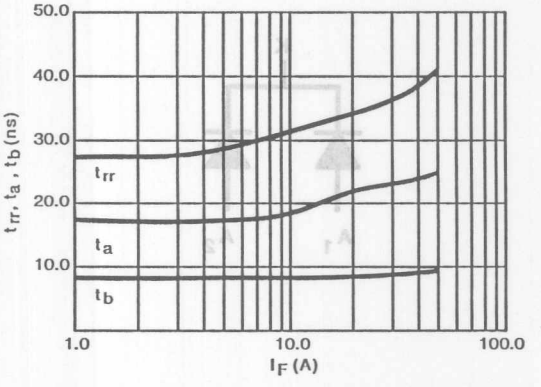


FIGURE 5. TYPICAL t_{rr}, t_a, t_b vs FORWARD CURRENT

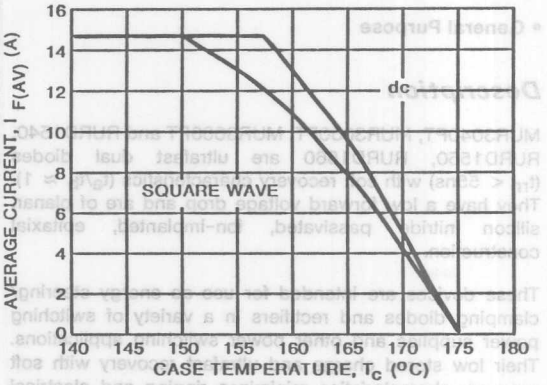


FIGURE 6. TYPICAL CURRENT DERATING CURVE w.r.t. CASE TEMPERATURE

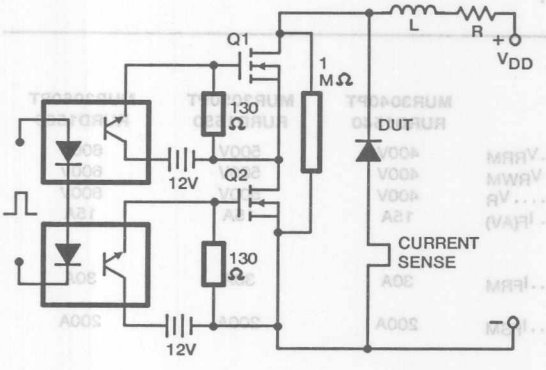


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

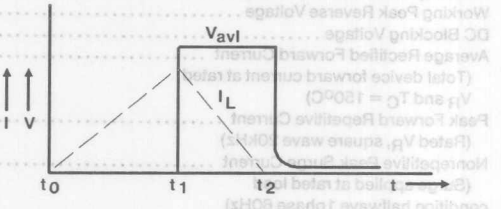


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L peak = 1A$, $L = 40mH$, $R < 0.1\Omega$, $W_{avl} = (1/2)\, LI^2[V_{avl}/(V_{avl}-V_{dd})]$

HARRIS

MUR3040PT RURD1540
MUR3050PT RURD1550
MUR3060PT RURD1560

15A Ultrafast Dual Diode With Soft Recovery Characteristic

May 1992

Features

- Ultrafast with Soft Recovery Characteristic (t_{rr} < 55ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 600V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

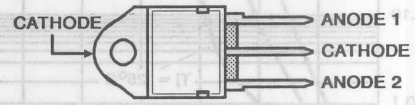
MUR3040PT, MUR3050PT, MUR3060PT and RURD1540, RURD1550, RURD1560 are ultrafast dual diodes (t_{rr} < 55ns) with soft recovery characteristics ($t_a/t_b \approx 1$). They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

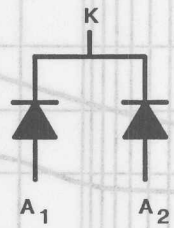
All are supplied in TO-218AC packages.

Package

TO-218AC
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		MUR3040PT RURD1540	MUR3050PT RURD1550	MUR3060PT RURD1560
Peak Repetitive Reverse Voltage	V_{RRM}	400V	500V	600V
Working Peak Reverse Voltage	V_{RWM}	400V	500V	600V
DC Blocking Voltage	V_R	400V	500V	600V
Average Rectified Forward Current (Total device forward current at rated V_R and T_C = 150°C)	$I_{F(AV)}$	15A	15A	15A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHz)	I_{FRM}	30A	30A	30A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1phase 60Hz)	I_{FSM}	200A	200A	200A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

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File Number 2774.1

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS									UNITS
		MUR3040PT, RURD1540			MUR3050PT, RURD1550			MUR3060PT, RURD1560			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A T_C = +150°C	-	-	1.12	-	-	1.20	-	-	1.20	V
	I_F = 15A T_C = +25°C	-	-	1.25	-	-	1.50	-	-	1.50	V
IR @ T_C = +150°C	V_R = 400V	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	500	µA
IR @ T_C = +25°C	V_R = 400V	-	-	10	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	10	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	10	µA
t_{rr}	I_F = 1A	-	-	55	-	-	55	-	-	55	ns
	I_F = 15A	-	-	60	-	-	60	-	-	60	ns
t_a	I_F = 1A	-	20	-	-	20	-	-	20	-	ns
	I_F = 15A	-	30	-	-	30	-	-	30	-	ns
t_b	I_F = 1A	-	15	-	-	15	-	-	15	-	ns
	I_F = 15A	-	17	-	-	17	-	-	20	-	ns
$R_{\Theta jc}$		-	-	1.5	-	-	1.5	-	-	1.5	°C/W
W_{avl}	see Fig. 7&8	-	-	20	-	-	20	-	-	20	mj

Definitions

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current (pw = 300µs, D = 2%).

t_{rr} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_a + t_b$.

t_a = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

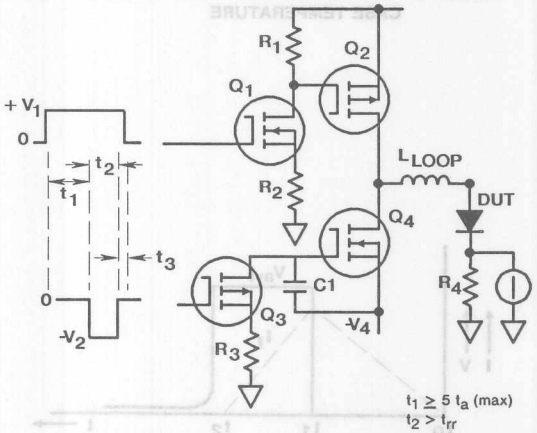
t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM}. (See Figure 2)

$R_{\Theta jc}$ = Thermal resistance junction to case.

W_{avl} = Controlled avalanche energy (See Figures 7 & 8).

pw = pulse width.

D = duty cycle.



$t_1 \geq 5\ t_a$ (max)
$t_2 > t_{rr}$
$t_3 > 0$
$\frac{L_1}{R_4} \leq \frac{t_a(min)}{10}$

V_1 amplitude controls i_F
V_2 amplitude controls di/dt
L_1 = self inductance of R_4

FIGURE 1. t_{rr} TEST CIRCUIT

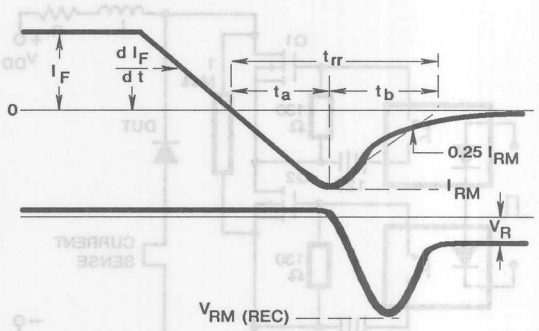


FIGURE 2. DEFINITIONS OF t_{rr}, t_a AND t_b

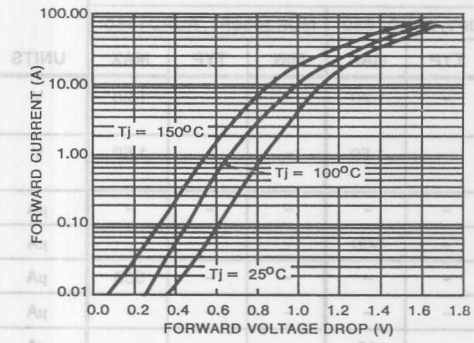


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

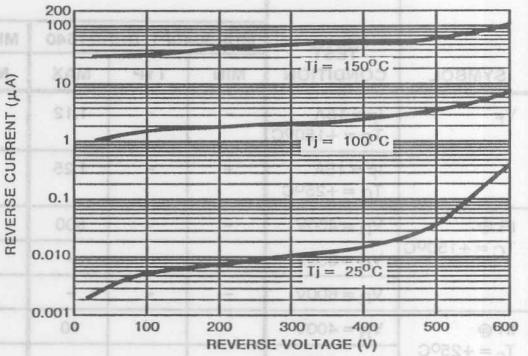


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

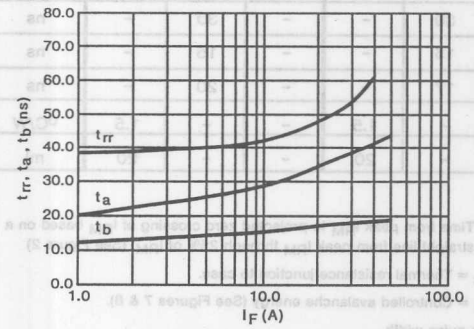


FIGURE 5. TYPICAL t_{rr}, t_a, t_b vs FORWARD CURRENT

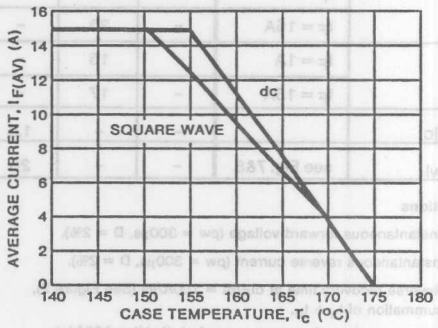


FIGURE 6. TYPICAL CURRENT DERATING CURVE w.r.t. CASE TEMPERATURE

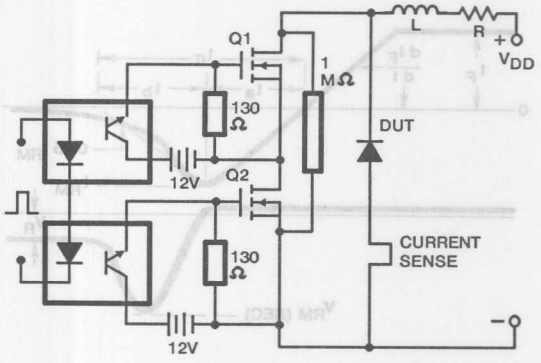


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

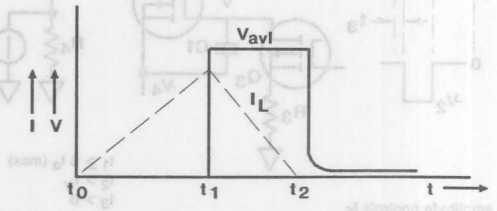


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $W_{avl} = (1/2)\ LI^2[V_{avl}/(V_{avl}-V_{dd})]$

HARRIS

RURD1610
RURD1615
RURD1620

Dual 16A High-Speed, High-Efficiency Epitaxial Silicon Rectifiers

August 1991

Features

- Ultrafast Recovery Time (t_{rr} < 35ns)
- Low Forward Voltage
- Low Thermal Resistance
- Planar Design
- Wire-Bonded Construction

Applications

- General Purpose
- Power Switching Circuits to 100kHz
- Full-Wave Rectification

Description

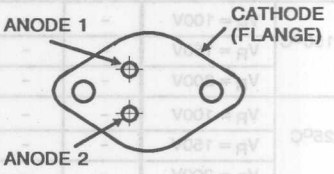
The RURD1610, RURD1615, RURD1620 are low forward voltage drop ultrafast rectifiers (t_{rr} < 35ns). They use an ion-implanted planar epitaxial construction.

These devices are intended for use as output rectifiers and flywheel diodies in a variety of high frequency pulse width modulated and switching regulators. Their low stored charge and attendant fast reverse recovery behavior minimize electrical noise generation and in many circuits markedly reduce the turn-on dissipation of the associated power switching transistors.

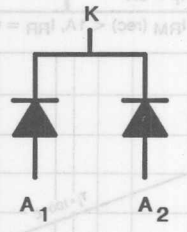
All are supplied in TO-204AA hermetic packages.

Package

TO-204AA
BOTTOM VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		RURD1610	RURD1615	RURD1620
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Average Rectified Forward Current				
T_A = 25°C (No Heat Sink)	$I_{F(AV)}$	6A	6A	6A
T_A = 25°C (With Heat Sink)*	$I_{F(AV)}$	16A	16A	16A
T_C = 125°C	$I_{F(AV)}$	16A	16A	16A
Nonrepetitive Peak Surge Current (8.3ms, ½ cycle)	I_{FSM}	275A	275A	275A
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	1.5°C/W	1.5°C/W	1.5°C/W
Thermal Resistance Junction-to-Case (Total)	$R\theta_{JC}$	1.2°C/W	1.2°C/W	1.2°C/W
Thermal Resistance Junction-to-Ambient	$R\theta_{JA}$	30°C/W	30°C/W	30°C/W
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +150°C	-55°C to +150°C	-55°C to +150°C
Maximum Lead Temperature During Solder (At distance > ⅛" (3.17mm) from case or 10s max)	T_L	260°C	260°C	260°C

*Wakefield type 621 heat sink with convection cooling.

12

ULTRA-FAST RECTIFIERS

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File Number 1383.1

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURD1610			RURD1615			RURD1620			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 16A, T_C = +150°C	–	–	0.83	–	–	0.83	–	–	0.85	V
	I_F = 16A, T_C = +25°C	–	–	0.975	–	–	0.975	–	–	1	V
IR @ T_C = +150°C	V_R = 100V	–	–	500	–	–	500	–	–	500	µA
	V_R = 150V	–	–	–	–	–	1.5	–	–	–	µA
	V_R = 200V	–	–	–	–	–	–	–	–	1.5	µA
IR @ T_C = +25°C	V_R = 100V	–	–	15	–	–	–	–	–	–	µA
	V_R = 150V	–	–	–	–	–	15	–	–	–	µA
	V_R = 200V	–	–	–	–	–	–	–	–	15	µA
t_{rr}	I_F = 4A*	–	–	35	–	–	35	–	–	35	ns
$R_{\Theta jc}$		–	–	1.5	–	–	1.5	–	–	1.5	°C/W
$R_{\Theta ja}$		–	–	30	–	–	30	–	–	30	°C/W
C_J	V_R = 10V, I_F = 0A	–	80	–	–	80	–	–	80	–	pF

*dI_F/dt = 40A/µs, I_{RM} (rec) < 1A, I_{RR} = 0.25A.

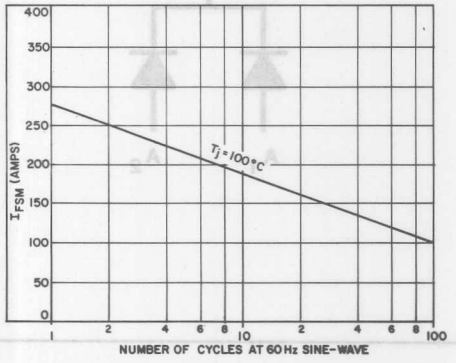


FIGURE 1. PEAK SURGE FORWARD CURRENT vs SURGE DURATION

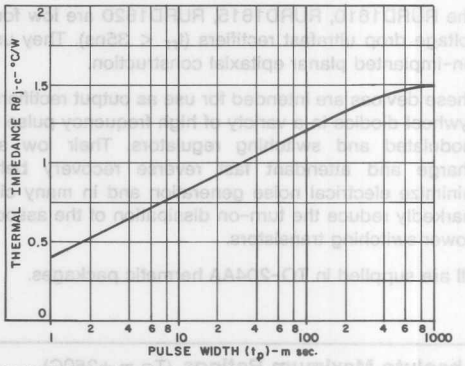


FIGURE 2. THERMAL IMPEDANCE vs PULSE WIDTH (PER JUNCTION)

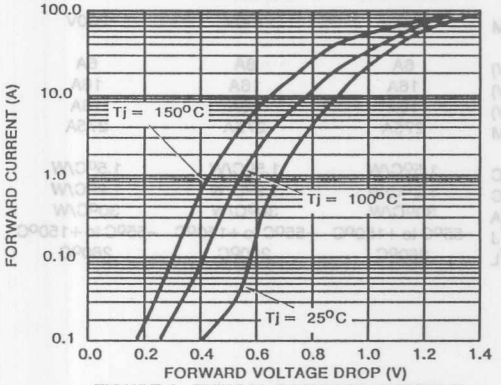


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

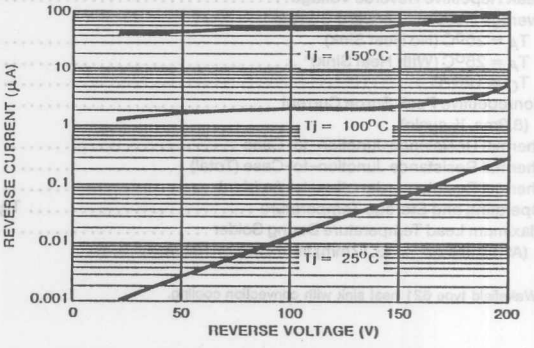


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

HARRIS

RURD3010
RURD3015
RURD3020

30A Ultrafast Dual Diode With Soft Recovery Characteristic

May 1991

Features

- Ultrafast with Soft Recovery Characteristic (t_{rr} < 45ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 200V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

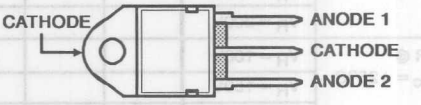
RURD3010, RURD3015, RURD3020 are ultrafast dual diodes (t_{rr} < 45ns) with soft recovery characteristics ($t_a/t_b \approx 1$). They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

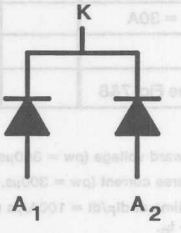
All are supplied in TO-218AC packages.

Package

TO-218AC
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		RURD3010	RURD3015	RURD3040
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Working Peak Reverse Voltage	V_{RWM}	100V	150V	200V
DC Blocking Voltage	V_R	100V	150V	200V
Average Rectified Forward Current (Total device forward current at rated V_R and T_C = 150°C)	$I_{F(AV)}$	30A	30A	30A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHz)	I_{FRM}	70A	70A	70A
Nonrepetitive Peak Surge Current (Surge Applied at rated load condition halfwave 1phase 60Hz)	I_{FSM}	325A	325A	325A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

12

ULTRA-FAST RECTIFIERS

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File Number 2773.1

Electrical Characteristics At Case Temperature (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	RURD3010 LIMITS			RURD3015 LIMITS			RURD3020 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +150°C			0.85			0.85			0.85	V
	I_F = 30A, T_C = +25°C			1.00			1.00			1.00	V
IR @ T_C = +150°C	V_R = 100V			500							µA
	V_R = 150V						500				µA
	V_R = 200V									500	µA
IR @ T_C = +25°C	V_R = 100V			30							µA
	V_R = 150V						30				µA
	V_R = 200V									30	µA
t_{rr}	I_F = 1A			45			45			45	ns
	I_F = 30A			50			50			50	ns
t_a	I_F = 1A		24			24			24		ns
	I_F = 30A		28			28			28		ns
t_b	I_F = 1A		17			17			17		ns
	I_F = 30A		20			20			20		ns
$R_{\Theta jc}$				1.2			1.2			1.2	°C/W
W_{avl}	see Fig. 7&8			20			20			20	mj

Definitions

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current (pw = 300µs, D = 2%).

t_{rr} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_a + t_b$.

t_a = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

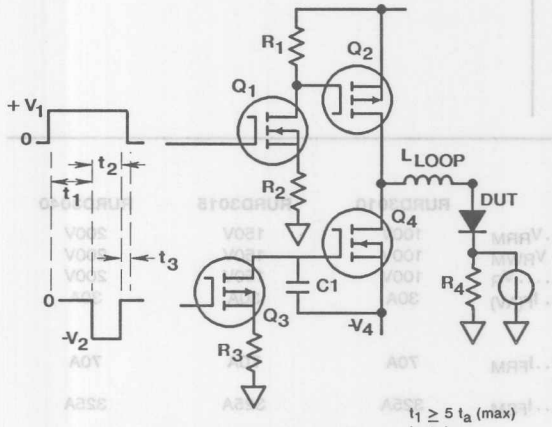
t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM}. (See Figure 2)

$R_{\Theta jc}$ = Thermal resistance junction to case.

W_{avl} = Controlled avalanche energy (See Figures 7 & 8).

pw = pulse width.

D = duty cycle.



V_1 amplitude controls I_F
V_2 amplitude controls di/dt
L_1 = self inductance of R_4

$t_1 \geq 5\ t_a$ (max)
$t_2 > t_{rr}$
$t_3 > 0$
$\frac{L_1}{R_4} \leq \frac{t_a\ (min)}{10}$

FIGURE 1. t_{rr} TEST CIRCUIT

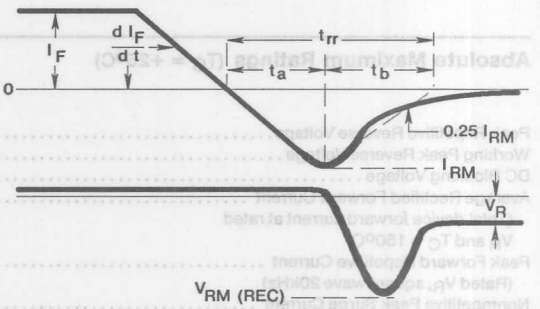


FIGURE 2. DEFINITIONS OF t_{rr}, t_a AND t_b

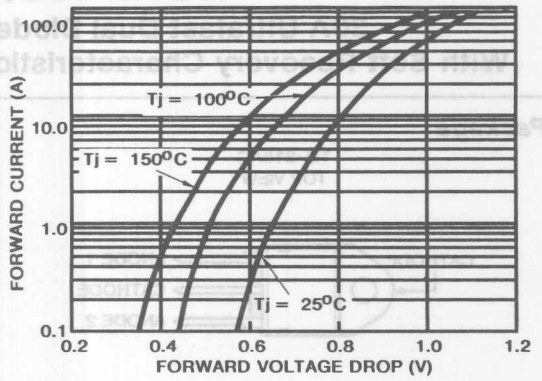


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

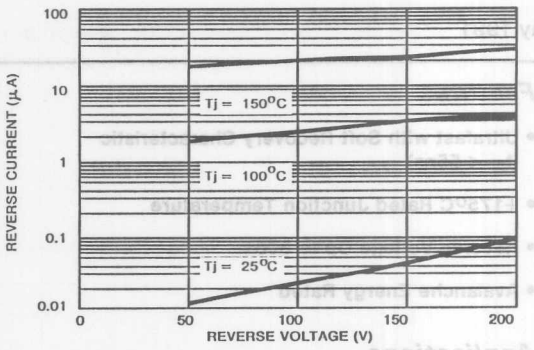


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

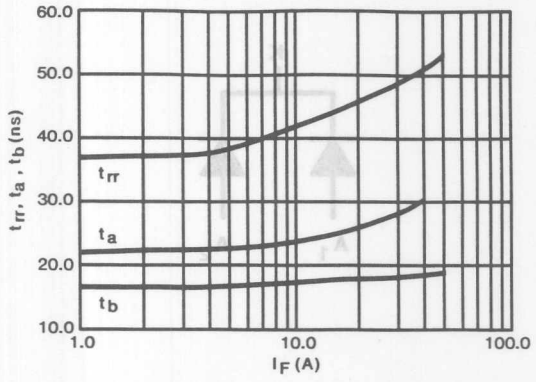


FIGURE 5. TYPICAL t_{rr}, t_a, t_b vs FORWARD CURRENT

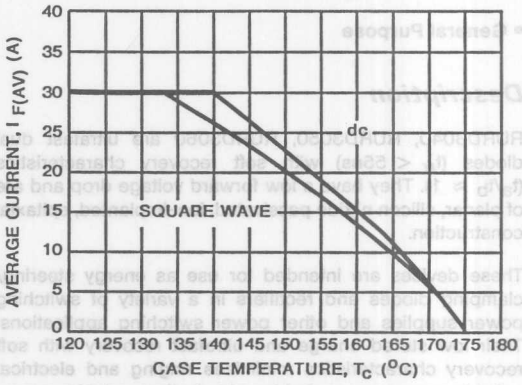


FIGURE 6. TYPICAL CURRENT DERATING CURVE w.r.t. CASE TEMPERATURE

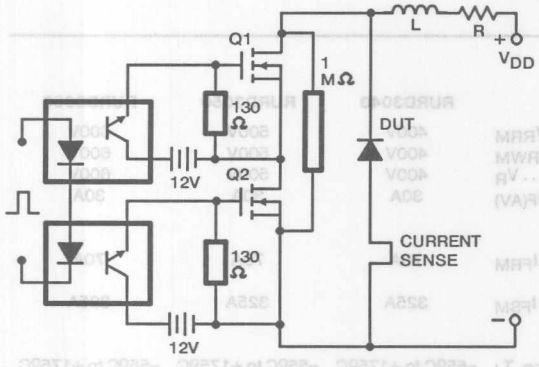


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

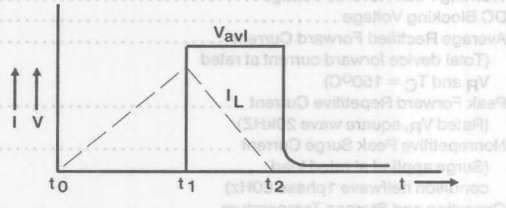


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L peak = 1A$, $L = 40mH$, $R < 0.1\Omega$, $W_{avl} = (1/2)\ LI^2[V_{avl}/(V_{avl}-V_{dd})]$

HARRIS

RURD3040
RURD3050
RURD3060

30A Ultrafast Dual Diode With Soft Recovery Characteristic

May 1991

Features

- Ultrafast with Soft Recovery Characteristic (t_{rr} < 55ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 600V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

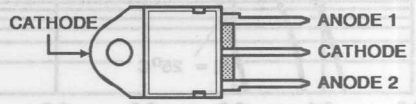
RURD3040, RURD3050, RURD3060 are ultrafast dual diodes (t_{rr} < 55ns) with soft recovery characteristics ($t_a/t_b \approx 1$). They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

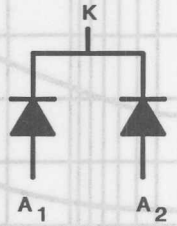
All are supplied in TO-218AC packages.

Package

TO-218AC
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		RURD3040	RURD3050	RURD3060
Peak Repetitive Reverse Voltage	V_{RRM}	400V	500V	600V
Working Peak Reverse Voltage	V_{RWM}	400V	500V	600V
DC Blocking Voltage	V_R	400V	500V	600V
Average Rectified Forward Current (Total device forward current at rated V_R and T_C = 150°C)	$I_{F(AV)}$	30A	30A	30A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHZ)	I_{FRM}	70A	70A	70A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1phase 60Hz)	I_{FSM}	325A	325A	325A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

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File Number **2772.1**

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified.

SYMBOL	TEST CONDITION	RURD3040 LIMITS			RURD3050 LIMITS			RURD3060 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +150°C	-	-	1.30	-	-	1.30	-	-	1.30	V
	I_F = 30A, T_C = +25°C	-	-	1.50	-	-	1.50	-	-	1.50	V
IR @ T_C = +150°C	V_R = 400V	-	-	1	-	-	-	-	-	-	mA
	V_R = 500V	-	-	-	-	-	1	-	-	-	mA
	V_R = 600V	-	-	-	-	-	-	-	-	1	mA
IR @ T_C = +25°C	V_R = 400V	-	-	30	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	30	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	30	µA
t_{rr}	I_F = 1A	-	-	55	-	-	55	-	-	55	ns
	I_F = 30A	-	-	60	-	-	60	-	-	60	ns
t_a	I_F = 1A	-	20	-	-	20	-	-	20	-	ns
	I_F = 30A	-	38	-	-	38	-	-	38	-	ns
t_b	I_F = 1A	-	15	-	-	15	-	-	15	-	ns
	I_F = 30A	-	20	-	-	20	-	-	20	-	ns
$R_{\Theta jc}$		-	-	1.2	-	-	1.2	-	-	1.2	°C/W
W_{avl}	see Fig. 7&8	-	-	20	-	-	20	-	-	20	mj

Definitions

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current (pw = 300µs, D = 2%).

t_{rr} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_a + t_b$.

t_a = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

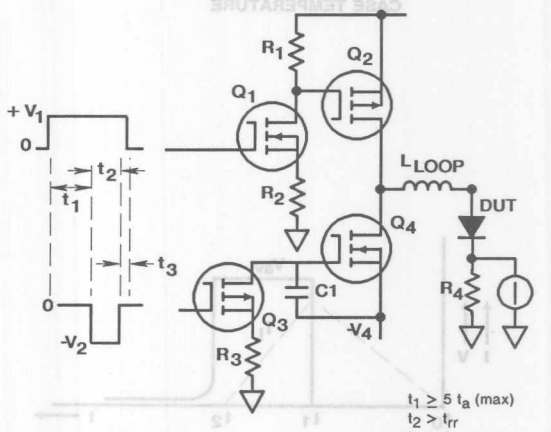
t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM}. (See Figure 2)

$R_{\Theta jc}$ = Thermal resistance junction to case.

W_{avl} = Controlled avalanche energy (See Figures 7 & 8).

pw = pulse width.

D = duty cycle.



$t_1 \geq 5\ t_a$ (max)
$t_2 > t_{rr}$
$t_3 > 0$
$\frac{L_1}{R_4} \leq \frac{t_a\ (min)}{10}$

V_1 amplitude controls I_F
V_2 amplitude controls di/dt
L_1 = self inductance of R_4

FIGURE 1. t_{rr} TEST CIRCUIT

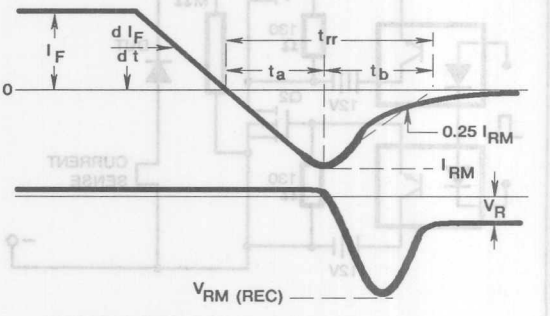


FIGURE 2. DEFINITIONS OF t_{rr}, t_a AND t_b

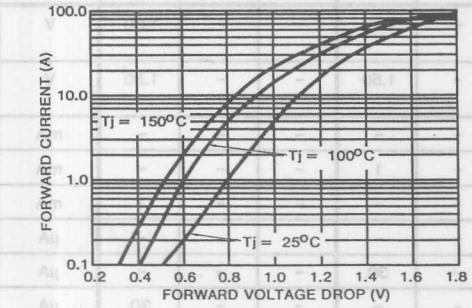


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

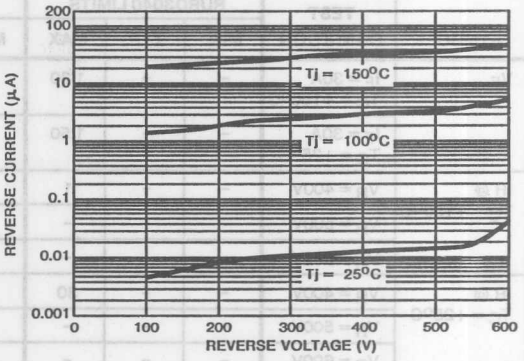


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

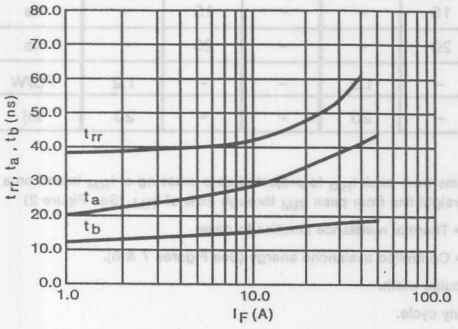


FIGURE 5. TYPICAL t_{rr}, t_a, t_b vs FORWARD CURRENT

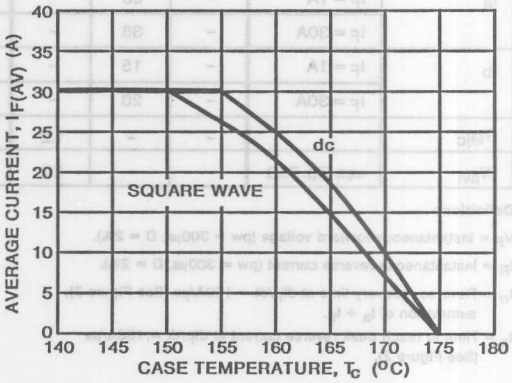


FIGURE 6. TYPICAL CURRENT DERATING CURVE w.r.t. CASE TEMPERATURE

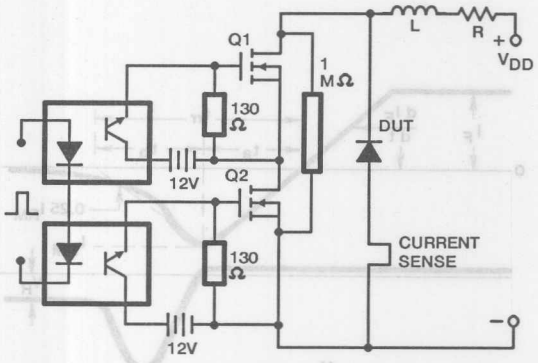


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

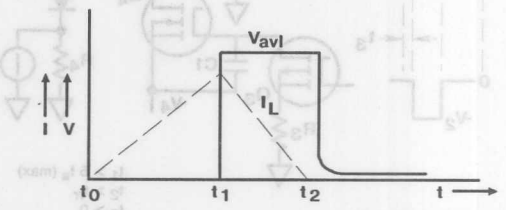


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $W_{avl} = (1/2)\ LI^2[V_{avl}/(V_{avl}-V_{dd})]$

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Harris Semiconductor

APPNOTE

No. 7244.1 May 1992

Harris Power MOSFETs

UNDERSTANDING POWER MOSFETs

Author: Tom McNulty

Power MOSFETs (Metal Oxide Semiconductor, Field Effect Transistors) differ from bipolar transistors in operating principles, specifications, and performance. In fact, the performance characteristics of MOSFETs are generally superior to those of bipolar transistors: significantly faster switching time, simpler drive circuitry, the absence of a second-breakdown failure mechanism, the ability to be paralleled, and stable gain and response time over a wide temperature range. This note provides a basic explanation of general MOSFET characteristics, and a more thorough discussion of structure, thermal characteristics, gate parameters, operating frequency, output characteristics, and drive requirements.

General Characteristics

A conventional n-p-n bipolar power transistor is a current-driven device whose three terminals (base, emitter, and collector) are connected to the body by silicon contacts. Bipolar transistors are described as minority-carrier devices in which injected minority carriers recombine with majority carriers. A drawback of recombination is that it limits the device's operating speed. And because of its current-driven base-emitter input, a bipolar transistor present a low-impedance load to its driving circuit. In most power circuits, this low-impedance input requires somewhat complex drive circuitry.

By contrast, a power MOSFET is a voltage-driven device whose gate terminal, Figure 1(a), is electrically isolated from its silicon body by a thin layer of silicon dioxide (SiO_2). As a majority-carrier semiconductor, the MOSFET operates at much higher speed than its bipolar counterpart because there is no charge-storage mechanism. A positive voltage applied to the gate of an n-type MOSFET creates an electric field in the channel region beneath the gate; that is, the electric charge on the gate causes the p-region beneath the gate to convert to an n-type region, as shown in Figure 1(b). This conversion, called the surface-inversion phenomenon, allows current to flow between the drain and source through an n-type material. In effect, the MOSFET ceases to be an n-p-n device when in this state. The region between the drain and source can be represented as a resistor, although it does not behave linearly, as a conventional resistor would. Because of this surface-inversion phenomenon, then, the operation of a MOSFET is entirely different from that of a bipolar transistor, which always retain its n-p-n character.

By virtue of its electrically-isolated gate, a MOSFET is described as a high-input impedance, voltage-controlled device, whereas a bipolar transistor is a low-input-impedance, current-controlled device. As a majority-carrier semiconductor, a MOSFET stores no charge, and so can switch faster than a bipolar device. Majority-carrier semiconductors also tend to slow down as temperature increases. This effect, brought about by another phenomenon called carrier mobility (where mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) makes a MOSFET more resistive at elevated temperatures, and much more immune to the thermal-runaway problem experienced by bipolar devices.

A useful by-product of the MOSFET process is the internal parasitic diode formed between source and drain, Figure 1(c). (There is no equivalent for this diode in a bipolar transistor other than in a bipolar darlington transistor.) Its characteristics make it useful as a clamp diode in inductive-load switching.

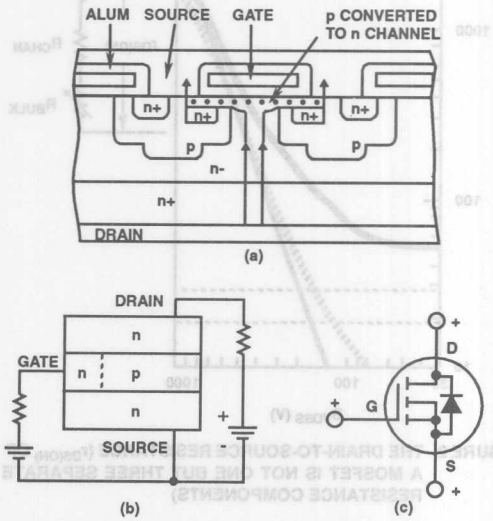


FIGURE 1. THE MOSFET, A VOLTAGE-CONTROLLED DEVICE WITH AN ELECTRICALLY ISOLATED GATE, USES MAJORITY CARRIERS TO MOVE CURRENT FROM SOURCE TO DRAIN (A). THE KEY TO MOSFET OPERATION IS THE CREATION OF THE INVERSION CHANNEL BENEATH THE GATE WHEN AN ELECTRIC CHARGE IS APPLIED TO THE GATE (B). BECAUSE OF THE MOSFETs CONSTRUCTION, AN INTEGRAL DIODE IS FORMED ON THE DEVICE (C), AND THE DESIGNER CAN USE THIS DIODE FOR A NUMBER OF CIRCUIT FUNCTIONS.

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Structure

Harris Power MOSFETs are manufactured using a vertical double-diffused process, called VDMOS or simply DMOS. A DMOS MOSFET is a single silicon chip structured with a large number of closely packed, hexagonal cells. The number of cell varies according to the dimensions of the chip. For example, a 120-mil^2 chip contains about 5,000 cells; a 240-mil^2 chip has more than 25,000 cells.

One of the aims of multiple-cells construction is to minimize the MOSFET parameter $r_{DS(ON)}$, or resistance from drain to source, when the device is in the on-state. When $r_{DS(ON)}$ is minimized, the device provides superior power-switching performance because the voltage drop from drain to source is also minimized for a given value of drain-to-source current.

Since the path between drain and source is essentially resistive, because of the surface-inversion phenomenon, each cell in the device can be assumed to contribute an amount, R_n, to the total resistance. An individual cell has a fairly low resistance, but to minimize $r_{DS(ON)}$, it is necessary to put a large number of cells in parallel on a chip. In general, therefore, the greater the number of paralleled cells on a chip, the lower its $r_{DS(ON)}$ value:

$r_{DS(ON)} = R_N/N$, where N is the number of cells.

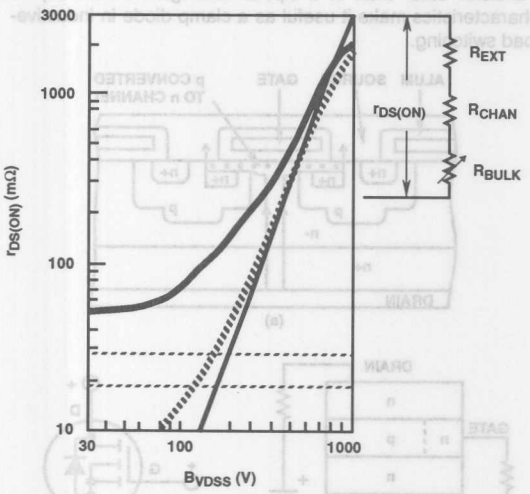


FIGURE 2. THE DRAIN-TO-SOURCE RESISTANCE ($r_{DS(ON)}$ OF A MOSFET IS NOT ONE BUT THREE SEPARATE RESISTANCE COMPONENTS)

TABLE 1. PERCENTAGE RESISTANCE COMPONENTS FOR A TYPICAL CHIP

B_{VDSS}	40V	150V	500V
$R_{CHANNEL}$	50%	23%	2.4%
R_{BULK}	35%	70%	97%
$R_{EXTERNAL}$	15%	7%	<1%

In reality, $r_{DS(ON)}$ is composed of three separate resistances. Figure 2 shows a curve of the three resistive components for a single cell and their contributions to the overall value of $r_{DS(ON)}$. The value of $r_{DS(ON)}$ at any point of the curve is found by adding the values of the three components at that point:

$$r_{DS(ON)} = R_{BULK} + R_{CHAN} + R_{EXT}$$

where R_{CHAN} represents the resistance of the channel beneath the gate, and R_{EXT} includes all resistances resulting from the substrate, solder connections, leads, and the package. R_{BULK} represents the resistance resulting from the narrow neck of n material between the two players, as shown in Figure 1(a), plus the resistance of the current path below the neck and through the body of the device to the drain.

Note in Figure 2 that R_{CHAN} and R_{EXT} are completely independent of voltage, while R_{BULK} is highly dependent on applied voltage. Note also that below about 150 volts, $r_{DS(ON)}$ is dominated by the sum of R_{CHAN} and R_{EXT}. Above 150 volts, $r_{DS(ON)}$ is increasingly dominated by R_{BULK}. Table 1 gives a percentage breakdown of the contribution of each resistance for three values of voltage.

Two conclusions, inherent consequences of the laws of semiconductor physics, and valid for any DMOS device, can be drawn from the preceding discussion: First, $r_{DS(ON)}$ obviously increases with increasing breakdown-voltage capability of a MOSFET. Second, minimum $r_{DS(ON)}$ performance must be sacrificed if the MOSFET must withstand ever-higher breakdown voltages.

The significance of R_{BULK} in devices with a high voltage capability is due to the fact that thick, lightly doped epi layers are required for the drain region in order to avoid producing high electric fields (and premature breakdown) within the device. And as the epi layers are made thicker and more resistive to support high voltages, the bulk component of resistance rapidly increases (see Figure 2) and begins to dominate the channel and external resistance. The $r_{DS(ON)}$ therefore, increases with increasing breakdown voltage capability, and low $r_{DS(ON)}$ must be sacrificed if the MOSFET is to withstand even higher breakdown voltages.

There is a way around these obstacles. The $r_{DS(ON)}$ in Figure 2 holds only for a relatively small chip. Using a larger chip results in a lower value for $r_{DS(ON)}$ because a large chip has more cells (See Figure 3). A larger chip also increases MOSFET breakdown voltage capability.

The penalty for using a larger chip, however, is an increase in cost, since chip size is a major cost factor. And because chip area increases exponentially, not linearly, with voltage, the additional cost can be substantial. For example, to obtain a given $r_{DS(ON)}$ at a breakdown voltage twice as great as the original, the new chip requires an area four or five times larger than the original. Although the cost does not rise exponentially, it is substantially more than the original cost.

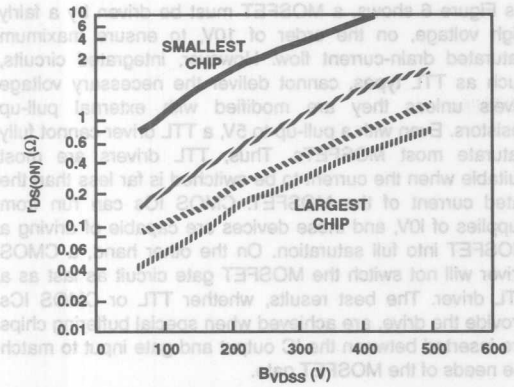


FIGURE 3. AS CHIP SIZE INCREASES, $r_{DS(ON)}$ DECREASES, & VOLTAGE HANDLING CAPABILITY INCREASES

Effects of Temperature

The high operating temperatures of bipolar transistors area frequent cause of failure. The high temperatures are caused by hot-spotting, the tendency of current in a bipolar device to concentrate in areas around the emitter. Unchecked, this hot-spotting results in the mechanism of thermal runaway, and eventual destruction of the device. MOSFETs do not suffer this disadvantage because their current flow is in the form of majority carriers. The mobility of majority carriers (where, again, mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) is temperature dependent in silicon: mobility decreases with increasing temperature. This inverse relationship dictates that the carriers slowdown as the chip gets hotter. In effect, the resistance of the silicon path is increased, which prevents the concentrations of current that lead to hot spots. In fact, if hot spots do attempt to form in a MOSFET, the local resistance increases and defocuses or spreads out the current, rerouting it to cooler portions of the chip.

Because of the character of its current flow, a MOSFET has a positive temperature coefficient of resistance, as shown by the curves of Figure 4.

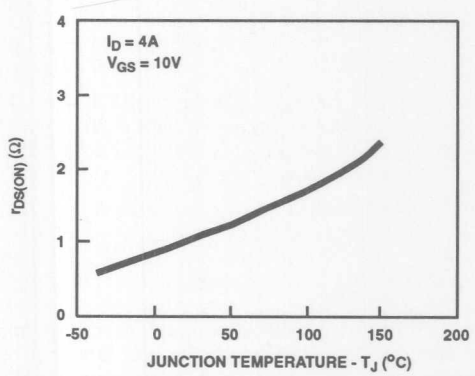


FIGURE 4. MOSFETs HAVE A POSITIVE TEMPERATURE COEFFICIENT OF RESISTANCE, WHICH GREATLY REDUCES THE POSSIBILITY OF THERMAL RUNAWAY AS TEMPERATURE INCREASES

The positive temperature coefficient of resistance means that a MOSFET is inherently stable with temperature fluctuation, and provides its own protection against thermal runaway and second breakdown. Another benefit of this characteristic is that MOSFETs can be operated in parallel without fear that one device will rob current from the others. If any device begins to overheat, its resistance will increase, and its current will be directed away to cooler chips.

Gate Parameters

To permit the flow of drain-to-source current in an n-type MOSFET, a positive voltage must be applied between the gate and source terminals. Since, as described above, the gate is electrically isolated from the body of the device, theoretically no current can flow from the driving source into the gate. In reality, however, a very small current, in the range of tens of nanoamperes, does flow, and is identified on data sheets as a leakage current, I_{GSS}. Because the gate current is so small, the input impedance of a MOSFET is extremely high (in the megohm range) and, in fact, is largely capacitive rather than resistive (because of the isolation of the gate terminal).

Figure 5 illustrates the basic input circuit of a MOSFET. The elements are equivalent, rather than physical, resistance, R, and capacitance, C. The capacitance, called C_{ISS} on MOSFET data sheets, is a combination of the device's internal gate-to-source and gate-to-drain capacitance. The resistance, R, represents the resistance of the material in the gate circuit. Together, the equivalent R and C of the input circuit determine the upper frequency limit of MOSFET operation.

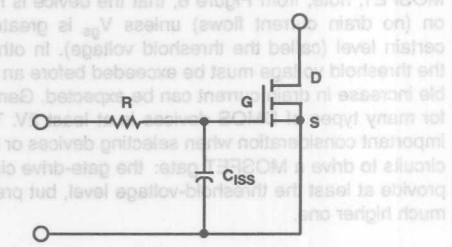


FIGURE 5. A MOSFETs SWITCHING SPEED IS DETERMINED BY ITS INPUT RESISTANCE R AND ITS INPUT CAPACITANCE C_{ISS}

Operating Frequency

Most DMOS processes develop the polysilicon gate structure rather than the older metal-gate type. If the resistance of the gate structure (R in Figure 5) is high, the switching time of the DMOS device is increased, thereby reducing its upper operating frequency. Compared to a metal gate, a polysilicon gate has a higher gate resistance. This property accounts for the frequent use of metal-gate MOSFET in high-frequency (greater than 20MHz) applications, and polysilicon-gate MOSFETs in higher-power but lower-frequency systems.

Since the frequency response of a MOSFET is controlled by the effective R and C of its gate terminal, a rough estimate can be made of the upper operating frequency from

datasheet parameters. The resistive portion depends on the sheet resistance of the polysilicon-gate overlay structure, a value of approximately 20W/□. But whereas the total R value is not found on datasheets, the C value (C_{ISS}) is; it is recorded as both a maximum value and in graphical form as a function of drain-to-source voltage. The value of C_{ISS} is closely related to chip size; the larger the chip, the greater the value. Since the RC combination of the input circuit must be charged and discharged by the driving circuit, and since the capacitance dominates, larger chips will have slower switching times than smaller chips, and are, therefore, more useful in lower-frequency circuits. In general, the upper frequency limit of most power MOSFETs spans a fairly broad range, from 1MHz to 10MHz.

Output Characteristics

Probably the most used MOSFET graphical data is the output characteristics or plot of drain-to-source voltage (V_{DS}) as a function of drain-to-source current (I_D). A typical characteristic, shown in Figure 6, gives the drain current that flows at various V_{DS} values as a function of the gate-to-source voltage (gs). The curve is divided into two regions: a linear region in which V_{DS} is small and drain current increases linearly with drain voltage, and a saturated region in which increasing drain voltage has no effect on drain current (the device acts as a constant-current source). The current level at which the linear portion of the curve joins with the saturated portion is called the pinch-off region.

Drive Requirements

When considering the V_{gs} level required to operate a MOSFET, note, from Figure 6, that the device is not turned on (no drain current flows) unless V_{gs} is greater than a certain level (called the threshold voltage). In other words, the threshold voltage must be exceeded before an appreciable increase in drain current can be expected. Generally V_{gs} for many types of DMOS devices is at least 2V. This is an important consideration when selecting devices or designing circuits to drive a MOSFET gate: the gate-drive circuit must provide at least the threshold-voltage level, but preferably, a much higher one.

As Figure 6 shows, a MOSFET must be driven by a fairly high voltage, on the order of 10V, to ensure maximum saturated drain-current flow. However, integrated circuits, such as TTL types, cannot deliver the necessary voltage levels unless they are modified with external pull-up resistors. Even with a pull-up to 5V, a TTL driver cannot fully saturate most MOSFETs. Thus, TTL drivers are most suitable when the current to be switched is far less than the rated current of the MOSFET. CMOS ICs can run from supplies of l0V, and these devices are capable of driving a MOSFET into full saturation. On the other hand, a CMOS driver will not switch the MOSFET gate circuit as fast as a TTL driver. The best results, whether TTL or CMOS ICs provide the drive, are achieved when special buffering chips are inserted between the IC output and gate input to match the needs of the MOSFET gate.

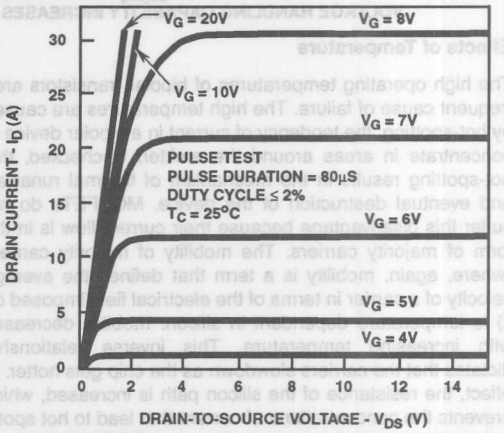


FIGURE 6. MOSFETs REQUIRE A HIGH INPUT VOLTAGE (AT LEAST 10V) IN ORDER TO DELIVER THEIR FULL RATED DRAIN CURRENT

APPNOTE

No. 7254.1 May 1992

SWITCHING WAVEFORMS OF THE L²FET: A 5 VOLT GATE-DRIVE POWER MOSFET

Author: C. Frank Wheatley, Jr. and Harold R. Ronan, Jr.

The switching waveforms of a newly announced series of power MOSFET devices called Logic Level FETs (L²FETs) and featuring a 5V gate drive are presented and contrasted with those of the more conventional 10V gate drive devices. A new method of characterizing MOSFET switching performance is discussed in which the MOSFET is treated as a vertical JFET driven in cascade from a low voltage lateral MOS. The 2:1 advantage in rise and fall time and the 4:1 reduction in switching "dynamic $V_{(SAT)}$" dissipation with constant drive power of the L²FET over the 10V MOSFET are demonstrated and discussed

Background

A new series of power MOSFET devices called Logic Level FETs, or L²FETs, is compatible with the 5V power supply used for logic circuitry. L²FETs retain the on resistance, drain current, and blocking voltage ratings of their 10V predecessors, but operate from a much less costly 5V supply.

The reduction in gate drive voltage is the result of halving the thickness of the gate insulator from the industry standard 100nm to 50nm (500Å). Since the surface inversion of the MOS channel is determined by the gate insulator voltage field, halving the insulator thickness halves the applied gate voltage without compromising drain characteristics.

The apparent conclusion from a study of the switching waveforms of the new device that halving the gate oxide thickness would double the gate capacitance and halve the switching speed does not prove true. Measurements demonstrate empirically a 2:1 increase in switching speed for the L²FET over its 100nm predecessor, where gate drive power is the same for both devices. The "dynamic $V_{(SAT)}$" dissipation is lowered by a factor of four. The apparent anomalies are explained with the aid of a new method of switching characterization developed by treating the power MOSFET as a grounded gate, depletion mode, vertical JFET driven in cascade by a grounded source, enhancement mode, lateral MOS. The waveforms and switching characterization methods are described in detail below.

L²FET Characteristics Compared to Standard Types - A Brief Review

Thirty-two different power MOSFETs of the L²FET structure have been announced. These devices were designed to be totally interchangeable with the standard power MOSFET with respect to output characteristics, while offering twice the gate sensitivity, as shown in Figures 1, 2, and 3, which are comparisons of the industry standard RFM10N15 with its Logic Level FET counterpart, the RFM10N15L. (Although the L suffix notation in the type number will ultimately be valid for the entire product matrix, the L²FET product currently available is limited to n-channel devices handling 200V or less, with 15A ratings or less.)

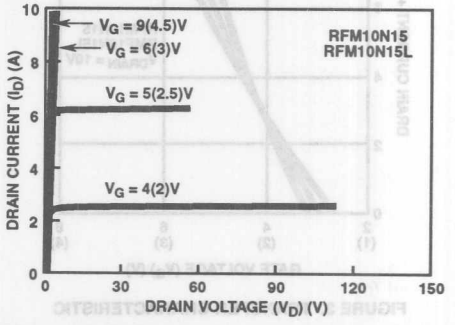


FIGURE 1. DRAIN CURRENT vs. DRAIN VOLTAGE CURVES FOR REPRESENTATIVE STANDARD AND L²FET DEVICES

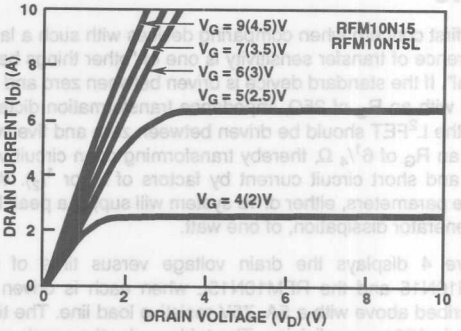


FIGURE 2. DRAIN CURRENT vs. LOW DRAIN VOLTAGE CURVES FOR REPRESENTATIVE STANDARD AND L²FET DEVICES DEMONSTRATING THAT R_{ON} HAS NOT BEEN SACRIFICED IN THE L²FET

Figures 1 and 2 are plots of drain current versus drain voltage with gate voltage as the running parameter. The L²FET gate voltage is in parenthesis. The low drain voltage curves of Figure 2 demonstrate that RON has not been sacrificed in the L²FET. Figure 3 is the transfer characteristic comparison

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for three different temperatures. The abscissa has two scales to reflect the different gate sensitivities; again, L values are in parenthesis. It is evident from the curve that:

1. The threshold voltage is scaled down by a factor of two for the L^2FET.
2. The thresholf voltage temperature coefficient in mV/°C is scaled down.
3. The current level for zero temperature coefficient is unchanged.
4. The transconductance is scaled up by a factor of two.

All other L^2FETs have similar relationships to their respective predecessors.

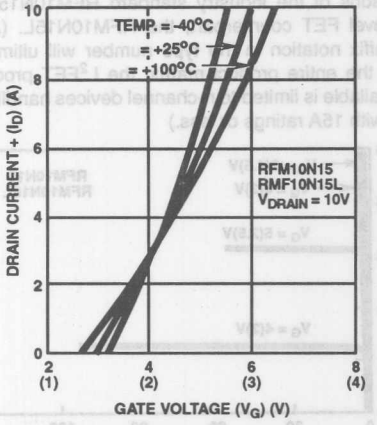


FIGURE 3. TRANSFER CHARACTERISTIC

Switching Waveforms with Conventional Drive

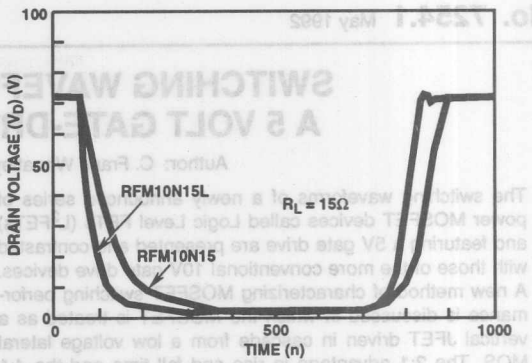
The first concern when comparing devices with such a large difference of transfer sensitivity is one of "other things being equal". If the standard device is driven between zero and ten volts with an R_G of 25Ω, impedance transformation dictates that the L^2FET should be driven between zero and five volts with an R_G of $6^1/_4$ Ω, thereby transforming open circuit voltage and short circuit current by factors of 2 (or $^1/_2$). With these parameters, either drive system will supply a peak R_G, or generator dissipation, of one watt.

Figure 4 displays the drain voltage versus time of the RFM10N15 and the RFM10N15L when each is driven as described above with a 5A, 75V resistive load line. The time scale is 100ns per division. The table under the graph compares on delay time, rise time, off delay time, and fall time for each device. The times are measured in the normal manner, that is, involving the 10% and 90% points of the input voltage and output voltage waveforms.

Note that:

1. The rise and fall times are not symmetrical
2. The is L^2FET faster
3. There is a "dynamic $V_{(SAT)}$" type of behavior
4. The "dynamic $V_{(SAT)}$" is of a lesser amplitude for the L^2FET

These observations are discussed below.



TYPE	GATE DRIVE	R_G (Ω)	$t_{D(ON)}$ (ns)	$t_{(RISE)}$ (ns)	$t_{D(OFF)}$ (ns)	$t_{(FALL)}$ (ns)
RFM10N15 (100nm)	0-10V	25	15	120	123	73
RFM10N15L (50nm)	0-5V	6.25	11	57	104	62

FIGURE 4. DRAIN VOLTAGE vs. TIME CURVES FOR REPRESENTATIVE STANDARED AND L^2FET DEVICES

Switching Waveforms with Constant Current Drive

The power MOSFET is a current driven device during transitions due to the charging or discharging of capacitances. In actual applications, most drive circuits exhibit a first order approximation to a constant current where the voltage compliance is determined by ground potential or the drive circuit power supply voltage. The on current may not equal the off current; this situation is addressed below.

Figure 5 presents the curves for the RFM10N15 and RFM10N15L when each is driven from a current generator whose $I_{G1} = I_{G2}$, with gate voltage limits of zero and 10 or (5) volts. The drive current is kept the same for both devices in this case even though the L^2FET receives less drive power or energy. The value for I_{G1} and I_{G2} was chosen as 5mA; the time scale is 1µs/division.

Note that:

1. The rise and fall times of a given device are the same with current drive.
2. The two devices have similar output waveforms in most regions.
3. There is a persistent "dynamic $V_{(SAT)}$" even at slow switching speeds.

4. The "dynamic $V_{(SAT)}$" curves are symmetrical during the low drain voltage portion of the turn on and turn off portion.
5. The "dynamic $V_{(SAT)}$" curves are lower in amplitude by a factor of approximately two for the L^2FET.

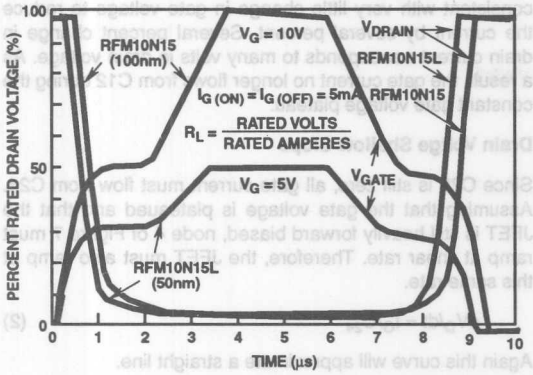


FIGURE 5. CHARACTERIZATION CURVES FOR REPRESENTATIVE DEVICES DRIVEN FROM A CURRENT GENERATOR

Large Signal Equivalent Circuit of the MOSFET

If we are to understand the differences and similarities of the L^2FET relative to the conventional power MOSFET, the conventional poer MOSFET must first be understood. Figure 6 shows a properly proportioned cross sectional view of the power MOSFET.

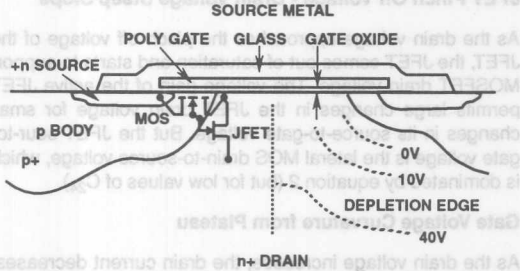


FIGURE 6. CROSS SECTION OF POWER MOSFET

When the drain voltage is very low and the gate is forward biased, an accumulation layer exists for the n- region beneath the gate. This layer may be thought of as serving the function of the drain for the lateral MOS. In addition, it serves as a source for a vertical depletion mode JFET. The gate of the JFET is formed by the body diffusion, particularly in the neck region. The JFET drain is the n+ region usually though of as being the MOSFET drain. This situation is shown in Figure 6, where the cross sectional view of the MOSFET is shown. The lateral MOS and the vertical JFET are schematically implied by the left half of Figure 6. The right half indicates the edge of the depletion width for several drain voltges. Note how the JFET pinches off, such that increased drain voltage is supported predominately by the JFET. This structure is schematically represented as shown in Figure 7. Note that the third quadrant diode is caused by the p-n junction associated with the gate and drain characteristic (common to all JFETs). A parasitic n-p-n transistor is not shown, nor is it discussed in this Note. Voltage node (4) is within the device, and is not precisely a single node, as represented.

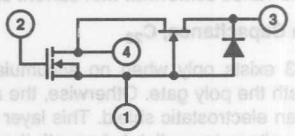


FIGURE 7. SCHEMATIC REPRESENTATION OF THE CROSS SECTION OF FIGURE 6

Interelectrode Capacitance

The equivalent circuit of Figure 7 contains four voltage nodes. Therefore, six capacitors will exist to couple these nodes. The switching waveforms are determined by these capacitors and the samll signal equivalent circuit of the MOS and JFET. Of course, the MOS and JFET small signal equivalent circuits are nonlinear functions of voltage and current and invarient with frequency. Similarly, the capacitors are nonlinear with voltage and current.

Industry data sheets show three terminal characterization of this four node network at zero drain current. Under this condition, the transconductance and output resistance are zero and infinity for both the MOS and the JFET. This condition reducesthe power MOSFET to the capactor network of Figure 8, which may be replaced by three capacitors. Note that this situation is valid only when no MOSFET current flows.

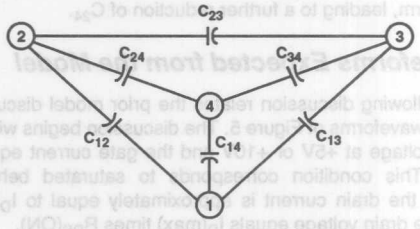


FIGURE 8. CAPACITOR NETWORK REPRESENTATION OF THE POWER MOSFET

When current does flow, node (4) of Figure 7 is a low impedance node due to the source follower characteristic of the JFET. Similarly, nodes (1) and (3) are generally low impedance nodes by virtue of the ground reference and the load resistance. Therefore, capacitive currents will usually be significant only to the input node, (2). Capacitors C_{12}, C_{23}, and C_{24} are examined below over most of the switching regime when current is flowing.

Gate to Source Capacitance, C_{12}

When all of the die except the actual MOSFET cells are ignored, Figure 6 shows that the gate to source capacitance (C_{12}) is that from the poly gate upward through the thick oxide to the source metal. In addition, there is a contribution from the poly gate to the n+ source through the thin gate oxide. Additionaly a fringing capacitance exists at the edge of the polysil gate. These components of C_{12} are invariant with voltage and current. There is a fourth component from the poly gate to a region about half way along the MOS channel through the gate oxide. This component is actually distributed, and varies somewhat with current and voltage.

Gate to Drain Capacitance, C_{23}

Capacitor C23 exists only when no accumulation layer is present beneath the poly gate. Otherwise, the accumulation layer acts as an electrostatic shield. This layer exists whenever the drain voltage immediately beneath the gate oxide is essentially negative relative to the poly gate. In addition, the capacitive coupling from drain to gate diminishes greatly when the JFET is pinched off. Therefore, C23 exists for only a small range of drain voltage. In addition, it should decrease rapidly as the pinch-off voltage level is approached because the effective area of concern is closed off similarly to the aperture of a camera (for a hex cell).

Gate to Internal Electrode Capacitance, C_{24}

Capacitor C_{24} is rather large for positive gate voltages. It is made up of that area between the poly gate and the accumulation layer, plus some of the area between the poly gate and the moddle of the MOS channel. In both cases, the dielectric is the thin gate oxide. So long as the gate voltage is positive relative to the n- layer beneath the poly gate, the accumulation layer exists and C_{24} is invariant. This accumulatin layer ceases to exist when the external drain voltage minus the IR drop through the n- neck region approximately equals the gate voltage. The area associated with the accumulation layer (JFET cathode) rapidly decreases with increased drain voltage. In addition, a depletion layer may now form, leading to a further reduction of C_{24}.

Waveforms Expected from the Model

The following discussion relates the prior model discussion to the waveforms of Figure 5. The discussion begins with the gate voltage at +5V or +10V and the gate current equal to zero. This condition corresponds to saturated behavior, where the drain current is approximately equal to I_D(max) and the drain voltage equals I_D(max) times R_{DS}(ON).

Gate Voltage Slope - t_{OFF} Delay

As time progresses, I_G = -5mA, which must flow through C_{12} + C_{23} + C_{24} of Figure 8 because the MOS and JFET are both heavily biased into conduction. Therefore, $dV_4/dt = dV_3/dt$ = nearly 0. With large positive gate bias and drain voltage near zero, C_{23} is zero and C_{12} and C_{24} are constant. As a result, the gate voltage should be a straight line with a slope equal to:

$$dV_G/dt = I_G/(C_{12} = C_{24}) \quad (1)$$

Gate Voltage Plateau

As the gate voltage decreases, the drain voltage will increase imperceptibly at first until the gate voltage drops enough to bias the MOS into its constant current mode. At this point, the very high transconductance of the MOS is consistent with very little change in gate voltage to reduce the current by several percent. Several percent change in drain current corresponds to many volts in drain voltage. As a result, the gate current no longer flows from C12 during the constant gate voltage plateau.

Drain Voltge Shallow Slope

Since C23 is still zero, all gate current must flow from C24. Assuming that the gate voltage is plateaued and that the JFET is still heavily forward biased, node 4 of Figure 7 must ramp at linear rate. Therefore, the JFET must also ramp at this same rate.

$$dV_D/dt = I_G/C_{24} \quad (2)$$

Again this curve will approximate a straight line.

Drain Transition Voltage

As mentioned above, C_{24} rapidly decreases once the drain voltage is slightly greater than the gate voltage. (Actually, this voltage is the n- voltage directly beneath the gae oxide, and differs from the drain voltage by an amount nearly equal to $I_D r_{DS}$(on).)

Since the drain voltage is still firly low and the drain current has not changed much, the gate plateau voltage still exists. Equation 2 still applies except that the value of C_{24} has materially decreased and C_{23} has become finite. This situation results in a substantial increase in dV_D/dt.

JFET Pinch Off Voltage - Drain Voltage Steep Slope

As the drain voltage approaches the pinch off voltage of the JFET, the JFET comes out of saturation and starts to support MOSFET drain voltage. The voltage gain of the active JFET permits large changes in the JFET drain voltage for small changes in its source-to-gate voltage. But the JFET sour-to-gate voltage is the lateral MOS drain-to-source voltage, which is dominated by equation 2 (but for low values of C_{24}).

Gate Voltage Curvature from Plateau

As the drain voltage increases, the drain current decreases. This condition requires significant decrease in gate voltage until the gate threshold is approached. A significant portion of the gate current must now flow through C_{12}. This flow produces a gradual transition in the gate voltage and some slowing of the drain voltage waveform.

Gate Voltage Slope - $t_{(ON)}$ Delay

When the drain is totally off, most of the gate current flows from C12. Again,this capacitance is constant, so that the waveform is a straight line with a slope equal to:

$$dV_G/dt = I_G/C_{12} \quad (3)$$

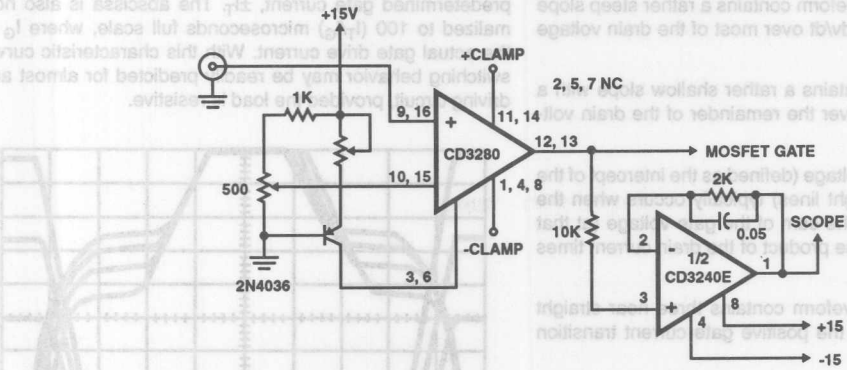


FIGURE 9. TEST CIRCUIT

New Switching Characterization for Power MOSFETs

The above discussion suggests that a new method of characterization may be provided for resistive switching with power MOSFETs, where constant current gate drive is employed during the transition time.[1] The below method bears some similarity to the gate charge concept.[2] The state of the gate charge is a continuous plot in this work, however, rather than a single point. This approach permits a knowledge of all waveforms with any drive dircuitry, rather than just the total elapsed time. In addition, the total elapsed time is fixed (at just under 50 microseconds) by choosing the required value of constant gate current. Circuit designers are usually more comfortable with milliamperes and microseconds (although the product is charged in nanocoulombs).

Test Circuit - Drive

A test circuit is shown in Figure 9. The heart of this circuit is the Harris CA3280 integrated circuit. This is an operational transconductance amplifier (OTA) operated as a comparator. An OTA is a current output circuit where the output current and output transconductance are programmed by the amplifier bias current (I_{ABC}). Internal chip circuit feedback assures an extremely high output impedance within a compliance range established by the supply voltages. The circuit of Figure 9 is actually two OTA's in parallel. The linearizing diodes on this chip are not used.

A value of I_{ABC} is established from the collector of the 2N4036. The current into the load (the gate of the MOSFET under test) may be varied between $+I_{ABC}$ and $-I_{ABC}$ times a constant of proportionality (approximaetly 0.9). The actual value depends upon the input differential input voltage. As a comparator, the differential voltage is large resulting in saturated behavior of $\pm I_{ABC}$. If the gate voltage comes within a volt of the rail voltages, this current goes to zero, producing a clamping voltage. For the purposes of this Note, these supply voltages are adjusted to clamp 0 volts and +10 volts for the normal n-channel MOSFET. The behavior of this IC is excellent from submicroamperes to about 2.5mA. Higher current may be achieved by stacking many CA3280 packages one on top of another and soldering the leads to aprallel the chips rather than wiring many sokets. However, this arrangement may require an increase in the bypass capacitor values.

A CA3240E MOS input op amp is used as a unity gain follower. Otherwise, the 1mΩ or 10mΩ shunting impedance of the scope would load the high impedance circuitry associated with the MOSFET gate.

Testing Conditions

A pulse generator is set for 50µs on time duration and approximately 25ms repetition rate (about 0.2% duty cycle). The ± clamp voltages are set to the appropriate values. The power MOSFET load resistor is chosen to equal the maximum rated voltage divided by the maximum rated current.

With a low value of drain supply voltage, observe the gate voltage while adjusting I_{ABC}. A convenient set f conditions occurs when a short dwell time of several µs exists at the +10V level. Minor adjustments may be desired for IABC as the drain supply voltage is increased to maximum rated value. The L^2FETs would be tested at +5V gate clamp.

Figure 10 exhibits the pertinent waveforms for an RFM15N15. All power MOSFETs have similar waveforms. Figure 10(a) is the 3V signal to the CA3280. Figure 10(b) is the power MOSFET gate current. In this example, the amplitude is ±1mA with a third state of 0mA. Figure 10(c) displays the gate voltage and the drain voltage, 10V peak-to-peak and 150V peak-to-peak. Figure 10(d) is a piece wise linear approximation of Figure 10(c). The datum line is zero volts and applies to both waveforms. The time scale of the waveforms of Figure 10 is 100µs full scale.

There are some features of the gate and drain voltage waveforms that should be noted. These features are consistent with the equivalent model discussion.

1. The waveforms during the positive gate current time are symmetrical to those during the negative gate current time. Exceptions will occur for very fast or very slow switching, and for nonsymetrical current drive. These exceptions are discussed in the following.

2. The drain voltage waveform contains a rather steep slope with a fairly constant dv/dt over most of the drain voltage excursion.
3. The drain voltage contains a rather shallow slope with a fairly constant dv/dt over the remainder of the drain voltage excursion.
4. The drain transition voltage (defined as the intercept of the above two near straight lines) typically occurs when the drain voltage equals the sum of the gate voltage (at that instant of time) plus the product of the drain current times $r_{DS}(on)$.
5. The gate voltage waveform contains three near straight line segments during the positive gate current transition time.

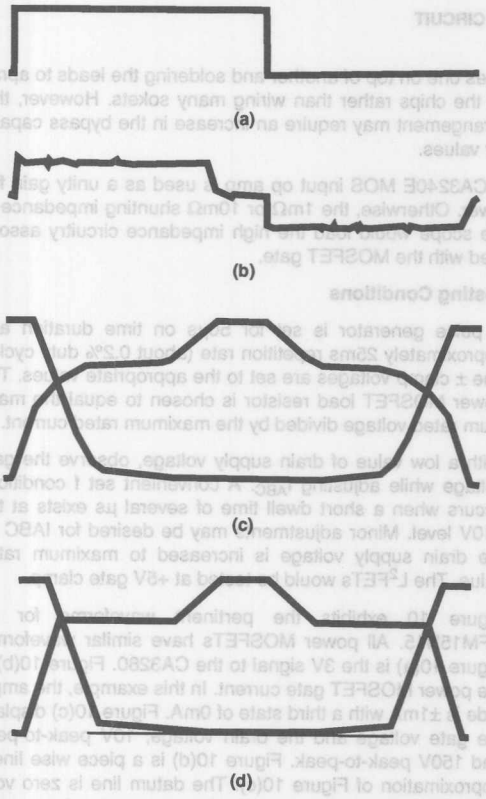


FIGURE 10. (a) 3V SIGNAL TO THE CA3280, (b) POWER MOSFET GATE CURRENT, (c) GATE AND DRAIN VOLTAGE, (d) PIECE WISE LINEAR APPROXIMATION OF 10(c)

Application of the Switching Data

Figure 11 is a family of curves similar to Figure 10(c), where the drain supply voltage is fixed at four values. Note that the ordinate is 10V full scale for the gate voltage, while it is normalized to 100% of maximum-rated drain voltage for the drain-voltage curves. All four sets of curves are taken with a predetermined gate current, $\pm I_T$. The abscissa is also normalized to 100 (I_T/I_G) microseconds full scale, where I_G is the actual gate drive current. With this characteristic curve, switching behavior may be readily predicted for almost any driving circuit, provided the load is resistive.

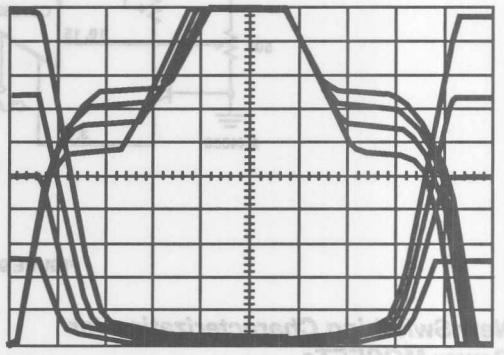


FIGURE 11. CURVES SIMILAR TO THOSE OF FIGURE 10(c) WITH DRAIN SUPPLY VOLTGE FIXED AT FOUR VALUES

Symmetrical Current Drive

Waveforms of Figure 11 will scale in an inverse manner with gate current. Driving current was varied from ±200mA to ±2µA for the device of Figure 1l. Measurements of delay time (on), rise time, delay time (off), and fall time are plotted in Figure 12 and compared to the inverse scaling suggested by Figure 11.

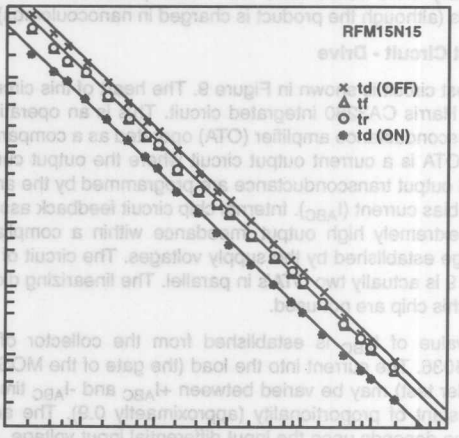


FIGURE 12. VARIOUS TIME MEASUREMENTS COMPARED TO THE INVERSE SCALING SUGGESTED BY FIGURE 11.

It is anticipated that very slow switching (in the millisecond region) will result in the chip thermally tracking the power dissipation, which would cause some deviation from the

inverse scaling. This condition was not noted on Figure 12 for gate currents as low as ±2μA.

Large gate currents result in very fast switching waveforms. The gate of each hex cell is accessed through a gate pad and gate runners, which are of a low resistivity metal followed by buried polysilicon of a moderate resistivity. Asa result, the high gate currents cause a propagation delay to exist for those cells far removed from the gate runners. This effect is not seen in Figure 12, even though the gate current was increased to ±200mA.

Asymmetrical Current Drive

The positive and negative gate drive will often be dissimilar. Of course, the scaling must reflect this situation. At other times the gate current varies with amplitude. This condition is always true when driving from a pulse generator of fixed resistance. Piecewise linear methods will yield the gate current, which will permit the proper piecewise linear scaling. This calculation could be done in the following manner:

1. Mark eleven small x's along the gate waveform of Figure 11 dividing it into 10 equal voltage segments; for example, V_G = 0, 1, 2, . . . 9, 10V.
2. Draw a vertical line through each x the full height of the figure, creating 10 time segments.
3. If the driving-pulse amplitude is 0 to 10 volts with an internal resistance of 100 ohms, calculate the piecewise linear gate current for each time segment. I_{G1} = (10 - 0.5)/100 = 95mA, I_{G2} = (10 -1.5)/100 = 85mA, etc.
4. Then scale each waveform within the pertinent time segment by the proper gate current.
5. Smooth the curves.
6. Create 10 more time segments for the right half of Figure 11 corresponding to an average gate voltage of 9.5,8.5, . . . 1.5, 0.5 volts. Call these segments 11,12,... 19,20.
7. In that the pulse-generator voltage is now zero volts, calculate I_G as:
   I_{G11} = (0-9.5)/100 = -95mA, I_{G12} = (0-8.5)/100 = -85mA, etc.
8. Repeat 4 and 5. L^2FETs would be treated with smaller voltage segments.

Generally, the gate-voltage plateau of Figure 11 will not be located at the middle of the pulse-generator amplitude (5 volts). As a result, rise and fall times measured this way experience differing gate currents and are "nonsymmetrical". This type of measurement will also lead one to observe temperature sensitivities, load-current sensitivities, and device-to-device variability, all of which are more circuit dependent than device dependent.

Source-Lead Inductance

The gate-voltage waveforms may be corrected by the voltage across the source-lead inductance and external inductance, which may be mutually common to the input and output current loops. This voltage, L di/dt, may be approximated and applied to the gate-voltage waveform after scaling Figure 12 for the actual gate currents. Generally, this effect is not appreciable for gate current small relative to ±100mA. A very loose circuit wiring arrangement with inches of mutually common source wire will exaggerate this effect.

Gate Voltage Propagation Effects

Most power MOSFET applications need switch no faster than tenths of a microsecond, but should faster switching be required, this section will become important. It must be understood that the power MOSFET appears as a distributed network of many cells when used for very fast switching.

The thousands of individual MOSFET cells are connected in parallel with highly conductive metal for the sources and drains. However, the gates are paralleled with a moderately conductive film of doped polysilicon. As a result, a very steep voltage wavefront applied to the gate pad will bias those cells close by, but a delay will occur for turn on or turn off. Because of the nonlinear "input capacitance" of each cell, the delay cannot be characterized by a pure number of so many nanoseconds.

Presently, most manufacturers characterize typical switching speed for a single test condition. The test conditions are usually chosen to present the most favorable result, usually near the upper limit of usefulness.

Figures 13(a), (b), and (c) show the increasing effect of gate voltage propagation. The gate waveform is the only one shown because the drain is not affected so drastically. This is true because some cells are overdriven, offsetting the effect of the starved cells. Care must be exercised when operating with large gate effects similar to those of Figure 13(c).

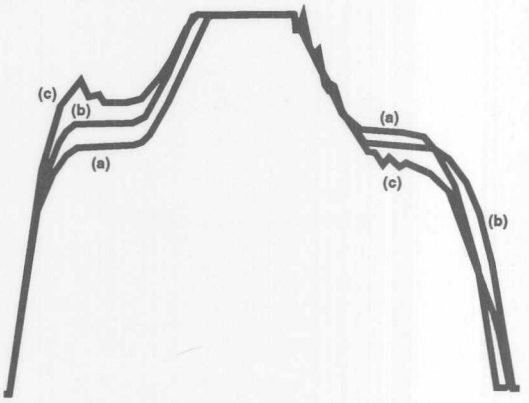
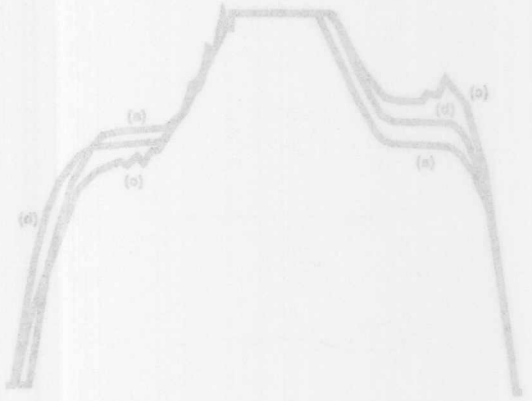


FIGURE 13. CURVES SHOWING THE INCREASING EFFECT OF GATE VOLTAGE PROPAGATION

Gate-propagation effects may be reduced by the following design methods:

1. Many gate runners.
2. More conductive polysilicon.
3. Silicide rather than polysilicon gates.
4. Less cells (resulting in lower transconductance and higher R_{ON}).
5. Substantially different lateral and vertical structure.
6. High-frequency packaging.

None of the above methods will yield "breakthrough" devices unless used in combination.



Any of the previous methods require trade-offs which would not be attractive to the needs of most components users. These trade-offs are in the realm of:

1. Reduction of R_{ON} per unit area.
2. Decreased yield.
3. Added cost (beyond the cost of yield impact).
4. RFI, self-oscillation, and other problems characteristic of very fast devices.

References

1. "Power MOSFET Switching Waveforms - A New Insight," H. R. Ronan, Jr., and C. F. Wheatley, Jr., Proc. Powercon 11, April 1984.
2. "Correlating the Charge-Transfer Characteristics of Power MOSFETs with Switching Speed," E. Oxner, Proc. Powercon 9, April 1982.

APPNOTE

No. 7260.1 May 1992

Harris Power MOSFETs

POWER MOSFET SWITCHING WAVEFORMS: A NEW INSIGHT

Author: Harold R. Ronan, Jr. and C. Frank Wheatley, Jr.

The examination of power MOSFET voltage and current waveforms during switching transitions reveals that the device characterization now practiced by industry is inadequate. In this Note, device waveforms are explained by considering the interaction of a vertical JFET driven in cascode from a lateral MOSFET in combination with the interelectrode capacitances. Particular attention is given to the drain-voltage waveform and its dual-slope nature. The three terminal capacitances now published by the industry are shown to be valid only for zero drain current. For cases where the gate drive is a voltage step generator with internal fixed resistance, the drain voltage characteristics are inferred from the gate current drive behavior and compared to observed waveforms. The nature of the "asymmetric switching times" is explained.

A waveform family is proposed as a more descriptive and accurate method of characterization. This new format is a plot of drain voltage and gate voltage versus normalized time. A family of curves is presented for a constant load resistance with V00 varied. Gate drive during switching transitions is a constant current with voltage compliance limits of 0 and 10 volts. Time is normalized by the value of gate driving current. The normalization shows excellent agreement with data over five orders of magnitude, and is bounded on one extreme by gate propagation effects and on the other by transition time self-heating (typically tens of nanoseconds to hundreds of microseconds).

Device Models

The keystone of an understanding of power MOSFET switching performance is the realization that the active device is bimodal and must be described using a model that accounts for the dual nature. Buried in today's power MOSFET devices is the equivalent of a depletion layer JFET that contributes significantly to switching speed.Figurei is a cross-sectional view of a typical power MOSFET, with MOSFET/JFET symbols superimposed on the structure.

Figure 2 is obtained by taking the lateral MOS and vertical JFET from this conception and adding all the possible node-to-node capacitances. Computed values of the six capacitances for a typical device structure suggest that device behavior may be adequately modeled using only three capacitors in the manner of Figure 3. This is the model to be employed for analysis and study

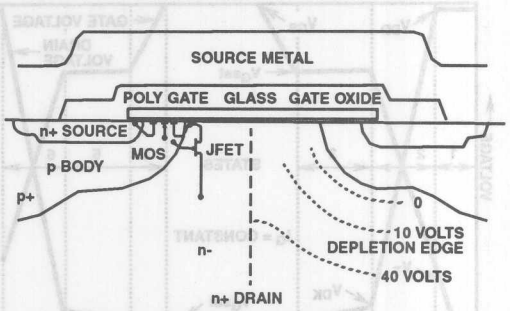


FIGURE 1. CROSS-SECTIONAL VIEW OF MOSFET SHOWING EQUIVALENT MOS TRANSISTOR AND JFET

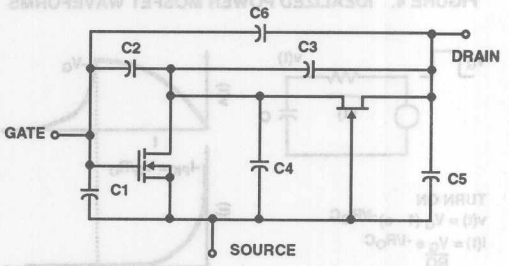


FIGURE 2. MOS TRANSISTOR WITH CASCODE-CONNECTED JFET AND ALL CAPACITORS

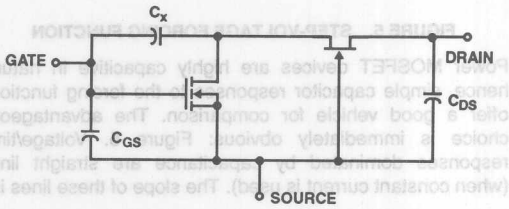


FIGURE 3. FIGURE 2 SIMPLIFIED

13 APPLICATION NOTES

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Gate Drive: Constant Voltage Or Constant Current

Before moving on to the study of the equivalent circuit states of the model, a gate-drive forcing function which is easy to represent, relates to reality, and best illustrates device behavior must be chosen. The choice may be immediately narrowed to two:

(1) An instantaneous step voltage with internal resistance R, Figure 4.

(2) An instantaneous step current with infinite internal resistance, Figure 5.

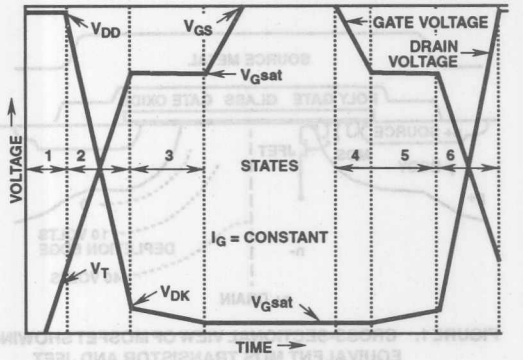


FIGURE 4. IDEALIZED POWER MOSFET WAVEFORMS

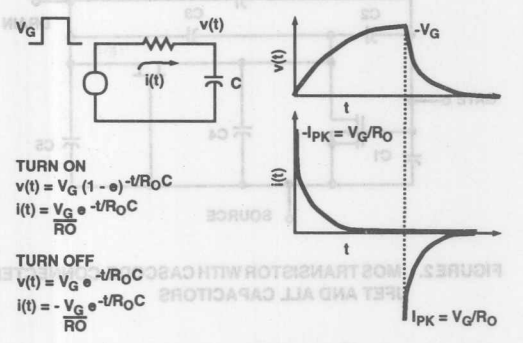


FIGURE 5. STEP-VOLTAGE FORCING FUNCTION

Power MOSFET devices are highly capacitive in nature; hence, simple capacitor responses to the forcing functions offer a good vehicle for comparison. The advantageous choice is immediately obvious: Figure 5. Voltage/time responses dominated by capacitance are straight lines (when constant current is used). The slope of these lines is

proportional to current and inversely proportional to capacitance. Analytically, then, constant current is most convenient. It is quite another matter, however, to build a bidirectional current drive that is accurate across the many decades of both current and time required to establish experimental verification.

Six States

To completely characterize power MOSFET switching waveforms, the six states that a device assumes, Figure 6, must be addressed:

STATE	MOS	JFET
Turn-on 1	Off	Off
Turn-on 2	Active	Active
Turn-on 3	Active	Saturated*
Turn-off 4	Saturated	Saturated
Turn-off 5	Active	Saturated
Turn-off 6	Active	Active

*The term saturated is taken to mean a constant low-voltage drain-source condition.

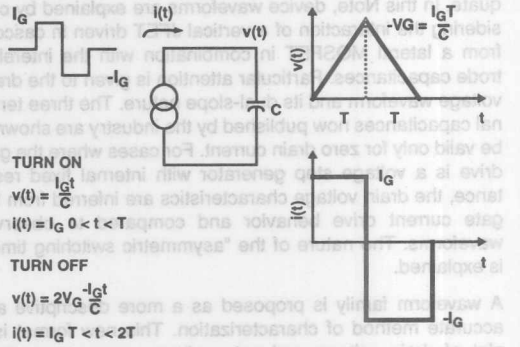
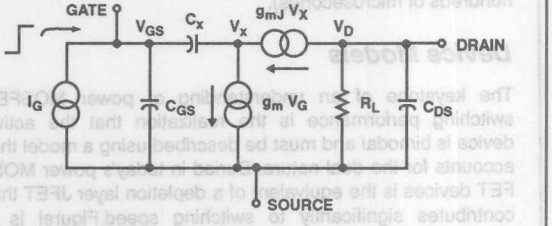


FIGURE 6. STEP CURRENT FORCING FUNCTION

Equivalent Circuit

The lumped-parameter model of Figure 3, with the cascode-connected JFET, can now be reduced to the linear equivalent circuit of Figure 7, and the six device states investigated from full off to full on.



LEGEND

V_{GS}	- Gate Voltage	C_{DS}	- Drain Source Capacitance
V_X	- JFET Driving Voltage	g_m	- MOSFET Transconductance
V_D	- Drain Voltage	g_{mJ}	- JFET Transconductance
C_{GS}	- Gate Source Capacitance	R_L	- Drain Load Resistance
C_x	- MOSFET Feedback Capacitance	I_G	- Constant Current Amplitude

FIGURE 7. POWER MOSFET EQUIVALENT CIRCUIT

State 1: MOS Off, JFET Off

In a power-MOSFET device, no drain current will flow until the device gate threshold voltage, V_T, is reached. During this time, the gate current drive is only charging the gate source capacitance. More accurately, I_G is charging C_{iss} ($C_{iss} = C_{GS} + C_{GD}$, C_{DS} shorted), the capacitance designation published by the industry.

The current generators, $g_m v_g$ and $g_{mJ} V_x$ are open circuits for zero drain current, and R_L is presumed to be so low as to represent a short circuit (generally true for practical applications). This is academic however since C_{GS} is very much larger that C_6. The time to reach threshold, then, is simply:

$$T = \frac{C_{iss} V_T}{I_G}$$

State 2: MOS Active, JFET Active

This state graphically illustrates the dramatic influence that the JFET has on the power MOSFET drain-voltage wave- form. Instead of having to discharge C_x from V_{DD} to ground, the lateral MOSFET need only swing v_X to ground, a much smaller voltage thanks to the grounded gate JFET. Since the interaction of R_L with the device capacitances has a second-order effect on the drain voltage, the equivalent circuit of Figure 7 predicts a drain voltage change of:

$$dv_G/dt = g_m R_L I_G/[C_{GS} + C_X(1 + g_m/g_{mj})]$$

In all but the smallest power-MOSFET devices, C_x is several thousand picofarads and g_m/g_{mj} is of the order of 3:1. Power-MOSFET devices exhibit a high dv_D/dt switching rate because of the cascode-connected J FET, not because C_{rss} ($C_{rss} = C_{GD}$) is a small value, as zero-drain-current data- sheet capacitance values might lead one to believe. If C_{rss} were, in actuality, small, long drain voltage tails would not exist. The tail response is a direct result of JFET saturation. In order to delineate the transition from state 2 to state 3, a drain voltage at which the transition occurs must be defined. V_{DK} is the knee voltage at which linear extrapolations of drain-voltage slopes intersect. The time duration of state 2 is:

$$t = (V_{DD} - V_{DK})[C_{GS} + C_X(1 + g_m/g_mJ)]/g_m R_L I_G$$

State 3: MOS Active, JFET Saturated

When the JFET saturates, the $g_{mJ} V_x$ current generator becomes a short circuit and the equivalent circuit predicts:

$$dv_D/dt = g_m R_L I_G/[C_{GS} + C_X(1 + g_m R_L)]$$

This is the Miller effect so often referred to in older texts that describe the behavior of grounded-cathode vacuum-tube amplifier circuits. Allowing for the fact that $1 + g_m R_L$ is approximately equal to $g_m R_L$ and $C_x(1 + g_m R_L)$ is very much larger than C_{GS}, the expression for drain-voltage tail time is:

$$t = (V_{DK} - V_D[sat])C_x/I_G$$

State 4: MOS Saturated, JFET Saturated (Turn-Off)

In this state, in addition to $g_{mj} V_x$ being shorted, the $g_m V_G$ current generator is shorted, and I_G is occupied with charging C_x and C_{GS}, in parallel, from the peak value of V_G to V_G(sat). The time required for this is:

$$t = (V_G - V_G(sat)(C_{GS} + C_x)/I_G$$

Since a value for C_{GS} may be measured independently of switching time, the method described is the simplest way of determining C_x.

On turn-off, the state time equations are equally applicable, but in reverse order (states 5 and 6); see the idealized waveform of Figure 4.

Experimental Verification

The four switching states just analyzed indicate that for a given device, all four switching state times are inversely proportional to the magnitude of the gate drive current. Figure 8 illustrates the switching performance of a typical power MOSFET across three decades of gate drive current and time. In each case the data slope is almost a perfect -1.

A New Device Characterization

Figure 8 could not be a reasonable device data sheet presentation because it does not give the designer any information on a typical value for C_x, nor does it convey how V_{DK}, g_m, g_m/g_{mJ}, and V_G(sat) vary with drain current. What would be of enormous value to the designer is a plot of $v_D(t)$, $v_G(t)$ for selected values of V_{DD} and I_D within device ratings.

A reasonable characterization would be as follows:

1. The x axis would be normalized in terms of gate current drive.
2. The y axis would be normalized in terms of percent maximum rated V_D (0 to 100%).
3. $R_L = V_D(max)/I_D(max)$ would define the drain load resistance.
4. Four plots of $v_D(t)$, $v_G(t)$ at 100%, 75%, 50%, and 25% V_D(max) would be shown.

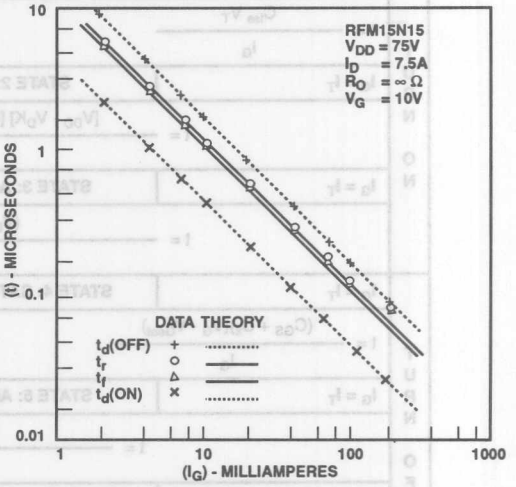


FIGURE 8. CONSTANT GATE CURRENT SWITCHING TIME

Figure 9 is such a plot for the RFM15N15 power MOSFET. With such a plot, a designer can estimate device switching performance under any resistive gate/drain conditions.

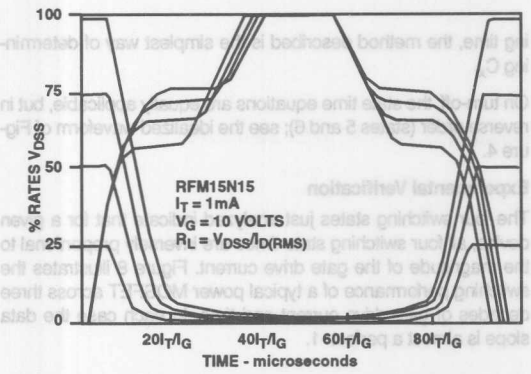


FIGURE 9. NORMALIZED RFM15N15 SWITCHING WAVEFORMS FOR CANSTANT GATE-CURRENT DRIVE.

Step-Voltage Gate Drive

The majority of power MOSFET applications employ a step gate-voltage input with a finite source resistance R_O.Often R_O for turn-on is not the same as R_O for turn-off. How can switching times for these situations be estimated using the switching characterization curves just described? The analysis for resistive step voltage inputs, which is complex because the gate current is no longer constrained to be constant, but is a function of device gate-voltage response, is covered in Appendix A. (A second, shorter appendix, B, has been added to illustrate the estimation of R0 for some practical gate drive circuits.) Table I summarizes the common switching equations, and indicates the appropriate 1G to be used in each state for relating step voltage drives to the characterization curves.

Experimental Verification

Since the switching equations for step currents and voltages differ only by gate-current magnitudes for the same device type, one would expect a plot of switching time versus 1/R0 to be of the same form as those obtained for a step current drive. This is exactly the case, as Figure 10 is merely a variation of Figure 8. Using the relationships of Table I, the observed differences between Figs. 7 and 9 can be pinpointed. The two sets of experimental curves confirm that, on the basis of the short-circuit drive current VU/R0 equalling the constant 1G, t6(on), t, td(off), and t1 will all be longer, as predicted by the ratios of the gate drive currents of Table 1. Notice also that t, t1 switching symmetry is disrupted by the use of a step voltage with source resistance R0. For states 2 and 6 the time ratio is:

TABLE 1. COMMON SWITCHING EQUATIONS

	CONSTANT CURRENT	STATE 1: MOS OFF, JFET OFF	CONSTANT VOLTAGE
TURN ON	$t = \frac{C_{iss} V_T}{I_G}$		$t = R_O C_{iss} \ln \frac{[1]}{[1 - V_T/G_V]}$
	$I_G = I_T$	STATE 2: ACTIVE, ACTIVE	$I_G = (V_G - V_T)/R_O$
	$t = \frac{[V_{DD} - V_D K][C_{GS} + C_x(1 + g_m/g_{mJ})]}{g_m R_L I_G}$		
	$I_G = I_T$	STATE 3: ACTIVE, SATURATED	$I_G = (V_G - V_{Gsat})/R_O$
	$t = \frac{(V_{DK} - V_{Dsat})C_x}{I_G}$		
TURN OFF	$I_G = I_T$	STATE 4: SATURATED, SATURATED	$I_G = -V_G/R_O$
	$t = \frac{(C_{GS} + C_x)(V_G - V_{Gsat})}{I_G}$		$t = R_O(C_{GS} + C_x) \ln (V_G/V_{Gsat})$
	$I_G = I_T$	STATE 5: ACTIVE, SATURATED	$I_G = (V_G - V_{Gsat})/R_O$
	$t = \frac{(V_{DK} - V_{Dsat})C_x}{I_G}$		
	$I_G = I_T$	STATE 6: ACTIVE, ACTIVE	$I_G = (V_G - V_{Gsat})/R_O$
	$t = \frac{[V_{DD} - V_D K][C_{GS} + C_x(1 + g_m/g_{mJ})]}{g_m R_L I_G}$		

Experimental Verification

Since the switching equations for step currents and voltages differ only by gate-current magnitudes for the same device type, one would expect a plot of switching time versus $1/R_O$ to be of the same form as those obtained for a step current drive. This is exactly the case, as Figure 10 is merely a variation of Figure 8. Using the relationships of Table I, the observed differences between Figs. 7 and 9 can be pinpointed. The two sets of experimental curves confirm that, on the basis of the short-circuit drive current V_G/R_O equalling the constant I_G, $t_d(on)$, t_r, $t_d(off)$, and t_f will all be longer, as predicted by the ratios of the gate drive currents of Table 1. Notice also that t_r, t_f switching symmetry is disrupted by the use of a step voltage with source resistance R_O. For states 2 and 6 the time ratio is:

$$\frac{t_{turn\text{-}on}}{t_{turn\text{-}off}} = \frac{V_G(sat)}{V_G - V_T}$$

For states 3 and 5 the time ratio is:

$$\frac{t_{turn\text{-}on}}{t_{turn\text{-}off}} = \frac{V_G(sat)}{V_G - V_G(sat)}$$

Utilization of available maximum gate drive voltage and current can be optimized for fastest power MOSFET switching speed through the use of constant-current gate drive at the expense of increased gate-drive circuit complexity.

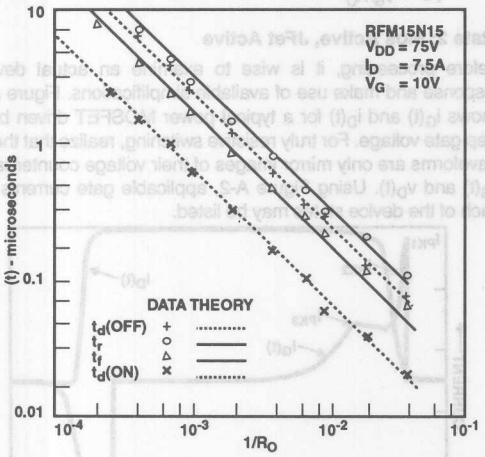


FIGURE 10. CONSTANT GATE VOLTAGE SWITCHING TIME

Using The Characterization Curves, Figure 9

To estimate the switching times for an RFM15N15 power MOSFET under the conditions V_G = 10V, V_{DD} = 75V, R_O = 100 ohms, and R_L = 10 ohms, precedes as follows:

State 1: MOS Off, JFET Off

This time can be estimated without recourse to the curves

$t = 100(1200 \times 10^{-12})$ in $[1/(1 - 4/10)]$

$t = 61$ ns

State 2: MOS Active, JFET Active

$I_G = (10 - 4)/100 = 60mA$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{60} = \frac{9}{60} = 150\ ns$$

State 3: MOS Active, JFET Saturated

$I_G = (10 - 7)/100 = 30mA$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{30} = \frac{14}{30} = 467\ ns$$

State 4: MOS Saturated, JFET Saturated

$C_{GS} + C_x$ = (gate voltage slope)(test current)

= $(1.5 \times 10^{-6}s/5\ volts)(10mA)$

= 3000pF

$t = 100(3000 \times 10^{-12})$ in $[10/6.6]$

$t = 125ns$

State 5: MOS Active, JFET Saturated

$I_G = 6.6/100 = 66mA$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{66} = \frac{8}{66} = 121\ ns$$

Figure 11 shows RFM15N15 waveforms using the conditions specified in the example.

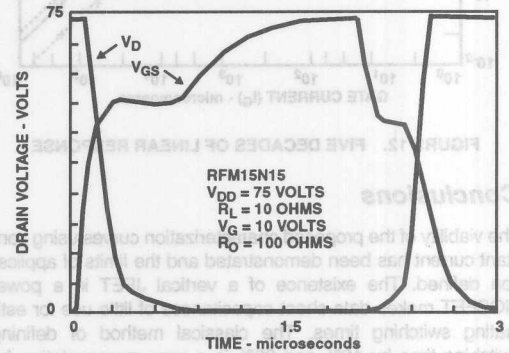


FIGURE 11. STEP GATE VOLTAGE INPUT TO AN RFM15N15

STATE	CALCULATED TIME (t_c, ns)	MEASURED TIME (t_m, ns)	RATIO (t_c/t_m)
1	61	60	1.02
2 + 3	671	670	0.92
4	125	137	0.91
5 + 6	318	375	0.85

For peak gate voltages other than 10 volts, and load resistances other than $V_{DSS}/I_{D(rms)}$, the equations of Table 1 may be used in conjunction with slope estimates from the characterization curves for C_x and $C_{GS} + C_x(1 + g_m/g_{mJ})$ at the appropriate drain-current level.

Characterization-Curve Limits

The switching-time range over which the characterization can be applied is very impressive. For gate currents of the order of microamperes, device dissipation is the limiting factor. For gate currents of the order of amperes, the device response will be slowed by gate propagation delay. This delay, of course, degrades the linear switching relationship to gate current. However, as Figure 12 graphically shows, the characterization is valid across five decades of gate current and switching time, allowing all but a very few switching applications to be described by the characterization curves of Figure 9.

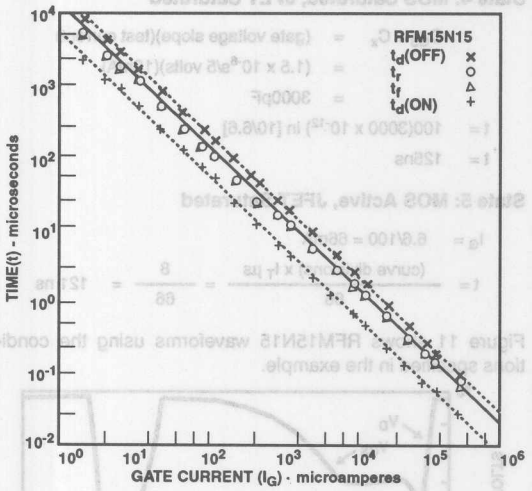


FIGURE 12. FIVE DECADES OF LINEAR RESPONSE

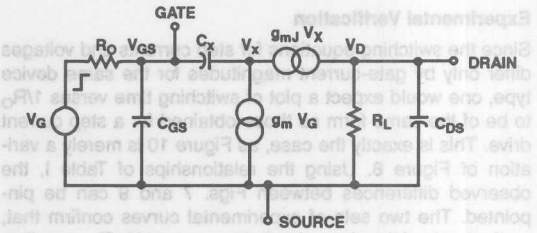
Conclusions

The viability of the proposed characterization curves using constant current has been demonstrated and the limits of application defined. The existence of a vertical JFET in a power MOSFET makes data-sheet capacitances of little use for estimating switching times. The classical method of defining switching time by 10% and 90% is a poor representation for power MOSFETs because of the dual- slope nature of the drain waveforms. Switching influences are masked because the 10% level is controlled by one mechanism and the 90% level by another. Device comparisons based on the classical switching definition can be very misleading.

Appendix A - Analysis For Resistive Step Voltage Inputs

Step Voltage Gate Drive

To obtain the necessary relationships, six device switching states must be examined using the same device equivalent circuit as was used for the constant-gate-current case, but with the forcing function replaced with a step voltage with internal resistance R_0, Figure A-1.



LEGEND

V_{GS}	- Gate Voltage	C_{DS}	- Drain Source Capacitance
V_X	- JFET Driving Voltage	g_m	- MOSFET Transconductance
V_D	- Drain Voltage	g_{mJ}	- JFET Transconductance
C_{GS}	- Gate Source Capacitance	R_L	- Drain Load Resistance
C_x	- MOSFET Feedback Capacitance	I_G	- Constant Current Amplitude

FIGURE A-1. POWER MOSFET EQUIVALENT CIRCUIT

State 1: Mos Off, JFet Off

As before, both current generators are open circuits, reducing the equivalent circuit to simply charging C_{iss} through R_0.

$$t = R_O C_{iss} \ln(1/(1 - V_T/V_G))]$$

$$t = V_G/R_O$$

State 2: Mos Active, JFet Active

Before proceeding, it is wise to examine an actual device response and make use of available simplifications. Figure A-2 shows $i_G(t)$ and $i_D(t)$ for a typical power MOSFET driven by a step gate voltage. For truly resistive switching, realize that these waveforms are only mirror images of their voltage counterparts $v_G(t)$ and $v_D(t)$. Using Figure A-2, applicable gate currents for each of the device states may be listed.

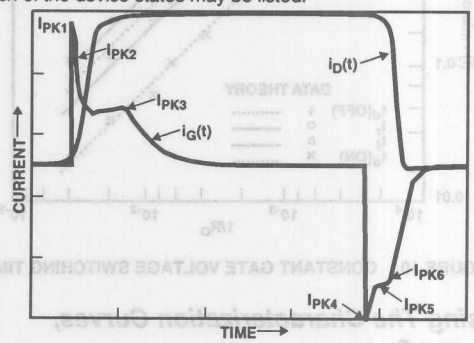


FIGURE A-2. $i_G(t)$ AND $i_D(t)$ FOR A TYPICAL POWER MOSFET DRIVEN BY A STEP GATE VOLTAGE

Turn-On

State 1: MOS Off, JFET Off

$I_{PK1} = V_G/R_O$

State 2: MOS Active, JFET Active

$I_{PK2} = (V_G - V_T)/R_O$

State 3: MOS Active, JFET Saturated

$I_{PK3} = (V_G - V_G(sat))/R_O$

Turn-Off

State 4: MOS Saturated, JFET Saturated

$I_{PK4} = V_G/R_O$

State 5: MOS Active, JFET Saturated

$I_{PK5} = V_G(sat)/R_O$

State 6: MOS Active, JFET Active

$I_{PK6} = V_G(sat)/R_O$

The equivalent circuit of Figure A-1 predicts that:

$$dv_D/dt = -g_m R_L(V_G - V_T)e^{-t/T1}/T1$$

where $T1 = R_O C_{GS} + (1 + g_m/g_{mJ})R_O C_x$

Note that $g_m R_L(V_G - V_T)$ is usually an order of magnitude greater than V_{DD}, indicating that the drain voltage is discharging toward a very large negative value. The device operation, then, is on the early, almost linear, portion of the exponential, where $e^{-t/T1}$ approximates unity. The drain current of Figure A-2, and hence the drain voltage, does indeed exhibit a linear decrease with time.

Thus, for state 2:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_x(1 + g_m/g_{mJ})]}{g_m R_L I_{PK2}}$$

where $I_{PK2} = (V_G - V_T)/R_O$

State 3: Mos Active, JFet Saturated

Because of the Miller effect, the gate voltage and, hence, the gate current, is almost constant during the tail time. The equivalent circuit then predicts:

$$\frac{dV_D}{dt} = \frac{g_m R_L I_G}{C_{GS} + (1 + g_m R_L)C_x} = \frac{I_G}{C_x}$$

$$I_G = I_{PK3} = (V_G - V_G(sat))/R_O$$

and $$t = \frac{(V_{DK} - V_D[sat])C_x}{I_{PK3}}$$

State 4: Mos Saturated, JFet Saturated (Turn-off)

Both equivalent-circuit generators are short circuits, and the gate drive is discharging C_x in parallel with C_{GS} through R_O.

$$t = R_O(C_{GS} + C_x)\ \ln[V_G/V_G(sat)]$$

$$I_{PK4} = V_G/R_O$$

State 5: Mos Active, JFet Saturated

The JFET current generator $V_x g_{mJ}$, is operative.

$$t = \frac{[V_{DK} - V_D[sat])C_x}{I_{PK5}}$$

$I_{PK5} = V_G(sat)/R_O$

State 6: Mos Active, JFet Active

The Miller effect is now reduced by the activation of $V_G g_{mJ}$, and the equivalent circuit predicts:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_x(1 + g_m/g_{mJ})]}{g_m R_L I_{PAK6}}$$

$I_{PAK6} = V_G(sat)/R_O$

Appendix B - Estimating R_O For Some Typical Gate-Drive Circuits

Case 1: Typical Pulse-Generator Drive, Figure B-1

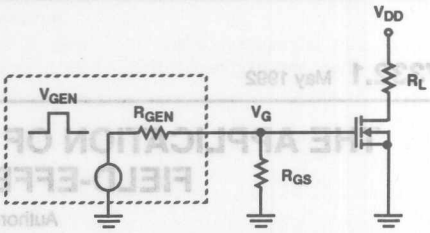


FIGURE B-1. TYPICAL PULSE-GENERATOR DRIVE CIRCUIT

Turn-On and Turn-Off

$$R_O = R_{GEN}R_{GS}/(R_{GEN} + R_{GS})$$

For the typical case where $R_{GEN} = 50\Omega$, and a coaxial-cable termination of 50 ohms, $R_O = 25\Omega$ and $V_G = V_{GEN}/2$.

Case 2: Voltage-Follower Gate Drive, Figure B-2

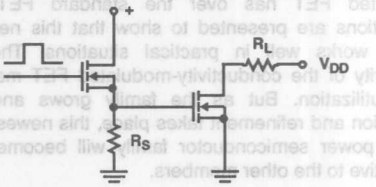


FIGURE B-2. VOLTAGE-FOLLOWER GATE-DRIVE CIRCUIT

Turn-On

R_O is approximately equal to $1/g_m$ for R_S very much greater than $1/g_m$.

gm = transconductance of driving MOSFET transistor.

Turn Off

$R_O = R_S$

Case 3: Common-Source Gate Drive, Figure B-3

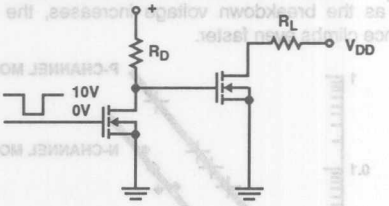


FIGURE B-3. COMMON-SOURCE GATE-DRIVE CIRCUIT

Turn-On

$R_O = R_D$ (drain-to-ground capacitance of driving device adds to C_{GS} of driven MOSFET.)

Turn Off

$R_O = R_{DS}(on)$ of driving MOSFET

R_D is very much greater than $R_{DS}(on)$

Harris Semiconductor

APPNOTE

No. 7332.1 May 1992

Harris Power MOSFETs

THE APPLICATION OF CONDUCTIVITY-MODULATED FIELD-EFFECT TRANSISTORS

Author: Jack Wojslawowicz

Summary

The development of conductivity-modulated field-effect transistors, FETs, makes available to the system designer another solid-state device that can be used to implement power switching control. This paper reviews differences between the standard and the newly developed FET. It shows the significant advantages that the conductivity-modulated FET has over the standard FET. Several applications are presented to show that this new type of device works well in practical situations. The relative inmaturity of the conductivity-modulated FET may limit its initial utilization. But as the family grows and product innovation and refinement takes place, this newest member of the power semiconductor family will become a viable alternative to the other members.

General Considerations

The development of the power field-effect transistor has made available to the power-stage designer an entire new family of power semiconductors. Over the past 5 to 6 years, the breadth of product has grown to encompass the requirements of a large number of applications. A limiting factor that has slowed the utilization of power FETs in the high-current, high-voltage applications is the fact that the on-state resistance ($R_{DS(ON)}$) in a standard FET is related to its breakdown voltage (B_{VDSS}) by a nearly cubic power, i.e., $R_{DS(ON)} \approx B_{VDSS}$ 2.8. What this implies, as Figure 1 shows, is that as the breakdown voltage increases, the on-state resistance climbs even faster.

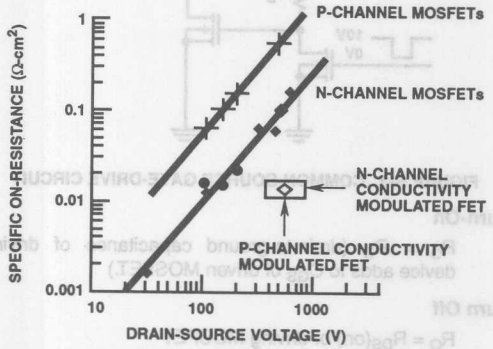


FIGURE 1. SPECIFIC ON-RESISTANCE OF P AND N-CNANNEL MOSFETS AND CONDUCTIVITY-MODULATED FETS vs. FORWARD BLOCKING VOLTAGE.

The MOSFET on-state resistance is contributed to primarily by three components of the transistor: the MOS channel, the neck region, and the extended drain region. The extended drain region contributes the most to the on-state resistance in high-voltage MOSFETs. To achieve a lower on-state resistance at a given blocking voltage, the usual technique is simply to make the die larger. However, increasing the die size has its limitations from a manufacturing point of view, since MOSFETs, with their very fine horizontal geometries, are highly defect-yield sensitive. As die size increases, the likelihood of a defect resulting in a nonfunctional part increases exponentially. This tendency, combined with a smaller number of parts per wafer, limits the availability of low-on-state-resistance, high-voltage MOSFETs.

A change in the horizontal geometry of the MOSFET can lower the specific on-state resistance per unit area. By using more channel width with smaller source cells placed closer together, a reduction in on-state resistance can be achieved. A limitation on how close these cells can be placed arises from a possible localization of field concentrations that will limit the voltage breakdown of the structure to less than the theoretical rating due only to mpurity concentrations. Therefore, for a given breakdown voltage, there exists a minimum spacing of the cell structure. Generally, the higher the required breakdown voltage, the further apart the cells must be placed.

As stated earlier, the extended drain region of the MOSFET generally contributes the most to the on-state resistance in high-voltage MOSFETs. As the required blocking voltage is increased, this region must be made thicker and more lightly doped to be able to support the desired voltage. It is this region's contribution to on-state resistance that the condictivity-modulated field-effect transistor drastically reduces. This reduction occurs as the result of the injection of minority carriers from the substrate and, in specific on-state resistance per unit area, is about 10 times less than in a standard MOSFET at the 400V BV_{DSS} level, as shown in Figure 1.

Further analysis has shown that the specific on-state resistance may be nearly independent of blocking-voltage level. This finding implies that at a BV_{DSS} of 1000V, the reduction in conductivity-modulated FETs over the standard MOSFETs could be perhaps 50 to 1. These reductions in on-state resistance per unit area that the conductivity-modulated FETs can achieve present the possibility that

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high-voltage high-current FET-type devices can become more readily available because of the smaller die sizes associated with conductivity-modulated FETs.

Comparison of Standard and Conductivity-Modulated FETs

Standard and conductivity-modulated FETs share some characteristics, but are substantially different in others. Shown in Table 1 is a listing of the major characteristics that make the conductivity-modulated FETs unique among power semiconductor families. Foremost, it is a voltage-gated device; its input characteristics are similar to standard power MOSFETs of comparable chip size. Very little drive power is required at low to moderate switching frequencies. The device remains under the control of the gate within its normal operating conditions. It exhibits the normal linear mode as well as the fully saturated on-state of conventional power MOSFETs. When the gate voltage is removed, the device turns off, unlike the thyristor family of power semiconductors, which must be either externally or naturally (internally) commutated.

TABLE 1. CONDUCTIVITY-MODULATED FET CHARACTERISTICS

Voltage Gated	Small gate power required. Similar to standard power MOSFET.
Turn Off	When gate drive is removed... Unlike an SCR!
Nonlinear On-State Voltage drop	Like that of an SCR.
Turn On Speed	Fast! Comparable to a standard power MOSFET.
Turn-Off Speed	Slow! Comparable to a bipolar transistor.
Temperature Independent On-State Voltage Drop	Unlike the typical 2x variation of a power MOSFET.

The on-state voltage drop or resistance characteristic of a conductivity-modulated FET is markedly different from that of a standard power MOSFET, and is similar to that of a thyristor family member, the SCR. There is an offset voltage component (typically 0.6V) due to the p-n junction on the drain side, and a somewhat nonlinear resistive component, both of which are in series between the drain and source terminals. This series arrangement results in a highly nonlinear equivalent resistance, unlike the linear resistive characteristic of $V_{DS(ON)}$ of a standard FET.

The structure of the conductivity-modulated FET operates during its turn on just as a standard FET does, hence its turn-on speed is very similiar to that of a standard FET. With its high input impedance and its short propagation delay, the turn-on transistion of the conductivity-modulated FET, as well as the standard power FET, is easily controlled by the gate driving circuit. This characterstic allows the designer the ability to control EMI and RPI generation easily. With other power semiconductors, it may be necessary to employ elaborate circuit schemes to limit rapidly rising in-rush currents.

A significant characteristic that must be considered in power switching applications is that of turn-off speed. The internal action that makes the conductivity-modulated FET such a silicon-efficient device also makes it an inherently slower device during turn-off. The injection of the minority carriers during the on-state conduction of current results in these carriers being present at the moment of turn-off. Without any way of removing these carriers by external means, they must recombine within the structure itself before the device can revert to its fully off-state condition. The quantity of these carriers and how fast they can deplete themselves determines the turn-off switching speed of the conductivity-modulated FET. This process of recombination is considerably slower than the simple discontinuance of majority carrier flow by which the standard power FET turns off. Hence, again, the conductivity-modulated FET is an inherently slower device. Its turn-off speed lies somewhere between the performance ofathyristorand that of a bipolar transistor.

The final characteristic that makes the conductivity-modulated FET different from a conventional FET is the variance of on-state voltage with temperature. The characteristic of the conductivity-modulated FET is similar to that of an SCR, varying about -0.6mV/°C. The conventional FET has a positive temperature coefficient such that on high-voltage devices the $R_{DS(ON)}$ will double from its 25°C value when the junction temperature reaches 150°C. The system designer must take this characteristic into consideration when the heat sink is being designed for the system.

It is these similarities and differences that make the conductivity-modulated FET a unique member of the family of power-semiconductor switching devices. Applications of this alternative power switching device invariably make use of one or more of its unique characteristics.

Applications

Automotive Ignition

An application that can take advantage of the low drive-power capability of the conductivity-modulated FET is the electronic automotive ignition system. In Figure 2, the control IC takes the signal from the pickup coil located in the distributor and regulates the current through the ignition coil. At the proper time, the IC removes base drive from the bipolar transistor, which all systems currently employ as their coil driver. This removal of base drive allows the transistor to shut off which, in turn, causes a rapid decrease in the ignition-coil primary current. As the primary current decreases to zero, the energy stored in the field surrounding the primary is transferred to the secondary coil. The secondary coil, consisting of many more turns than the primary, transforms this energy into a higher voltage, resulting in a spark being generated in the cylinder. The control IC determines when this spark occurs, so as to derive usable power. With the use of a bipolar transistor, it is estimated that approximately two-thirds of the power dissipation that occurs in the control IC is the result of the need to be able to drive the required base current of the ignition output transistor. The high-impedance input of the

conductivity-modulated FET virtually eliminates the base-current drive dissipation of the control IC.

With improved silicon usage, the conductivity-modulated FET brings to power semiconductor switching devices the die size necessary to attain the required voltage and current-handling capabilities of the electronic ignition. This smaller-sized die makes possible smaller modules, whether they be hybrid or standard PC-based systems, than those currently implemented with bipolar-transistor technology.

Brushless DC Motors

Another emerging application that can make use of conductivity-modulated FETs is the emerging field of brushless DC motors. In this class of application, the solid-state devices are used to electronically switch the voltage to the multiplicity of windings that are employed. The motor consists of an armature that has a number of N and S poles consisting of high-strength permanent magnets. The stator is made up of the multiplicity of windings that were mentioned above; the windings are spaced incrementally about the outside frame of the housing. The voltages to these windings are all electronically switched to create a rotating magnetic field. The armature then rotates to maintain its relative position within the moving magnetic field. The switching of the voltage on the stator windings is done by means of power semiconductor devices. A basic block diagram of such a system is shown in Figure 3.

The control logic provides the proper sequence of drive signals based on the rotation direction desired, the speed desired, and the enable input. These requirements are combined with the inputs from the hall-effect sensors to determine which power devices should be activated. Since the current through the stator windings must be bidirectional, the half-bridge or totem-pole output configuration is used to steer the current. This circuit implementation is generally performed with complementary devices, although single-polarity devices can be used with increased circuit complexity.

In a typical 120V off-line system, like the one shown in Figure 3, the switching devices must have a 300V to 400V blocking capability. For larger size motors, where larger currents are necessary, the use of power FETs generally implies the use of large die to achieve a low power dissipation to meet the heat-dissipation capability of the packaging. The conductivity-modulated FET, with its temperature-independent on-state-voltage-drop characteristic, helps this situation by keeping the dissipation lower than can be achieved with a standard power FET because of the increasing $R_{DS(ON)}$ characteristic of that device. The small die size of the conductivity-modulated FET, the result of better silicon utilization, again makes them the practical choice in motor control not only because of their electrical characteristics, but also because of the lower manufacturing cost of the die.

As stated above, system complexity can be reduced with complementary devices. Although p-channel conductivity-modulated FETs are not yet commerically available, laboratory samples have been fabricated which offers better silicon utilization efficiency than their conventional p-channel counterparts. This statement is based on the fact that p-channel MOSFETs require a 2.5 times larger area than an n-channel device for the same $R_{DS(ON)}$. The easier

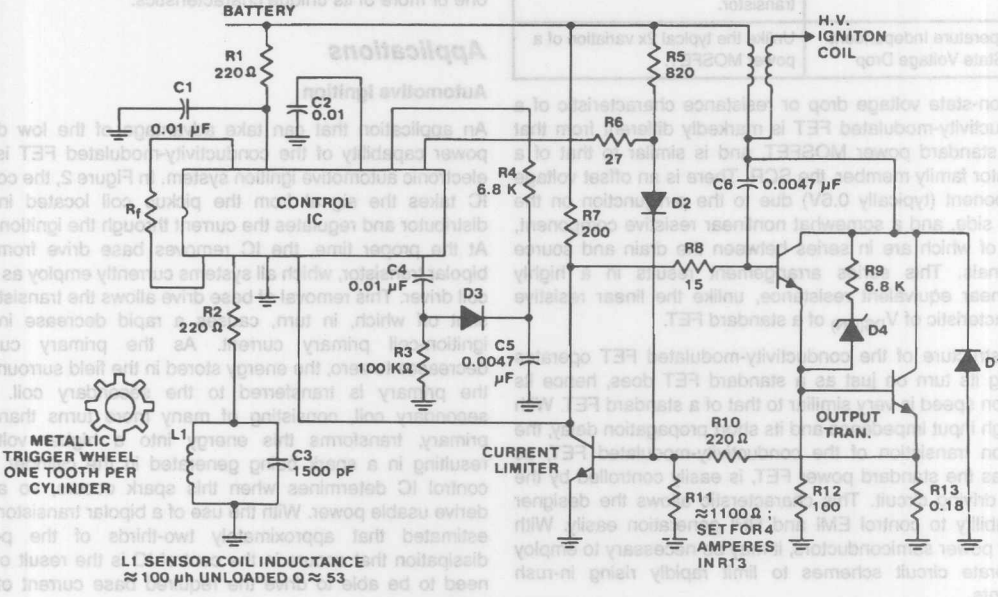


FIGURE 2. TYPICAL IGNITION SYSTEM

drive requirements for the n-channel (directly driven from the control IC) and the simplified voltage-translation circuit for driving the p-channel devices, combined with the smaller die size with potentially lower device cost for comparable power handling capability, makes the conductivity-modulated FET a natural for the brushless DC motor application.

Switching Power Supply

One final application that has the potential for conductivity-modulated FET usage is the switching power supply. A half bridge configuration implementation is presented in Figure 4. The system shown uses astandard PWM control IC to drive the conductivity-modulated FETs through the T2 transformer. The voltage drive characteristic of these devices makes the design of transformer T2 quite simple. The control IC is more lightly loaded because it does not have to supply a continuous base drive, as would be necessary with bipolar transistors.

The operating frequency and the "dead time" are the limitations placed on this system when conductivity-modulated FETs are used. The inherent lower switching speeds of these types of devices make these limitations necessary. The system is currently limited to the 20kHz to 30kHz range, with dead times as low as 1 to 2 microseconds. This characteristic is comparable to many existing bipolar systems.

Improvements in switching speeds will occur as the conductivity-modulated FET matures. It is, however, unlikely that they will ever have the same switching speeds as standard power FETs. This limitation prohibits their use in some of the newer higher-frequency power supplies being designed now with conventional FETs. However, in higher-power supplies, where conventional FETs must be paralled to achieve a low enough $R_{DS(ON)}$ for good efficiency, the conductivity-modulated FET may present a viable alternative with its smaller die size. Although the operating frequency of the system may have to be compromised to use them.

Conclusion

The conductivity-modulated FET represents a progression in the ever-advancing state-of-the-art development that occurs in the world of solid-state devices. The unique structure of these devices presents characteristics that make them equivalent in many ways to conventional FETs but superior in other ways. The system designer must take into account these similar and dissimilar characteristics to properly use them. The capabilities of the conductivity-modulated FETs allow them to make inroads into applications currently served by bipolar transistors, and in some cases conventional power FETs. As the devices mature through innovation and product refinement, conductivity-modulated FETs will become vital members of the family of solid-state power-semiconductor devices.

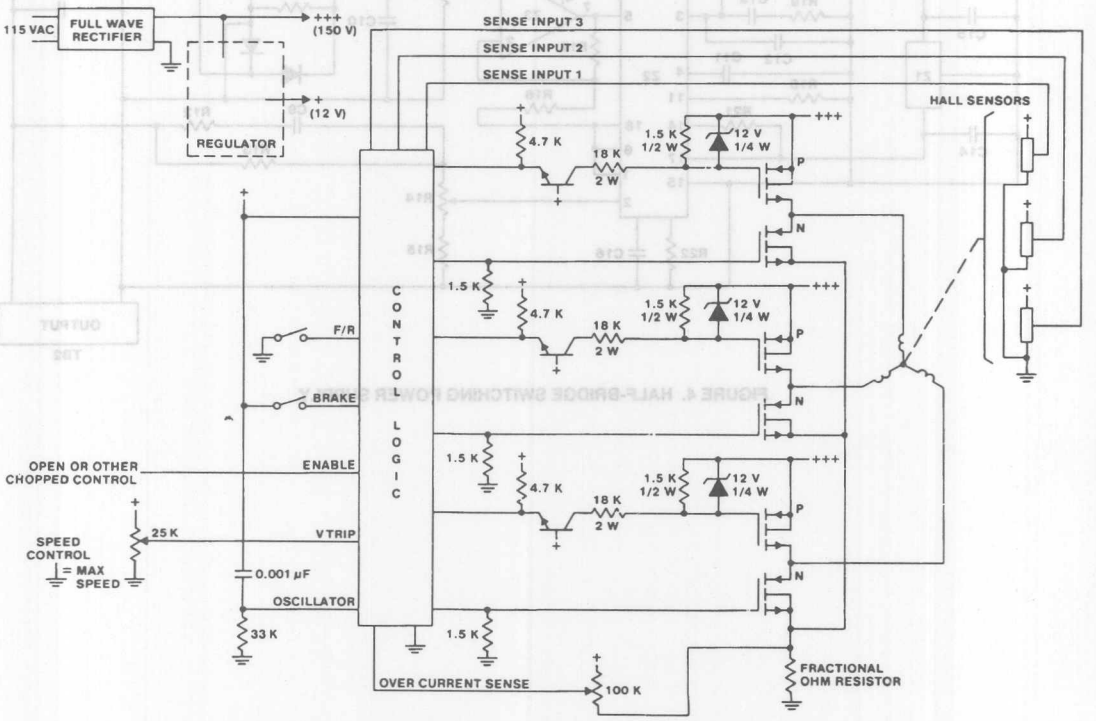


FIGURE 3. CONTROL CIRCUIT FOR THREE-PHASE BRUSHLESS DC MOTOR

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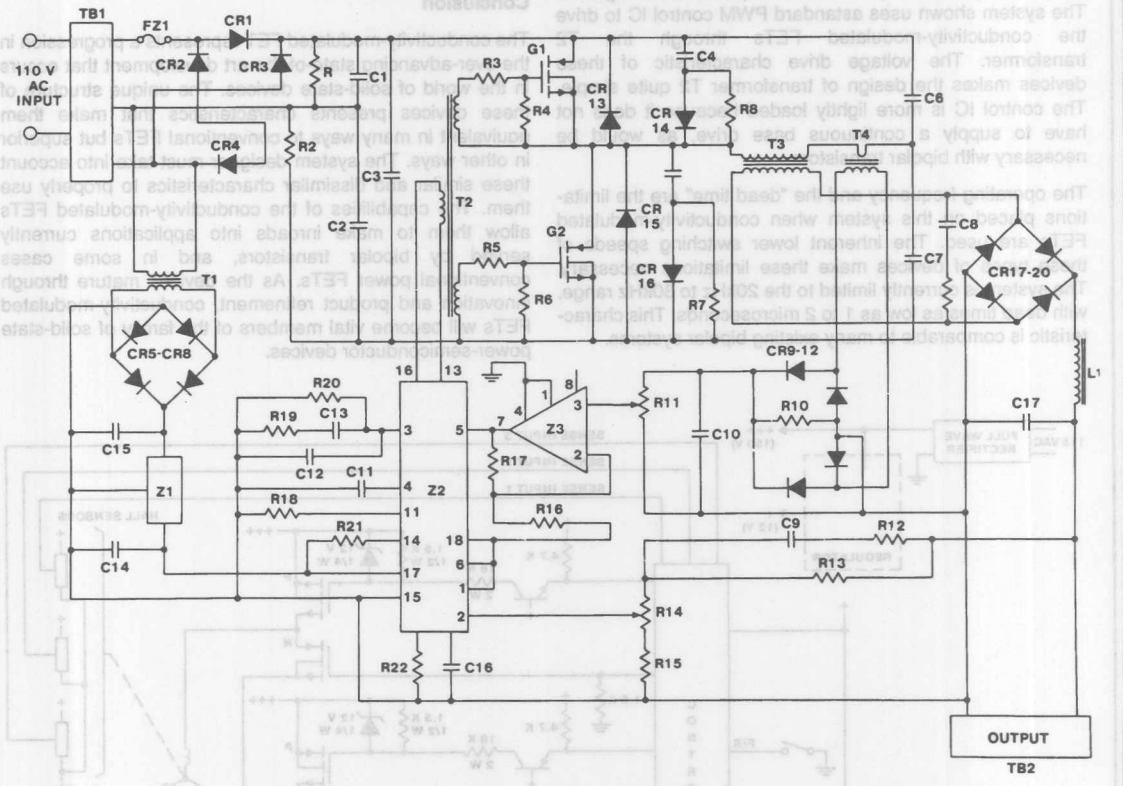


FIGURE 4. HALF-BRIDGE SWITCHING POWER SUPPLY

APPNOTE

No. 8602.1 May 1992

THE IGBTs - A NEW HIGH CONDUCTANCE MOS-GATED DEVICE

Author: J.P. Russell, A.M. Goodman, L.A. Goodman and J.M. Neilson

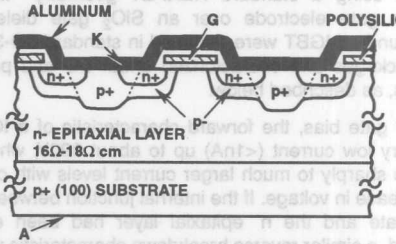
Abstract

A new MOS gate-controlled power switch with a very low on-resistance is described. The fabrication process is similar to that of an n-channel power MOSFET but employs an n^--epitaxial layer grown on a p^+ substrate. In operation, the epitaxial region is conductivity modulated (by excess holes and electrons) thereby eliminating a major component of the on-resistance. For example, on-resistance values have been reduced by a factor of about 10 compared with those of conventional n-channel power MOSFETs of comparable size and voltage capability.

Introduction

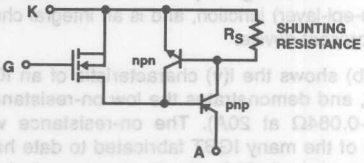
Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times, and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability,[1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. In this letter, we describe the fabrication and characteristics of a new vertical power MOSFET structure that provides an on-resistance value about 10 times smaller than that of conventional power MOSFETs of the same size and voltage capability. In this device, the conductivity of the epitaxial drain region of a conventional MOSFET is dramatically increased (modulated) by injected carriers; this mechanism results in a significant reduction in the device on-resistance and leads to the acronym IGBTs (Insulated Gate Bipolar Transistor).

This device, while similar in structure to the MOS-gated thyristor,[4,5] is different in a fundamental way; it maintains gate control (doesn't latch) over a wide range of anode current and voltage.[6] The structure and the equivalent circuit for the IGBTs are shown in Figure 1(a) and (b); they are similar to those of an MOS-gated thyristor, except for the presence of the shunting resistance R_S in each unit cell. The fabrication is like that of a standard n-channel power MOSFET except that the n^--epitaxial Si layer is grown on a p^+ substrate instead of an n+ substrate. The heavily doped p^+ region in the center of each unit cell, combined with the sintered aluminum contact shorting the n^+ and p^+ regions, provides the shunting resistance shown in Figure 1(b). This has the effect of lowering the current gain of the n-p-n transistor (αn-p-n) so that αn-p-n + αp-n-p <1. Thus latching is prevented and gate control is maintained within a large operating range of anode voltage and current.[6]



REGION	THICKNESS (μm)
EPI	60 - 62
n^+	1.0 - 1.5
p^-	3.5 - 4.0
p^+	5.0 - 5.5

a.) Structure



B.) EQUIVALENT CIRCUIT

In the remainder of this note we describe the operation and characteristics of this device.

Device Operation

The IGBT is a four-layer (n-p-n-p) device with an MOS-gated channel connecting the two n-type regions. In the normal mode of operation, a positive voltage is applied to the anode (A) relative to the cathode (K). When the gate (G) is at zero potential with respect to K, no anode current (i_A) flows for anode voltage V_A below the breakdown level V_{BF}. When $V_A < V_{BF}$ and the gate voltage is larger than the threshold value V_{gt}, electrons pass into the n^--region (base of the p-n-p transistor). These electrons lower the potential of the n^--region, forward biasing the p^+ - n^- (substrate-epi-layer) junction, thereby causing holes to be injected from the p+ substrate into the n^- epi-layer region. The excess electrons and holes modulate the conductivity of the high-resistivity n-region, which dramatically reduces the on-resistance of the

13 APPLICATION NOTES

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device. During normal operation, the shunting resistor (R_S) keeps the emitter current of the n-p-n transistor very low, which keeps αn-p-n very low. However, for sufficiently large i_A, significant emitter injection may occur in the n-p-n transistor, causing αn-p-n to increase; in this case the four-layer device may latch, accompanied by loss of control by the MOS gate. In this event, the device may be turned off by lowering i_A below some "holding" value, as is typical of a thyristor.

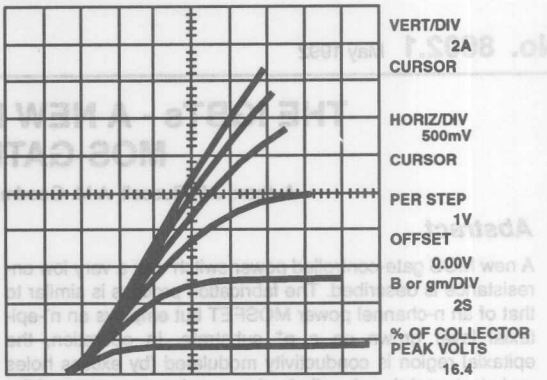
Device Characterization

Two different lots of IGBT structures, consisting of about 10 wafers/lot, have been successfully prepared to date. From these wafers, 1.5mm and 3mm square devices were fabricated using a standard HEXFET geometry[7] with a polysilicon gate electrode over an SiO_2 gate dielectric. Several hundred IGBT were mounted in standard TO-3 and TO-66 packages and characterized under DC and pulsed conditions, as described below.

With zero gate bias, the forward characteristic of a IGBTs shows very low current (<1nA) up to about 390V, where it breaks up sharply to much larger current levels with only a slight increase in voltage. If the internal junction between the p^+ substrate and the n^- epitaxial layer had been edge-passivated, a similar reverse breakdown characteristic would be expected. The actual reverse breakdown voltage for our devices was about 100V because edge passivation was not used.

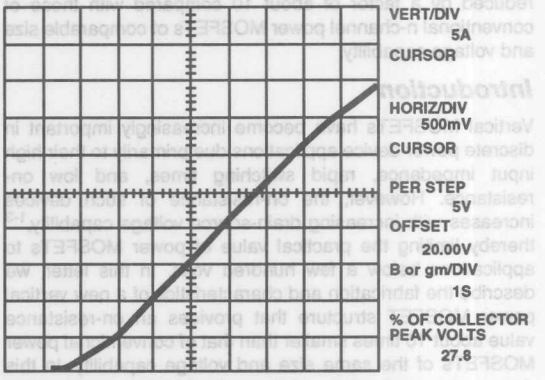
Figure 2(a) shows the MOSFET-like transfer characteristics of an IGBT in the low gate-voltage region. A noteworthy feature of the IGBT characteristic is the ~0.7V offset, from the origin, of the steeply rising portion of the i(v) characteristics. This offset is the voltage required to forward bias the p^+ - n^- (substrate-epi-layer) junction, and is an integral characteristic of the present device.

Figure 2(b) shows the i(v) characteristic of an IGBT with V_g = 20V, and demonstrates the low on-resistance of the device (~0.084Ω at 20A). The on-resistance values of nearly all of the many IGBT fabricated to date have been less than 0.1Ω (at 20A) for the 3mm square devices. Such values compare very favorably with those of conventional power MOS structures, as illustrated in Figure 3. Here, the open data points (and the upper curve) are from data sheet specifications of commercial power MOSFETs (Harris, IRC, and Motorola). The solid data points (and the lower curve) are those of Baliga, which he labelled "state-of-the-art",[3] supplemented with some of the "best" of Harris' commercial and developmental MOSFETs. Note that the on-resistance of the IGBT is approximately l0 times less than that of a 400V state-of-the-art MOSFET. Moreover, similarly low on-resistance values should be obtainable from IGBT designed for higher drain-source voltages. This is due to the fact that the resistance of the modulated region is determined by the concentrations and mobilities of the excess carriers (as in a p-i-n diode)[8] rather than by the background doping of the layer. In particular, the epi-layer doping and thickness of our present IGBT structures were designed for 600V, but V_{BF} was limited to 400V by the edge design of the device. An improved edge design should provide a blocking capability closer to bulk breakdown, without altering the on-resistance of the device. This would make the IGBTs on-resistance of less than 0.1Ω even more attractive for high-voltage applications.



PULSE TEST: PULSE WIDTH = 250μs, DUTY CYCLE < 0.5%

a.)



PULSE TEST: PULSE WIDTH = 250μs, DUTY CYCLE < 0.5%

b.)

FIGURE 2 - (a) MOSFET - Like Characteristic (b) IGBT i(v) with V_g = 20V

Transient Response Measurement

Switching time measurements under pulsed gate-voltage operation were used to characterize the transient operation of the device. The response of the anode current to a square-wave gate-voltage pulse is comprised of a rapid turn-on (with a typical time less than 1μs) and a somewhat slower turn-off. We observed that the turn-off transient consists of an initial "fast" component, followed by a "slow" tail, as shown in Figure 4.

We believe that the initial rapid decay is due to the turn-off of the MOS portion of the equivalent circuit, and the turn-off tail is due to the time required for the excess carriers in the epitaxial drain region to decay. In general, turn-off times in the range of 5μs to 20μs were observed, with the precise value depending on circuit conditionsand the turn-off time of the gate pulse.

The n-p-n-p structure of the IGBTs is similar to that of a thyristor and can be forced to latch under sufficiently high drive conditions. We have observed latching currents in the range 10A - 30A in 3mm square chips. The magnitude of the latching current has been found to depend on both anode voltage and temperature, decreasing with increasing anode voltage or increasing temperature.

More interestingly, the latching current is also strongly influenced by the gate voltage turn-off time. Slow gate turn-off (~10μs) permits anode currents up to 30A without latching. However, rapid gate turn-off (≤ 1μs) leads to latching at a much lower anode current level (~10A) in the same device. We believe that latching during rapid turn-off of the gate voltage is due to current being forced through the n-p-n transistor causing αn-p-n to increase, and leading to the condition for latching, αn-p-n + αp-n-p = 1. Slow turn-off of the gate voltage prevents this, since the induced channel turns off slowly and partially shunts the n-p-n transistor; the small current through this transistor keeps αn-p-n sufficiently low to avoid latching.

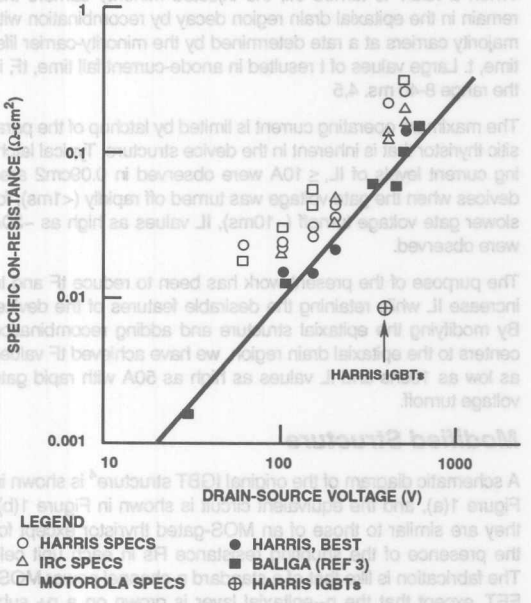


FIGURE 3. SPECIFIC ON-RESISTANCE vs. DRAIN-SOURCE VOLTAGE CAPABILITY FOR STATE-OF-THE-ART POWER MOSFETS AND THE IGBTs

Summary

A new MOS-gate-controlled power device, the IGBTs, has been described. The device has the desirable feature of a very low on-resistance similar to that of a thyristor, but is capable of maintaining gate control of the anode current over a wide range of operating conditions. The low on- resistance is due to conductivity modulation of the n epitaxial layer equivalent to the extended drain in a power MOSFET; this carries with it the penalty of slow switching compared with that of a conventional power MOSFET.

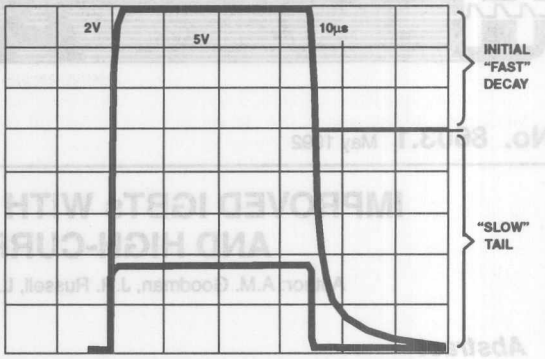


FIGURE 4. GATE VOLTAGE (LOWER TRACE) AND ANODE CURRENT (UPPER TRACE) WAVEFORMS FOR I_A(MAX) = 8A

Acknowledgment

The authors gratefully acknowledge the various helpful contributions of C. Nuese, D. Bergman, R. Ford, R. Jarl, G. Looney, P. Robinson, W. Romito, L. Skurkey, R. Stolzenberger, C. Wheatley, J. Wojslawowicz, and the staff of the Integrated Circuit Technology Center at RCA Laboratories. Added Note: Following submission of this Note, a similar device was described by B. J. Baliga in a presentation on December 14, 1982 at the International Electron Devices Meeting in San Francisco, CA. (B. J. Baliga et al., "The Insulated Gate Rectifier (IGR): A New Power-Switching Device", in IEDM Tech. Dig. 1982, pp 264-267.

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APPNOTE

No. 8603.1 May 1992

Harris Power MOSFETs

IMPROVED IGBTs WITH FAST SWITCHING SPEED AND HIGH-CURRENT CAPABILITY

Author: A.M. Goodman, J.R. Russell, L.A. Goodman, C.J. Nuese and J.M. Neilson

Abstract

Conventional vertical power MOSFETs are limited at high voltages (>500V) by the appreciable resistance of their epitaxial drain region. In a new MOS-gate controlled device called a IGBT, this limitation is overcome by modulating the conductivity of the resistive drain region, thereby reducing the on-resistance of the device by a factor of at least 10. However, the device previously described is slow in turnoff, having a fall time in the range 8 to 40μs. The purpose of our present work has been to reduce the fall time significantly and to increase the latching current level of the IGBTs, while retaining its desirable features. By modification of the epitaxial structure and addition of recombination centers, we have achieved fall times as low as 0.1μs and latching currents as high as 50A, while retaining on-resistance values <0.2Ω for a 0.O9cm^2 chip area. The techniques used for the introduction of recombination centers include electron, gamma-ray, and neutron irradiation, as well as heavy metal doping. For a series of IGBTss (with forward-blocking voltage capabilities of 400-600V), the fall time can be reduced by more than one order of magnitude with a penalty of less than a 20% increase in on-resistance.

Introduction

Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability,[1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. This limitation has been effectively overcome by the development of a new MOS power device in which the conductivity of the n-type epitaxial drain region is greatly increased (modulated) by the injection of minority carriers from a p-type substrate. We have called this device a COMFET-an acronym for COnductivity Modulated Field Effect Transistor;[4] the device has also been called an IGBT or Insulated Gate Bipolar Transistor.

The devices, as originally described, had most of the advantages of conventional power MOSFETs; in addition, they exhibited more than an order-of-magnitude reduction in high current on-resistance values, permitting improved utilization of silicon chip area. However, they also had two disadvantages:

When a IGBT is turned off, the injected minority carriers that remain in the epitaxial drain region decay by recombination with majority carriers at a rate determined by the minority-carrier lifetime, t. Large values of t resulted in anode-current fall time, tF, in the range 8-40 ms. 4,5

The maximum operating current is limited by latchup of the parasitic thyristor that is inherent in the device structure. Typical latching current levels of IL, ≤ 10A were observed in 0.09cm2 area devices when the gate voltage was turned off rapidly (<1ms); for slower gate voltage turnoff (~10ms), IL values as high as ~30A were observed.

The purpose of the present work has been to reduce tF and to increase IL while retaining the desirable features of the device. By modifying the epitaxial structure and adding recombination centers to the epitaxial drain region, we have achieved tF values as low as 100ns and IL values as high as 50A with rapid gate voltage turnoff.

Modified Structure

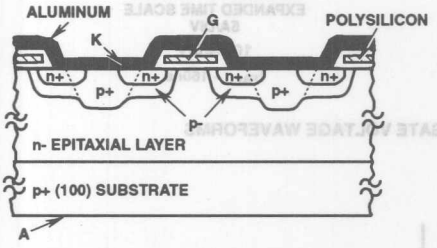
A schematic diagram of the original IGBT structure[4] is shown in Figure 1(a), and the equivalent circuit is shown in Figure 1(b); they are similar to those of an MOS-gated thyristor except for the presence of the shunting resistance Rs in each unit cell. The fabrication is like that of a standard n-channel power MOSFET, except that the n--epitaxial layer is grown on a p+ substrate instead of an n+ substrate. The heavily doped p+ region in the center of each unit cell, combined with the aluminum contact shorting the n+ and p+ regions, provides the shunting resistance RS. This has the effect of lowering the current gain of the n-p-n transistor in the equivalent circuit so that anpn + apnp <1, thereby preventing latching over a large operating range of anode voltage VA and anode current iA. However, for sufficiently large iA, emitter injection in the n-p-n transistor will increase, accompanied by an increase in anpn. When anpn + apnp increases to 1, the four-layer device will latch; the level of iA at which this occurs is the latching current level, IL. Thus, it

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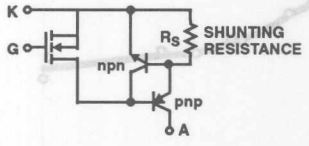
can be seen that a structure modification that lowers apnp will allow a greater range of iA (and anpn) without latching; that is, a reduction in apnp corresponds to an increase in IL.

The modified structure shown in Figure 1(c) differs from that in Figure 1(a) by the addition of a thin (~10mm) layer of n+ silicon in the epitaxial structure between the n- region and the p+ substrate. This n+ layer lowers the emitter injection efficiency of the p-n-p transistor in the equivalent circuit, and results in an increase in IL by a factor of 2 to 3. In addition, there is also a reduction in tF.

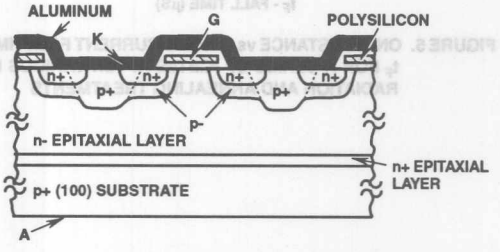
These results are illustrated in Figure 2, in which t_F, is plotted versus i_A for each device structure. It should be noted that IGBTss with the modified structure can block high voltage only in the forward voltage direction since the emitter junction (p+ - n+) of the p-n-p transistor breaks down at a low level when the polarity of the applied voltage is reversed.



(a) ORIGINAL STRUCTURE



(b) EQUIVALENT CIRCUIT



(c) MODIFIED STRUCTURE

FIGURE 1. (a) SCHEMATIC DIAGRAM OF ORIGINAL IGBTs STRUCTURE. (b) EQUIVALENT CIRCUIT (c) SCHEMATIC DIAGRAM OF MODIFIED STRUCTURE

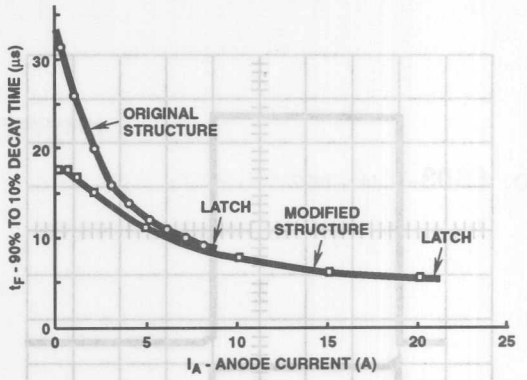


FIGURE 2. ANODE-CURRENT FALL TIME t_F VERSES ANODE CURRENT FOR ORIGINAL STRUCTURE AND MODIFIED STRUCTURE.

Addition Of Recombination Centers

We have used a variety of techniques to add recombination centers to IGBTss; these include high energy electron, gamma ray, and fast neutron irradiation, as well as heavy metal doping. The irradiations were carried out after completion of all of the high-temperature processing steps, but in each case an additional heat treatment was necessary to stabilize the devices by annealing out gate oxide charge, as well as those radiation induced defects in the silicon (recombination centers) that would otherwise anneal out slowly at the device operating temperature.[7] Typical values of t_F of the order of 1µs or less were achievable using any of the techniques.

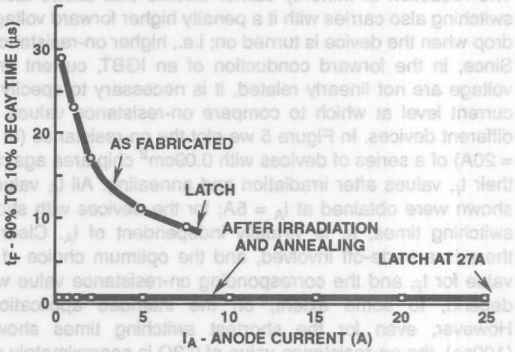
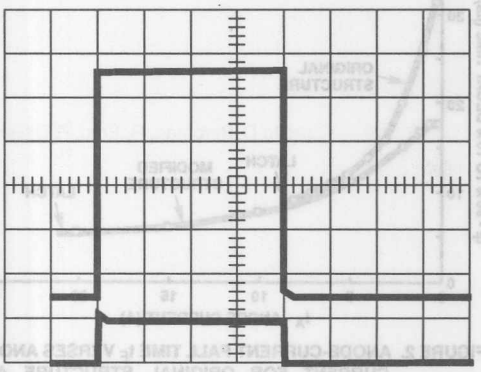
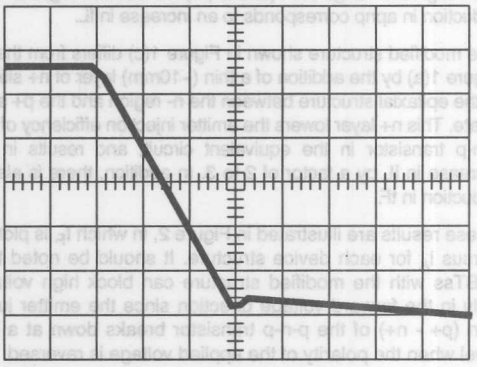


FIGURE 3. ANODE-CURRENT FALL TIME t_F VERSUS ANODE CURRENT FOR AN AS-FABRICATED DEVICE AND AFTER 14MeV NEUTRON IRRADIATION (10^{13}n/cm^2) FOLLOWED BY ANNEALING AT +300°C.

An example of the variation of t_F, with i_A (1) as fabricated and (2) after irradiation with 14MeV neutrons and annealing is shown in Figure 3. Here, the neutron fluence was ~10^{13}n/cm^2; this was followed by annealing at +300°C. Note that t_F, has not only been drastically reduced, but is virtually constant at ~0.6µs; i.e., almost independent of i_A.



TOP: ANODE CURRENT, 5A/DIV
BOTTOM: GATE VOLTAGE, 20V/DIV
5μs/DIV



ANODE CURRENT ON
EXPANDED TIME SCALE
5A/DIV
100ns/DIV
t_{FALL} ~ 160ns

FIGURE 4. IGBTs ANODE CURRENT AND GATE VOLTAGE WAVEFORMS

It is possible to lower tf, still further by appropriate irradiation and annealing or by heavy metal doping procedures, although this is not necessarily desirable for reasons that are discussed below. The smallest values of t_F that we have obtained for fully stabilized IGBT is in the range 100ns to 200ns. This is illustrated in Figure 4.

The reduction in minority carrier lifetime that allows faster switching also carries with it a penalty higher forward voltage drop when the device is turned on; i.e., higher on-resistance. Since, in the forward conduction of an IGBT, current and voltage are not linearly related, it is necessary to specify a current level at which to compare on-resistance values of different devices. In Figure 5 we plot the on-resistance (at i_A = 20A) of a series of devices with 0.09cm^2 chip area against their t_F values after irradiation and annealing. All t_F values shown were obtained at i_A = 5A; for the devices with short switching times, t_F is virtually independent of i_A. Clearly, there is a trade-off involved, and the optimum choice of a value for t_F and the corresponding on-resistance value will depend, to some extent, on the intended application. However, even for the shortest switching times shown (100ns), the on-resistance value of 0.2Ω is approximately an order-of-magnitude less than that of comparably sized n-channel MOSFETs.

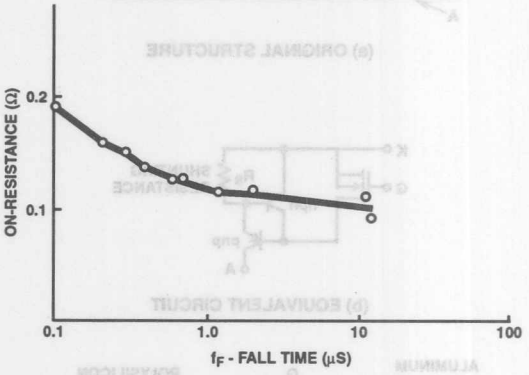


FIGURE 5. ON-RESISTANCE vs. ANODE-CURRENT FALL TIME t_F FOR A SERIES OF IGBTsS AFTER VARIOUS IRRADIATION AND ANNEALING TREATMENTS

Temperature Dependence Of T_f And I_l

All of the device performance data presented thus far have been measured at room temperature. However, power devices are often operated at elevated temperatures, and it is important to determine how their performance varies with temperature. In Figure 6 the variation of t_F and I_L for a device that has been irradiated and annealed is plotted versus temperature in the range +25°C to +150°C. This behavior is typical of all of the devices we have tested; i.e., tf increases and I_L decreases with increasing temperature, both by a factor of between 2 and 3 in the interval +25°C to +150°C.

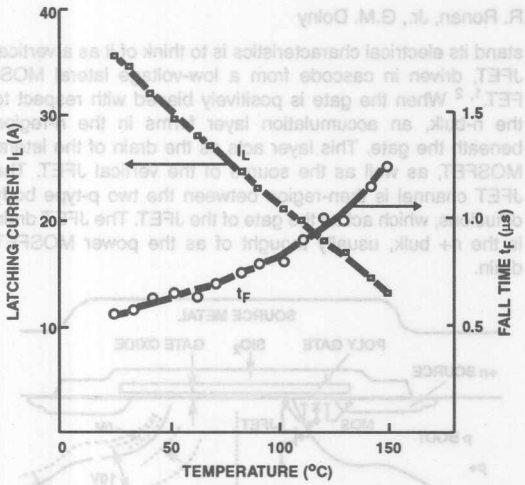


FIGURE 6. VARIATION OF ANODE-CURRENT FALL TIME t_F AND LATCHING CURRENT I_L WITH TEMPERATURE

Summary

By modification of the epitaxial structure of the IGBT and the addition of recombination centers, we have achieved anode-current fall times as low as 100ns in IGBT with latching currents as high as 50A for a 0.09cm^2 chip area. We have described the trade-off between on-resistance and anode-current fall time that may be obtained, and have demonstrated the variation of anode-current fall time and latching current with operating temperature.

Acknowledgment

The authors are indebted to D. Bergman, R. Ford, F. DiGeronimo, G. Looney, P. Robinson, W. Romito, L. Skurkey, M. Snowden, R. Stolzenberger, and the staff of the Integrated Circuit Technology Center at RCA Laboratories for their various contributions to the fabrication and characterization of the IGBTss. A special thank you goes to F. Taft, Z. Streletz, and H. Hendel who carried out the device irradiations.

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APPNOTE

No. 8610.1 May 1992 Harris Power MOSFETs

SPICING-UP SPICE II SOFTWARE FOR POWER MOSFET MODELING

Author: C.F. Wheatley, Jr., H.R. Ronan, Jr., G.M. Dolny

The SPICE II simulation software package is familiar to most designers working in computer-aided design of integrated circuits. Developed by L. W. Nagel in 1973, SPICE II has become a widely available, well-understood design tool for IC modeling and analysis. But, SPICE II has a shortcoming: its standard simulation programs were developed when all MOSFETs were low-power devices. Power MOS devices are growing in use today, both as discrete components and, potentially, as output stages of power integrated circuits. SPICE II in its current form doesn't recognize these new developments. Its built-in FET models aren't able to simulate all the modes of new power MOS device operation. For example, SPICE II doesn't recognize the way a power MOSFET's internal capacitances change with bias conditions, the presence of a cascode JFET that complicates both static and dynamic operation, or the presence of a parasitic body diode that affects operation in the third quadrant. Without this information, SPICE II will predict power MOSFET performance that is incorrect.

Since SPICE II's internal device models can't be easily changed for all existing copies, we looked for another approach to update the capabilities of this widely used simulation package in its standard form. Adding a "subcircuit" of external components that complement the devices within the SPICE II software, so as to form a true, equivalent circuit of a power MOSFET, is the answer.

The subcircuit works nicely with the standard SPICE II software, providing a model with all the terminal characteristics of a power MOSFET. Parameters of the subcircuit model can be determined from simple terminal measurements or from standard data sheets, using the algorithmic and empirical approach described below. Once these parameters are in place, SPICE II can be used to accurately simulate either p-channel or n-channel power MOSFET devices over a wide range of currents and voltages. The subcircuit functions as an embedded subroutine, so it can be used repetitively for any number of power MOSFETs in a design. This technique can be used to model power MOSFETs with any version of the SPICE II program presently available, without any modifications to its internal source code. The technique can also be used with other commercially available or in-house-developed circuit simulators.

Modeling The Power MOSFET

A cross-sectional view of a cell of a Harris IRF130 power MOSFET is shown in Figure 1. The easiest way to understand its electrical characteristics is to think of it as a vertical JFET, driven in cascode from a low-voltage lateral MOSFET.[1, 2] When the gate is positively biased with respect to the n-bulk, an accumulation layer forms in the n-region beneath the gate. This layer acts as the drain of the lateral MOSFET, as well as the source of the vertical JFET. The JFET channel is then-region between the two p-type body diffusions, which act as the gate of the JFET. The JFET drain is the n+ bulk, usually thought of as the power MOSFET drain.

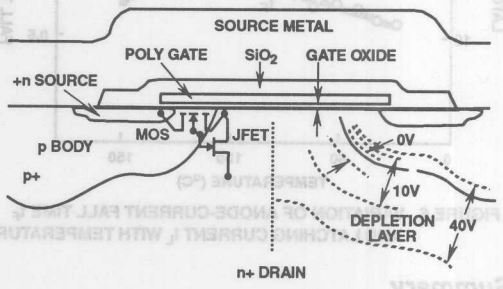


FIGURE 1. A CROSS-SECTIONAL VIEW SHOWS THE PHYSICAL MAKEUP OF THE LATERAL LOW-VOLTAGE MOSFET AND VERTICAL JFET THAT OPERATE IN CASCODE AS THE POWER MOSFET.

When you look at the power MOSFET this way, it becomes possible to use the standard SPICE II built-in device models, because SPICE II can simulate both the vertical JFET and the lateral MOSFET. When we use the subcircuit to add the rest of the Harris IRF130 power MOSFET to these SPICE II-simulated devices, we get a satisfactory equivalent circuit, shown in Figure 2.

The gate-to-source capacitance of the Harris IRF130 power MOSFET is represented by C_{21}. It is really a composite of two capacitances. The first is formed between the polysilicon gate and source metal (with the thick oxide as a dielectric). The second is formed between the gate and the n+ source (with the thin oxide acting as the dielectric). The value of C_{21} is essentially unchanged by voltage or current.

Capacitor C_{24} is formed between the power MOSFET gate and the accumulation layer, with the thin gate oxide as a dielectric. So long as the gate is positive with respect to the n-neck region, the accumulation layer exists and C_{24} doesn't

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change. But, if the external drain voltage (less their voltage drop across then-drift region) approaches the gate voltage, the accumulation layer starts to disappear. When that happens, C_{24} abruptly drops in value. This sudden change has to be taken into consideration.

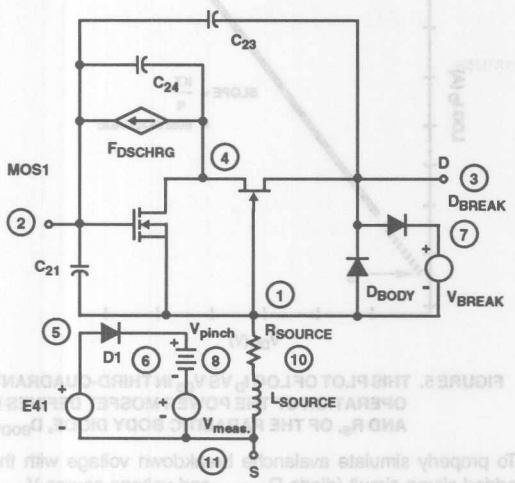


FIGURE 2. THE EQUIVALENT CIRCUIT OF THE POWER MOSFET IS MADE BY COMBINING SPICE II MODEL ELEMENTS WITH SOFTWARE SPECIFIED COMPONENTS ON A "SUBCIRCUIT."

Capacitor C_{23} represents the gate-to-drain capacitance of the Harris IRF130 power MOSFET. Because the accumulation layer normally acts as an electrostatic shield, C_{23} has no significance until the layer ceases to exist under the conditions just described. When it does disappear, the effect upon C_{23} is abrupt, and also has to be taken into consideration. The sudden changes in C_{24} and C_{23} cannot be easily modeled with the standard SPICE II software.

Figure 2 illustrates what happens: If the JFET source voltage (node 4) is very low compared to its pinch-off voltage, the JFET will be highly conductive, tightly coupling C_{24} to the JFET drain (which is also the drain of the Harris IRF130 power MOSFET). However, as the node 4 voltage approaches the pinch-off voltage (V_{PINCH}) of the JFET, it operates in a constant-current mode. This action decouples C_{24} from the JFET drain, making possible a much faster slew-rate, determined by C_{23}. If the node 4 voltage is allowed to exceed V_{PINCH} of the JFET, errors will exist in the output waveforms predicted by the standard SPICE II model.

To correct the situation, the added subcircuit includes a current-controlled current source, F_{DSCHRG}, and a current-sense network containing D1. If node 4 voltage begins to exceed V_{PINCH} of the JFET, D1 conducts, and its current is sensed at V_{MEAS}. The high-gain current source F_{DSCHRG} is turned-on rapidly and partially discharges C_{24}, pinning node 4 voltage at the pinch-off voltage of the JFET. In setting up the parameters of the subcircuit, the ideality factor of D1 is set at 0.03 to assure that node 4 voltage will never exceed V_{PINCH} of the JFET by more than a few millivolts. This condition results in waveform predictions from the SPICE II model that represent the true characteristics of the power MOSFET.

The body diode (D_{BODY} in Figure 2) is formed by the drain-to-body diffusion pn junction of the Harris IRF130 power MOSFET. D_{BODY} is added as an external component in the subcircuit because the built-in gate-to-drain diode of the SPICE II JFET model is inconvenient when it comes to modeling third-quadrant conduction of a power MOSFET. We want most of the third-quadrant current to flow in D_{BODY}. So, we effectively delete the SPICE II model's built-in diode by setting its saturation current parameter to an artificially low value, such as 10^{-20} ampere.

To round-out the subcircuit, a resistor value is chosen for the JFET drain of the SPICE II model to represent the series resistance of the n-drain region of the Harris IRF130 power MOSFET.[3] We also add resistor R_{SOURCE} to represent the series source resistance of the Harris IRF130 power MOSFET: a composite of resistances in the n+ source region, contact resistance, and source-metal series resistance. Finally, we add inductor L_{SOURCE} to represent the source inductance of the power MOSFET contributed by the source metallization and bond wires.

Choosing Parameters to Simulate A Power MOSFET

To accurately simulate the terminal characteristics of the physical power MOSFET you are working with, you will need to adjust the SPICE II model parameters and select subcircuit component values. Look first at adjustment of the SPICE II model. The static current-voltage characteristics of the power MOSFET are determined by the low-voltage lateral MOSFET included in the SPICE II model; Figure 2. In saturation (large values of V_{DS}), the lateral MOSFET device is modeled according to the following equation:

$$I_{DS} = \frac{(K_P)W\,(V_{GS} - V_{TO})^2}{2L}$$

where

K_P = Process Transconductance Parameter

V_{TO} = Threshold Voltage

W = L = 1μm (Fixed In This Note For Convenience)

I_{DS} = MOSFET Drain Current

V_{GS} = MOSFET Gate-To-Source Voltage

Continuing with the example device, the Harris IRF130 power MOSFET, a plot of the square root of I_{DS} versus gate voltage (V_{GS}) provides the curves shown in Figure 3 for V_{DS} = 10 volts. These curves provide the process transconductance parameter, $(K_P/2)^{0.5}$, and threshold voltage, V_{TO}, directly. This data can then be used to find the value of source resistance, R_{SOURCE}. This series resistance is important because it causes the curve produced by plotting the square root of I_{DS} versus V_{GS} to depart from linearity at high current levels. Departure at very low current levels is caused by subthreshold conduction, which we ignore in this model.

To find the JFET drain resistance, we use the value of source resistance, R_{SOURCE}, and plots of I_{DS} versus V_{DS} for operation in the linear region, as shown in Figure 4.

To find the current, resistance and capacitance parameters of the body diode (D_{BODY} in Figure 2), first plot log I_{DS} versus V_{DS}, as shown in Figure 5, holding the gate voltage, V_{GS}, negative for third-quadrant operation; i.e., where V_{DS} is less than 0. This plot gives the saturation current and resistance of D_{BODY}. The minority-carrier transit-time parameter (TT) of the SPICE II program is chosen to provide the best fit to measured transient reverse-recovery data. The junction capacitance value of D_{BODY} is equal to the power MOSFET device output capacitance, C_{OSS}, at zero volts. This value can be obtained from the device data sheet, or by bridge measurement. It is usually specified at 25 volts, and may be converted to zero volts by multiplying by 6.

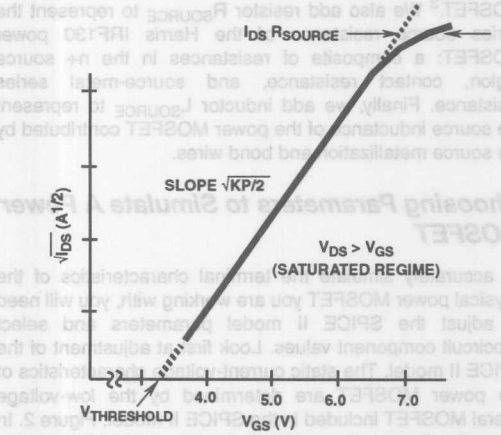


FIGURE 3. THIS PLOT OF THE SQUARE ROOT OF DRAIN CURRENT vs. GATE VOLTAGE DEFINES THE THRESHOLD VOLTAGE, V_{TO}, $(K_P/2)^{0.5}$, AND R_{source}, FOR THE POWER MOSFET.

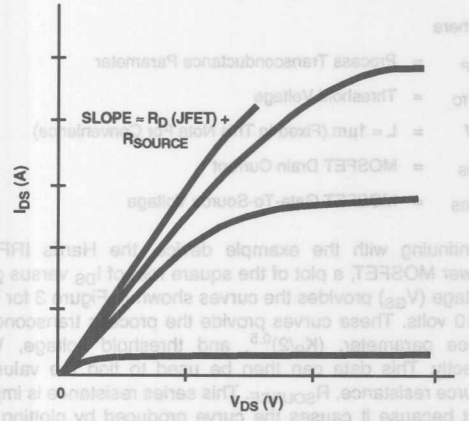


FIGURE 4. DRAIN CURRENT vs. DRAIN VOLTAGE OF THE POWER MOSFET PLOTTED USING CONSTANT GATE VOLTAGES. THIS CURVE DEFINES THE ON RESISTANCE OF THE DEVICE.

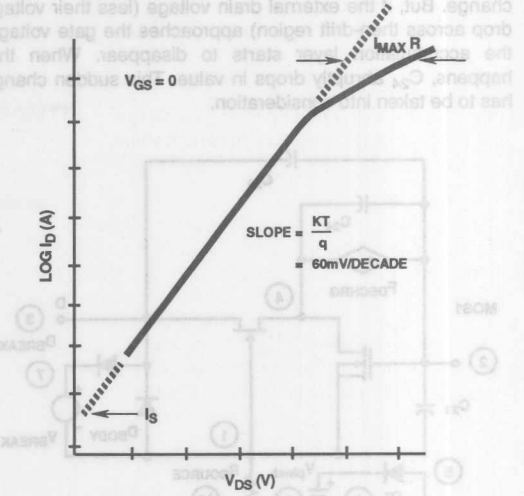


FIGURE 5. THIS PLOT OF LOG I_D VS V_{DS} IN THIRD-QUADRANT OPERATION OF THE POWER MOSFET DEFINES I_S AND R_S, OF THE PARASITIC BODY DIODE, D_{BODY}.

To properly simulate avalanche breakdown voltage with the added clamp circuit (diode D_{BREAK} and voltage source V_{break} in Figure 2), first set the voltage level of V_{BREAK} equal to the measured value of drain breakdown voltage. Then, adjust the SPICE II model parameters I_S, N, and R_S for D_{break} to obtain the best fit to the measured breakdown voltage curve.

Selection of capacitors C_{21}, C_{23}, and C_{24}, and the parameters of the JFET (all shown in Figure 2), can be made using the curves of Figure 6. This is a plot of drain and gate voltage versus time for a power MOSFET driven with constant

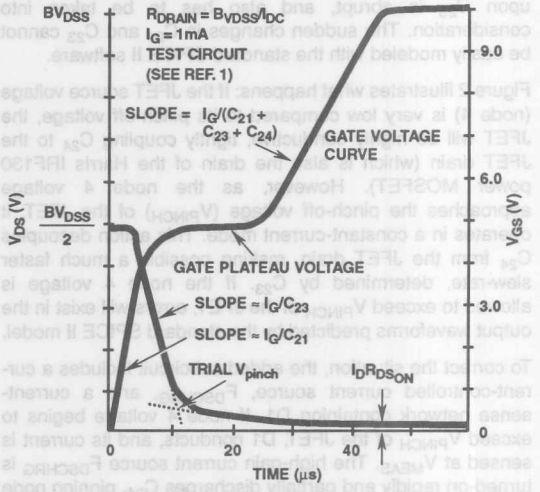


FIGURE 6. PLOTTING DRAIN AND GATE VOLTAGES OF THE POWER MOSFT VS TIME DETERMINES THE VALUES OF C_{21}, C_{23}, C_{24}, AND V_{pinch}.

gate current (I_G).[1] The initial slope of the V_{GS} curve defines C_{21} (since for any value of gate voltage, V_{GS}, less than threshold voltage, V_{TO}, the power MOSFET is in its off-state, so that the gate-to-source capacitance, C_{21}, charges linearly under constant-current conditions). As V_{TO} is reached, the low-voltage lateral MOSFET (Figure 2) turns on, and its drain voltage drops toward its minimum value.

At the outset, the JFET is operating beyond pinch-off, and the slope of the V_{DS}-versus-time curve is controlled by C_{23}. However, when the drain voltage falls below V_{PINCH}, the JFET conducts, strongly coupling C_{24} to the JFET drain and greatly reducing the drain voltage slew rate. Thus, the value of C_{23} can be approximated from the steep slope of the VDS curve in Figure 6, while the value of C_{21}+C_{23}+C_{24} corresponds to the labelled V_{GS} slope. These values can be adjusted slightly to give the best slope fit. A trial value of V_{PINCH} (and V_{TO}) is given by the labelled intercept of the V_{DS} curve. Adjustments of this value will control the length of the gate plateau voltage needed to complete the curve fit.

Table I lists the preferred algorithm for parameter extraction; Table II summarizes the required empirical inputs. Together, these tables will aid in setting up the parameters for evaluation of a power MOSFET with SPICE II and the subcircuit. As an example, Table 3 summarizes the input parameters for the SPICE II model and subcircuit, determined for the Harris IRF130 power MOSFET, using the approach just described. The IRF130 is rated at 14 amperes and has a 100-volt blocking capability.

TABLE 1. PREFERRED ALGORITHM FOR PARAMETER EXTRACTION

1.	Determine K_P of lateral MOS
2.	Determine V_{TO} of lateral MOS
3.	Determine C_{21}
4.	Determine $C_{21} + C_{23} + C_{24}$
5.	Determine Rsource and JFET drain resistance
6.	Assign beta of JFET = 100 x K_P of lateral MOS
7.	Use trial V_{PINCH}
8.	Use trial C_{23} and calculate C_{24}
9.	Curve fit for slope by repeating step 8 with different values of C_{23}.
10.	Adjust V_{PINCH} and V_{TO} of JFET to fix gate-voltage plateau

TABLE 2. EMPIRICAL INPUTS

MOSFET	Enhancement mode:W = L = 1µm; K_P (Figure 3); V_{TO} (Figure 3); C's = 0; T_{OX} = 1E6µm
JFET	Depletion mode; area factor = 1; Beta = 100K_P (Figure 3); V_{TO} = -V_{pinch} (Figure 6); C's = diode lifetime = 0; diode ideality factor = 1.0; Is = 1E - 20; R_D (Figure 4)
D_{BODY}	I_S from Figure 5; Ideality Factor = 1.0; R_S from Figure 5 (must be very much smaller than R_D); C (from C_{OSS}); lifetime = best fit to T_{RR}

TABLE 2. EMPIRICAL INPUTS (Continued)

D_{BREAK}	I_S = arbitrary; C = lifetime = 0; ideality factor = best low-current fit; R = best high-current fit
D1	I_S = 1E - 13; C = lifetime = 0; ideality factor = 0.03; R_S = 1
R_{SOURCE}	Figure 3
L_{SOURCE}	Approx. (5L)ln(4L/d) nH; L and d are source wire inches
V_{PINCH}	Figure 6
V_{BREAK}	Avalanche voltage
C_{21}	Figure 6
C_{23}	Figure 6
C_{24}	Figure 6

TABLE 3 - INPUT PARAMETERS OF IRF130 TO SPICE MODEL

SPICE PARAMETER	HARRIS IRF130 VALUE
LATERAL MOS	
Model Level	1
T_{OX}	1E06µ
V_{TO}	3.4V
K_P	6.4A/V^2
W, L	1.0µ
VERTICAL JFET	
JMOD Area	1
V_{TO}	-6.4V
Beta	640
I_S	10^{-20}
R_D	42.15 x $10^{-3}\Omega$
D_{BODY}	
CJO	1650pF
IT	70 x 10^{-9}
I_S	3 x 10^{-12}
R_S	2.5 x $10^{-3}\Omega$
PASSIVE ELEMENTS	
C_{21}	900pF
C_{23}	40pF
C_{24}	1360pF
R_{SOURCE}	17.5 x $10^{-3}\Omega$
L_{SOURCE}	7.5 x 10^{-9}H
V_{BREAK}	117V

Implementing The Subcircuit in SPICE II

Table IV is the input listing for the implementation of the power MOSFET subcircuit in SPICE II software. Nodes are identified for drain, gate, and source of the power MOSFET. The subcircuit then "hooks" to these nodes wherever specified in the SPICE II simulation. Any number of power MOSFETs can be specified. The parameters listed are for an IRF130 power MOSFET.

The Results

The real test oftheenhanced SPICE II model is how closely its predicted performance compares with actual measurements. Using the input parameters for the Harris IRF130 device example given in Table III, we calculated transfer and output curves for the model. These curves were then compared against measured static data. Figures 7 and 8 show the precise fit between predicted and measured static data, even at low values of drain voltage.

To see how the model performs in dynamic prediction, we simulated first-quadrant operation (including avalanche mode) and third-quadrant operation for the Harris IRF130 power MOSFET. Once again, the predicted performance of the enhanced SPICE II model fits actual measurements satisfactorily over the entire operating range of the Harris IRFI30, as shown in Figures 9 and 10.

To compare calculated switching performance versus actual measurement on the Harris IRF130, we used the enhanced SPICE II model to generate switching curves. Figure11 shows drain and gate voltages versus time with a constant gate-current drive. Figure 12 shows drain and gate voltages versus time for a step gate-voltage input. Actual measured data was then taken and overlaid on the points predicted by the enhanced SPICE II model. Again, the fit was accurate in each case.

TABLE 4 - INPUT LISTING OF SUBCIRCUIT MODEL
Listed Parameters Valid for a Harris IRFI30 Power MOSFET

```
* THIS IS THE POWER MOS SUBCIRCUIT
* NODE 3 IS THE POWERMOS DRAIN
* NODE 2 IS THE POWERMOS GATE
* NODE 11 IS THE POWERMOS SOURCE
*
*
.OPTIONS NOMOD NOLIST NOACCT NONODE LIMPTS=250 GMIN=1.0E-20
.SUBCKT POWMOS 3 2 11
.C21 2 1 900P
.C23 2 3 40P
.C24 2 4 1360P
.FDSCHRG 4 2 VMEAS 1.0
.MOS1 4 2 11 MOSMOD L=1U W=1U
.JFET 3 1 4 JMOD AREA=1
.DBODY 1 3 DMOD2
.RSOURCE 1 10 17.5E-03
.LSOURCE 10 11 7.5N
.E41 5 11 4 1 1.0
.D1 5 6 DMOD
.VPINCH 6 8 DC 6.4
.VMEAS 8 11 DC 0.0
.DBREAK 3 7 DMOD3
.VBREAK 7 1 DC 117
.MODEL MOSMOD NMOS VTO=3.4 KP=6.40 TOX=1.0E+06U
.MODEL JMOD NJF VTO=-6.4 BETA=640 IS=1.0E-20 RD=42.5E-03
.MODEL DMOD D IS=1.0E-13 N=0.03 RS=1.0
.MODEL DMOD2 D CJO=1650P TT=70N IS=3.0E-12 RS=2.5E-03
.MODEL DMOD3 D IS=1E-13 RS=2.0 N=1.0
.ENDS
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*
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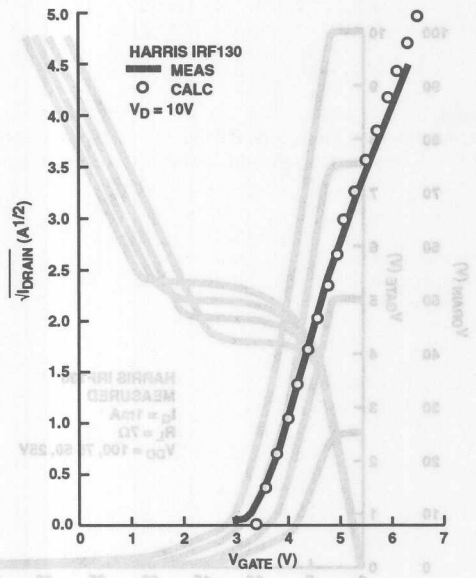


FIGURE 7. MEASURED SQUARE ROOT OF DRAIN CURRENT (DRAIN VOLTS = 10) vs. GATE VOLTAGE FOR THE HARRIS IRF130 POWER MOSFET IS PLOTTED ALONG WITH THE CALCULATED VALUES FOR THE ENHANCED SPICE II MODEL. AN EXCELLENT FIT IS OBTAINED.

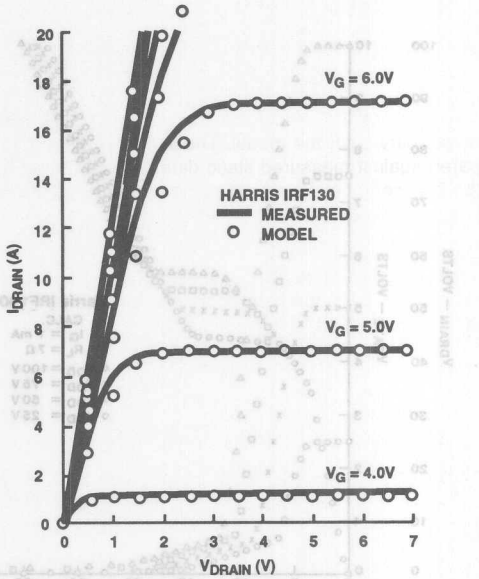


FIGURE 8. PLOTS OF DRAIN CURRENTvs. DRAIN VOLTAGE FOR THE HARRIS IRF130 POWER M0SFET SHOW AN EXCELLENT FIT BETWEEN MEASURED VALUES AND THOSE CALCULATED BY THE ENHANCED SPICE II MODEL FOR VARIOUS VALUES OF CONSTANT GATE VOLTAGE.

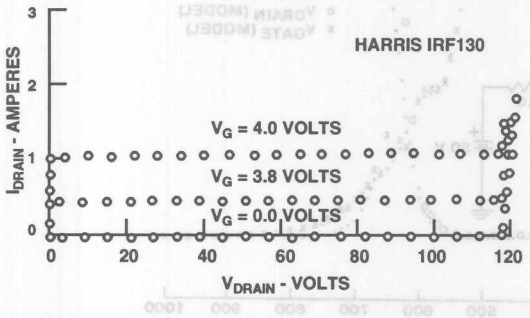


FIGURE 9. FIRST QUADRANT DRAIN CURRENT vs. DRAIN VOLTAGE WITH V_{GS} HELD CONSTANT IS CALCULATED BY THE ENHANCED SPICE II MODEL OF THE HARRIS IRF130 POWER M0SFET. NOTE THAT THE MODEL PREDICTS AVALANCHE BREAKDOWN.

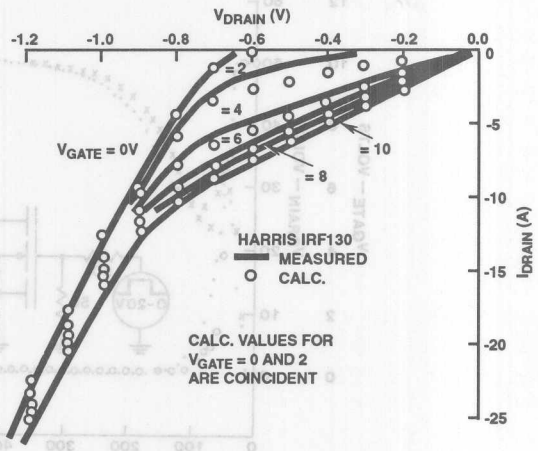


FIGURE 10. THIRD-QUADRANT OPERATION OF THE HARRIS IRF130 SHOWS AGREEMENT BETWEEN THE PREDICTED VALUES OF THE ENHANCED SPICE II MODEL AND ACTUAL MEASURED VALUED OF DRAIN CURRENT vs DRAIN VOLTAGE AT DIFFERENT VALUED OF CONSTANT GATE VOLTAGE.

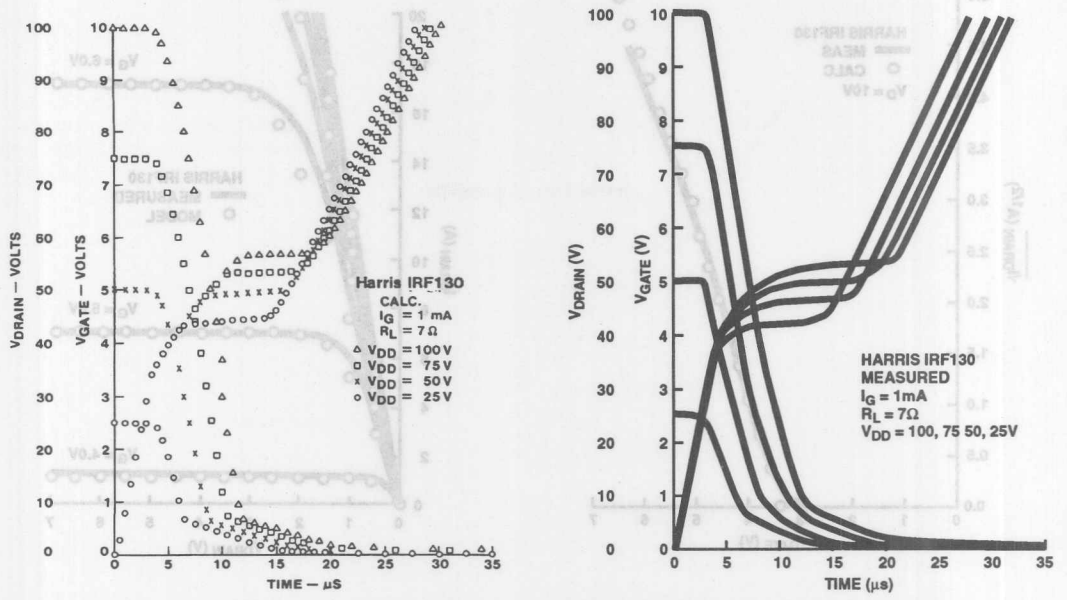


FIGURE 11. THESE PLOTS OF DRAIN AND GATE VOLTAGES vs. TIME FOR CONSTANT GATE CURRENT SHOW AGREEMENT BETWEEN THE PREDICTIONS OF THE ENHANCED SPICE II MODEL (a) AND MEASURED PERFORMANCE OF THE HARRIS IRF130 POWER M0SFET (b).

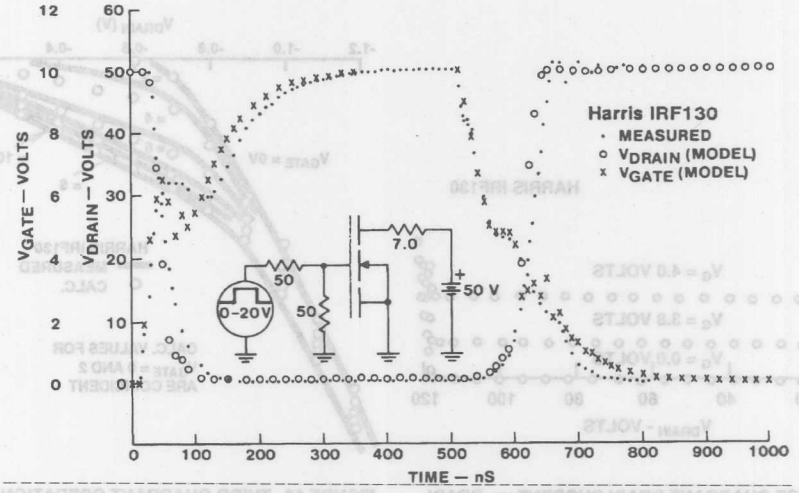


FIGURE 12. SWITCHING PERFORMANCE OF THE HARRIS IRF130 POWER MOSFET IS CLOSELY PREDICTED BY THE ENHANCED SPICE II MODEL IN THIS PLOT OF MEASURED AND CALCULATED VALUES OF DRAIN AND GATE VOLTAGES vs. TIME IN A STANDARD SWITCHING CIRCUIT.

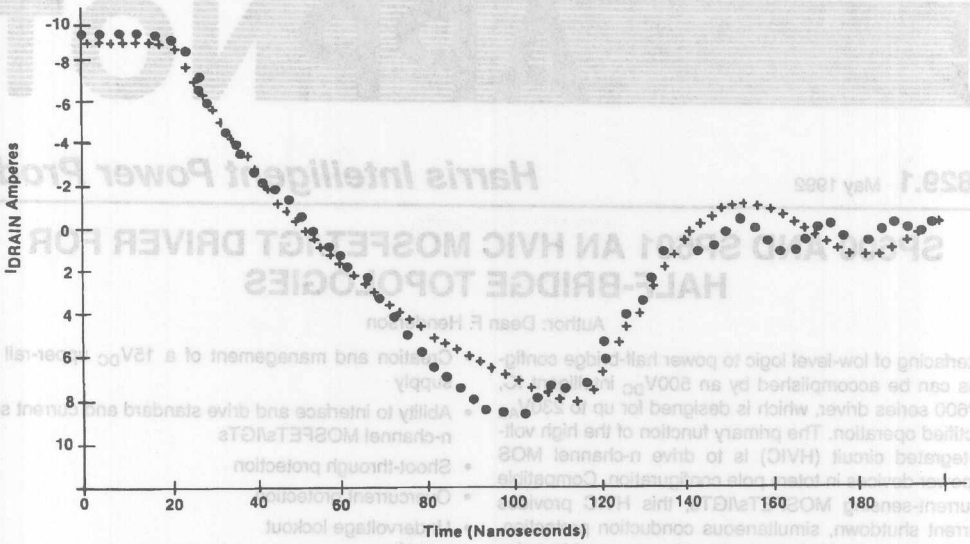


FIGURE 13. THE CALCULATED THIRD-QUADRANT DIODE RECOVERY WAVEFORM OF THE ENHANCE SPICE II MODEL SHOWS GOOD AGREEMENT WITH THAT ACTUALLY MEASURED FOR THE HARRIS IRF130 POWER MOSFET

Finally, the enhanced model was used to compare calculated and measured body diode (D_{BODY} in Figure 2) recovery time curves in third-quadrant operation of the Harris power MOSFET. Figure 13 shows the good agreement between predicted and actual results.

This approach provides excellent results when there is a need to model the performance of a power MOSFET. Not only will the approach update SPICE II (or other circuit simulation CAD program) so that it will simulate the latest state-of-the-art in MOS power, but it will allow quick analysis of every static and dynamic characteristic for suitability in a proposed design.

References

1. Wheatley, Jr., C.F. and Ronan Jr., H.R., "Switching Waveforms of the L^2FET: A 5-Volt Gate Drive Power MOSFET," Power Electronic Specialist Conference Record, June 1984, p. 238.
2. Ronan Jr., H.R. and Wheatley Jr., C.F., "Power MOSFET Switching Waveforms: A New Insight," Proceedings of Powercon 11, April 1984, p. C3.
3. Niehaus, H.A., Bowers, J.C. and Herren Jr., P.C., "A High Power MOSFET Computer Model," Power Conversion International, January 1982, p. 65.

Harris Semiconductor

APPNOTE

No. 8829.1 May 1992

Harris Intelligent Power Products

SP600 AND SP601 AN HVIC MOSFET/IGT DRIVER FOR HALF-BRIDGE TOPOLOGIES

Author: Dean F. Henderson

The interfacing of low-level logic to power half-bridge configurations can be accomplished by an $500V_{DC}$ intelligent IC, the SP600 series driver, which is designed for up to $230V_{AC}$ line rectified operation. The primary function of the high voltage integrated circuit (HVIC) is to drive n-channel MOS gated power devices in totem pole configuration. Compatible with current-sensing MOSFETs/IGTs, this HVIC provides overcurrent shutdown, simultaneous conduction protection, and undervoltage lockout. Logic level inputs provide noise immune control of power element switching.

The SP600 has demonstrated high frequency (130 kHz) operation as well as the ability to withstand high dv/dt. Its semicustom design flexibility makes it easily adaptable to a wide range of single and multiple phase applications. Other salient features of the device are described below.

Technology Overview

BiMOS structures are implemented in a junction-isolation process, known as "lateral charge control",[1] that supports high voltage laterally. By the use of this thin epi process, low voltage analog and digital circuitry can be combined monolithically with high voltage transistors. Low voltage circuits can be constructed to float up to $500V_{DC}$ with respect to the substrate. Additionally, $500V_{DC}$ NMOS and n-p-n transistors can also be fabricated.[2] Since this process conforms to mainstream low voltage IC manufacturing, it is cost effective.

Totem Pole Drivers

Historically, designers have been faced with awkward decisions regarding the upper-rail drive of bridge topologies. P-channel MOSFETs, while easy to drive, are more than twice as expensive as equivalent n-channel devices having the same rds(on). Economic barriers and product availability generally prohibit design beyond $200V_{DC}$. On the other hand, the driving of upper rail n-channel MOS gated devices requires a floating gate supply that must be 5 to $20V_{DC}$ greater than the upper rail link. While several discrete approaches for implementing this floating supply are known, the designer is burdened with additional components and potential dv/dt problems associated with voltage translation.

The SP600 series driver provides the economical solution as an intelligent totem pole n-channel driver. With the addition of as few as five, user defined, external, passive components (three if current detection isn't employed) a functional half-bridge driver can be built that has the following features:

- Creation and management of a $15V_{DC}$ upper-rail power supply
- Ability to interface and drive standard and current sensing n-channel MOSFETs/IGTs
- Shoot-through protection
- Overcurrent protection
- Undervoltage lockout
- CMOS logic-level input compatibility
- Semicustom flexibility through metal-mask changes
- Standard 22-pin DIP packaging

Theory of Operation

Figure 1 is the basic block diagram of the SP600. CMOS logic compatible input signals are filtered to ensure reliable operation when the device is subjected to noisy industrial environments. Digital commands at TOP and BOTTOM inputs cause the upper or lower drivers, respectively, to turn on or off. The $I_{TRIP\ SELECT}$ input provides a higher than nominal current limit on a pulse-by-pulse basis. The input signals are decoded to drive the appropriate output device. High voltage translation is provided by current mirror pulses used to communicate upward to the top gate driver to initiate turn on or off (I_{ON}/I_{OFF} pulses). These momentary pulses are captured by local latches to maintain the desired state. This feature minimizes power dissipation in the level shifter and provides added noise immunity as well. The bottom gate driver circuitry is similar. The floating bootstrap power supply is provided by low voltage capacitor C_F and high voltage diode D_F. Each time the V_{OUT} node goes low, C_F charges to roughly a diode drop less than Vdd ($15V_{DC}$). This situation prevails each time the lower output device is activated or, in the case of an inductive load, whenever the upper device is switched off and freewheeling load current forces the output node to a diode drop below ground. In either case, D_F is forward biased, allowing C_F to charge through the current limiting resistor R_{BS} to approximately V_{DD}. Noise dropping resistor R_{ND}, along with capacitor C_{DD}, provides localized filtering of the bias supply and bypasses bias supply series inductance facilitating fast and complete bootstrap refresh.

Each output device is protected on a pulse-by-pulse basis from overcurrent (OC) by sense resistor R_S, which is connected to 100mV comparators. This arrangement permits the designer to take advantage of nearly lossless current-sensing MOSFETs or IGTs.

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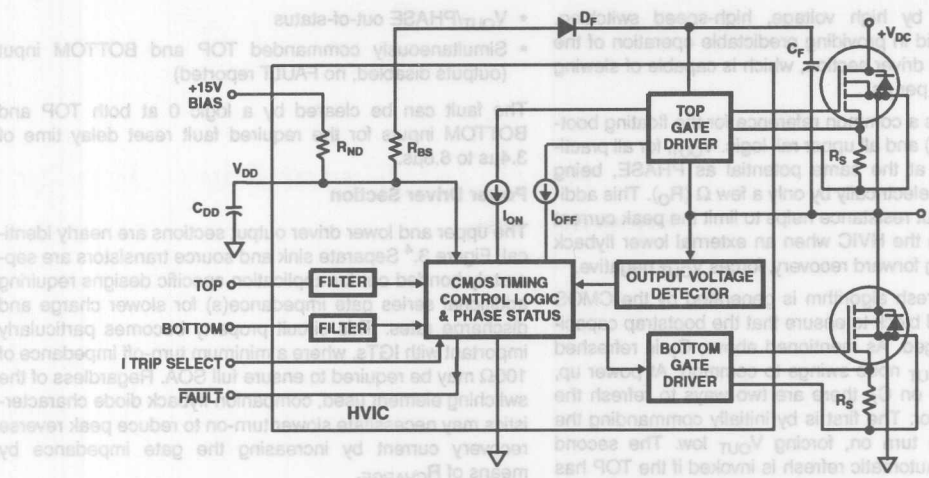


FIGURE 1. BLOCK DIAGRAM OF THE HVIC

Upon detection of any OC, the output is immediately disabled. In the case of the lower switch, a FAULT is directly detected and reported. Upper rail OC FAULTs are indirectly reported via the output voltage monitor when it detects an output state not in agreement with the commanded TOP input signal. With local OC detection and shutdown of the upper device, an inductive load will force V_{OUT} low due to freewheeling. This "out of status" detector recognizes a fault when V_{OUT} is typically less than $5.5V_{DC}$.

Logic And Timing

Figure 2 is a detailed functional circuit of the SP600. The filtered inputs, TOP, BOTTOM, and $I_{TRIP\ SELECT}$, ignore pulse widths less than typically 400ns to prevent false triggering. During the generation of I_{ON} and I_{OFF} pulses, the control logic ignores further changes in the input signal. For each I_{ON} pulse, an I_{OFF} pulse is simultaneously sent to the opposite driver, thus eliminating the possibility of spurious shoot

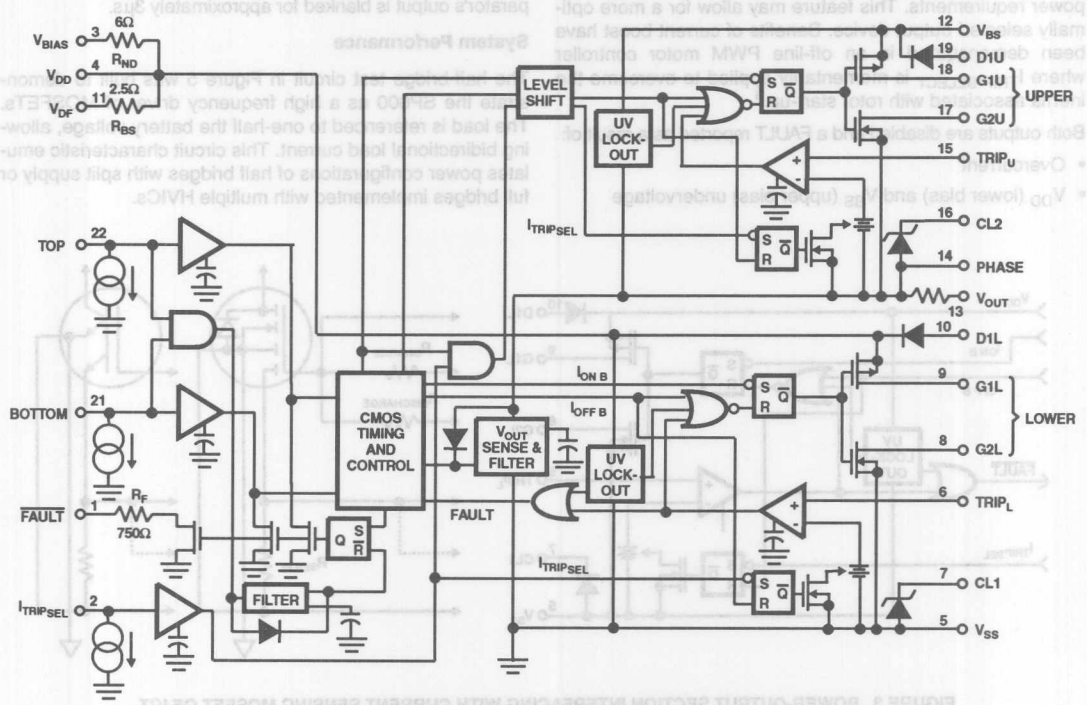


FIGURE 2. FUNCTIONAL DIAGRAM OF THE HVIC

through caused by high voltage, high-speed switching. These features aid in providing predictable operation of the floating upper rail driver section, which is capable of slewing over 10,000 volts per µs.

PHASE serves as a common reference for the floating bootstrap supply (V_{BS}) and all upper rail logic. V_{OUT}, for all practical purposes, is at the same potential as PHASE, being separated from it electrically by only a few Ω (R_O). This additional series output resistance helps to limit the peak current being drawn from the HVIC when an external lower flyback diode, undergoing forward recovery, forces V_{OUT} negative.

An automatic refresh algorithm is generated by the CMOS timing and control block to ensure that the bootstrap capacitor remains charged. As mentioned above, C_F is refreshed each time the V_{OUT} node swings to common. At power up, with zero voltage on C_F, there are two ways to refresh the bootstrap capacitor. The first is by initially commanding the bottom device to turn on, forcing V_{OUT} low. The second occurs when an automatic refresh is invoked if the TOP has been commanded on for longer than 200µs to 500µs. The logic momentarily ignores the inputs, and turns on the lower output (subsequent to an I_{OFF} TOP) for typically 2.0µs, charges C_F and finally restores control to the input commands. Automatic refresh is overridden at switching rates greater than 5kHz, the minimum refresh timer period.

A dual level current limit provision allows for a 30% higher current trip point (above nominal) on a pulse-by-pulse basis. A logic level 1 applied to $I_{TRIP\ SELECT}$ provides a boosted current limit suited for applications like uninterruptable power supplies (UPS), which may have occasional shifted peak power requirements. This feature may allow for a more optimally selected output device. Benefits of current boost have been demonstrated in an off-line PWM motor controller where $I_{TRIP\ SELECT}$ is momentarily applied to overcome the inertia associated with rotor start-up.[3]

Both outputs are disabled and a FAULT reported as a result of:

- Overcurrent
- V_{DD} (lower bias) and V_{BS} (upper bias) undervoltage
- V_{OUT}/PHASE out-of-status
- Simultaneously commanded TOP and BOTTOM input (outputs disabled, no FAULT reported)

The fault can be cleared by a logic 0 at both TOP and BOTTOM inputs for the required fault reset delay time of 3.4µs to 6.6µs.

Power Driver Section

The upper and lower driver output sections are nearly identical, Figure 3.[4] Separate sink and source transistors are separately bonded out for application specific designs requiring additional series gate impedance(s) for slower charge and discharge rates. This circuit property becomes particularly important with IGTs, where a minimum turn-off impedance of 100Ω may be required to ensure full SOA. Regardless of the switching element used, companion flyback diode characteristics may necessitate slower turn-on to reduce peak reverse recovery current by increasing the gate impedance by means of R_{CHARGE}.

A nominal 100mV_{DC} comparator provides overcurrent (OC) protection when used with either current sensing IGTs or MOSFETS. OC can also be implemented by using low impedance shunts with noncurrent sensing power output devices, Figure 4.

Clamp CL1 in Figure 4 provides overvoltage protection for current sensing structures during switching intervals, and protects the comparator from any voltage transients due to external lead inductances. To avoid nuisance OC trips caused by reverse recovery current during turn-on transitions, the comparator's output is blanked for approximately 3µs.

System Performance

The half-bridge test circuit in Figure 5 was built to demonstrate the SP600 as a high frequency driver of MOSFETs. The load is referenced to one-half the battery voltage, allowing bidirectional load current. This circuit characteristic emulates power configurations of half bridges with split supply or full bridges implemented with multiple HVICs.

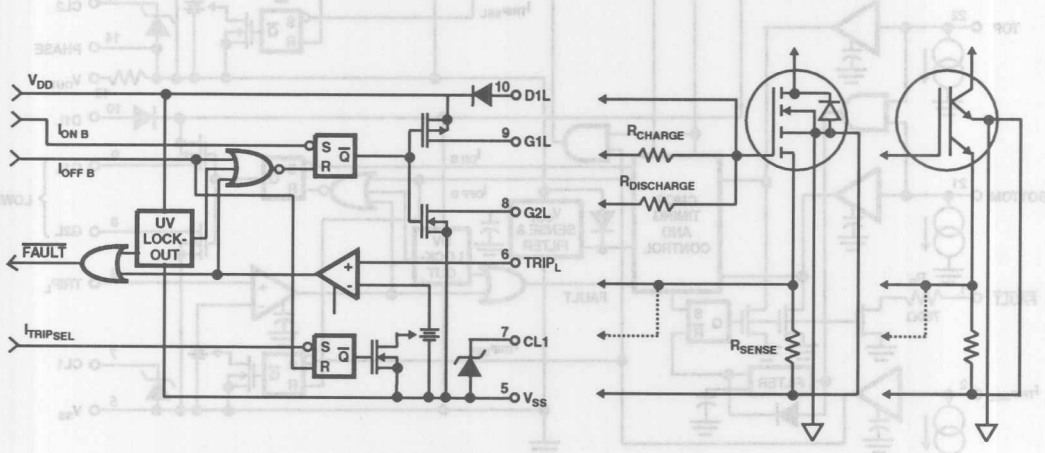


FIGURE 3. POWER-OUTPUT SECTION INTERFACING WITH CURRENT SENSING MOSFET OF IGT.

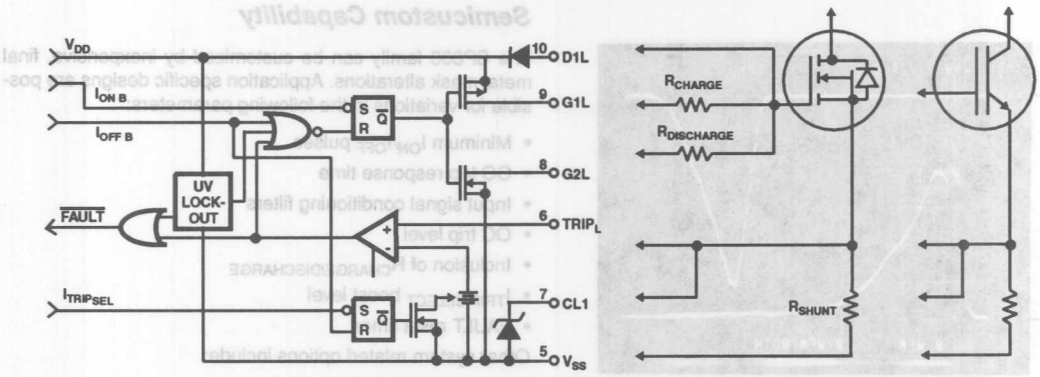


FIGURE 4. POWER OUTPUT SECTION INTERFACING WITH NONCURRENT SENSING MOSFET OR IGT.

For ultimate switching speed, no additional series gate impedances were used. Peak MOSFET gate charge and discharge current waveforms of 400 and 510mA_{DC}, respectively, were observed, Figure 6.

High frequency, high voltage operation requires that upper rail drive and level translator circuitry be immune to high dv/dt, as this section floats with respect to V_{OUT}/PHASE. Interjunction capacitance can dynamically inject displacement currents, raising havoc in circuit performance or even causing catastrophic failures, including the breakdown of voltage isolation tubs or latch-up in adjacent four layer structures.

At rail voltages of 200V_{DC} to 400V_{DC}, rise and fall transitions of V_{OUT}/PHASE were measured in the 20ns to 35ns region.

The HVIC operated flawlessly while being subjected to output swings beyond 11,000V per µs. Figure 7 demonstrates the HVIC's ability to sustain such dv/dt when driving IRF820 devices.

IRF 842s were driven at 130kHz in this same half-bridge circuit, Figure 8. The ultimate switching speed of the SP600 series HVIC will depend on gate capacitance and the duty cycle limits dictated by the minimum I_{ON} and I_{OFF} times. A minimum I_{ON} time (1.6µs to 3.1µs) ensures time for refresh, while a minimum I_{OFF} time (1.3µs to 3.4µs) prevents simultaneous conduction by allowing for gate discharge prior to an opposite I_{ON} pulse. The same promising technology has been shown to operate a half-bridge resonant converter at frequencies up to 600kHz.[6]

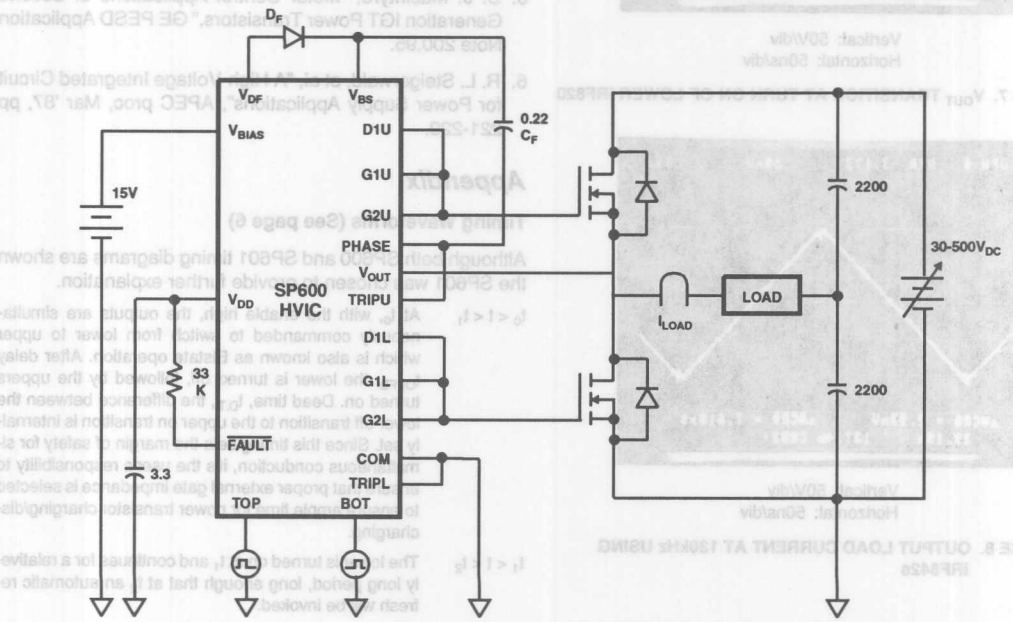
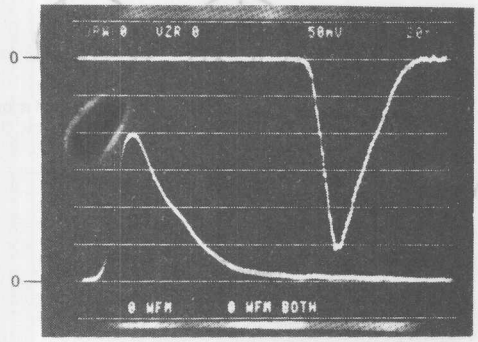
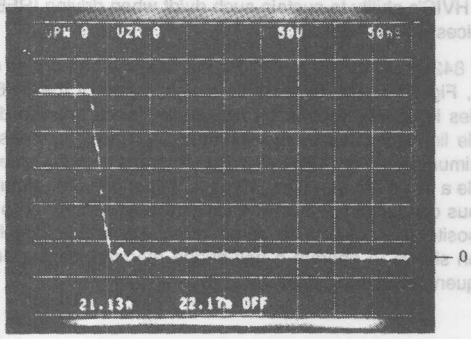


FIGURE 5. HALF-BRIDGE TEST CIRCUIT



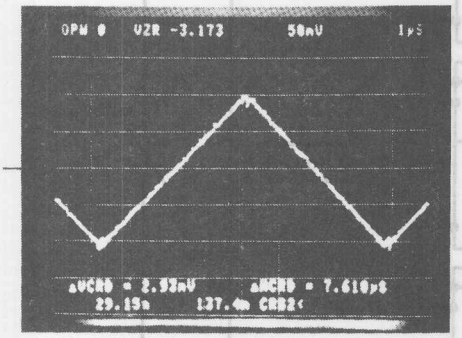
Top: Turn Off Vertical: 100mA/div
Bottom: Turn On Horizontal: 20ns/div

FIGURE 6. GATE-CURRENT WAVEFORMS DRIVING AN IRF820



Vertical: 50V/div
Horizontal: 50ns/div

FIGURE 7. V_{OUT} TRANSITION AT TURN ON OF LOWER IRF820



Vertical: 50V/div
Horizontal: 50ns/div

FIGURE 8. OUTPUT LOAD CURRENT AT 130kHz USING IRF842s

Semicustom Capability

The SP600 family can be customized by inexpensive, final metal mask alterations. Application specific designs are possible for variations in the following parameters:

- Minimum I_{ON}/I_{OFF} pulses
- OC trip response time
- Input signal conditioning filters
- OC trip level
- Inclusion of $R_{CHARGE/DISCHARGE}$
- $I_{TRIP\ SELECT}$ boost level
- FAULT reset timer

Other system related options include:

- Input protocol
- Automatic FAULT reset
- Ability to disable the automatic refresh algorithm

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1. E. J. Wildi, et al, "New High Voltage IC Technology," IEDM 84 Conference proc, pp 262-265.
2. E. J. Wildi, et al, "500V BiMOS Technology and its Applications," Electro 85 paper #24/2.
3. J. G. Mansmann, et al, "ASIC Like HVIC for Interfacing to Half-Bridge Based Power Circuits," PESC March 88.
4. J. G. Mansmann, et al "A Flexible High Voltage Controller Core for Half "He" N-Channel Bridge Operation," MOTORCON proc, Sept '87, pp 194-205.
5. D. J. MacIntyre, "Motor Control Applications of Second Generation IGT Power Transistors," GE PESD Application Note 200.95.
6. R. L. Steigerwald, et al, "A High-Voltage Integrated Circuit for Power Supply Applications", APEC proc, Mar '87, pp 221-229.

Appendix

Timing Waveforms (See page 6)

Although both SP600 and SP601 timing diagrams are shown the SP601 was chosen to provide further explanation.

$t_0 < t < t_1$ At t_0, with the enable high, the outputs are simultaneously commanded to switch from lower to upper which is also known as Bistate operation. After delay t_{OFFD}, the lower is turned off, followed by the uppers turned on. Dead time, $t_{D.T.}$, the difference between the lower off transition to the upper on transition is internally set. Since this timing sets the margin of safety for simultaneous conduction, it's the user's responsibility to ensure that proper external gate impedance is selected to ensure ample time for power transistor charging/discharging.

$t_1 < t < t_2$ The lower is turned on at t_1 and continues for a relatively long period, long enough that at t_2 an automatic refresh will be invoked.

$t_2 < t < t_3$ The HVIC has blinded itself to the logic inputs during this refresh mode. The upper is turned off, with its associated turn off delay, t_{OFFD}. After the fixed dead time, $t_{D.T.}$, the lower is briefly turned on, ton, providing a charge refresh path for the bootstrap capacitor, C_F. Once again the dead time is observed before turning the upper back on again and restoring control to the user inputs. This refresh cycle can be detected as a few µs wide pulse of lower MOSFET/ IGT current.

$t_3 < t < t_5$ The upper remains commanded on for a period of time less than t_{REF}. At t_4, the UP/$\overline{DOWN}$ time is brought low, commanding a lower turn on. Similar to the t_0-t_1 interval, the upper turns off after delay t_{OFFD} and the lower turns on after the dead time, $t_{D.T.}$

$t_5 < t < t_7$ The SP601 is disabled by the ENABLE line low at t_5. Previously conducting lower turns off after its delay, t_{OFFD}. Since the ENABLE line was previously brought low and neither output transistors are conducting, termed as tristate mode. The state of the output phase waveform remains unknown. At t_6, the ENABLE is once again pulled high. The lower turns on after delay, t_{ONDB}.

$t_7 < t < t_9$ At t_7, the SP601 is disabled and the UP/ DOWN line is toggled to the upper position. The lower turns off and the power devices go into a tristate mode. At t_8, upper turn on sequence begins. Since the auto one shot hasn't timed out yet, the turn on delay, t_{ONDB}, is relatively short.

$t_9 < t < t_{11}$ The chip shuts off as the ENABLE line is brought low at t_9, and is enabled again at t_{10} as the UP/DOWN line had remained high. Since the disable period was long and the refresh one shot had timed out, the turn on delay, t_{ONDT}, is slow. Keep in mind that the delay time includes the time for automatic refresh. In an attempt to not further complicate the drawing, the detailed refresh cycle isn't actually shown.

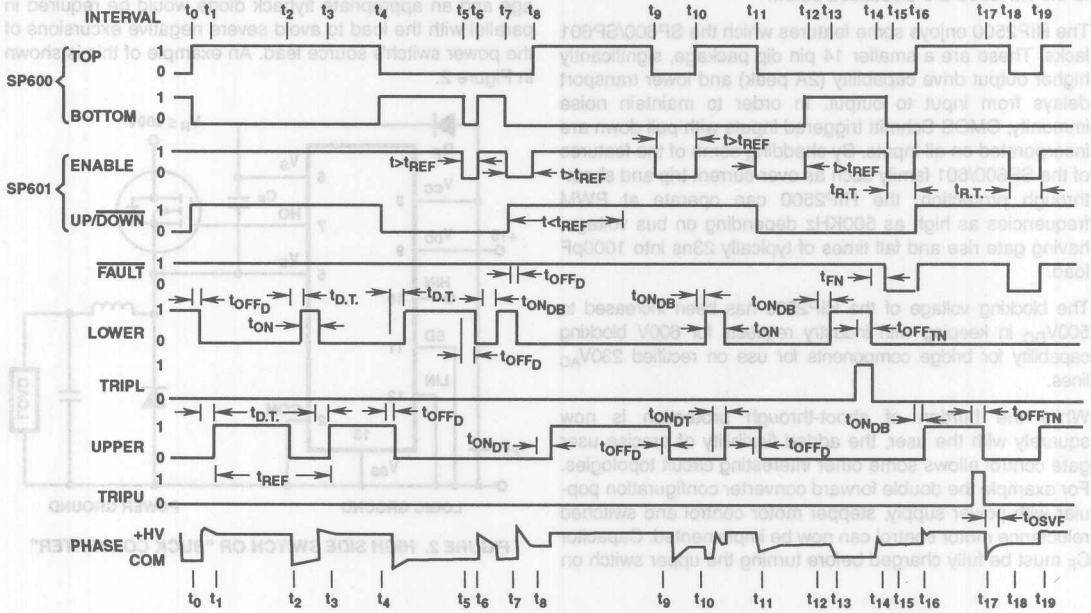
$t_{11} < t < t_{13}$ Both inputs are brought low at t_{11} for a duration longer than t_{REF}. At t_{13} the ENABLE is restored, initiating the turn on sequence for the lower. This follows a long period of time where the one shot had timed out, but in this case the lower is commanded on. Since it doesn't need the refresh algorithm, the turn on delay, t_{ONDB}, is fast.

$t_{11} < t < t_{13}$ This sequence of events depicts the detection of a lower overcurrent trip. Between t_{13}-t_{14}, the lower is on. Beyond the filter delay, t_{OFFTN}, the overcurrent trip shuts off the lower driver. A fraction of a µs later, t_{FN}, the flag report delay, FAULT goes low.

$t_{15} < t < t_{16}$
$t_{18} < t < t_{19}$ By holding both ENABLE and UP/DOWN lines low for the required fault filter reset time, $t_{R.T.}$, the fault is cleared.

$t_{16} < t < t_{17}$ The upper is turned on and an overcurrent trip begins. Beyond the filter delay, t_{OFFTN}, the overcurrent comparator shuts off the upper drive at t_{17}. Since the control logic can only communicate upwards, there is no direct means of reporting an upper trip. As the fault has been remotely captured by the floating upper section, shutdown has occurred. The Phase or V_{OUT} node will quickly fall to a diode drop below common due to inductive flyback current. Via the V_{OUT}/V_{PHASE} monitor this is detected as not being in agreement with the commanded input and reports the fault. Reporting this phase out of status delay is t_{OSVF}.

SP600 Series Timing Diagram



Harris Semiconductor

APPNOTE

No. 9010.2 May 1992

Harris Intelligent Power

HIP2500 HIGH VOLTAGE ($500V_{DC}$) HALF-BRIDGE DRIVER IC

Author: George E. Danz

Introduction

The HIP2500 is a high voltage, high speed dual driver for MOS gated power devices. The drivers are isolated from each other, each controlled by an independent input line referenced to the system common voltage. The HIP2500 was designed using the same proprietary technology which was started more than 5 years ago, resulting in the first products in the HVIC family, the SP600/SP601 Half-Bridge Drivers. Many of the benefits of the SP600/SP601 family also apply to the HIP2500. For example, these HVICs offer a very inexpensive means for driving an n-channel power switch from low side referenced logic without special isolation circuitry, such as optocoupler (not known for extreme reliability) or transformer means (often too expensive). Highly integrated low level logic and high-level drive circuitry minimize propagation delays, allowing higher switching frequencies and often lower switching losses than would be attainable using more conventional techniques. In addition to cost savings and performance increases, the HVIC simplifies and reduces the effort needed to design an efficient driver for MOS gated high and low side switches. Features specific to the HIP2500 are discussed below.

The HIP2500 enjoys some features which the SP600/SP601 lacks. These are a smaller 14 pin dip package, significantly higher output drive capability (2A peak) and lower transport delays from input to output. In order to maintain noise immunity, CMOS Schmitt triggered inputs with pull down are incorporated on all inputs. By shedding some of the features of the SP600/601 family such as over-current trip and shoot-through protection, the HIP2500 can operate at PWM frequencies as high as 500KHz depending on bus voltage, having gate rise and fall times of typically 23ns into 1000pF load.

The blocking voltage of the HIP2500 has been increased to $500V_{DC}$ in keeping with industry requests for 600V blocking capability for bridge components for use on rectified $230V_{AC}$ lines.

While the burden of shoot-through protection is now squarely with the user, the added flexibility of precise user gate control allows some other interesting circuit topologies. For example the double forward converter configuration popular with power supply, stepper motor control and switched reluctance motor control can now be implemented. Capacitor C_F must be fully charged before turning the upper switch on the first time by holding the lower switch on long enough to charge C_F through the load impedance. See Figure 1.

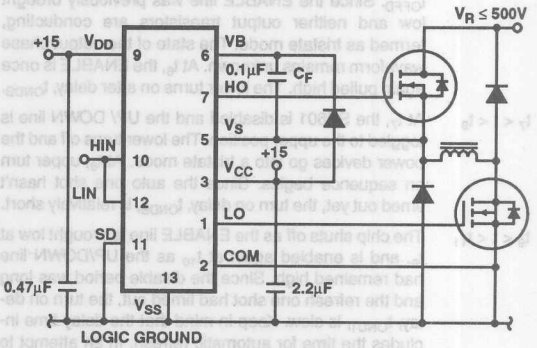


FIGURE 1. DOUBLE FORWARD CONVERTER SCHEMATIC

Also with the HIP2500 it is possible to drive a high side switch which can be switched independently from the low side switch. The load itself could supply initial bootstrap voltage and an appropriate flyback diode would be required in parallel with the load to avoid severe negative excursions of the power switch's source lead. An example of this is shown in Figure 2.

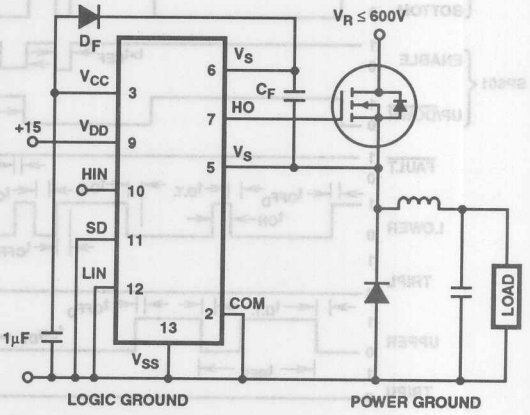


FIGURE 2. HIGH SIDE SWITCH OR "BUCK CONVERTER"

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Description of the HIP2500

The block diagram of the HIP2500 is shown in Figure 3. The HIP2500 is comprised of a ground referenced gate drive circuit and a high voltage bus referenced (floating) gate drive circuit. The input logic circuit for the high side driver incorporates level translation circuitry to interface between the low voltage logic section and the high voltage logic section which controls the upper (or floating) gate driver.

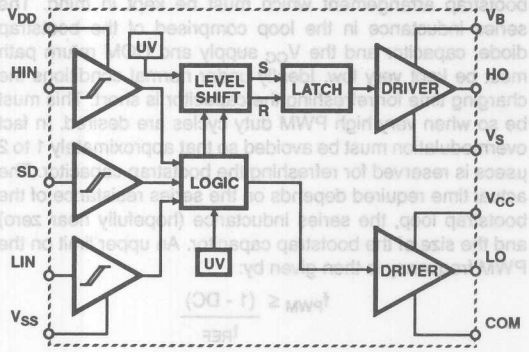


FIGURE 3. HIP2500 FUNCTIONAL BLOCK DIAGRAM

Input Logic

There are three inputs to the HIP2500; HIN controls the floating high side driver, LIN controls the low side (ground referenced) driver and SD which controls the "shutdown" function. All inputs pass through Schmitt buffers employing hysteresis with transition thresholds proportional to the logic supply V_{DD}. Slower or ramped inputs therefore are squared up before being passed to the level translation circuits, which translate the logic level inputs to signal levels compatible with the fixed driver (10V to 15V) supply. The level translation circuit allows the ground reference of the logic supply (V_{SS} on pin 13) to swing plus or minus by a couple of volts with respect to the power ground (COM on pin 2) thereby enhancing noise immunity.

Each channel, including the shutdown input, is independently controlled. The gate drive responds within a short (typically 400ns) propagation delay of the input signal. In applications where deadtime is required to prevent conduction overlap or "shoot-through", the HI and LO input commands must be spaced by external circuitry. For example in a half-bridge configuration, where the upper and lower switches are series connected between the high and low sides of the power bus, effort must be taken to turn off each of the switches in advance of turning on the other. The designer must ensure that one switch is completely off before trying to turn on the other or high currents can flow through both, possibly leading to destruction of one or both power switches. Often a few passive components added to delay switch turn-on without delaying turn-off can effectively control shoot-through (see the diode resistor parallel combination in Figure 4). As power levels and power switch devices become larger, passive techniques may become a more appropriate means to provide turn-on blanking of one switch while the other switch is turning off.

Shutdown is accomplished by a logic level 1 at the SD input. This input must be at logic level 0 to "gate" the HIN and LIN inputs to their respective drivers. The SD logic also removes bias to the high voltage translation pulse circuits, thereby reducing bias current to the HIP2500 when in shutdown mode.

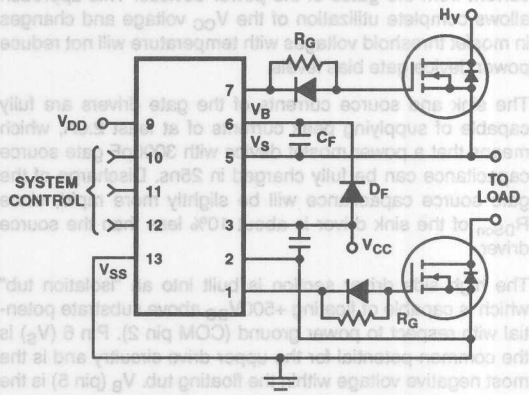


FIGURE 4. SIMPLIFIED SHOOT-THROUGH CONTROL

Protection Features

The HIP2500 is protected internally from insufficient bootstrap supply voltage (in the case of the upper floating driver) and insufficient bias supply voltage (in the case of the lower driver). Also circuitry is provided which allows the high voltage power to be applied prior to the low voltage control power without inducing false gating from the HIP2500.

The undervoltage circuitry functions differently for upper and lower drivers. The lower undervoltage lockout blocks drive to both upper and lower power switches. Upon reestablishment of proper lower supply voltage levels the drive signals are unblocked and gate drive to both upper and lower switches is reestablished provided the appropriate LIN and HIN signals are enabled. The upper undervoltage circuit controls only the gating of the upper (floating) switch which is latched off when an undervoltage is sensed. Latching is released when the upper undervoltage circuit is satisfied. A subsequent "on" pulse from the HIN terminal is necessary to trigger the upper switch. The HIN terminal must have previously gone low since all communications with the upper driver are "edge" triggered. The purpose for latching either driver off in the event of an undervoltage condition is to ensure direct control from the HIN input. Without latching, the undervoltage circuit could cycle at a frequency dependent upon the size of the bootstrap capacitor, gate capacitance, and undervoltage hysteresis levels. Latching the undervoltage detector provides in essence an "alarm" that an undervoltage condition has occurred. The circuit designer must pick values of bootstrap capacitance which avoids undervoltage triggering at the PWM design frequency. Guidance on choosing the right value can be found under "Floating Supply Considerations" later in this note.

Driver Circuits

The driver circuits for the upper and lower gate drives are identical. Since it is desirable to provide the greatest possible gate drive voltage consistent with the user supplied voltage, p-channel mosfets have been used in the output stage of the drivers for sourcing gate current to the power device. Likewise, n-channel devices have been employed for sinking current from the gates of the power devices. This approach allows complete utilization of the V_{CC} voltage and changes in mosfet threshold voltages with temperature will not reduce power device gate bias levels.

The sink and source currents of the gate drivers are fully capable of supplying peak currents of at least 2.0A, which means that a power mosfet device with 3000pF gate source capacitance can be fully charged in 25ns. Discharge of the gate source capacitance will be slightly more rapid, since R_{DSon} of the sink driver is about 10% less than the source driver.

The high side driver section is built into an "isolation tub" which is capable of floating +500V_{DC} above substrate potential with respect to power ground (COM pin 2). Pin 6 (V_S) is the common potential for the upper drive circuitry and is the most negative voltage within the floating tub. V_B (pin 5) is the positive rail within the floating tub and is usually +15 above V_S. The gate drive output, HO (pin 7) swings between V_S and V_B according to the state of the HIN input pin.

Floating Supply Considerations

The floating supply which ties between V_B and V_S is supplied typically by a capacitor, C_F, referred to as the bootstrap capacitor. A fast recovery, low leakage diode, D_F, refreshes or charges this capacitor whenever the V_S terminal swings to common (see Figure 4). A low leakage, fast recovery diode should be chosen for the bootstrap diode and should exhibit low reverse recovery charge. Accomplish this by choosing a diode with a blocking voltage rating greater than 500V_{DC}. For example, the Harris A114P diode is a high voltage 1A, fast recovery diode rated at 1000V blocking. It is used with great success on rectified 230V_{AC} circuits where normally a 500V or 600V diode would be used. The high voltage diode results in a naturally lower junction capacitance than would be attainable in a comparable low voltage diode.

The refresh charging "loop" is a circuit beginning at the V_{CC} node and comprising the bootstrap diode (forward biased), the bootstrap capacitor, either the lower power device or the flyback diode and the COM terminal. Normally V_S voltage will be one diode drop below the COM terminal whenever the upper power switch is turned off due to the inductive nature of the load current commutating from the upper switch to the lower flyback (or body) diode around the lower power switch. When no inductive load current is flowing through the lower flyback diode, then the V_S terminal voltage will operate at a voltage above the COM terminal determined by the lower power device's forward voltage drop. The ultimate voltage attained on the bootstrap capacitor is dependent on whether it was refreshed through the flyback diode or the lower power switch device. Lead inductance associated with the flyback diode can actually cause the V_S terminal to transiently go 5V to 20V below COM depending on dv/dt. This occurs when the upper switch is turned off very rapidly and the load current is rapidly commutated to the lower flyback diode. Although this can help to dump some charge very quickly onto the bootstrap capacitor, it can cause trouble with the HVIC if allowed to exceed more than about 4 volts. It is wise to minimize this inductance by tight power circuit layout practices.

A number of considerations in the implementation of this bootstrap arrangement which must be kept in mind. The series inductance in the loop comprised of the bootstrap diode, capacitor and the V_{CC} supply and COM return path must be kept very low. Ideally under normal conditions the charging time for refreshing the capacitor is short. This must be so when very high PWM duty cycles are desired. In fact overmodulation must be avoided so that approximately 1 to 2 µsecs is reserved for refreshing the bootstrap capacitor. The actual time required depends on the series resistance of the bootstrap loop, the series inductance (hopefully near zero) and the size of the bootstrap capacitor. An upper limit on the PWM frequency is then given by:

$$f_{PWM} \leq \frac{(1 - DC)}{t_{REF}}$$

where:

DC = Duty cycle fraction

t_{REF} = refresh time (sec.)

t_{PWM} = PWM frequency (Hz)

Another consideration in the design of the bootstrap circuit concerns the sizing of the bootstrap capacitor. If it is assumed that all of the gate charge comes from the bootstrap capacitor, which is a good assumption, then enough charge must be placed on the bootstrap capacitor such that when it "dumps" the turn-on gate charge to the power switch, there is still enough voltage on the bootstrap capacitor such that undervoltage lockout is not triggered. For turn-on gate charge of Q_G, flying capacitor of C_F, supply voltage V_{CC} and final gate voltage V_G (which must be greater than the maximum value for the undervoltage trip threshold), the minimum bootstrap capacitor is given by:

$$C_F > \frac{Q_G}{V_{CC} - V_G}$$

The above assumes an inductive load which would tend to cause the bootstrap diode drop to be approximately cancelled by the drop associated with the body diode (mosfet) or flyback diode in parallel with an IGBT. If the load is not somewhat inductive, the bootstrap diode drop must be subtracted from V_{CC} along with any drop associated with the lower switch. The effects of leakage current in the reverse biased bootstrap diode and the small quiescent bias current of the upper driver circuit must be taken into account when sizing C_F. Therefore the sum of the above currents and the charge removed from C_F in charging the gate capacitance, Q_G, determines the minimum size of C_F. Therefore:

$$C_F > \frac{Q_G + (I_{QBS} + I_R) \bullet t_{ON}(max)}{V_{CC} - V_G}$$

The previous discussion on refreshing has been made with a half-bridge or "totem-pole" configuration of the power switches in mind. Other topologies are of interest such as the "double forward converter" configuration shown in Figure 1. Once current is established in the inductor of the double forward converter, simply turning off the switches causes the inductor current to freewheel through the commutating diodes. The V_S lead will be pulled to approximately a diode drop below COM while the inductor current ramps to zero.

This action will charge the bootstrap capacitor in all cases but those wherein the inductor current is minute. During start-up when there is no current in the inductor, it is necessary to precharge the bootstrap capacitor. This can be accomplished in a number of ways, but one can simply turn on the lower MOSFET or IGBT long enough to charge up the capacitor. Voltage overshoot due to the resulting series RLC circuit will be clamped by the internal zener clamps and/or the substrate diode within the HIP2500. Alternatively, a small auxiliary MOSFET can be placed around the lower flyback diode and driven by an inverted LO gate drive signal. When the lower is turned "off", the auxiliary MOSFET will be turned "on" thereby supplying a charging path for the bootstrap capacitor.

The buck converter (Figure 2) is another possible application for the HIP2500. With this type of converter configuration, as soon as the HIP2500 bias supply power is applied, the bootstrap capacitor will be charged through the load impedance. After having waited for complete charging of the capacitor, it is then possible to operate the HIP2500 normally. Subsequent refreshing will occur each time the buck converter switch is turned off which it must do in order to refresh the bottstrap capacitor.

Level Shifting Circuits

As shown in Figure 4, the high side channel input commands require level shifting from a level near COM to a level near that at which the high voltage tub is floating, which can be 500V. The on/off commands for the high side are transformed into narrow current source commands which sink current through burden resistors in the high side circuit. After squaring up these pulses they are "and" gated with the output from the under voltage circuit and latched before being sent to the driver section.

Switching dv/dt as high as 50V/ns is possible with the HIP2500. Also, when the upper switch is turned off, the short lived negative excursions of the V_S terminal due to so-called "forward recovery" and lead wire inductance in series with the upper and lower power switches will not cause problems with HIP2500 operation.

Power Dissipation

Power dissipation in the HIP2500 results from static losses and switching losses. The static losses are due to the bias supply in both upper and lower driver sections and leakage losses in the high voltage level translation transistors. The sum of all these losses at 15V is approximately 19.5mW at +25°C. At +125°C these losses are not normally over 30mW.

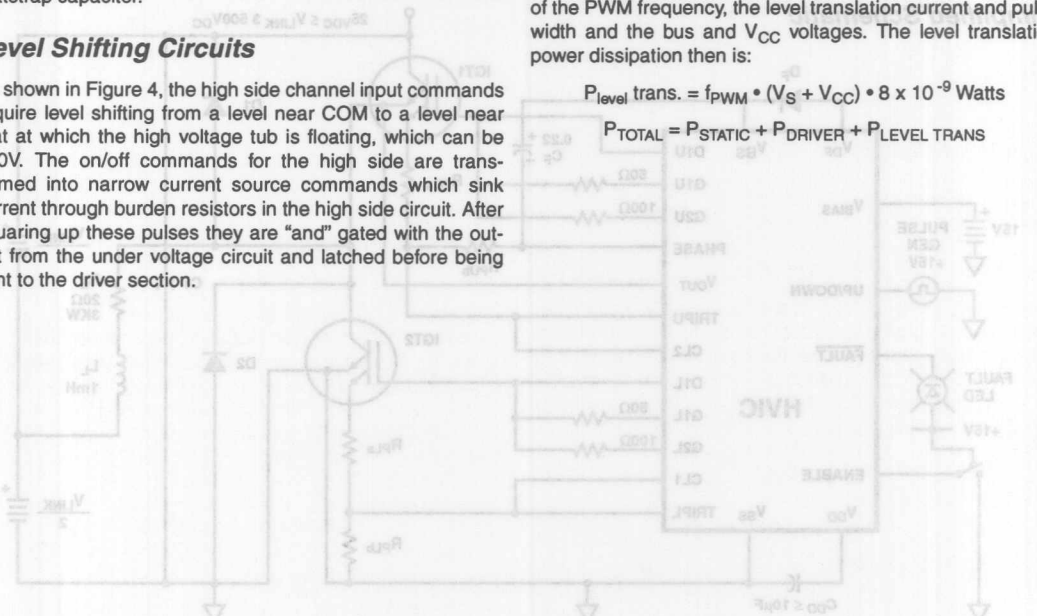
The dynamic losses are due to low voltage and high voltage switching losses. The low voltage switching losses derive primarily from the upper and lower driver output stages. The energy required in charging and discharging the gate of the power switches must flow through the resistance in the gates of the power devices, the R_{DSon} of the driver output stage, and all of the lumped wiring and connection and supply sources resistances. The sharing of these resistances between the HIP2500 and the external source and switch devices must be known before an accurate calculation of losses can be attempted. The maximum total loss can easily be calculated once the PWM frequency, supply voltage and power device gate charge is known:

$$P_{driver} \cong 2 \bullet f_{PWM} \bullet Q_G \bullet V_{CC} \text{ Watts.}$$

The high voltage switching losses are due predominantly to the level translation transistors. These losses are a function of the PWM frequency, the level translation current and pulse width and the bus and V_{CC} voltages. The level translation power dissipation then is:

$$P_{level\ trans.} = f_{PWM} \bullet (V_S + V_{CC}) \bullet 8 \times 10^{-9} \text{ Watts}$$

$$P_{TOTAL} = P_{STATIC} + P_{DRIVER} + P_{LEVEL\ TRANS}$$



APPNOTE

No. 9105.1 May 1992

Harris Intelligent Power

HVIC/IGBT HALF-BRIDGE CONVERTER EVALUATION CIRCUIT

The HVIC high voltage integrated circuit is designed to drive n-channel IGBTs or MOSFETs in a half-bridge configuration up to $500V_{DC}$. Power supply and motor control inverters can be configured for voltages up to $230V_{AC}$ using the HVIC, IGBTs and a few other components.

A few precautions should be taken in using the circuit. Lead lengths between the external power circuit (including gate and pilot leads), the 15V bypass capacitor (C_{DD}), the bootstrap diode (D_F) and capacitor (C_F) and the HVIC should be minimized.

The basic components required to evaluate the features of the SP601 are shown in the simplified schematic. The recommended load is largely resistive so that the largest current component will flow through the IGBTs, IGT1 and IGT2.

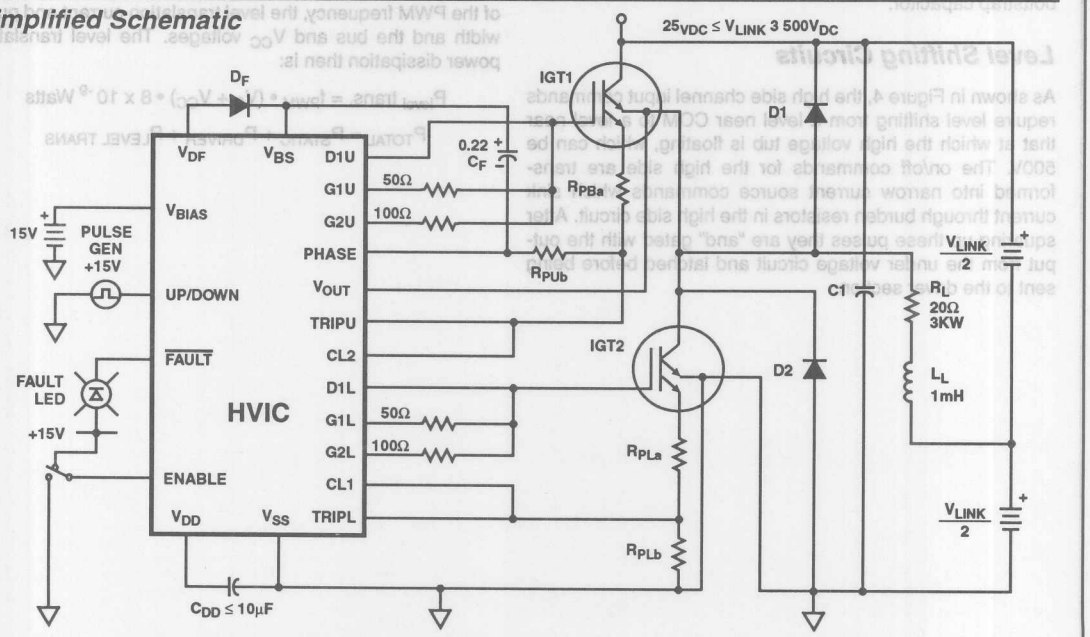
The flyback diodes, D1 and D2, rated 8A, will carry a much smaller flyback current component. A small amount of load inductance will cause the switching waveforms to simulate the conditions which would normally be observed with motor or transformer loads, while limiting the current carried by the lower rated flyback diodes in this circuit.

The values for R_{PUa}, R_{PUb}, etc., have been chosen to result in overcurrent trip at approximately 25Apk. At this level of current, heat sinking for the IGTs and flyback diodes is required. The series resistance of the upper and lower pilot resistor dividers would be approximately 1KΩ; the divider ratio should cause 0.1V at the tap at the desired trip current.

When first energizing your evaluation circuit, begin with a reduced bus voltage of about $20V_{DC}$ to $30V_{DC}$ to verify proper circuit operation before proceeding to higher voltages.

More specific information can be found in File Number 2428 and File Number 2429 Half-Bridge $500V_{DC}$ Driver data sheets and in the Application Note, AN-8829.1.

Simplified Schematic



HVIC - Harris Part # SP601 (Formerly GS601)
IGT1, 2 - Harris Part # HGTA24N60D1C
D1, 2 - Harris Part # RUR860
D_F - Harris Part # A114M
R_{PUa}, R_{PLa} - 910Ω, 1.8W
R_{PUb}, R_{PLb} - 68Ω, 1.8W
C1 - 0.1µF, $600V_{DC}$
R_L - 20Ω, 3KW 13 -50

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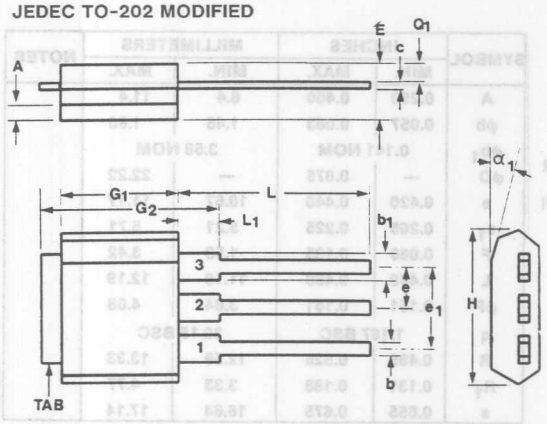
DIMENSIONAL OUTLINES AND MOUNTING HARDWARE

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Dimensional Outlines

JEDEC TO-202 MODIFIED

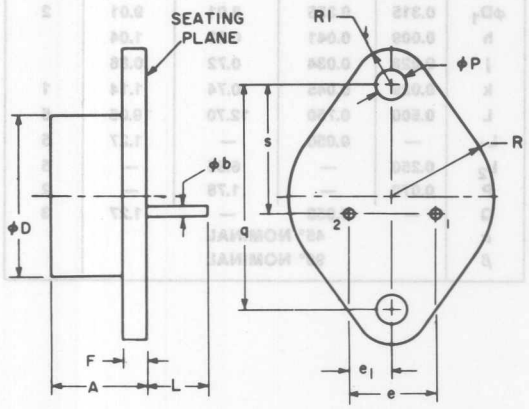


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.05	—	1.270	1
b	0.023	0.029	0.584	0.736	
b_1	0.045	0.055	1.143	1.397	1
c	0.018	0.026	0.457	0.660	
E	0.130	0.150	3.302	3.810	
e	0.095	0.105	2.413	2.667	
e_1	0.190	0.210	4.826	5.334	
G_1	0.220	0.260	5.588	6.624	
G_2	0.415	0.425	10.54	10.80	
H	0.330	0.380	8.382	9.652	
L	0.390	0.450	9.906	11.43	
L_1	—	0.110	—	2.794	1, 2
Q_1	0.039	0.050	0.990	1.270	
α_1	—	50°	—	50°	1

NOTES: 1. Package contour optional within dimensions specified.

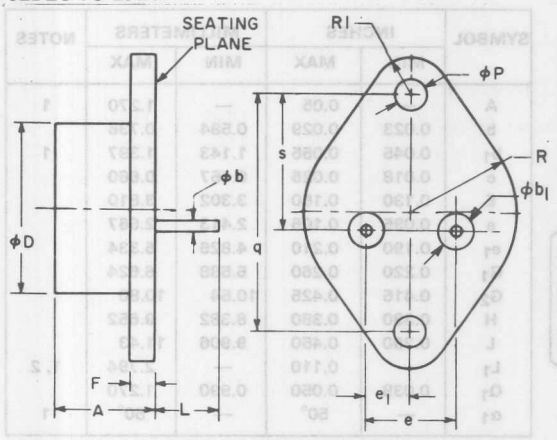
2. Lead dimensions uncontrolled in this zone.

JEDEC TO-204AA



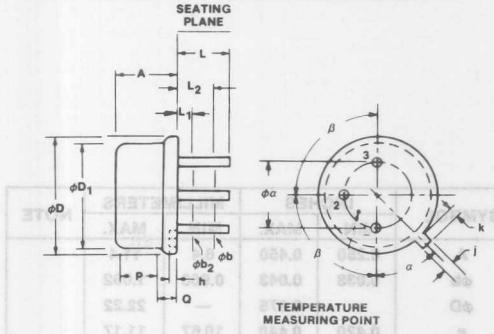
SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.4	11.4	
ϕb	0.038	0.043	0.966	1.092	
ϕD	—	0.875	—	22.22	
e	0.420	0.440	10.67	11.17	
e_1	0.205	0.225	5.21	5.71	
F	—	0.135	—	3.42	
L	0.312	—	7.93	—	
ϕP	0.151	0.161	3.84	4.08	
q	1.187 BSC		30.15 BSC		
R	—	0.525	—	13.33	
R_1	—	0.188	—	4.77	
s	0.655	0.675	16.64	17.14	

JEDEC TO-204AE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.4	11.4	
φb	0.057	0.063	1.45	1.60	
$φb_1$	0.141 NOM		3.58 NOM		
φD	—	0.875	—	22.22	
e	0.420	0.440	10.67	11.17	
e_1	0.205	0.225	5.21	5.71	
F	0.060	0.135	1.53	3.42	
L	0.440	0.480	11.18	12.19	
φP	0.151	0.161	3.84	4.08	
q	1.187 BSC		30.15 BSC		
R	0.495	0.525	12.58	13.33	
R_1	0.131	0.188	3.33	4.77	
s	0.655	0.675	16.64	17.14	

JEDEC TO-205AF

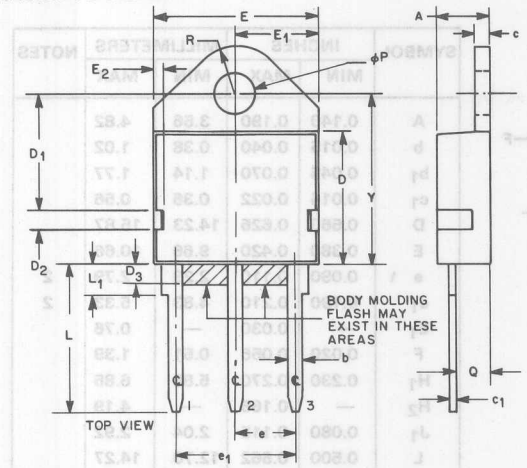


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.200 BSC		5.08 BSC		4
A	0.160	0.180	4.07	4.57	
φb	0.016	0.021	0.41	0.53	5
$φb_2$	0.016	0.019	0.41	0.48	5
φD	0.340	0.370	8.64	9.39	
$φD_1$	0.315	0.355	8.01	9.01	2
h	0.009	0.041	0.23	1.04	
j	0.028	0.034	0.72	0.86	
k	0.029	0.045	0.74	1.14	1
L	0.500	0.750	12.70	19.05	5
L_1	—	0.050	—	1.27	5
L_2	0.250	—	6.35	—	5
P	0.070	—	1.78	—	2
Q	—	0.050	—	1.27	3
α	45° NOMINAL				
β	90° NOMINAL				

Notes:

1. Dimension k measured from φD maximum.
2. $φD_1$ shall not vary more than 0.010 in Zone P. This zone controlled for automatic handling.
3. Details of outline in this zone optional.
4. Leads at gauge plane 0.054-0.055 below seating plane shall be within 0.007 radius of positional tolerance at MMC relative to tab at MMC. Device may be measured by direct methods or by gauge and gauging procedure described on JEDEC gauge drawing GS-1.
5. $φb_2$ applies between L_1 and L_2. φb applies between L_2 and L minimum. Diameter is uncontrolled in L_1 and beyond L minimum.

JEDEC TO-218AC

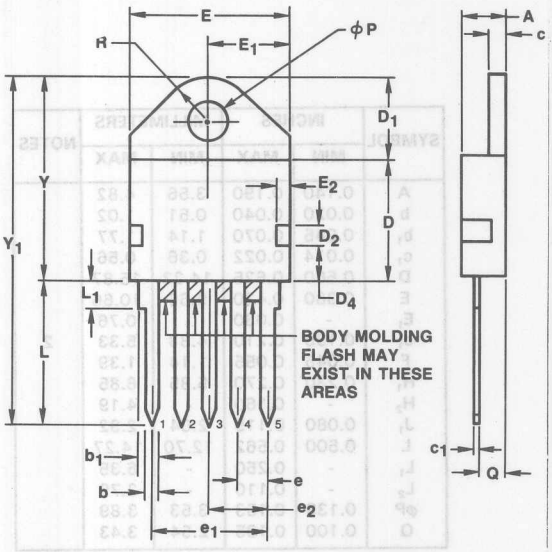


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.165	0.200	4.191	5.080	
b	0.040	0.065	1.016	1.651	
c	0.053	0.065	1.346	1.651	
c_1	0.015	0.030	0.381	0.762	
D	0.460	0.505	11.68	12.827	
D_1	0.395	0.415	10.033	10.541	
D_2	0.070	0.090	1.778	2.286	
D_3	—	0.600	—	1.524	
E	0.610	0.640	15.494	16.256	1
E_1	0.305	0.320	7.747	8.128	
E_2	0.040	0.060	1.016	1.524	
e	0.205	0.225	5.207	5.715	4
e_1	0.420	0.440	10.688	11.176	4
L	0.500	0.632	12.700	16.05	
L_1	—	0.150	—	3.81	2
φP	0.157	0.167	3.988	4.241	
Q	0.093	0.126	2.36	3.200	
R	0.170	0.190	4.318	4.826	1
Y	0.600	0.650	15.24	16.51	

NOTES:

1. Tab outline optional within boundaries of dimensions E and R.
2. Lead dimensions uncontrolled in L_1.
3. Maximum radius of 0.050" on all body edges and corners.
4. Position of lead to be measured 0.185-0.190" from bottom of dimension D.
5. Controlling dimension: inch.

JEDEC MO-093

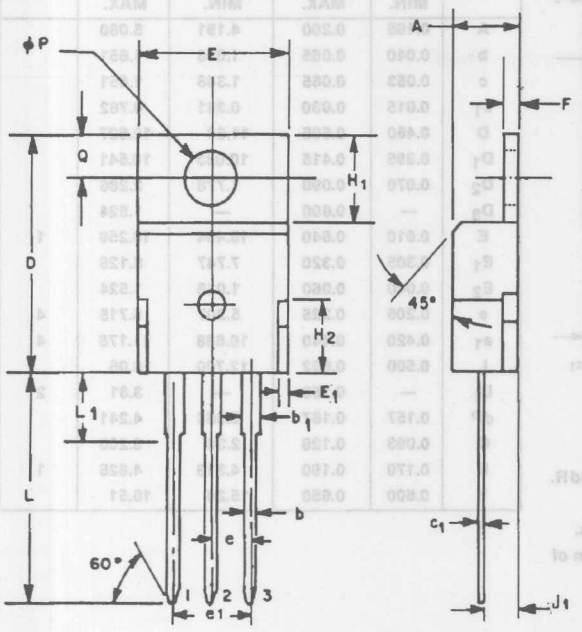


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.190	—	4.826	
b	0.049	0.053	1.243	1.346	
b_1	—	0.075	—	1.905	
c	0.059	0.061	1.499	1.549	
c_1	0.019	0.021	0.483	0.533	
D	0.475	0.495	12.065	12.973	
D_1	—	0.325	—	8.255	
D_2	—	0.080	—	2.032	
D_3	—	0.600	—	15.240	
E	0.615	0.625	15.621	15.875	1
E_1	—	0.310	—	7.874	
E_2	—	0.050	—	1.270	
e	0.105	0.113	2.667	2.870	4
e_1	0.430	0.446	10.922	11.328	4
e_2	0.215	0.223	5.461	5.664	
L	0.575	0.595	14.603	15.113	
L_1	—	0.110	—	2.794	2
φP	0.159	0.163	4.039	4.140	
Q	—	0.120	—	3.048	
R	—	0.181	—	4.597	1
Y	0.800	0.820	20.320	20.828	
Y_1	—	1.395	—	35.433	

NOTES:

1. Tab outline optional within boundaries of dimensions E and R.
2. Lead dimensions uncontrolled in L_1.
3. Maximum radius of 0.050" on all body edges and corners.
4. Position of lead to be measured 0.185-0.190" from bottom o dimension D.
5. Controlling dimension: inch.

JEDEC TO-220AB

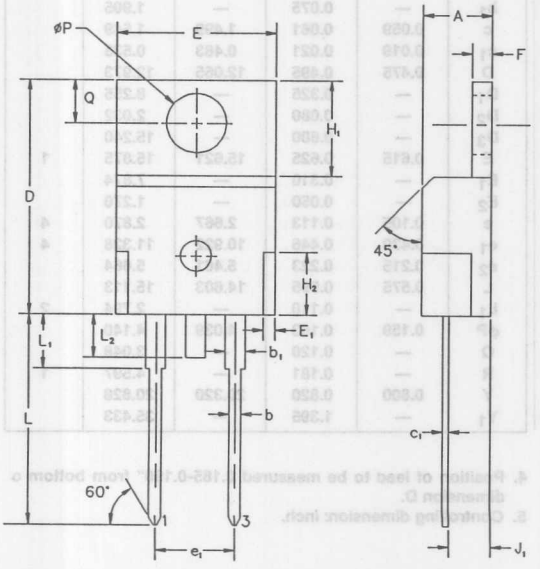


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.140	0.190	3.56	4.82	
b	0.015	0.040	0.38	1.02	
b_1	0.045	0.070	1.14	1.77	
c_1	0.014	0.022	0.36	0.56	
D	0.560	0.625	14.23	15.87	
E	0.380	0.420	9.66	10.66	
e	0.090	0.110	2.29	2.79	2
e_1	0.190	0.210	4.83	5.33	2
E_1	—	0.030	—	0.76	
F	0.020	0.055	0.51	1.39	
H_1	0.230	0.270	5.85	6.85	
H_2	—	0.165	—	4.19	
J_1	0.080	0.115	2.04	2.92	
L	0.500	0.562	12.70	14.27	
L_1	—	0.250	—	6.35	
ϕP	0.139	0.153	3.53	3.89	
Q	0.100	0.135	2.54	3.43	

NOTES: 1. These dimensions are within allowable dimensions of revision J of JEDEC TO-220AB outline dated 3-24-87.

2. Position of lead to be measured 0.250-0.255 (6.350-6.477mm) from case.

JEDEC TO-220AC



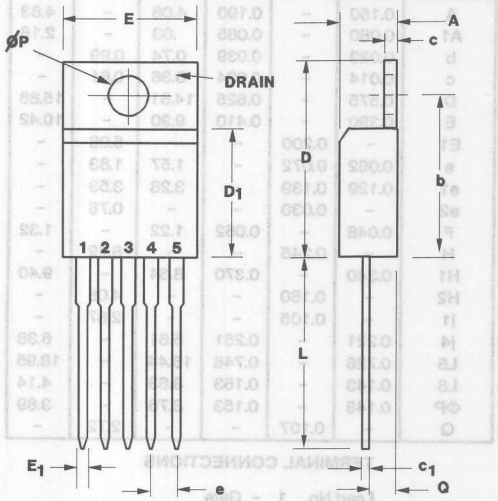
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.140	0.190	3.56	4.82	
b	0.020	0.040	0.51	1.02	
b_1	0.045	0.070	1.14	1.77	
c_1	0.014	0.022	0.36	0.56	
D	0.560	0.625	14.23	15.87	
E	0.380	0.420	9.66	10.66	
E_1	-	0.030	-	0.76	
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.14	1.39	
H_1	0.230	0.270	5.85	6.85	
H_2	-	0.160	-	4.19	
J_1	0.080	0.115	2.04	2.92	
L	0.500	0.562	12.70	14.27	
L_1	-	0.250	-	6.35	
L_2	-	0.110	-	2.79	
ϕP	0.139	0.153	3.53	3.89	
Q	0.100	0.135	2.54	3.43	

NOTES:

1. These dimensions are within allowable dimensions of revision J of JEDEC TO-220AC outline dated 3-24-87.

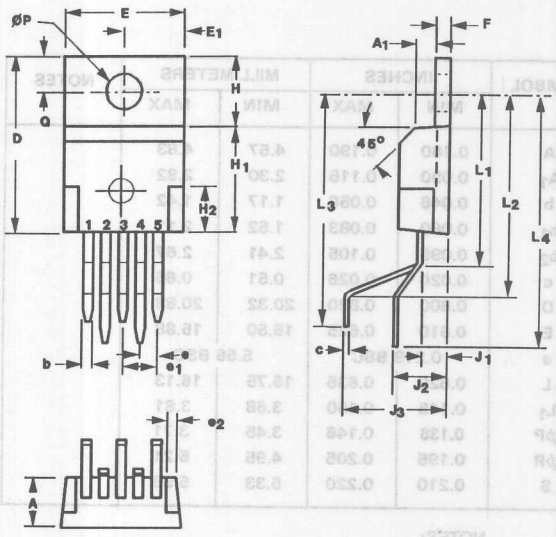
2. Position of lead to be measured 0.250-0.255 inches (6.350-6.477mm) from case.

JEDEC TS-001



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.180	4.32	4.57	
b	0.470	0.500	11.94	12.70	
c	0.048	0.052	1.22	1.32	
c_1	0.016	0.020	0.41	0.51	
D	0.580	0.594	14.73	15.09	
D_1	0.330	0.350	8.38	8.89	
E	0.405	0.415	10.29	10.54	
E_1	0.28	0.32	0.71	0.81	
e	0.057	0.077	1.45	1.96	
L	0.530	0.575	13.46	14.61	
ϕP	0.139	0.149	3.53	3.78	
Q	0.107	0.117	2.72	2.97	

JEDEC TS-001 VERTICAL MOUNT (VM) LEADFORM

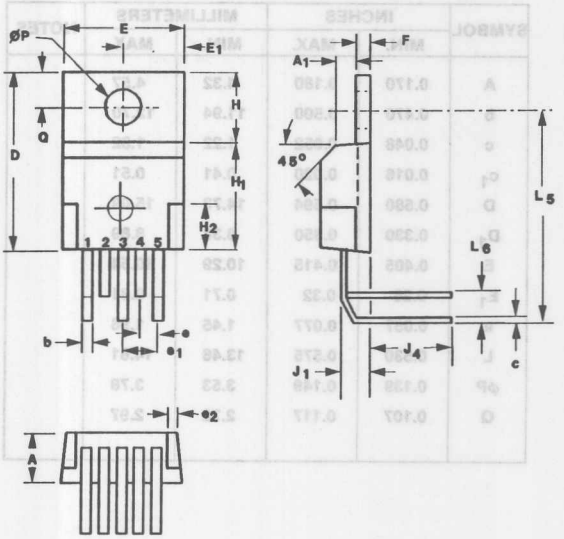


SYMBOL	INCHES			MILLIMETERS		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.160	–	0.190	4.06	–	4.83
A1	0.080	–	0.085	.03	–	2.16
b	0.029	–	0.039	0.74	0.99	–
c	0.014	–	0.024	0.36	0.61	–
D	0.575	–	0.625	14.61	–	15.88
E	0.390	–	0.410	9.90	–	10.42
E1	–	0.200	–	–	5.08	–
e	0.062	0.072	–	1.57	1.83	–
e1	0.129	0.139	–	3.28	3.53	–
e2	–	0.030	–	–	0.76	–
F	0.048	–	0.052	1.22	–	1.32
H	–	0.245	–	–	6.22	–
H1	0.340	–	0.370	8.64	–	9.40
H2	–	0.160	–	–	4.06	–
j1	–	0.105	–	–	2.67	–
j2	0.168	–	0.188	4.27	–	4.78
j3	0.320	–	0.340	8.13	–	8.64
L	0.400	–	0.430	10.16	–	10.92
L1	0.600	–	0.620	15.24	–	15.75
L2	0.680	–	0.710	17.27	–	18.03
L3	0.825	–	0.845	20.96	–	21.46
L4	0.876	–	0.896	22.25	–	22.76
ΦP	0.148	–	0.153	3.76	–	3.89
Q	–	0.107	–	–	2.72	–

TERMINAL CONNECTIONS

Lead No. 1 – Gate
Lead No. 2 – Current Sense
Lead No. 3 – Drain
Lead No. 4 – Source Kelvin
Lead No. 5 – Source
Mounting Flange – Drain

JEDEC TS-001 HORIZONTAL MOUNT (HM) LEADFORM

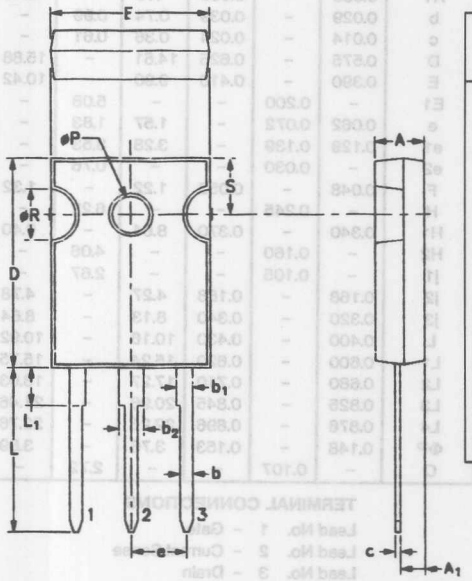


SYMBOL	INCHES			MILLIMETERS		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.160	–	0.190	4.06	–	4.83
A1	0.080	–	0.085	.03	–	2.16
b	0.029	–	0.039	0.74	0.99	–
c	0.014	–	0.024	0.36	0.61	–
D	0.575	–	0.625	14.61	–	15.88
E	0.390	–	0.410	9.90	–	10.42
E1	–	0.200	–	–	5.08	–
e	0.062	0.072	–	1.57	1.83	–
e1	0.129	0.139	–	3.28	3.53	–
e2	–	0.030	–	–	0.76	–
F	0.048	–	0.052	1.22	–	1.32
H	–	0.245	–	–	6.22	–
H1	0.340	–	0.370	8.64	–	9.40
H2	–	0.160	–	–	4.06	–
j1	–	0.105	–	–	2.67	–
j4	0.221	–	0.251	5.61	–	6.38
L5	0.726	–	0.746	18.44	–	18.95
L6	0.143	–	0.163	3.63	–	4.14
ΦP	0.148	–	0.153	3.76	–	3.89
Q	–	0.107	–	–	2.72	–

TERMINAL CONNECTIONS

Lead No. 1 – Gate
Lead No. 2 – Current Sense
Lead No. 3 – Drain
Lead No. 4 – Source Kelvin
Lead No. 5 – Source
Mounting Flange – Drain

JEDEC TO-247 Style

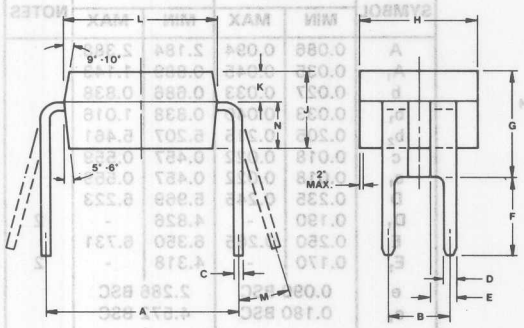


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.57	4.83	
A_1	0.090	0.115	2.30	2.92	
b	0.046	0.056	1.17	1.42	
b_1	0.060	0.083	1.52	2.11	
b_2	0.095	0.105	2.41	2.67	
c	0.020	0.026	0.51	0.66	
D	0.800	0.820	20.32	20.83	
E	0.610	0.625	15.50	15.88	
e	0.219 BSC		5.56 BSC		
L	0.620	0.635	15.75	16.13	
L_1	0.145	0.150	3.68	3.81	
ϕP	0.138	0.146	3.45	3.71	
ϕR	0.195	0.205	4.95	5.21	
S	0.210	0.220	5.33	5.59	

NOTES:

1. Lead dimension (without solder).
2. Add typically 0.006 inch for solder coating.
3. Lead and body finish uncontrolled in L_1

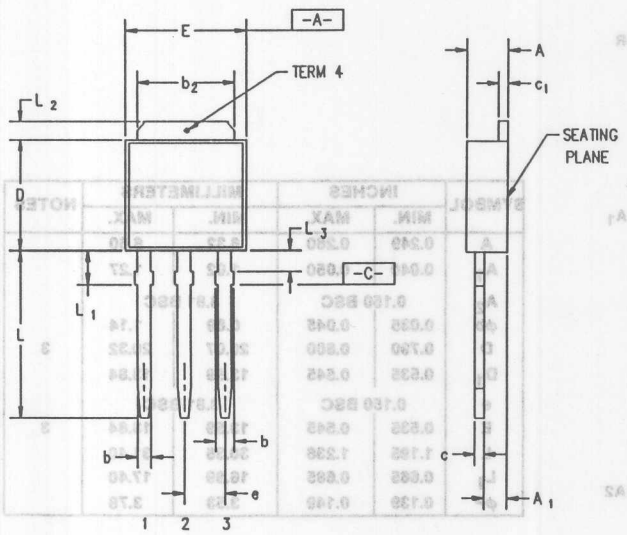
4-PIN DIP



SYMBOL	INCHES		MILLIMETER		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.300	–	7.62	–	
B	.100 NOM.		2.54 NOM.		
C	.013	.017	.34	.43	
D	.020	.024	.51	.60	
E	.035	.045	.89	1.14	
F	.140	.160	3.56	4.06	
G	.160	.180	4.07	4.57	
H	.194	.198	4.93	5.02	
J	.124	.134	3.15	3.40	
K	.034	.044	.87	1.11	
L	.238	.248	6.05	6.29	
M	0°	15°	0°	15°	
N	.085	.095	2.16	2.41	

NOTE: CONTROLLING DIMENSIONS: MILLIMETERS

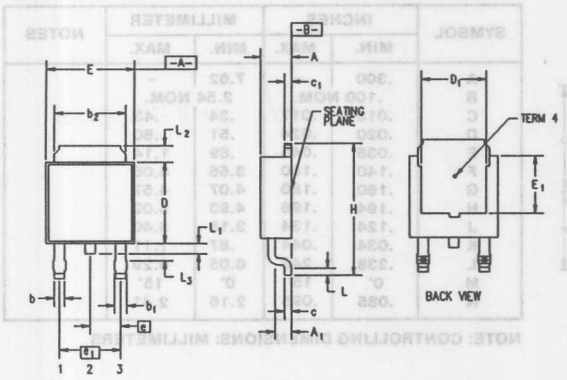
JEDEC TO-251AA



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.184	2.388	
A_1	0.035	0.045	0.889	1.143	
b	0.027	0.033	0.686	0.838	
b_1	0.033	0.040	0.838	1.016	
b_2	0.205	0.215	5.207	5.461	
c	0.018	0.022	0.457	0.559	
c_1	0.018	0.022	0.457	0.559	
D	0.235	0.245	5.969	6.223	
E	0.250	0.265	6.350	6.731	
e	0.090BSC		2.286BSC		
L	0.355	0.375	9.017	9.525	
L_1	0.075	0.090	1.905	2.286	
L_2	0.035	0.050	0.889	1.270	
L_3	0.045	0.060	1.143	1.524	1

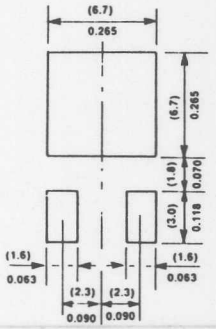
1. Lead dimension uncontrolled in L_3.
2. Controlling dimension: inch.

JEDEC TO-252AA



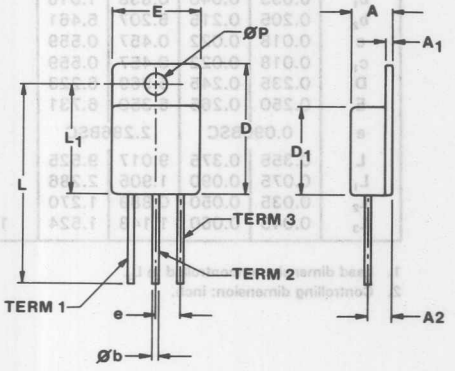
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.184	2.388	
A_1	0.035	0.045	0.889	1.143	
b	0.027	0.033	0.686	0.838	
b_1	0.033	0.040	0.838	1.016	
b_2	0.205	0.215	5.207	5.461	
c	0.018	0.022	0.457	0.559	
c_1	0.018	0.022	0.457	0.559	
D	0.235	0.245	5.969	6.223	
D_1	0.190	-	4.826	-	2
E	0.250	0.265	6.350	6.731	
E_1	0.170	-	4.318	-	2
e	0.090 BSC		2.286 BSC		
e_1	0.180 BSC		4.572 BSC		
H	0.370	0.410	9.398	10.41	
L	0.020 typ		0.508 typ		3
L_1	0.025	0.040	0.635	1.016	
L_2	0.035	0.050	0.889	1.270	
L_3	0.045	0.060	1.143	1.524	1

1. Lead dimension uncontrolled in L_3.
2. D_1 and E_1 establishes a minimum mounting surface for terminal 4.
3. L is the terminal length for soldering.
4. Controlling dimension: inch.



MINIMUM PAD SIZES RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

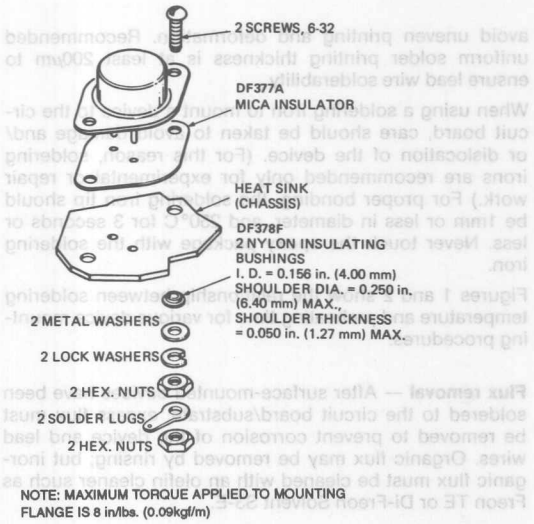
JEDEC TO-254AA



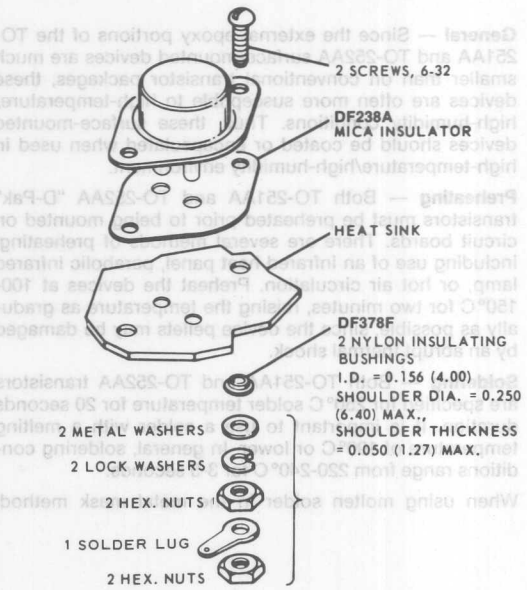
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.249	0.260	6.32	6.60	
A_1	0.040	0.050	1.02	1.27	
A_2	0.150 BSC		3.81 BSC		
øb	0.035	0.045	0.89	1.14	
D	0.790	0.800	20.07	20.32	3
D_1	0.535	0.545	13.59	13.84	
e	0.150 BSC		3.81 BSC		
E	0.535	0.545	13.59	13.84	3
L	1.195	1.236	30.35	31.40	
L_1	0.665	0.685	16.89	17.40	
øP	0.139	0.149	3.53	3.78	

Notes:
1. **Refer to applicable symbol list.**
2. **Dimensioning and tolerancing per ANSI Y14.5.M. 1982.**
3. **Glass meniscus included in Dim. D and E.**
4. **Controlling dimension: inch.**

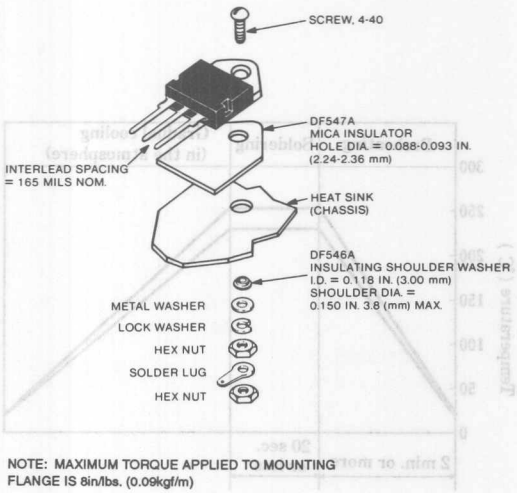
Mounting Hardware



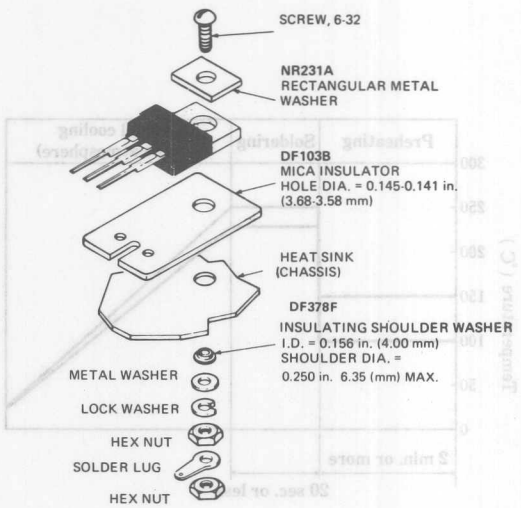
Suggested mounting hardware for JEDEC TO-204AA



Suggested mounting hardware for JEDEC TO-204AE



Suggested mounting hardware for JEDEC TO-218 and JEDEC MO-093



Suggested mounting hardware for JEDEC TO-220 and JEDEC TS-001

Surface-Mounted Devices Mounting and Handling Considerations

General — Since the external epoxy portions of the TO-251AA and TO-252AA surface-mounted devices are much smaller than on conventional transistor packages, these devices are often more susceptible to high-temperature/high-humidity conditions. Thus, these surface-mounted devices should be coated or encapsulated when used in high-temperature/high-humidity environment.

Preheating — Both TO-251AA and TO-252AA "D-Pak" transistors must be preheated prior to being mounted on circuit boards. There are several methods of preheating, including use of an infrared heat panel, parabolic infrared lamp, or hot air circulation. Preheat the devices at 100-150°C for two minutes, raising the temperature as gradually as possible, since the device pellets may be damaged by an abrupt thermal shock.

Soldering — Both TO-251AA and TO-252AA transistors are specified for 250°C solder temperature for 20 seconds duration. It is important to use a solder with a melting temperature of 190°C or lower. In general, soldering conditions range from 220-240°C for 3-5 seconds.

When using molten solder in the metal mask method, avoid uneven printing and deformation. Recommended uniform solder printing thickness is at least 200μm to ensure lead wire solderability.

When using a soldering iron to mount a device to the circuit board, care should be taken to avoid damage and/or dislocation of the device. (For this reason, soldering irons are recommended only for experimental or repair work.) For proper bonding, the soldering iron tip should be 1mm or less in diameter, and 250°C for 3 seconds or less. Never touch the epoxy package with the soldering iron.

Figures 1 and 2 show the relationship between soldering temperature and preheating time for various device mounting procedures.

Flux removal — After surface-mounted devices have been soldered to the circuit board/substrate, excess flux must be removed to prevent corrosion of the device and lead wires. Organic flux may be removed by rinsing; but inorganic flux must be cleaned with an olefin cleaner such as Freon TE or Di-Freon Solvent S3-E.

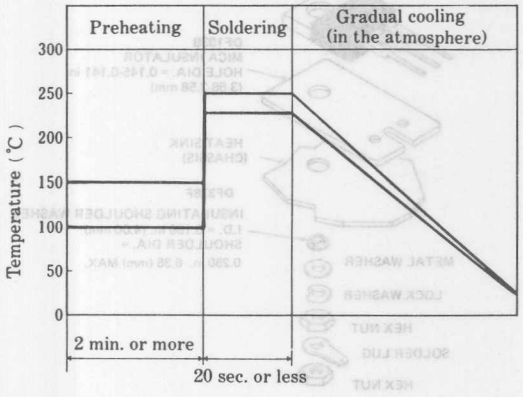


Fig. 1 — Solder dip method.

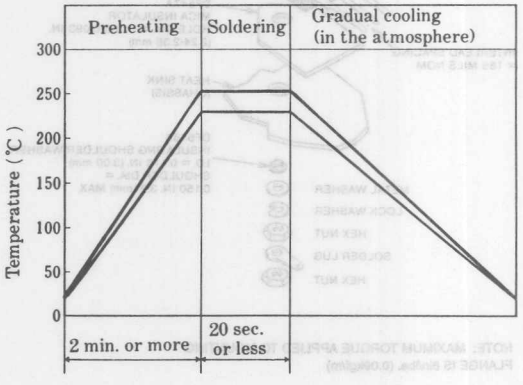


Fig. 2 — Reflow solder method.

Surface-Mounted Devices Power Dissipation Considerations

Maximum power dissipation for the TO-251AA is 1W; however, when the TO-252AA is mounted directly to a ceramic substrate, the power dissipation is increased to 2-3W. Figure 3 illustrates the maximum power dissipation for either the D72F5T1 or the D73F5T1 transistor mounted to a ceramic substrate.

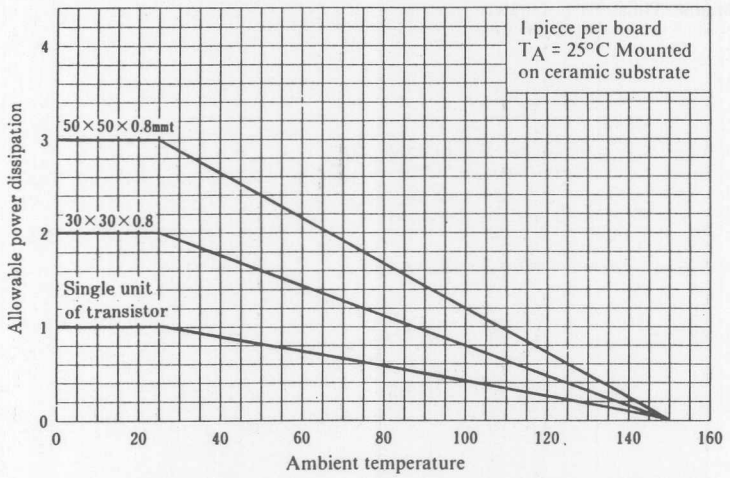


Fig. 3 — $P_{D(max)}$ vs. T_A characteristics of either the D72F5T1 or D73F5T1 transistor mounted on a ceramic substrate.

Certain circuit designs (such as motor drives and flash circuits) require devices to be rated for transient conditions as well as for their overall power dissipation capability. The relationship between maximum power dissipation and pulse width under transient conditions for typical TO-251AA devices is shown in figure 4.

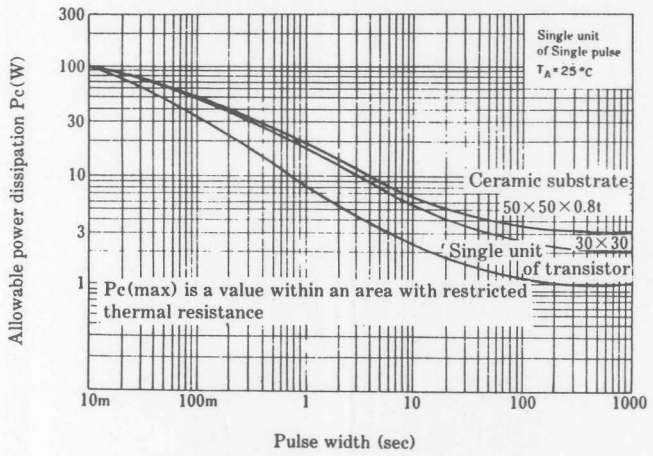


Fig. 4 — P_D vs. T_A characteristics of D72F5T1 and D73F5T1 under transient conditions.

Surface-Mounted Devices Power Dissipation Considerations

Maximum power dissipation for the TO-251AA is 1W; however, when the TO-252AA is mounted directly to a ceramic substrate, the power dissipation is increased to 2-3W. Figure 3 illustrates the maximum power dissipation for either the DZ7F5T1 or the DZ3F5T1 transistor mounted to a ceramic substrate.

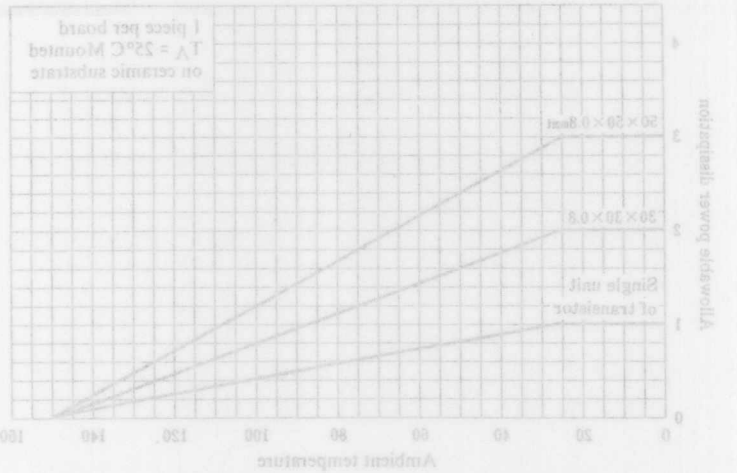


Fig. 3 — P_{Dmax} vs. T_A characteristics of either the DZ7F5T1 or DZ3F5T1 transistor mounted on a ceramic substrate.

Certain circuit designs (such as motor drives and flash circuits) require devices to be rated for transient conditions as well as for their overall power dissipation capability. The relationship between maximum power dissipation and pulse width under transient conditions for typical TO-251AA devices is shown in figure 4.

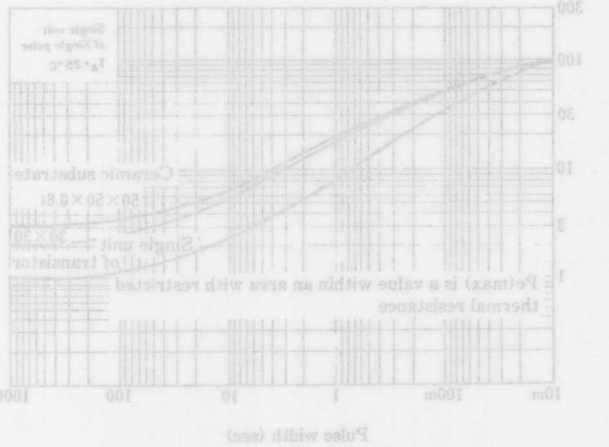


Fig. 4 — P_D vs. T_A characteristics of DZ7F5T1 and DZ3F5T1 under transient conditions.